CS2323 Computer Architecture Assignment 2018

Homework 1 Solutions

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1. Total energy = leakage energy + dynamic energy
leakage power = $0.07W$
leakage energy = leakage power $\times$ time taken = $0.07 \times 1 = 0.07J$
dynamic energy = $0.8nJ/access$
number of access = 50000000
total dynamic energy = dynamic energy $\times$ number of access = $0.04J$
total energy = $0.07 + 0.04 = 0.11J$
% leakage energy = $\frac{0.07 \times 100}{0.11} = 63.63\%$

2. reach of DTLB = $\sum$ $(page\ size \times entries)$

$$(4 \times 64) + (2 \times 32 \times 2^{10}) + (1 \times 8 \times 2^{20})\ KB$$
$$= 8454400\ KB$$
$$= 8.0627\ GB$$

3. Total bits = 8 , Offset bits = 2 , Set index bits = 3 and Tag bits = 3
(a)

Sequence	Tag	Set	Hit/Miss cache1
0	0	0	miss
63	1	7	miss
1	0	0	hit
62	1	7	hit
2	0	0	hit
61	1	7	hit
3	0	0	hit
60	1	7	hit
4	0	1	miss
59	1	6	miss
5	0	1	hit
58	1	6	hit
6	0	1	hit
57	1	6	hit
7	0	1	hit
56	1	6	hit
8	0	2	miss
55	1	5	miss
9	0	2	hit
54	1	5	hit
10	0	2	hit
53	1	5	hit
11	0	2	hit
52	1	5	hit

Hit ratio $= \frac{18}{24} = 0.75$

Sequence	Tag	Set	Hit/Miss cache2
0	0	0	miss
63	7	7	miss
1	1	0	miss
62	6	7	miss
2	2	0	miss
61	5	7	miss
3	3	0	miss
60	4	7	miss
4	4	0	miss
59	3	7	miss
5	5	0	miss
58	2	7	miss
6	6	0	miss
57	1	7	miss
7	7	0	miss
56	0	7	miss
8	0	1	miss
55	7	6	miss
9	1	1	miss
54	6	6	miss
10	2	1	miss
53	5	6	miss
11	3	1	miss
52	4	6	miss

Hit ratio = $\frac{0}{24} = 0$
(b)

Sequence	Tag	Set	Hit/Miss cache1
0	0	0	miss
64	2	0	miss
128	4	0	miss
192	6	0	miss
1	0	0	miss
65	2	0	miss
129	4	0	miss
193	6	0	miss
11	0	2	miss
75	2	2	miss
139	4	2	miss
203	6	2	miss
9	0	2	miss
137	4	2	miss
201	6	2	miss
73	2	1	miss

Hit ratio $= \frac{0}{16} = 0$

Sequence	Tag	Set	Hit/Miss cache2
0	0	0	miss
64	0	0	hit
128	0	0	hit
192	0	0	hit
1	1	0	miss
65	1	0	hit
129	1	0	hit
193	1	0	hit
11	3	2	miss
75	3	2	hit
139	3	2	hit
203	3	2	hit
9	1	2	miss
137	1	2	hit
201	1	2	hit
73	1	2	hit

Hit ratio $= \frac{12}{16} = 0.75$

4. Total Cycles $= \sum (Instructions \times CPI)$
Let C_1 and C_2 be the total Cycles taken by processor 1 and 2 respectively

$$C_1 = (I_A \times CPI_{1A}) + (I_B \times CPI_{1B}) + (I_C \times CPI_{1C}) + (I_D \times CPI_{1D})$$

$$C_2 = (I_A \times CPI_{2A}) + (I_B \times CPI_{2B}) + (I_C \times CPI_{2C}) + (I_D \times CPI_{2D})$$

Where CPI_{1A} , CPI_{1B} , CPI_{1C} , CPI_{1D} represents CPI of each class of instruction for Processor 1
Where CPI_{2A} , CPI_{2B} , CPI_{2C} , CPI_{2D} represents CPI of each class of instruction for Processor 2
$I = 10^6$ instructions
$I_A = 0.2 \times 10^6$ instructions
$I_B = 0.25 \times 10^6$ instructions
$I_C = 0.45 \times 10^6$ instructions
$I_D = 0.1 \times 10^6$ instructions

$$C_1 = 10^6 \times ((0.2 \times 1) + (0.25 \times 2) + (0.45 \times 3) + (0.1 \times 4)) = 2.45 \times 10^6 \; cycles$$

$$C_2 = 10^6 \times ((0.2 \times 2) + (0.25 \times 2) + (0.45 \times 2) + (0.1 \times 2)) = 2.00 \times 10^6 \; cycles$$

Let t_1 and t_2 be time take by processor 1 and 2.

$$t_1 = \frac{C_1}{Clock\ Rate_1} = 1.11 \times 10^{-3} s$$

$$t_2 = \frac{C_2}{Clock\ Rate_2} = 1.25 \times 10^{-3} s$$

So Processor 1 is fast.

5. initial state = | 0 | 0 | 0 | 0 | 0 | last bit is the exclusive bit

(i) | 1 | 0 | 0 | 0 | 0 |
(ii) | 0 | 1 | 0 | 0 | 1 |
(iii) | 0 | 0 | 0 | 1 | 1 |
(iv) | 0 | 0 | 1 | 1 | 0 |
(v) | 0 | 0 | 1 | 0 | 1 |
(vi) | 1 | 0 | 1 | 0 | 0 |

6. Let m_1 and w_1 be the misses and ways respectively for Application 1. Let m_2 and w_2 be the misses and ways respectively for Application 2. Since A.T.P there is a linear interpolation between m and w , the respective equations are:

$$m_1 = -150w_1 + 1300$$

$$m_2 = -50w_2 + 2100$$

L2 cache has in total 8 ways , So let Application one uses x ways and Application 2 uses $(8 - x)$ ways.
A.T.P number of ways of each application ≥ 2

$$x \geq 2$$

$$8 - x \geq 2 \Rightarrow x \leq 6$$

$$2 \leq x \leq 6$$

misses of Application 1 $= -150 \times x + 1300$
misses of Application 2 $= -50 \times (8 - x) + 2100$
total misses = misses of Application 1 + misses of Application 2

$$T = -150 \times x + 1300 + 2100 - 50 \times (8 - x)$$

$$T = -100x + 3000$$

Since T decreases with x , so minimum will be achieved at $x = 6$
So ways for **Application 1 is** 6 **and ways for Application 2 is** 2

7. Let T be the transaction rate
$T_p = 34$ per minute , $T_q = 58$ per minute , $T_r = 81$ per minute

$$Avg(T) = \frac{Total\ Transactions}{Total\ time}$$

Total Transactions = 500 + 500 + 500 = 1500

Total Time $= \frac{500}{T_p} + \frac{500}{T_q} + \frac{500}{T_r}$

$$Avg(T) = \frac{1500}{\frac{500}{T_p} + \frac{500}{T_q} + \frac{500}{T_r}}$$

$$Avg(T) = 50\ per\ minute$$

Since $Avg(T)$ is same as Harmonic mean , We conclude that we used **Harmonic Mean**

8. Let time taken by system 0 is t_0
Let t_i , t_v , t_s be time of initialization , vision processing and signal processing for system 0.
Let T_i , T_v , T_s be time of initialization , vision processing and signal processing for system 1.

$$t_i = 0.25t_0, \;\; t_v = 0.37t_0, \;\; t_s = 0.38t_0$$

Now A.T.P

$$T_i = t_i = 0.25t_0$$
$$T_v = \frac{t_v}{6} = \frac{0.37t_0}{6}$$
$$T_v = \frac{t_s}{10} = \frac{0.38t_0}{10}$$
$$T_0 = T_i + T_v + T_s = 0.25t_0 + \frac{0.37t_0}{6} + \frac{0.38t_0}{10} = 0.3496t_0$$

Speed up of System 1 over System 0 $= \frac{t_0}{T_0} = \frac{1}{0.3496} = 2.86$ times

9. From Linear relationship of voltage and frequency we get $f = 3V$ where $0.8 \leq V \leq 1.2$

$$f_0 = 3Hz, \; V_0 = 1V$$
$$P^0_{total} = 110W$$
$$P^0_{leakage} = 30W$$
$$P^0_{dynamic} = 80W$$
$$t_0 = 30s$$

(i)

$$t = \frac{(t_0 \times f_0)}{f}$$
$$t = \frac{(30 \times 3)}{3 \times V} = \frac{30}{V}$$

So at $V = 1.2$ Volts time taken will be minimum

$$t = \frac{30}{1.2} = 25s$$

(ii)

$$P_{total} = P_{dynamic} + P_{leakage}$$

$$P_{dynamic} = k \times V^2 \times f = k \times V^3$$

$$P_{leakage} = k \times V$$

$$P_{dynamic} = \frac{P^0_{dynamic} \times V^3}{V_0^3} = 80 \times V^3$$

$$P_{leakage} = \frac{P^0_{leakage} \times V}{V_0} = 30 \times V$$

$$P_{total} = (80 \times V^3) + (30 \times V)$$

So minimum Power is at $V = 0.8$ Volts = 64.96 W

(iii)

$$E_{total} = P_{total} \times t$$

$$E_{total} = (80V^3 + 30V) \times \frac{t_0}{V} = (80V^2 + 30) \times t_0$$

So minimum is at $V = 0.8$ Volts = 2436 Joules

10. RAM is 2 GB = 2^{31} bytes = 31 bit representation of Physical Address.
Page Size = 2 KB = 2^{11} bytes $\Rightarrow$ 11 offset bits
Virtual Number bits = Total bits - offset = $48 - 11 = 37$ bits
Physical Number bits = Total- offset = $31 - 11 = 20$ bits
bits in one entry of TLB = $20 + 37 = 57$ bits
TLB size = $entries \times TLB\ \ bits = 32 \times 57 = 228\ \ bytes$

11. Frame size = 1 KB = 2^{10} bytes $\Rightarrow$ 10 offset bits.
Virtual address is of 32 bits so Virtual address stored in Page table is first 22 bits as next 10 bits are offset.
Here $(.)_2$ represents bits are in base 2
(i) 0x4795BA21 $\Rightarrow$ 0x4795B $(10)_2$
(ii) 0x4795BB21 $\Rightarrow$ 0x4795B $(10)_2$
(iii) 0x5795BA21 $\Rightarrow$ 0x5795B $(10)_2$
(iv) 0x4785BA21 $\Rightarrow$ 0x4785B $(10)_2$

Now the Virtual Address number of (i) and (ii) are same , so only first will be transported.
So 3 access will be there i , iii and iv.

12. Access Pattern = **A , B , C , D , A , B , C , D , A , B , C , D**
(a) A : miss , B : miss , C : miss , D : miss , A : miss , B : miss , C : miss , D : miss , A : miss , B : miss , C : miss , D : miss
Total misses = 12

(b) A : miss , B : miss , C : miss , D : miss , A : hit , B : miss , C : miss , D : hit , A : miss , B : miss , C : hit , D : miss
Total misses = 9