Theory Assignment 2 : Homework on Memory Management, Virtual Memory and Flash memory architecture

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1. $(4095)_{10} = (1111111111111)_2$, Page Size = 2KB = 2^{11} bytes = 11 bit offset Page offset = $(111111111111)_2$ = **2047**

Page Number = 1

Page Size = 2KB = 2¹¹ bytes = 11 bit offset
 Physical Frame = 24 - 11 = 13 bit offset
 Inverted Page table contains Physical frame numbers so,
 #of entries = 2¹³

64 -> 32 + 32 (Not possible to hold 57 KB data)

So a segment of 64 KB will be allocated for 57 KB process.

4.

- a. 584
- b. Invalid address
- c. 6326

5.

Segment	Base Length	
0	1100	700
1	9350	550
2	5600	600
3	2200	3400
4	6200	2500

6. To remember the length of each page, to get size of each page and check each logical address to verify that address is in valid range for the process.

7. Outermost Level = 29 bits
Second Level = 13 bits
Third Level = 9 bits

Fourth Level = 6 bits

Offset = 7 bits

8. Initial Order: 320, 580, 480, 220, 890, 600,155

Algorithm	Process (KB)	New Order	
Best Fit	135	320, 580, 480, 220, 890, 600, 20	
	650	320, 580, 480, 220, 240, 600, 20	
	398	320, 580, 82, 220, 240, 600, 20	
	220	320, 580, 82, 0, 240, 600, 20	
	520	320, 60, 82, 0, 240, 600, 20	
	440	320, 60, 82, 0, 240, 160, 20	
Worst Fit	135	320, 580, 480, 220, 755, 600, 155	
	650	320, 580, 480, 220, 105, 600, 155	
	398	320, 580, 480, 220, 105, 202, 155	
	220	320, 360, 480, 220, 105, 202, 155	
	520	Not allocated	
	440	320, 360, 40, 220, 105, 202, 155	

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0 (VALID)	5 (VALID)	INVALID	4 (VALID)	INVALID
6 (VALID)	INVALID	2 (VALID)	1 (VALID)	INVALID
FREE	8 (VALID)	3 (VALID)	7 (VALID)	INVALID

4 erase operations were performed at write operation number 16,18,20,23.

10. # logical pages = $2^{36}/2^{12} = 2^{24}$ pages # physical pages = $4 \times 2^{24} = 2^{26}$ pages Table Size = TS = # logical pages*log(# physical pages) bits = $2^{24} \times 26$ bits = **52 MB**