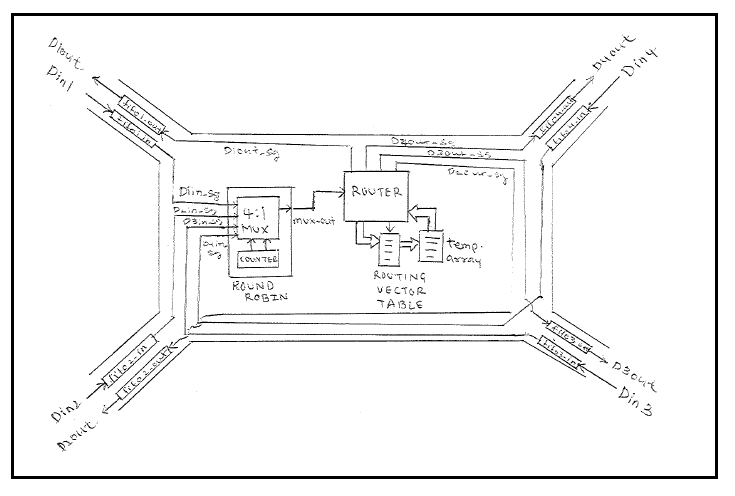
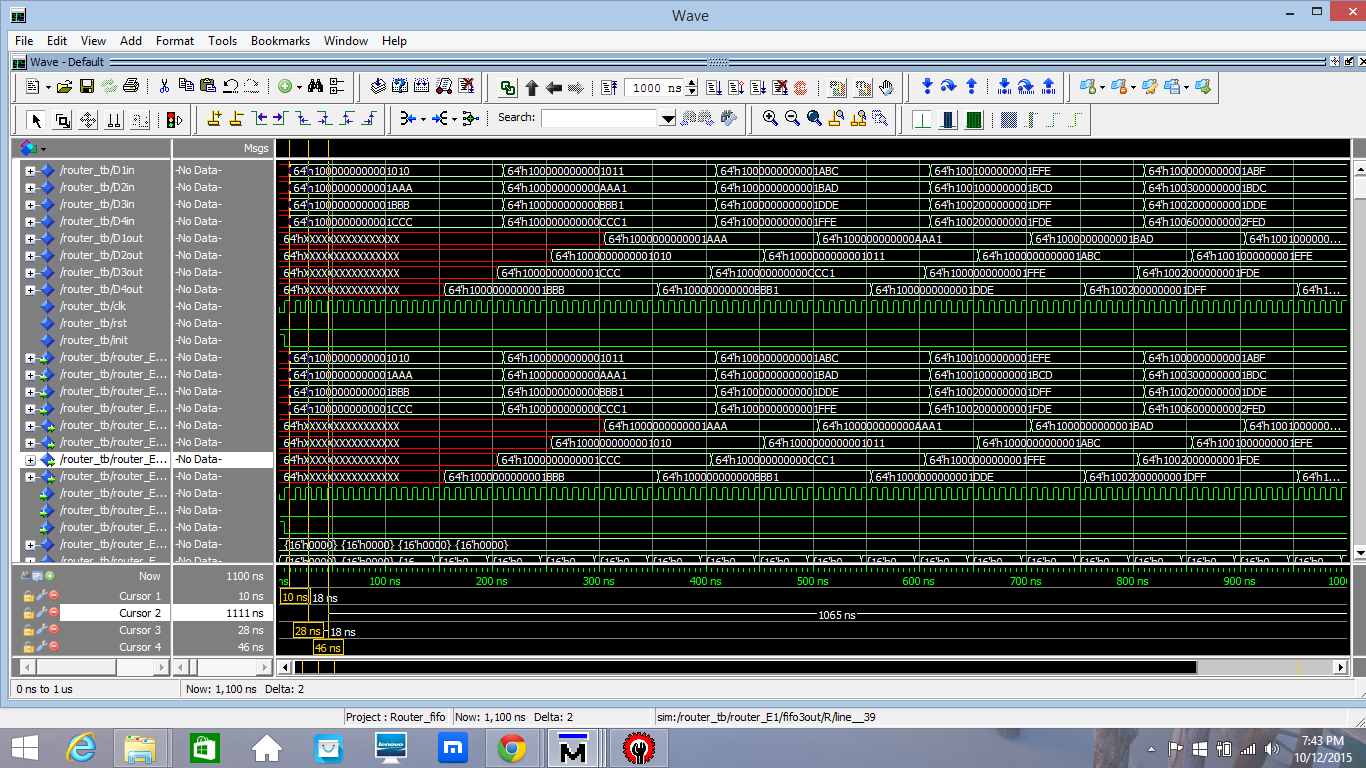
IMPLEMENTING GATEWAY ROUTER USING FIFOs in VHDL

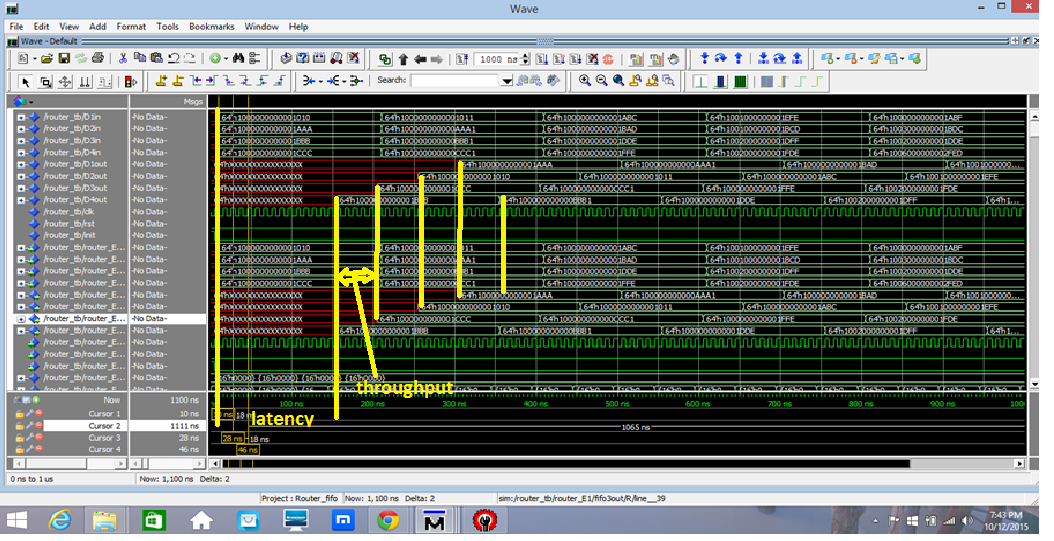
GATEWAY ROUTER SCHEMATIC:



OUTPUT WAVEFORMS



**LATENCY** is defined as the time taken for a particular signal to transverse from the input to the output of the system and **THROUGHPUT** is defined as the time between two consecutive outputs of the system.

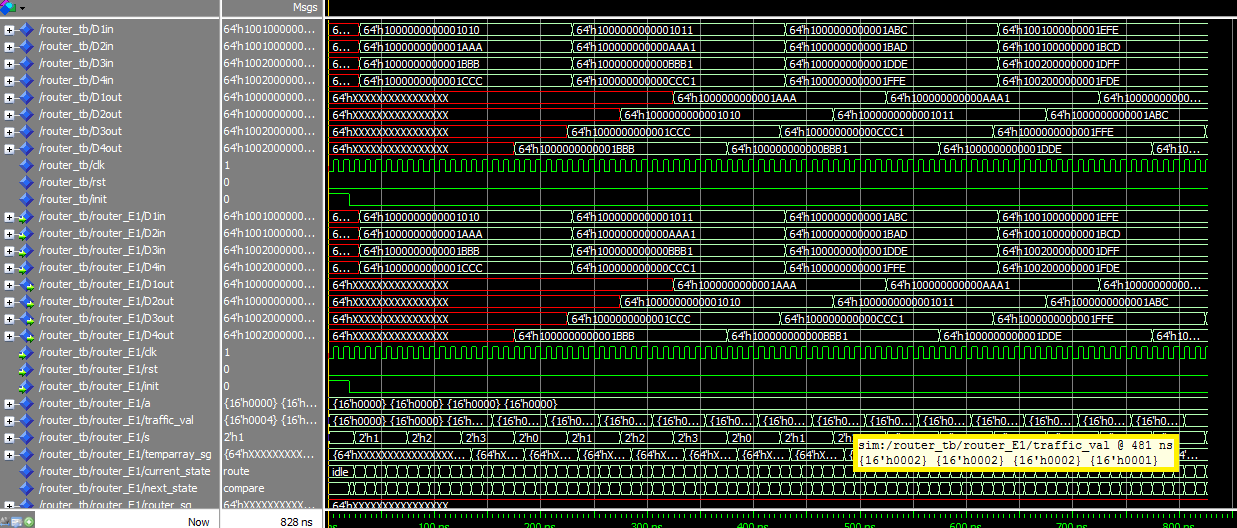


From the above waveforms it is clear that the average latency of the system is 14 clock cycles and throughput of the system is 5 clock cycles.

CLOCK PERIOD IS 10 ns.

**TRAFFIC DETAILS:**

**The array traffic\_val constantly updates the traffic at each output FIFO.**



The above waveforms clearly show that at the moment output of FIFO1 has least traffic (0001). The traffic details are in the order of FIFO 4 to 1. So, the next packet has to be routed from output FIFO of gateway1.

The next waveform shows this updation.

