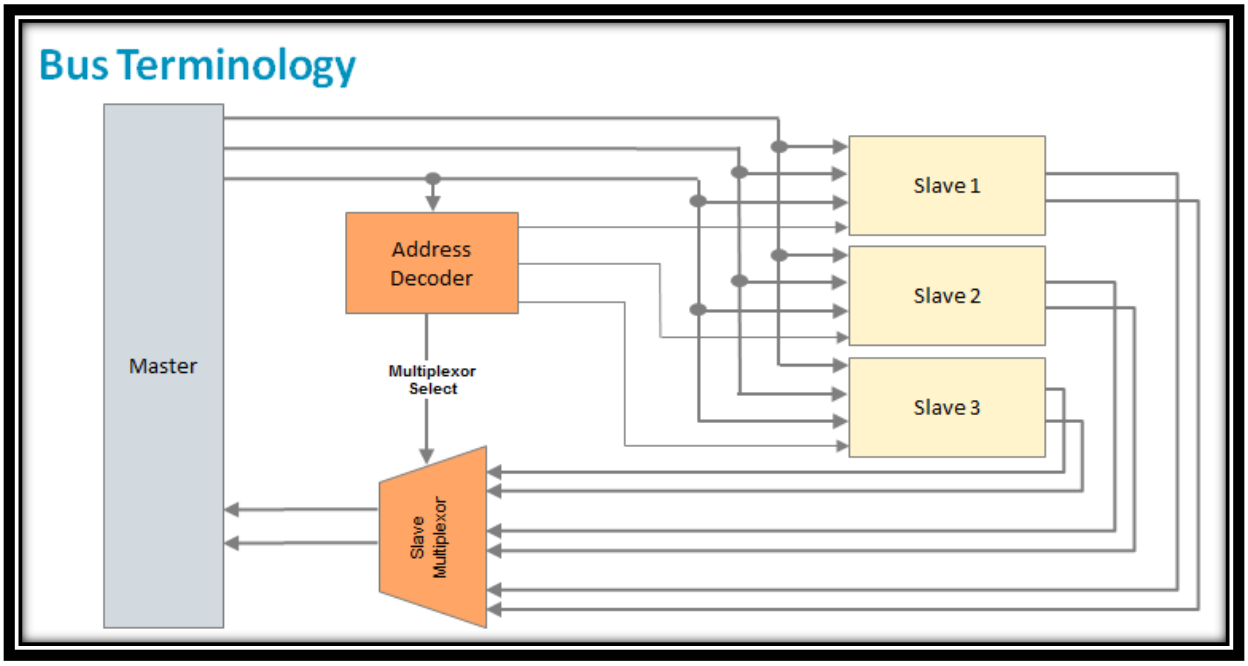
Synthesis of Cortex M0(AT510-MN-80001-r2p0-00rel0) in FPGA using DesignEval



A "**master**" (or initiator) refers to the IP component that initiates a read or write data transfer (e.g., processor or DSP).

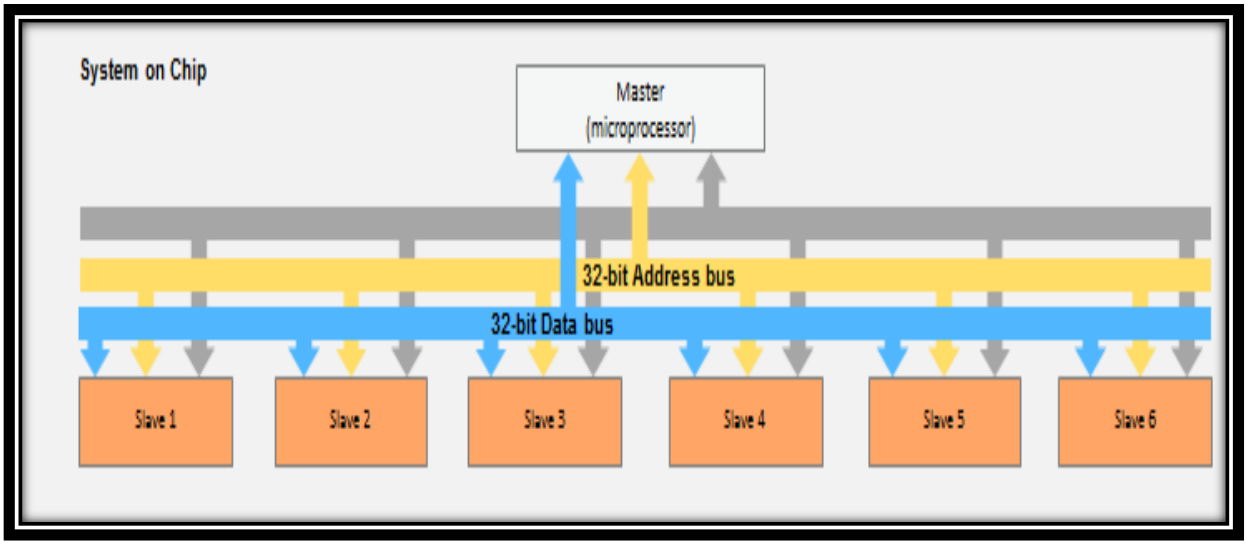
A "**slave**" (or target) refers to the IP component that does not initiate transfers and only responds to incoming transfer requests (e.g., memory block).

A "**decoder**" refers to a logic block that decodes the destination address of a data transfer initiated by a master, and selects the appropriate slave to receive the data.

A **multiplexor** is used to multiplex the read data bus and response signals from the slaves to the master. The decoder provides control for the multiplexor.

A bus typically consists of three types of signal lines:

- The data bus is used to exchange data information.
- The address bus is used to select one of the peripherals (or one register of a peripheral).
- Control signals are used to synchronize and identify transactions, such as ready, write/read, and transfer mode signals.



Arm AMBA System Bus

AMBA: Advanced microcontroller bus architecture

- AMBA protocol is an open standard on-chip interconnect specification.
- Provides the interface standard that enables IP reuse
- Facilitates right-first-time development of multiprocessor designs with large numbers of controllers and peripherals
- Widely used in modern portable mobile devices, such as tablets and smartphones

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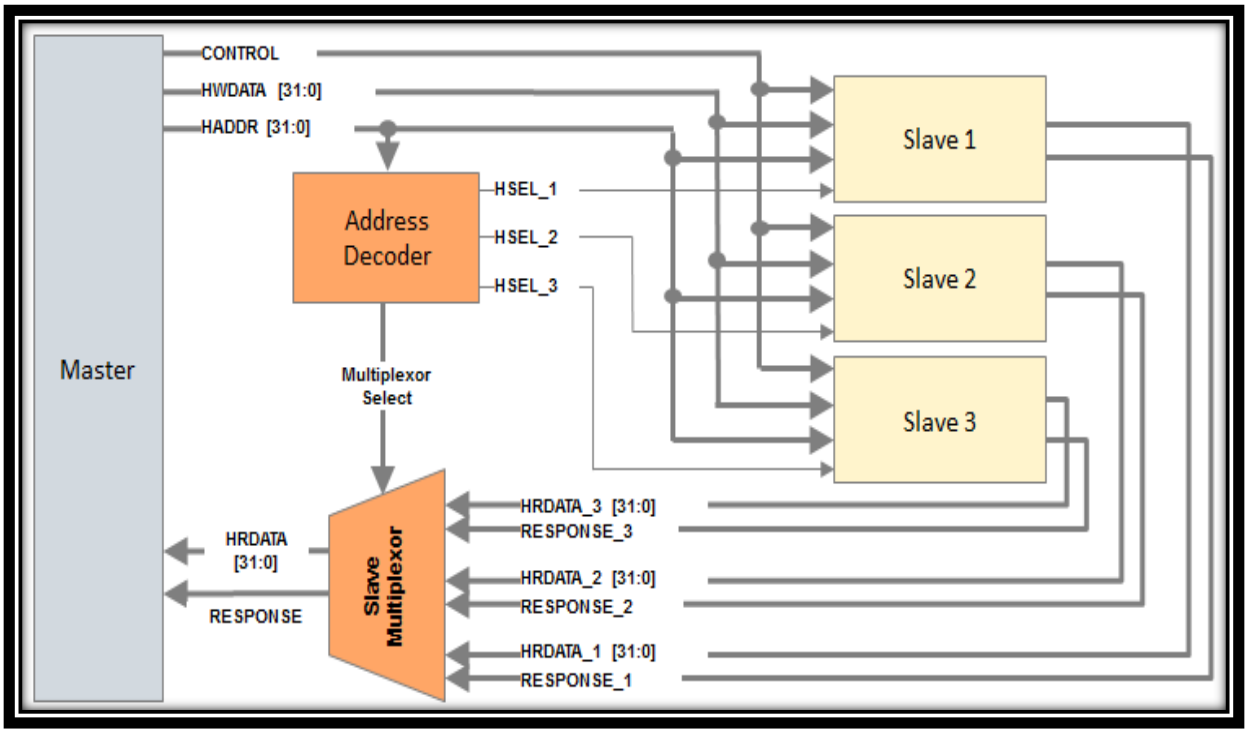
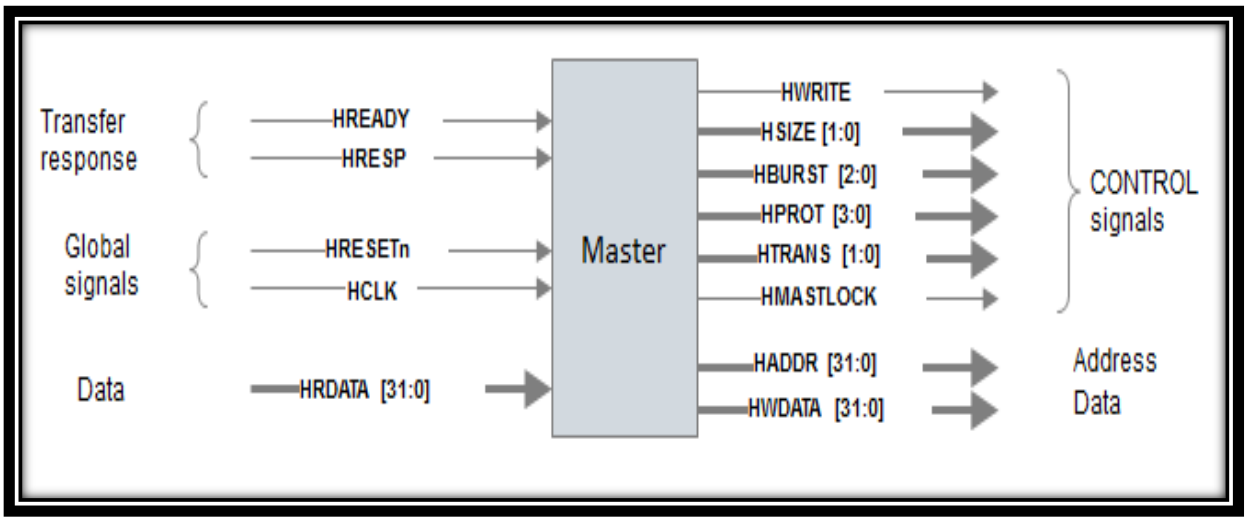


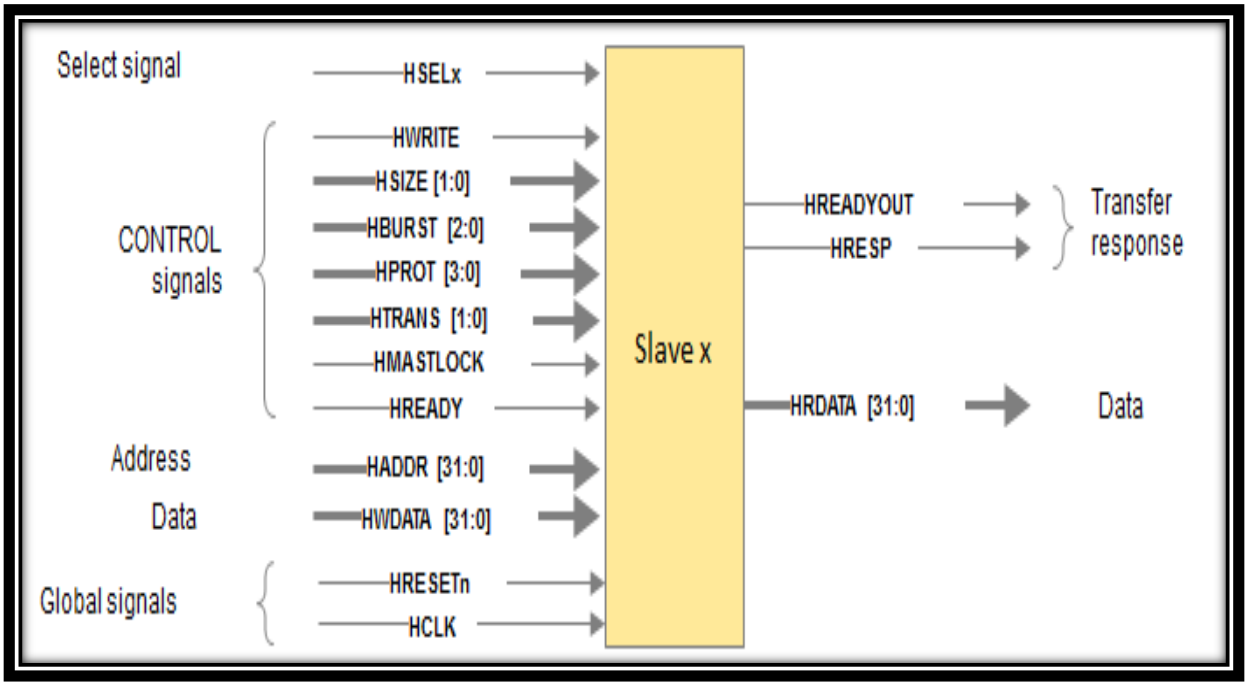
The above shows a single master AHB-Lite system design with one AHB-Lite master and three AHB-Lite slaves. The decoder block is controlled by the master that specifies which slave must be selected.

The multiplexor block is controlled by the decoder that chooses which slave output data must be connected to the master.

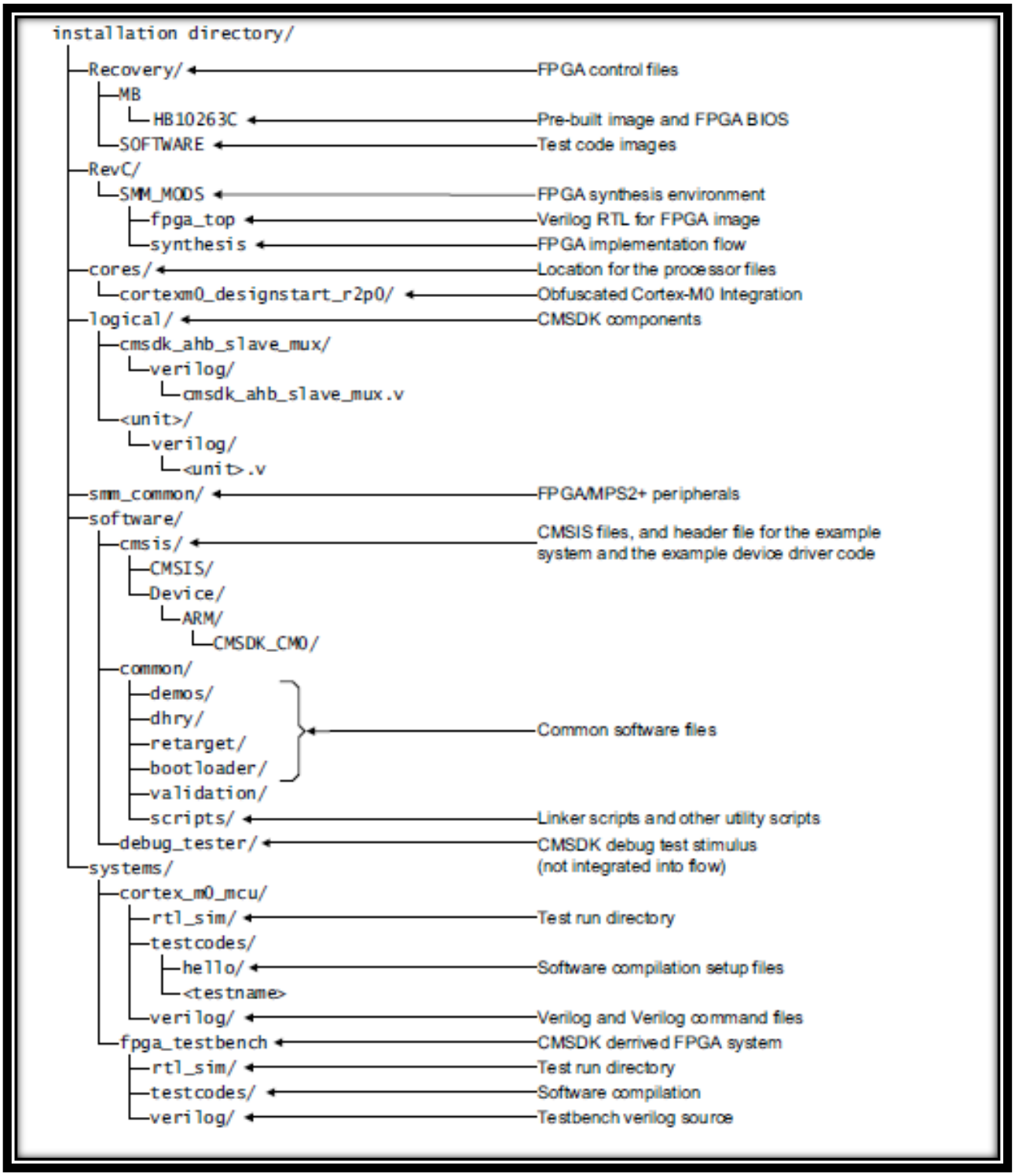
Master bus Interface



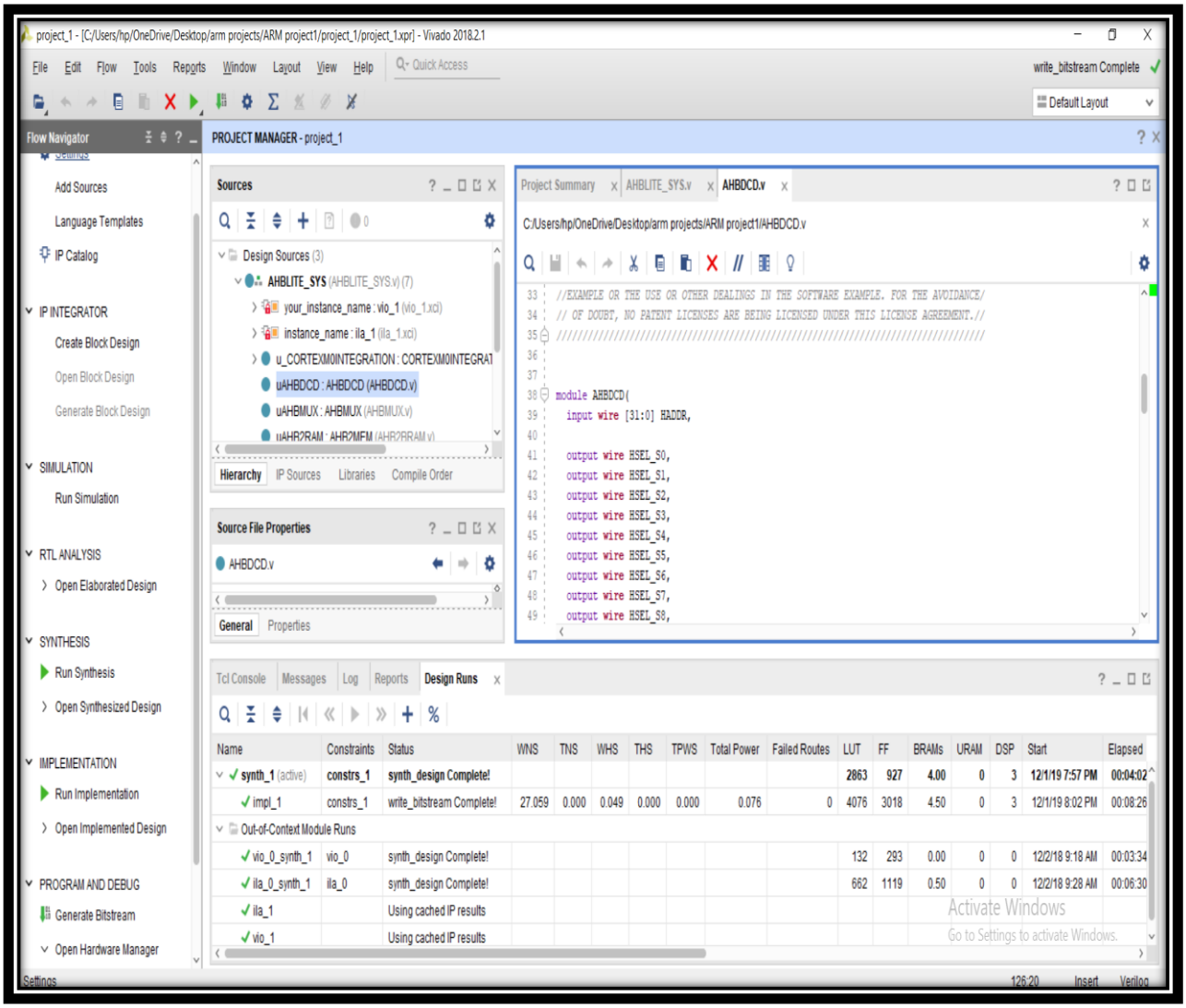
Slave Interface



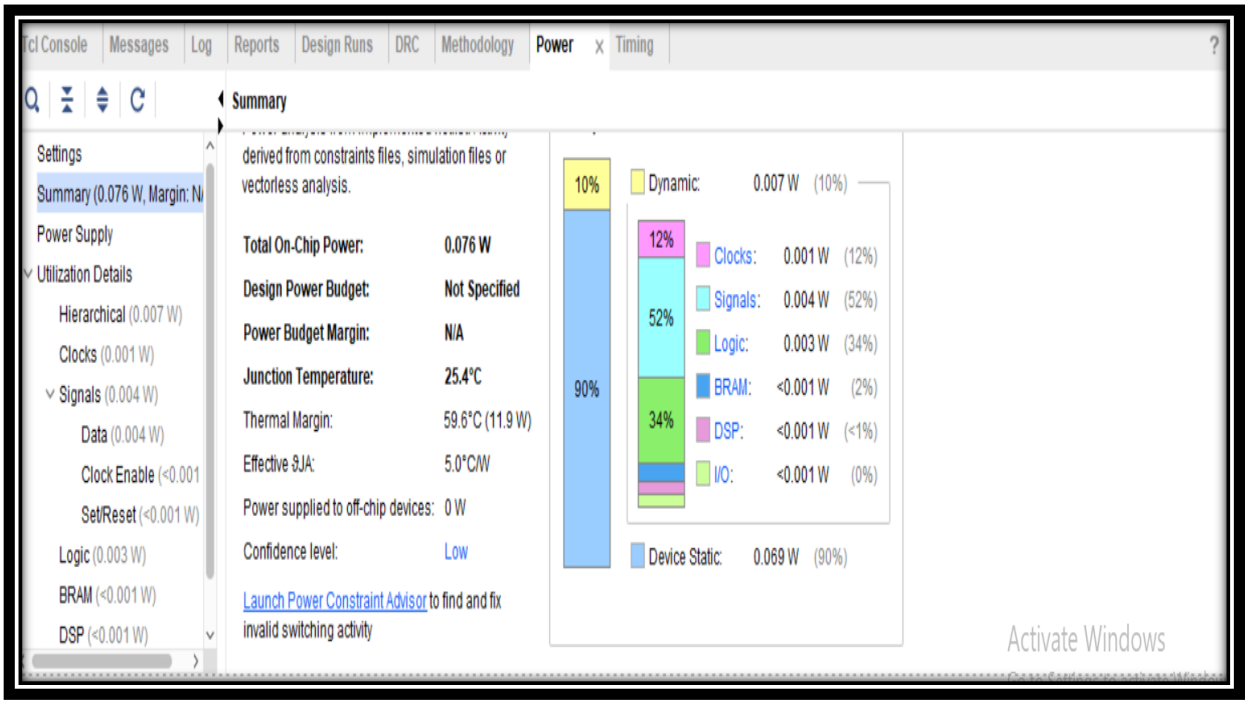
Structure of Cortex M0(AT510-MN-80001-r2p0-00rel0) Integration file



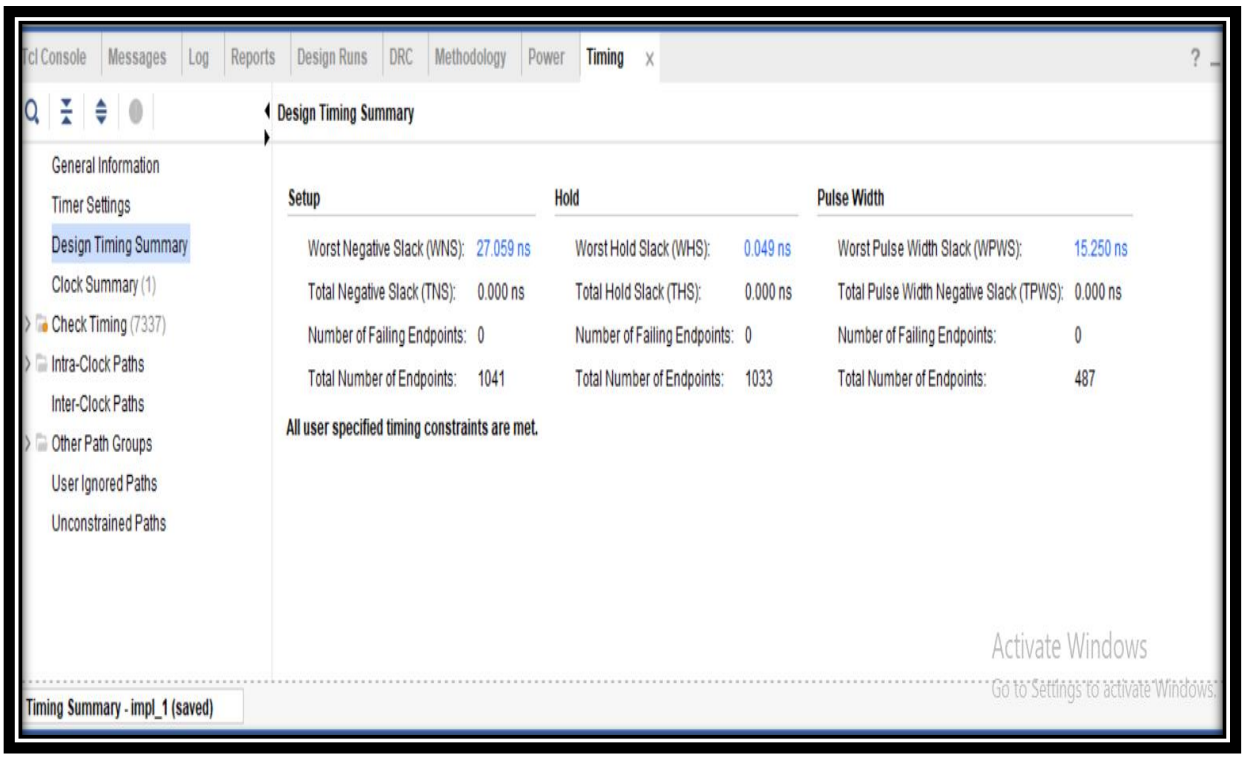
Verilog view



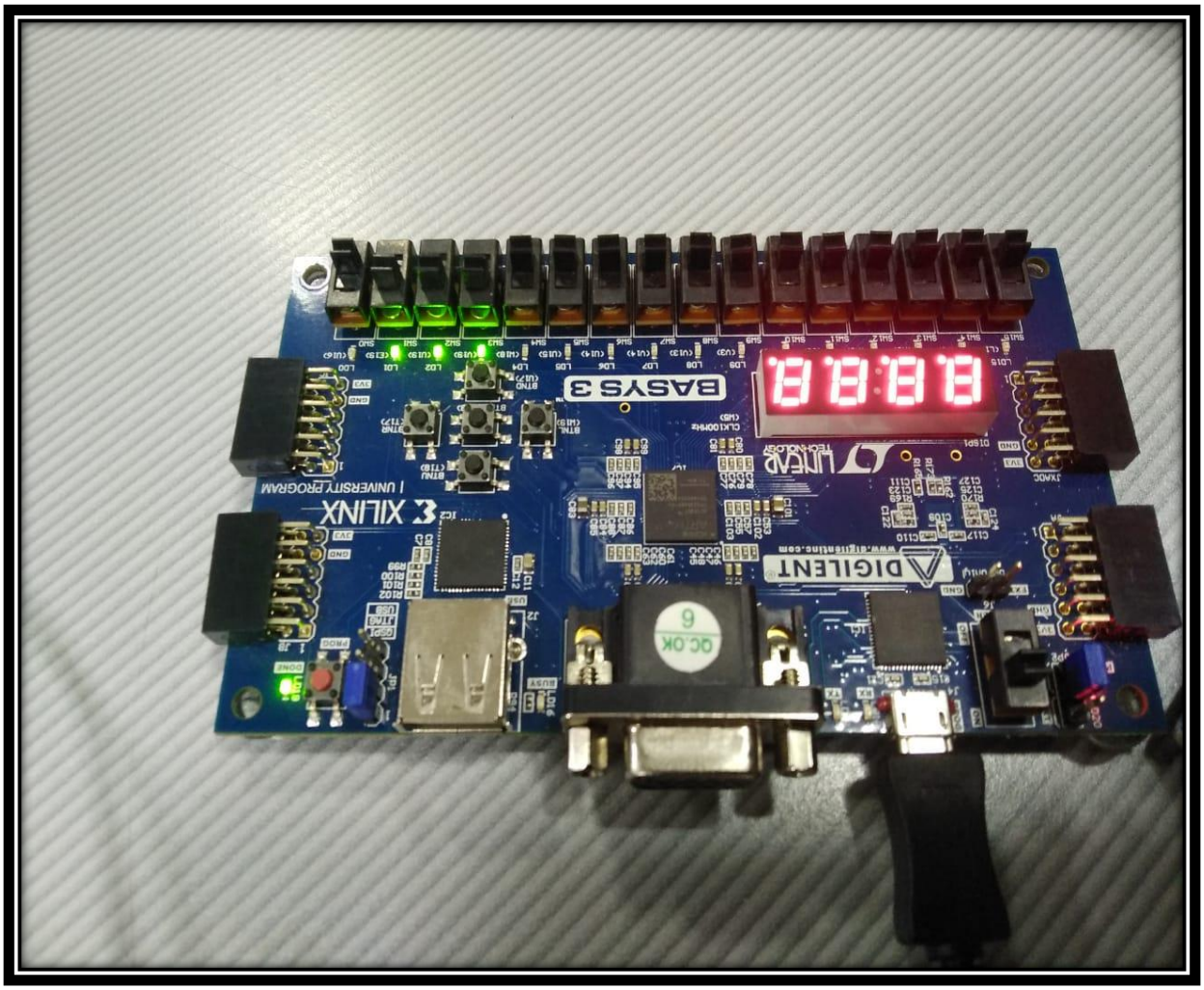
Power consumed during code synthesis



Timing summary



Result



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