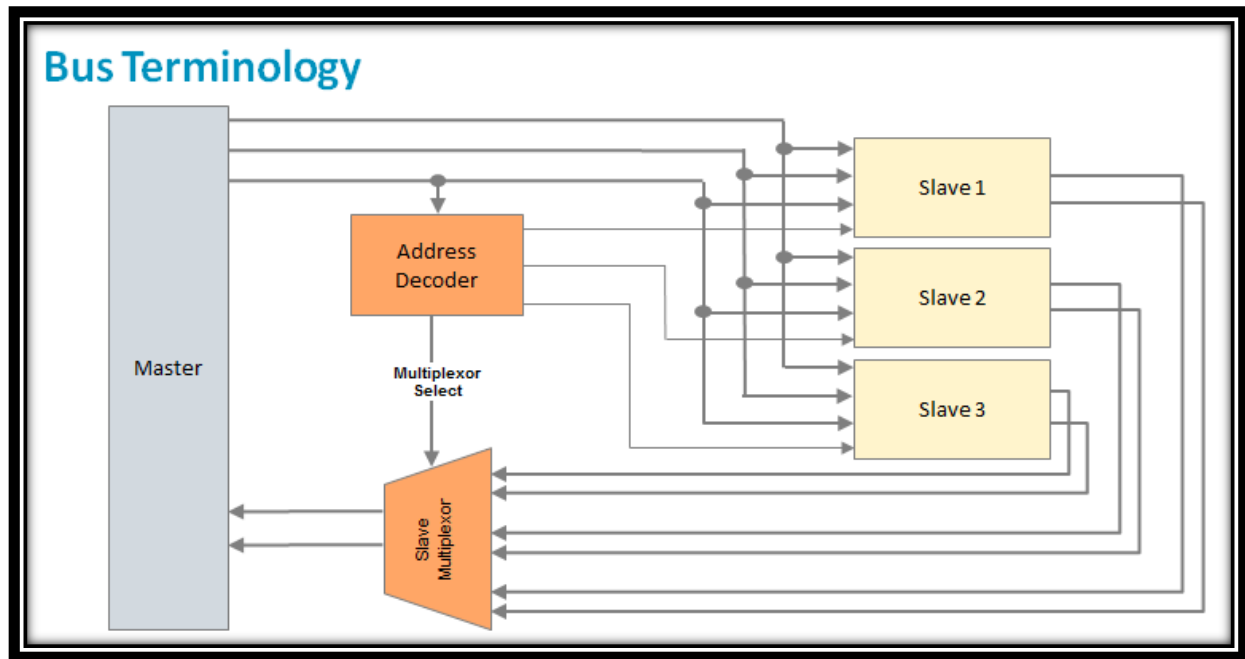


Synthesis of Cortex M0(AT510-MN-80001-r2p0-00rel0) in FPGA using DesignEval



A “**master**” (or initiator) refers to the IP component that initiates a read or write data transfer (e.g., processor or DSP).

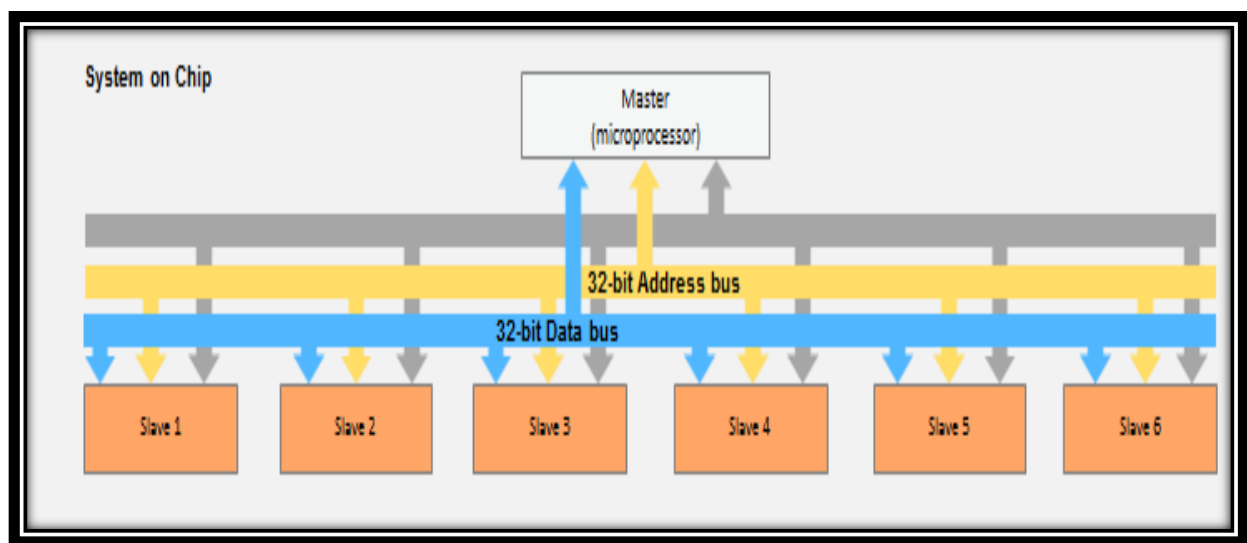
A “**slave**” (or target) refers to the IP component that does not initiate transfers and only responds to incoming transfer requests (e.g., memory block).

A “**decoder**” refers to a logic block that decodes the destination address of a data transfer initiated by a master, and selects the appropriate slave to receive the data.

A **multiplexor** is used to multiplex the read data bus and response signals from the slaves to the master. The decoder provides control for the multiplexor.

A bus typically consists of three types of signal lines:

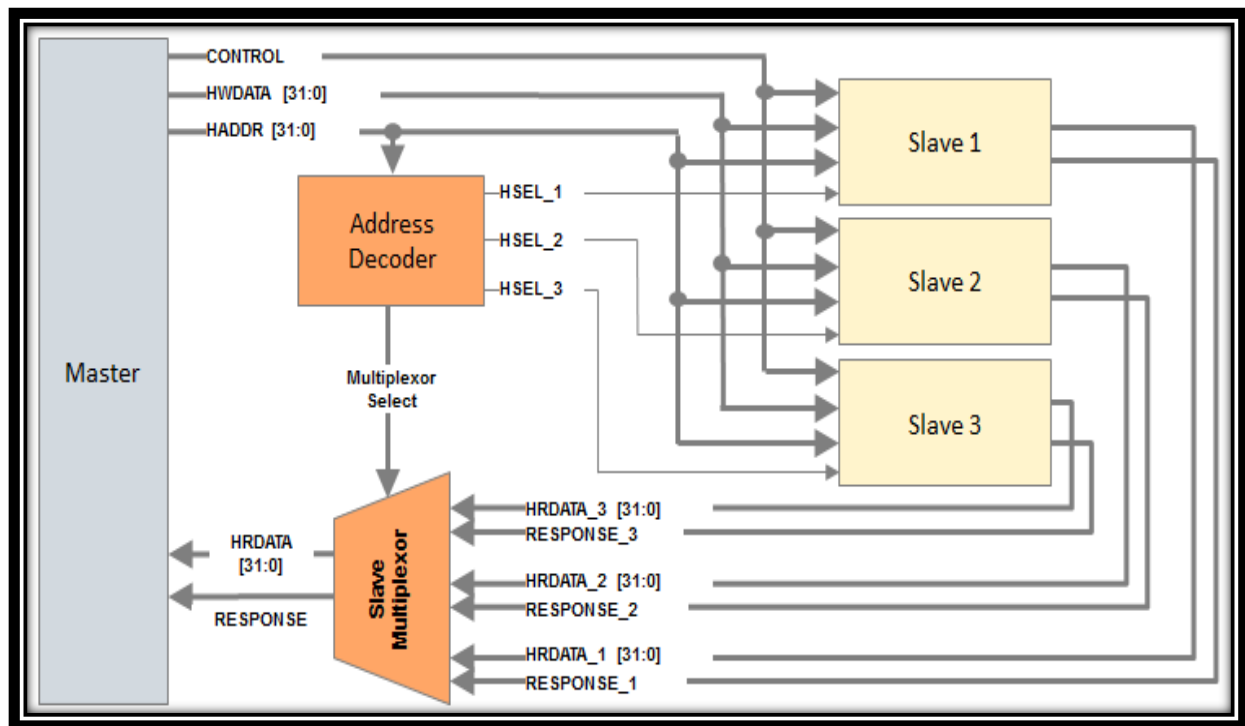
- The data bus is used to exchange data information.
- The address bus is used to select one of the peripherals (or one register of a peripheral).
- Control signals are used to synchronize and identify transactions, such as ready, write/read, and transfer mode signals.



Arm AMBA System Bus

AMBA: Advanced microcontroller bus architecture

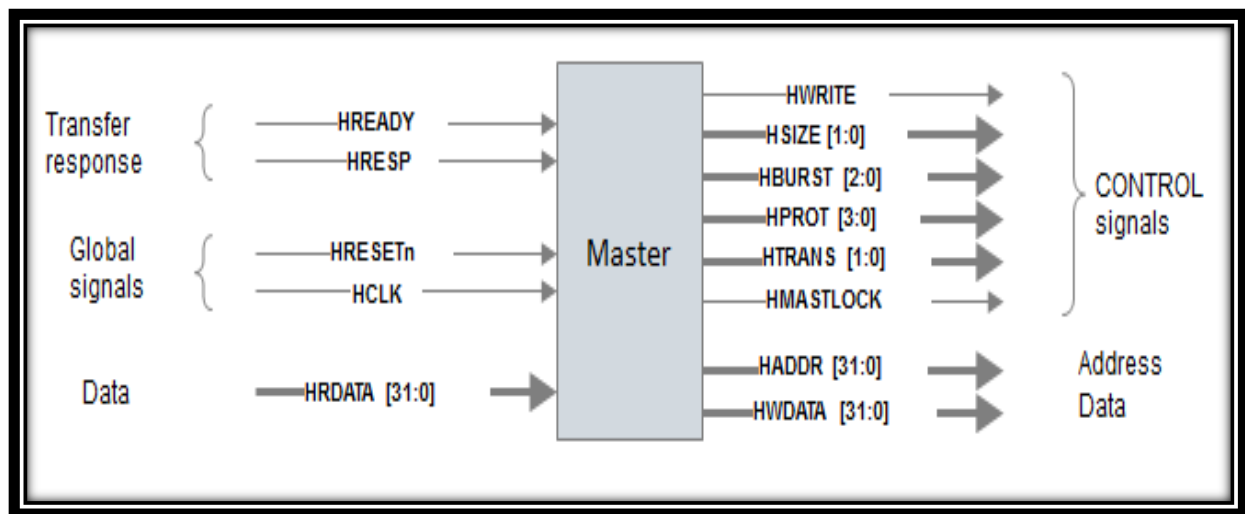
- AMBA protocol is an open standard on-chip interconnect specification.
- Provides the interface standard that enables IP reuse
- Facilitates right-first-time development of multiprocessor designs with large numbers of controllers and peripherals
- Widely used in modern portable mobile devices, such as tablets and smartphones



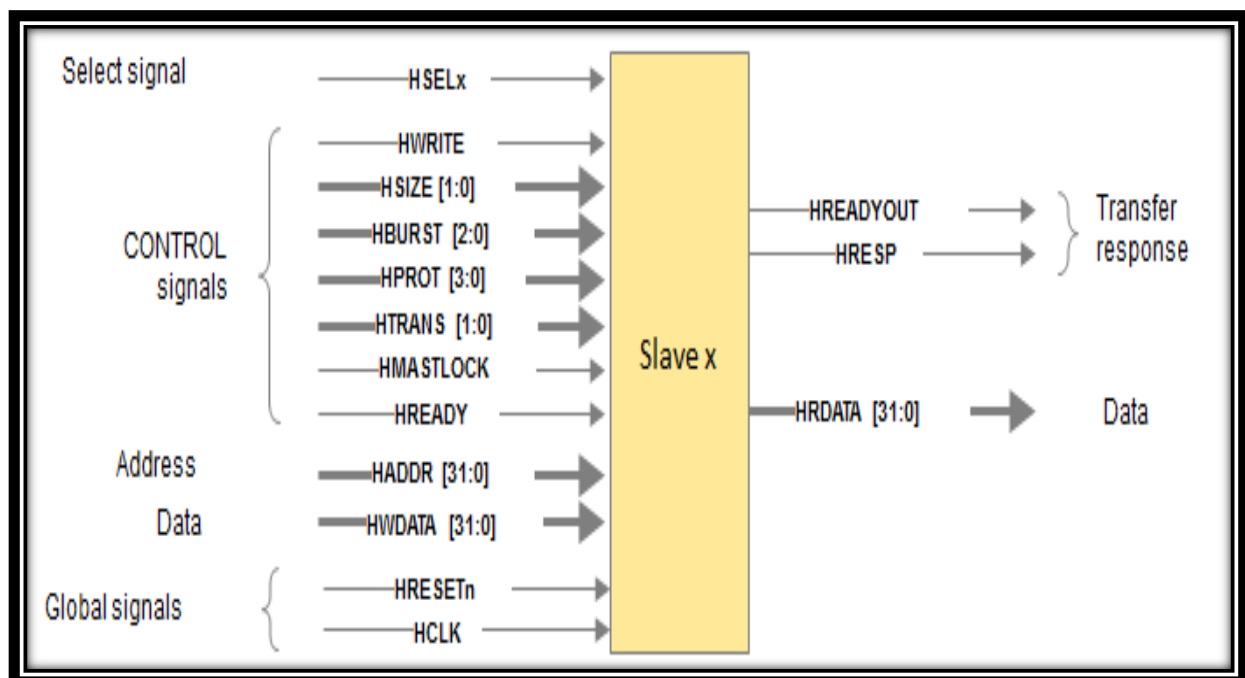
The above shows a single master AHB-Lite system design with one AHB-Lite master and three AHB-Lite slaves. The decoder block is controlled by the master that specifies which slave must be selected.

The multiplexor block is controlled by the decoder that chooses which slave output data must be connected to the master.

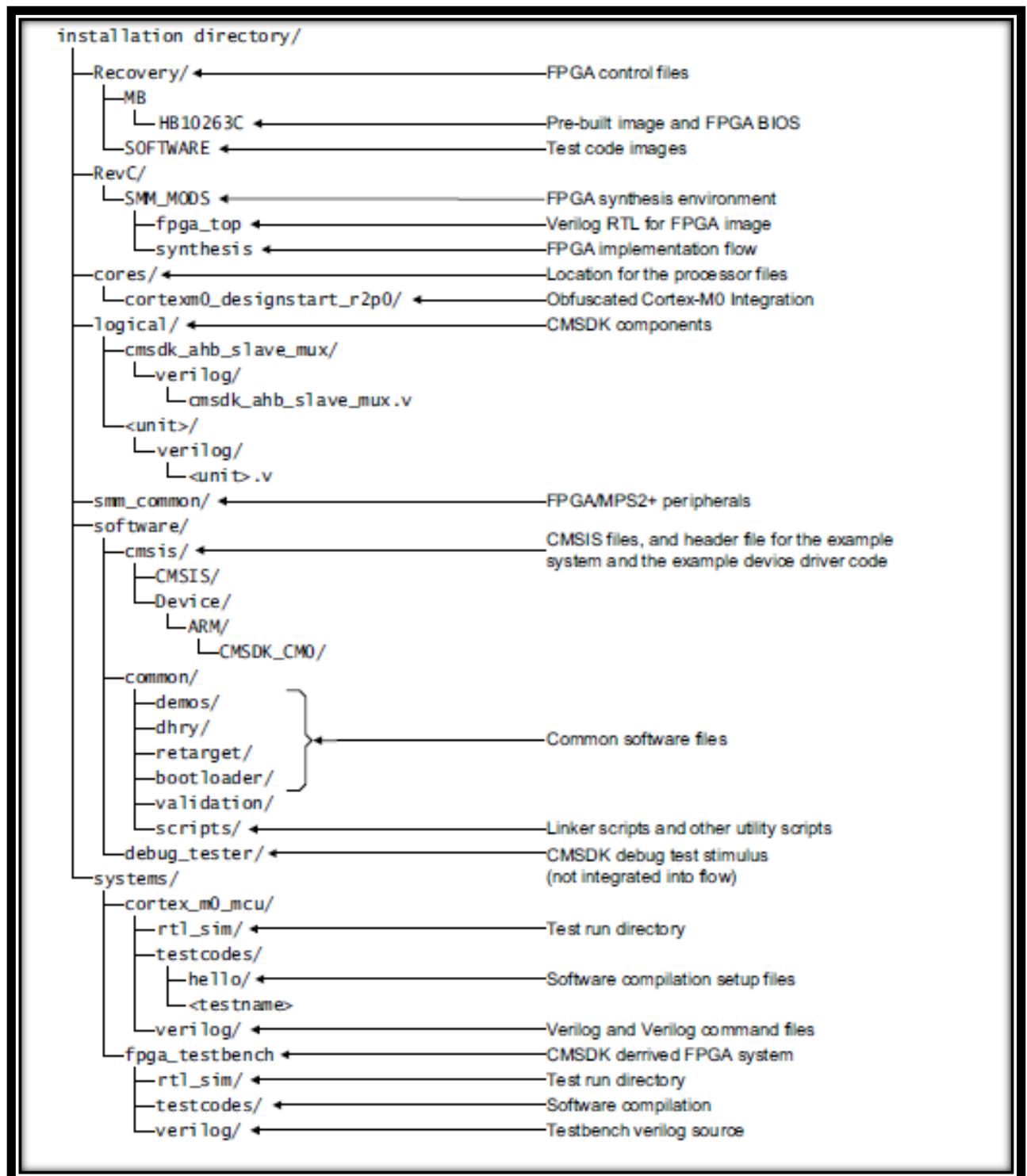
Master bus Interface



Slave Interface



Structure of Cortex M0(AT510-MN-80001-r2p0-00rel0) Integration file



Verilog view

project_1 - [C:/Users/hp/OneDrive/Desktop/arm projects/ARM project1/project_1xpr] - Vivado 2018.2.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

write_bitstream Complete

Default Layout

Flow Navigator

PROJECT MANAGER - project_1

Sources

Design Sources (3)

- AHBLITE_SYS (AHBLITE_SYS.v) (7)
 - your_instance_name : vio_1 (vio_1.xci)
 - instance_name : ila_1 (ila_1.xci)
 - u_CORTEXMMIOINTEGRATION : CORTEXMMIOINTEGRAT
 - uABBOCD : ABBOCD (ABBOCD.v)
 - uAHBMUX : AHBMUX (AHBMUX.v)
 - uAHR2RAM : AHR2MFM (AHR2RAM.v)

Hierarchy IP Sources Libraries Compile Order

Source File Properties

ABBOCD.v

General Properties

Project Summary x AHBLITE_SYS.v x ABBOCD.v x

C:/Users/hp/OneDrive/Desktop/arm projects/ARM project1/ABBOCD.v

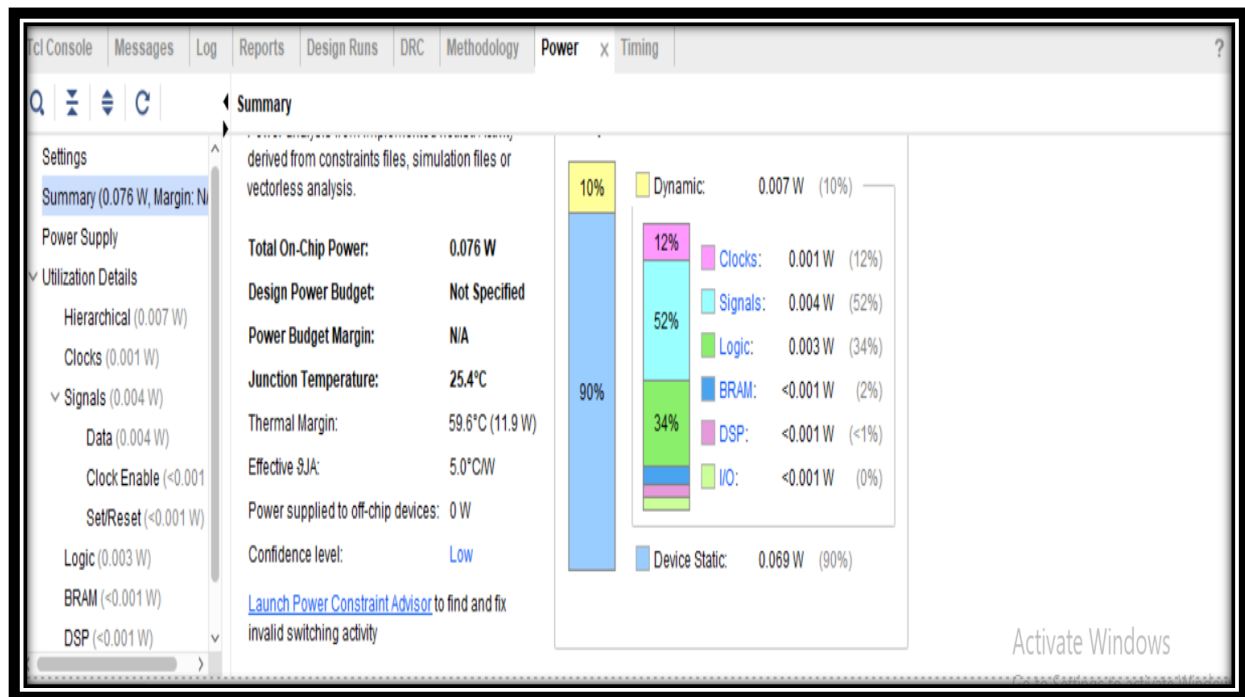
```
33 //EXAMPLE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE EXAMPLE. FOR THE AVOIDANCE//
34 // OF DOUBT, NO PATENT LICENSES ARE BEING LICENSED UNDER THIS LICENSE AGREEMENT.//
35 ///////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
36
37
38 module ABBOCD(
39     input wire [31:0] HADDR,
40
41     output wire HSEL_S0,
42     output wire HSEL_S1,
43     output wire HSEL_S2,
44     output wire HSEL_S3,
45     output wire HSEL_S4,
46     output wire HSEL_S5,
47     output wire HSEL_S6,
48     output wire HSEL_S7,
49     output wire HSEL_S8,
```

Tcl Console Messages Log Reports Design Runs x

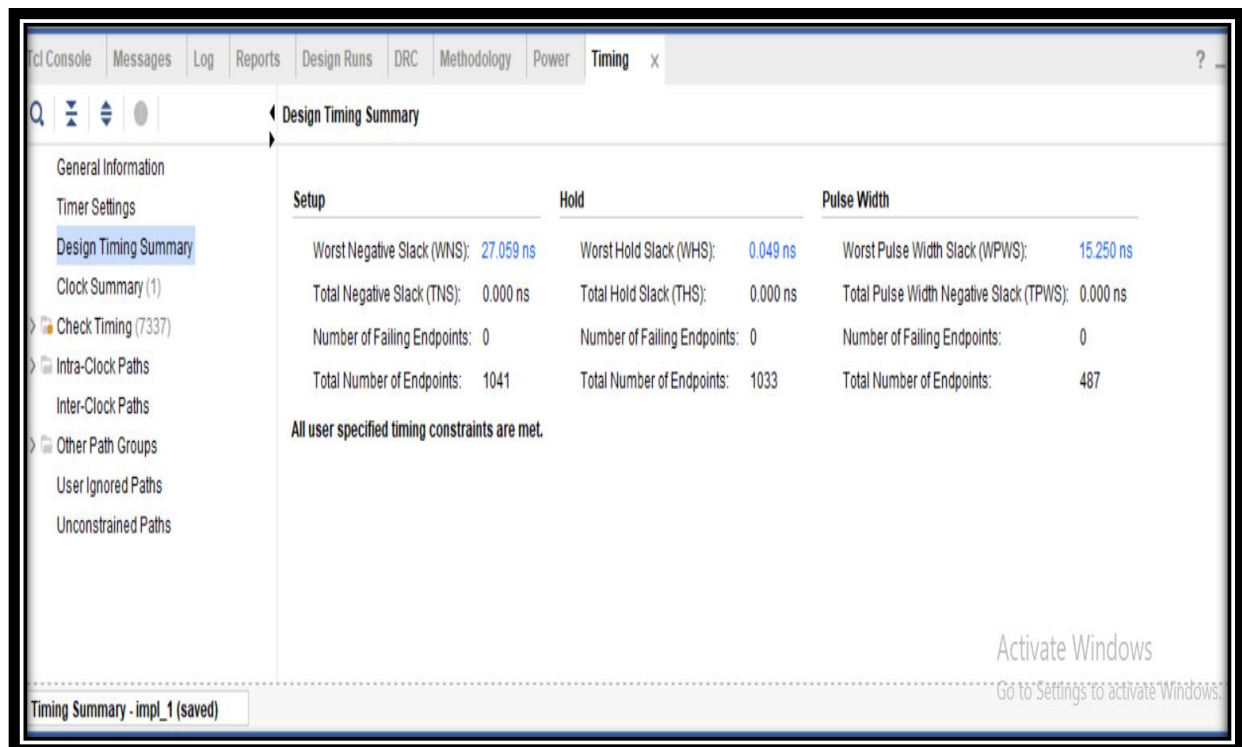
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed
✓ synth_1 (active)	constrs_1	synth_design Complete!								2863	927	4.00	0	3	12/1/19 7:57 PM	00:04:02
✓ impl_1	constrs_1	write_bitstream Complete!	27.059	0.000	0.049	0.000	0.000	0.076	0	4076	3018	4.50	0	3	12/1/19 8:02 PM	00:08:26
Out-of-Context Module Runs																
✓ vio_0_synth_1	vio_0	synth_design Complete!								132	293	0.00	0	0	12/2/18 9:18 AM	00:03:34
✓ ila_0_synth_1	ila_0	synth_design Complete!								662	1119	0.50	0	0	12/2/18 9:28 AM	00:06:30
✓ ila_1		Using cached IP results														
✓ vio_1		Using cached IP results														

Settings 128.20 Insert Verilog

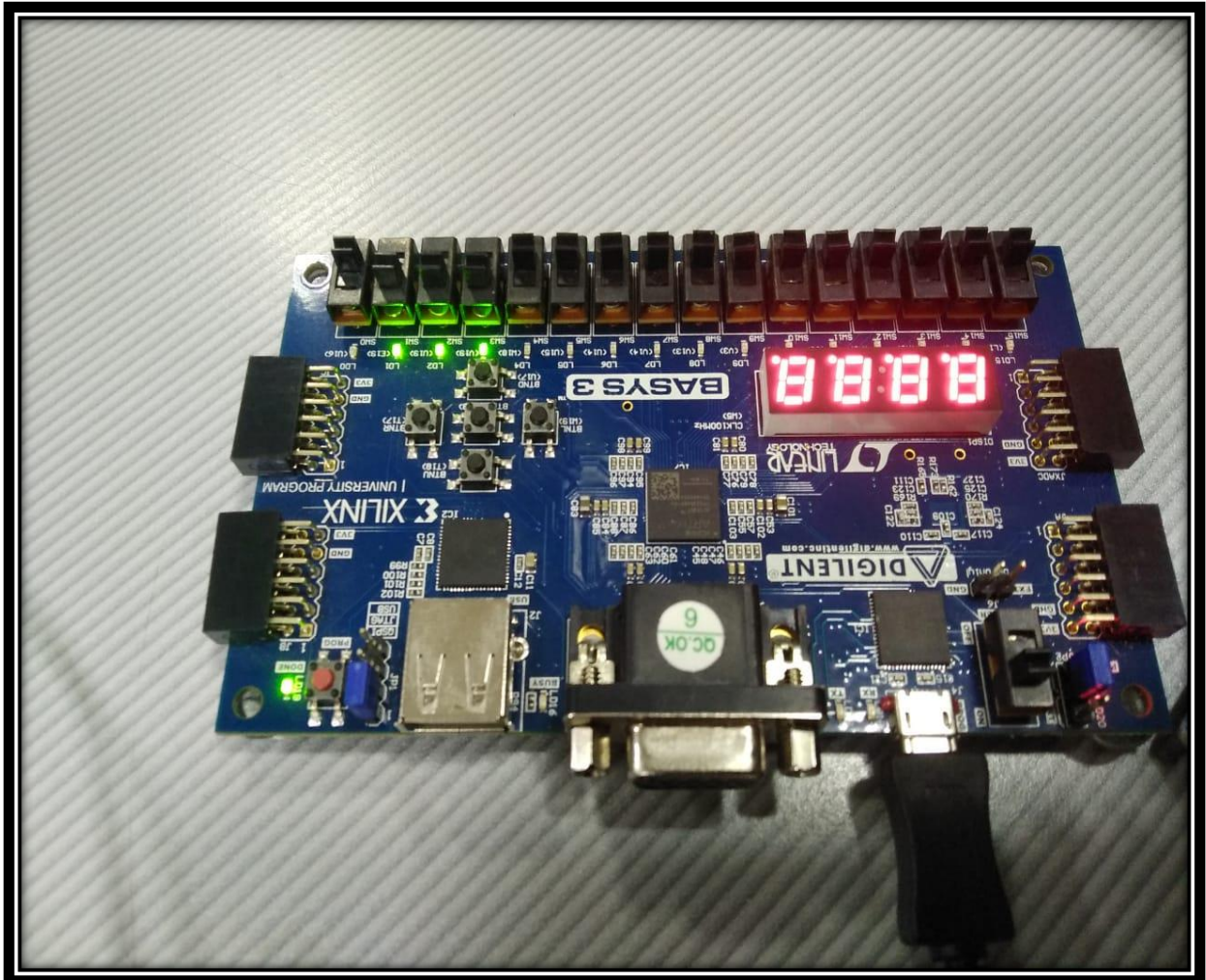
Power consumed during code synthesis



Timing summary



Result



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