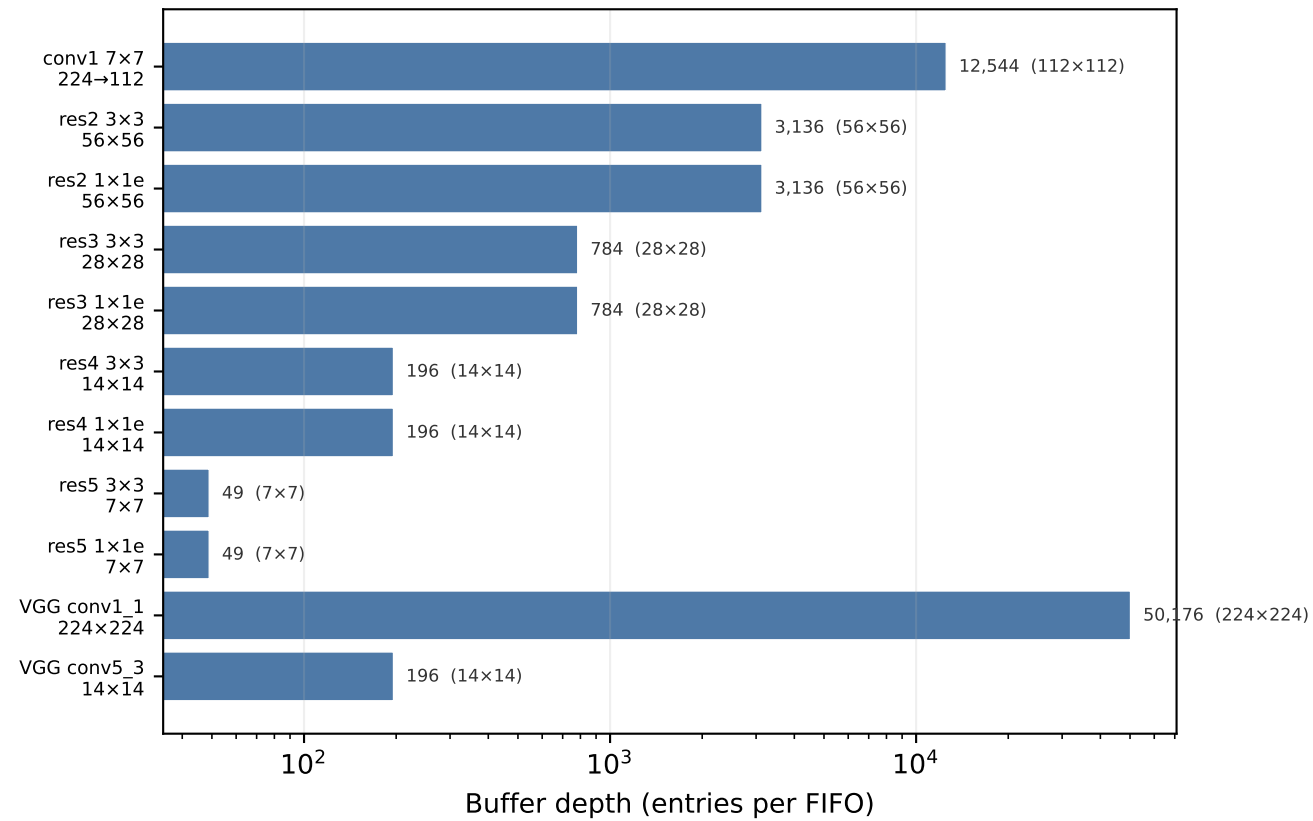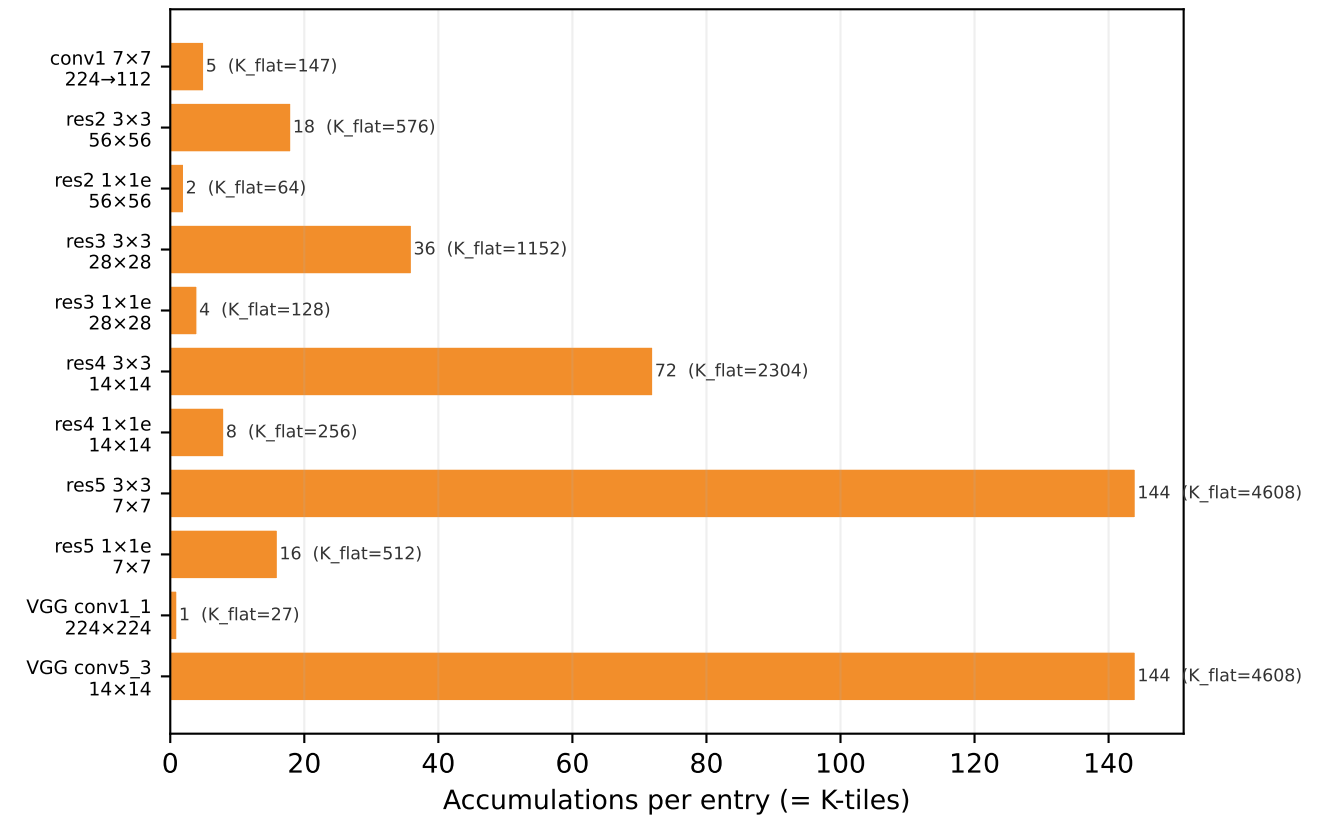**PSUM Direct-Mapped Routing — Buffer Analysis**
col c → buf c | FIFO sizing, accumulation depth, verification
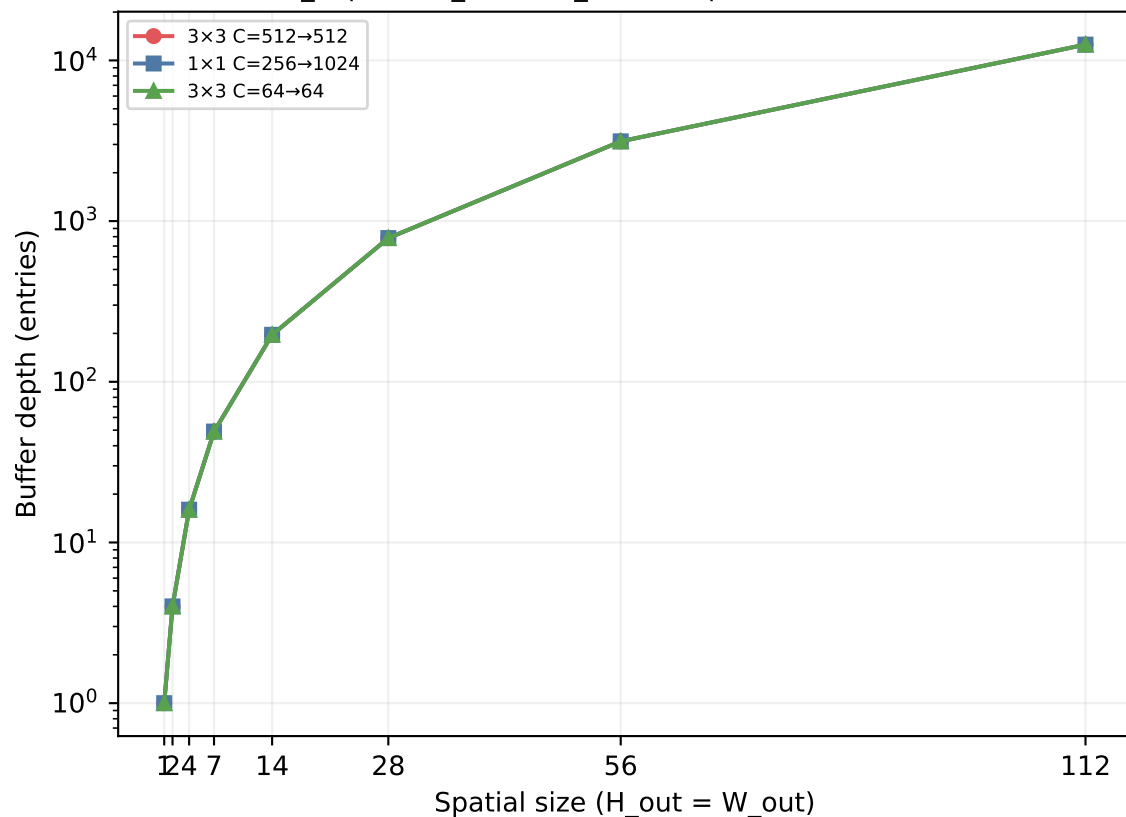
(a) FIFO Buffer Depth per Layer
= H_out × W_out (N=1)

- conv1 7×7 224→112: 12,544 (112×112)
- res2 3×3 56×56: 3,136 (56×56)
- res2 1×1e 56×56: 3,136 (56×56)
- res3 3×3 28×28: 784 (28×28)
- res3 1×1e 28×28: 784 (28×28)
- res4 3×3 14×14: 196 (14×14)
- res4 1×1e 14×14: 196 (14×14)
- res5 3×3 7×7: 49 (7×7)
- res5 1×1e 7×7: 49 (7×7)
- VGG conv1_1 224×224: 50,176 (224×224)
- VGG conv5_3 14×14: 196 (14×14)

Buffer depth (entries per FIFO)

(b) Accumulations per Buffer Entry
each entry accumulated K-tile times before drain

- conv1 7×7 224→112: 5 (K_flat=147)
- res2 3×3 56×56: 18 (K_flat=576)
- res2 1×1e 56×56: 2 (K_flat=64)
- res3 3×3 28×28: 36 (K_flat=1152)
- res3 1×1e 28×28: 4 (K_flat=128)
- res4 3×3 14×14: 72 (K_flat=2304)
- res4 1×1e 14×14: 8 (K_flat=256)
- res5 3×3 7×7: 144 (K_flat=4608)
- res5 1×1e 7×7: 16 (K_flat=512)
- VGG conv1_1 224×224: 1 (K_flat=27)
- VGG conv5_3 14×14: 144 (K_flat=4608)

Accumulations per entry (= K-tiles)

(c) Buffer Depth Scaling
buf_depth = H_out × W_out (independent of channels)

- 3×3 C=512→512
- 1×1 C=256→1024
- 3×3 C=64→64

Spatial size (H_out = W_out)
Buffer depth (entries)

(d) Sim-Verified Configs (green = PASS)
includes small IFMap, non-div-32, batched, strided

- 3×3 Cin=128 Cout=128 28×28: ✓ buf=784 K-tiles=36
- 1×1 Cin=256 Cout=1024 14×14: ✓ buf=196 K-tiles=8
- 7×7 Cin=3 Cout=64 224→112 s=2: ✓ buf=16 K-tiles=5
- 3×3 Cin=512 Cout=512 7×7: ✓ buf=49 K-tiles=144
- 1×1 Cin=512 Cout=2048 7×7: ✓ buf=49 K-tiles=16
- 3×3 Cin=256 Cout=256 4×4: ✓ buf=16 K-tiles=72
- 1×1 Cin=256 Cout=256 2×2: ✓ buf=4 K-tiles=8
- 1×1 Cin=512 Cout=2048 1×1: ✓ buf=1 K-tiles=16
- Kflat=90 Cout=48 (non-div-32): ✓ buf=16 K-tiles=3
- s=2 pad=1 N=2 (batched): ✓ buf=32 K-tiles=9

K-tiles (accumulations)