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Design of a Residue Amplifier for Pipelined ADCs

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Abstract

This document will present the design of a residue amplifier for a two stages, $13\,ENOB$*, pipelined ADC in STM* $28\,\mathrm{nm}$ *FDSOI technology.*
The amplifier is based on the folded cascode configuration and uses a positive feedback gain enhancing technique presented first in [2]. A second stage is used to increase the overall gain and the output swing. The results show a typical low frequency gain of $95\,\mathrm{dB}$*, a GBW of* $3.5\,\mathrm{GHz}$*, differential output swing of* $1.8\,\mathrm{V}_{pp}$ *and a overall power consumption of* $240\,\mu\mathrm{W}$ *with* $1\,\mathrm{V}$ *supply voltage.*
The amplifier uses a switched capacitor CMFB and it is inserted in a correlated double sampling switched capacitor feedback to achieve a closed loop gain of 128*.*

Acknowledgements

I would like to thank the Professor Trond Ytterdal for allowing me to have this experience, always supporting me with simulation issues and technical problems, while letting me make mistakes in the design steps, struggling alone to find the solution and therefore learning from them.

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Introduction 1

In a world that is pushing towards the technologization of everything that surrounds us, the analog to digital conversion represents one of the basic blocks used to interface the natured analog world with the digital domain, where implementing new features for the user is simple, cheap and reliable.

This project will focus on the design of a residue amplifier, that represents one of the building blocks of a pipelined ADC, an high speed and high accuracy analog to digital conversion architecture.
The main requirements on the amplifier are the high gain and high speed capabilities. To solve these problems different topologies and techniques were considered at the beginning, like inverter based amplifiers, self/active cascoding and positive feedback. Even though positive feedback is more commonly used in applications like oscillators and mixers, the interest was focused on this technique that can be implemented in multiple ways and on all the amplifier configurations.
The proposed positive feedback topology was firstly developed in [2] and makes use of a cascode stage, that could be a standard telescopic or a folded configuration. The design approach used in the paper is made for a $TSMC$ 0.25 µm technology and it lays on assumptions that are no longer true in such a scaled technology, like the STM 28 nm $FDSOI$ used in this project. Therefore, a new design approach was developed completely based on the gm/I_D methodology.
The open loop amplifier is then completed with a common source second stage to increase both the overall gain and the output voltage swing.

The report will be organized as follows:

- **Chapter 2** will introduce the pipelined ADC and the theory about the proposed topology, compensation, noise and mismatch contributions;
- **Chapter 3** is focused on the design of the amplifier, starting from the derivation of the requirements, through all the design steps;
- **Chapter 4** will present and discuss the results of the design;
- **Chapter 5** will draw the conclusions, explain the difficulties encountered and the overall result of the chosen topology. At the end, possible further works are presented.

Background theory 2

2.1. Analog to Digital Converters (ADC)

Analog to digital conversion is the operation of mapping an analog input signal into a digital word using a well defined transfer curve.
An analog signal, for nature, is continuous in both time and amplitude; this means that it is not possible to digitally store it as it is, because it would require an infinite accuracy in the values and an infinite number of samples. The tasks of the analog to digital conversion are, therefore, to map the analog input signal using a finite number of samples (discretization in the time) and with a finite accuracy (discretization in the amplitude). Both these operation have to be carefully carried out in order to produce a digital signal that contains the required information of the analog input.

The time discretization lays on the Shannon theorem that gives the outlines in order to perform a faithful conversion without, ideally, losing any information on the input signal. Assuming an input signal with a well defined bandwidth f_{MAX} and, defining $f_S = \frac{1}{T_S}$ the sampling frequency (T_S the sampling step), the Shannon theorem states that:

$$f_S \geq 2 \cdot f_{MAX}$$

The amplitude discretization is the second task of the analog to digital conversion. Since just a finite precision can be achieved, an error will always be present when the amplitude discretization is performed. This error is called *quantization error* or *quantization noise*, since it can be treated as a noise superimposed to the output signal.
Now we can distinct two types of ADCs: with an uncompensated transfer curve or with a compensated one. The difference between the two types is on the position of the threshold point between one bin and the next one. This leads to two different quantization errors:

$$\epsilon_{q_{uncomp}} \in [0 \div LSB]$$
$$\epsilon_{q_{comp}} \in \left[-\frac{LSB}{2} \div \frac{LSB}{2}\right]$$

where LSB is the width of one bin of the ADC (i.e. $LSB = \frac{V_{FS}}{2^n}$, with V_{FS} the full scale range and n the number of bits).
The quantization error will be considered in the analysis for the required loop gain of the amplifier.

No discussions will be done on the ADC topologies since they are not important for the

design of the amplifier.

2.1.1. Pipelined ADC

Pipelined ADC is a popular architecture for high accuracy and high speed analog to digital conversions.
The working principle is based on the use of multiple low accuracy ADCs connected in series, in such a way that the output quantization error of one stage is fed into the next stage that will convert it; this architecture is called multistep. The basic multistep topology uses one clock cycle to produce the output. This means that the maximum sampling frequency is set by the sum of the delays introduced by all the stages connected in cascade. The same architecture can be implemented using pipelining, where each clock cycle corresponds to one step in the ADC chain. In this case the delay is just the conversion time of one stage. Each sample will be converted in m clock cycles (where m is the number of stages), but the throughput of the entire ADC will be m time faster than in the basic multistep. The main drawback is that there is a delay of m clock cycles between the sampling of the the analog input and the computed digital output; this can be a problem in real time systems or, for example, where the ADC is used in a control feedback loop.

As mentioned, every stage of the ADC converts the output quantization error of the previous one that is in the range $[0 \div LSB]$. Instead of using different reference voltages for each stage, the quantization error is up-scaled by a so called $residue\ amplifier$, which is the topic of this project. The gain of each residue amplifier is set by the number of bits k of the previous stage (in particular, $A_V = 2^k$), while its accuracy is related to the number of bits downstream its position. A more detailed analysis will be discussed in the design chapter.
A block diagram of a general k bit stage is shown in Figure 2.1

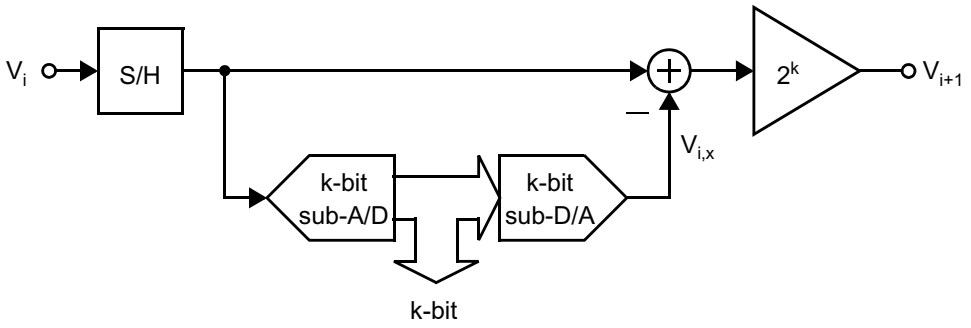

Figure 2.1.: General k bit stage of a pipelined ADC [1]

2.2. Folded Cascode topology

Cascoding is a well known technique since the beginning of electronics, but, over the time, its usage has changed shape. In fact, this topology was developed to mitigate the Miller effect in high gain stages and it has been used for this purpose till the advanced technology scaling of these days.

Nowadays, cascoding is a synonymous of gain and in fact it is used to improve the gain of an amplifier stage, since the intrinsic gain of a single transistor decreased dramatically over the time.

The first differential topology is the telescopic cascode, where both the differential input and the active load are buffered with a common gate cascode transistor. The telescopic cascode uses 5 transistors stacked on top of each other and this turns into a limit in low supply voltage designs. The solution to this problem is the folded cascode configuration that moves the differential pair by folding it into another branch. The schematic is visible in Figure 2.2. The main disadvantage of this configuration is in terms of power consump-

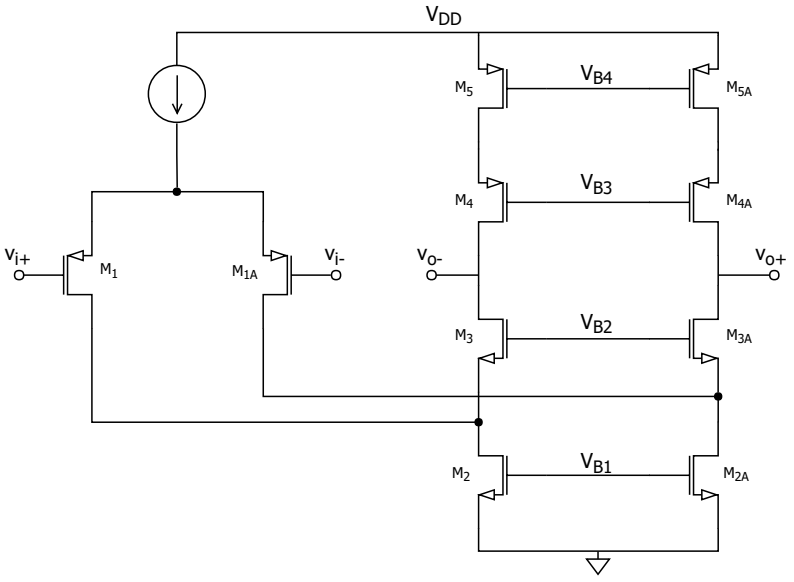

Figure 2.2.: Folded cascode differential amplifier

tion. In fact two different bias currents are needed for the differential input and the active load.

The calculation of the small signal gain can always be written as the product of the small signal transconductance of the input pair and the equivalent resistance seen at the output nodes:

$$R_{o_N} \approx r_{o_3}(1 + g_{m3} \cdot r_{o_1} || r_{o_2})$$
$$R_{o_P} \approx r_{o_4}(1 + g_{m4} \cdot r_{o_5})$$
$$A = \frac{v_o}{v_i} = g_{m_1} \cdot R_{o_N} || R_{o_P}$$

For the frequency response of the amplifier two new poles are introduced by the cascode nodes. In fact, beside the output pole ($\frac{1}{R_{o_N} || R_{o_P} \cdot C_L}$), the two nodes between $M2 - M3$

and $M4 - M5$ introduce other two poles respectively at:

$$\omega_{p_1} \approx \frac{g_{m3}}{C_{1,2,3}}$$
$$\omega_{p_2} \approx \frac{g_{m4}}{C_{4,5}}$$

where $C_{1,2,3}$ and $C_{4,5}$ are the parasitic capacitance seen at the respectively nodes. Since the resistance at the node is dominated by the input resistance of the common gate transistor ($\approx 1/g_m$), both poles are normally negligible in the stability analysis.

2.3. Positive Feedback Gain Boosting Technique

With the technology scaling the intrinsic gain of transistors is continuously decreasing while high precision - and then high gain - requirements are always more and more common. Gain boosting techniques are then needed to achieve high gain stages.
Positive Feedback concept, also known as *Transconductance Compensation*, is a gain boosting technique which principle lays on the reduction of the positive output conductance of an OTA stage by applying a negative conductance contribution.

In this chapter the Positive Feedback technique will be described, starting from the simple Cross-Coupled Pair topology and then its application in the implemented design.

2.3.1. Cross-coupled Pair

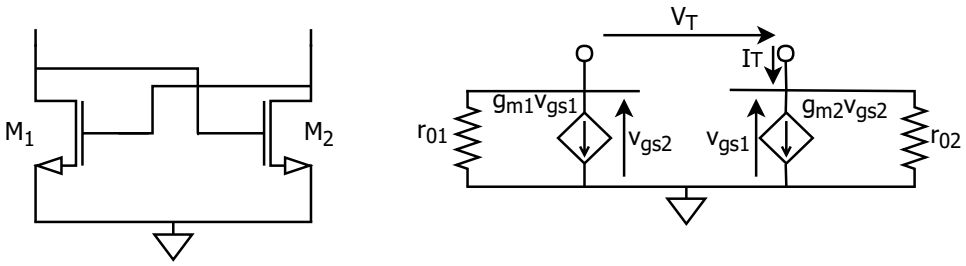

Figure 2.3.: Cross-Coupled Pair

The Cross-Coupled Pair is the basic configuration used to implement a positive feedback network. The configuration is visible in Figure 2.3 and the low frequency small signal model is also shown.
Its principle lays on the crossed connection of the two transistors. In fact, the inverting behaviour of both transistor is fed back to the opposite branch, creating a positive feedback.
Assuming the transistor identical and operating on the same bias point, it is possible to derive the small signal equivalent circuit seen from the two input nodes. The result can be written as a conductance G:

$$G = -\frac{g_m}{2} + \frac{g_{ds}}{2}$$

The result shows that the positive conductance contribution of the transistors can be mitigated or completely removed with this network. More in general, this behaviour can be used to control the impedance of two nodes of a circuit, for example boosting the output resistance of an OTA and then increasing its gain.
It must be mentioned that the analysis made above is directly dependent on the small signal parameters of the network and on the fact that the transistors are considered identical and working on the same operating point. This means that no precise matching can be easily achieved and therefore other configurations must be taken into account.

2.3.2. Proposed Positive Feedback Architecture

The proposed architecture uses a particular implementation of the positive feedback network discussed above that was first developed in [2]. The circuit structure is shown in Figure 2.4 and it is based on a Folded Cascode OTA.
The positive feedback principle is applied through the crossed connection of the two NMOS $M3$, $M3A$ that normally would be used as cascode transistors.

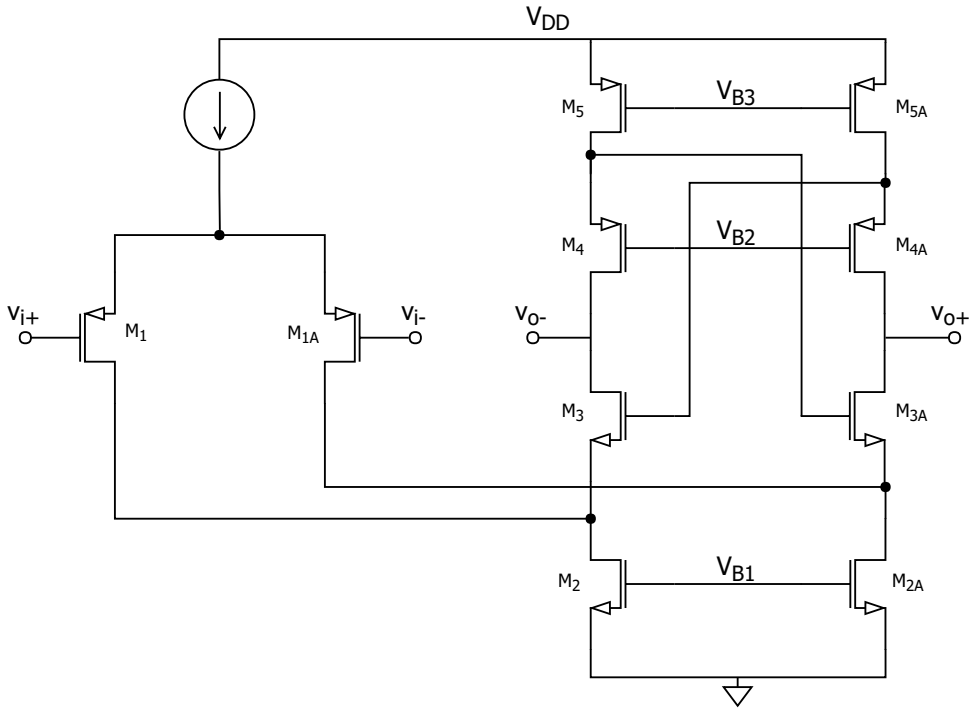

Figure 2.4.: Proposed Gain Boosting architecture [2]

To derive the low frequency input/output gain of the circuit, we consider the small signal equivalent model for the differential mode in Figure 2.5, where the cascode connection $M4$, $M5$ has already been simplified with its equivalent model.
The dependent current source $g_{m3}(-v_x - v_y)$ represents the positive feedback transistor. The fact that v_x is taken with the opposite sign is because that voltage is taken on the other branch of the OTA, which exhibits a symmetric but opposite behaviour.

From the small signal model it is possible to derive the low frequency gain of the circuit that can be written as:

$$A_0 = \frac{v_o}{v_i} = -\frac{g_{m1}g_{m3}g_{m4} + g_{m1}g_{m3}g_{ds_4} + g_{m1}g_{m4}g_{ds_3} + g_{m1}g_{ds_3}g_{ds_4}}{g_{ds_{12}}g_{ds_4}g_{ds_5} + g_{ds_3}g_{ds_4}g_{ds_5} + g_{ds_{12}}g_{ds_3}g_{ds_4} + g_{m3}g_{ds_4}g_{ds_5} + g_{m4}g_{ds_{12}}g_{ds_3} - g_{m3}g_{ds_{12}}g_{ds_4}}$$

The expression can be simplified considering $g_m >> g_{ds}$ and, in the case of $g_{m3}g_{ds_{12}}g_{ds_4} = g_{m3}g_{ds_4}g_{ds_5} + g_{m4}g_{ds_{12}}g_{ds_3}$ the expression will be:

$$A_0 = \frac{v_o}{v_i} = -\frac{g_{m1}g_{m3}g_{m4}}{g_{ds_{12}}g_{ds_4}g_{ds_5} + g_{ds_3}g_{ds_4}g_{ds_5} + g_{ds_{12}}g_{ds_3}g_{ds_4}}$$

Now the gain has the form of $\left(\frac{g_m}{g_{ds}}\right)^3$ and it would be equivalent to a double cascode configuration.
The gain boosting is based on the assumption made before that involves a perfect matching of various g_m, g_{ds} products that can be achieved only in an ideal case. Moreover, the negative term introduced by the positive feedback could be the dominant one and change the sign of the amplification, making the closed loop amplifier unstable. This means that a careful design is required in order to ensure the necessary gain boosting factor while keeping the amplifier stable against both mismatch and process variations.

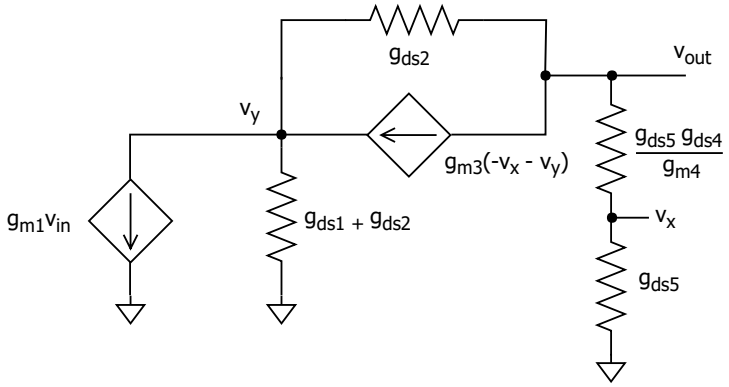

Figure 2.5.: Small signal model for the differential mode

After the mathematical analysis of the circuit it is important to make some considerations:

- the use of a cascode structure already produces a high gain configuration and therefore the gain boosting performance of the positive feedback network can be relaxed;
- the positive feedback transistors are connected to the nodes introduced by the cascode configuration; these nodes experience a limited voltage swing compared to the output voltage nodes. This means that the small signal analysis can be applied as a good approximation;
- the positive feedback network is implemented without increasing the power consumption of the basic cascode configuration since no additional current is used to bias the positive feedback network.

2.3.3. Second Stage and Miller Compensation

The use of a second stage is necessary in order to respect the gain requirements and to increase the output voltage swing. In fact, the folded cascode stage allows just a limited swing because of the four transistors stacked on top of each other. The solution chosen for the second stage is a common source that combines a moderate gain with high swing capabilities.

The use of a second stage in closed loop OTAs usually leads to stability problems and so compensation techniques are required to ensure the desired stability margin. The most common compensating technique is a dominant pole compensation with a Miller capacitance. The use of the Miller effect has two advantages:

- it limits the size of the capacitance
- it moves both the dominant pole of the first stage and the non-dominant pole of the second stage, increasing the splitting between the two:

No detailed analysis will be discussed, but the important results needed for the stability issue are the unity gain frequency of the amplifier UGF and the position of the non dominant pole ω_{p_2}:

$$UGF \approx \frac{g_{m1}}{C_c}$$
$$\omega_{p_2} \approx \frac{g_m 2}{C_{p_1} + C_L + \frac{C_{p_1} \cdot C_L}{C_c}}$$

where g_{m1}, g_{m2} represent the transconductance of drivers of the two stages, C_{p_1} the parasitic capacitance at the output node of the first stage and C_L the total load capacitance at the output of the second stage.

The compensating capacitance introduces also a right half plane zero (RHZ) in the open loop transfer function. This is an unwanted contribute that worsen the stability margin. To move the zero into the left half plane (LHZ), a *nulling resistor* R_Z is used in series to the compensating capacitance. The position of the zero becomes:

$$z = -\frac{1}{(R_Z - \frac{1}{g_{m2}})C_c}$$

R_Z can be designed in order to push the zero to infinity ($R_Z = \frac{1}{g_{m2}}$), or, more wisely, to cancel the non dominant pole ω_{p_2}, therefore increasing the overall stability margin. Although the introduction of the nulling resistance adds another pole in the system, it typically can be neglected.
The second stage with compensation is shown in Figure 2.6.

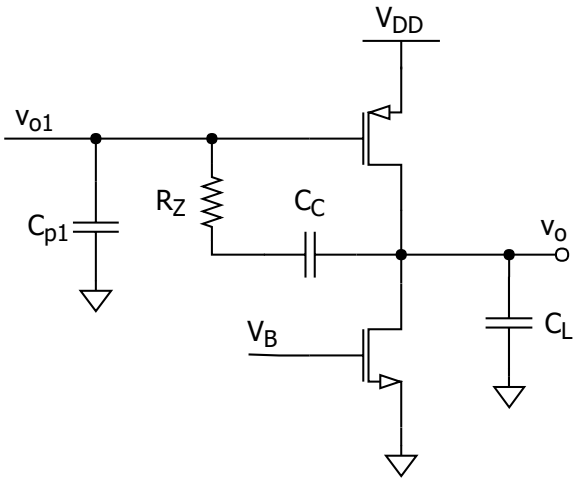

Figure 2.6.: Second stage with Miller compensation

2.3.4. Noise sources

Different types of noise sources can be found in analog circuits, most of them are introduced by the active devices or resistors. The noise folding will also be discussed since the amplifier will work in a switched capacitor feedback.

Shot noise

Shot noise is a white noise source related to the fact that, at a microscopic level, current is the result of the average amount of electrons moving randomly under the effect of an electric field or a gradient in the concentration. Since every electron has a discrete charge, the random fluctuation of the number of moving electrons determines the shot noise.
Shot noise is significant in bipolar devices or when low currents are considered. In MOSFET transistors it is important in highly weak inversion region, where the transistor behaves like a BJT. Since this is not the case in this project, any mathematical analysis is considered.

Thermal noise

Thermal noise is always related to the movement of the electron, but this time it is due to thermal stirring. Like in the previous case, thermal noise is another white noise source and, for a standard resistor R, the power spectral density is:

$$v_n^2(f) = 4K_BTR \leftrightarrow i_n^2(f) = \frac{4K_BT}{R}$$

where K_B is the Boltzmann's constant and T the absolute temperature. Thermal noise affects also MOSFET transistors since the conduction mode is based on the same principle, a drift current on a resistive channel. The power spectral density is, in this case, related

to the operating point of the transistor and it can be written as:

$$i_n^2(f) = 4K_BT\gamma g_m, \quad \gamma = \begin{cases} 1 & \text{triode region} \\ 2/3 & \text{saturation, long channel} \\ 2 & \text{saturation, short channel} \end{cases}$$

Let's consider now the circuit in Figure 2.7, where the thermal noise of the resistor is modelled as a current source, and derive the output integrated noise power of the circuit:

$$V_{O_{RMS}}^2 = \int_0^{+\infty} i_n^2(f)|H(j2\pi f)|^2 \mathrm{d}f = \int_0^{+\infty} \frac{4K_BT}{R} \left| \frac{R}{1 + j2\pi fRC} \right|^2 \mathrm{d}f = \frac{K_BT}{C}$$

The result shows that the output integrated noise power is not related to the resistor (the noise source) but just to the value of the capacitance.
A more general interpretation of this can be used also with the thermal noise generated by the active devices or, even more generally, by an entire amplifier. In fact, most of the OTAs can be modelled with a low pass filter transfer function; in this case the noise source is not the equivalent output resistance of the amplifier, but it is the sum of all the internal contributes. If we think this sum is N times the noise that the output resistance would produce (thinking as it is a noise source), we can use the result above and say that:

$$V_{O_{RMS}}^2 = N\frac{K_BT}{C}$$

The result shows that doubling the value of the band limiting capacitance, the output noise power is halved, and therefore the output noise voltage is divided by $\sqrt{2}$. N is normally a function of the gain of the amplifier and this means that up-scaling the circuit by changing the bias current does not affect N. Therefore, changing the value of the band limiting capacitance will lead to a change in the bias currents of the circuit, but N will be constant.
It must be kept in mind that this result is general for circuits that can be modelled with a single pole low pass characteristic, but it is limited just to the thermal noise component.

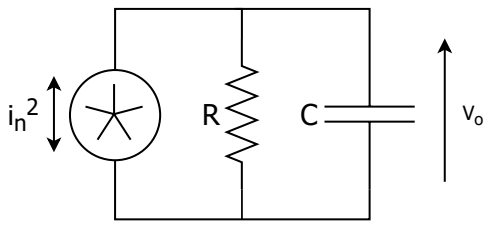

Figure 2.7.: Low pass filter with noise

Flicker noise

Flicker noise is another noise component present in all active devices. Even though there is no physical proof/model, the flicker noise seems to be generated by defects in the semiconductor crystal structure; a good example is the interface between silicon and gate

oxide in a MOSFET transistor.
Empirical measurement has shown that, in a MOSFET, the power spectral density of the flicker noise is frequency dependent, in particular:

$$i_n^2(f) = K_F \frac{I_D}{f}, \quad K_F \propto \frac{1}{L^2 C_{OX}}$$

For this reason, flicker noise is also called $1/f$ noise. Due to the different mobility of holes over electrons, PMOS normally exhibit less flicker noise than NMOS transistors.
An important parameter of active devices is the so called *corner frequency*, that is defined as the frequency where the flicker noise PSD is equal to the thermal noise PSD. Below the corner frequency, the noise is dominated by the flicker component, while, above it, the dominant contribute is due to the thermal noise. Comparing the corner frequency with the bandwidth of the circuit it is possible to understand which component will contribute for the most part in the output noise.

Noise Folding

Noise folding is not a direct noise source, but it is a consequence of the use of switched capacitor circuits. The basic idea behind noise folding lays on the fact that the switching frequency f_s used in switched capacitor amplifiers is $3-10$ times lower than the bandwidth of the amplifier itself. Considering the Nyquist/Shannon theorem, all the frequency above $f_s/2$ will produce aliasing in a sampled system. Since the equivalent noise bandwidth is even larger than the bandwidth of the amplifier, the noise will be undersampled and will produce low frequency aliasing. Considering for example a thermal noise source with noise bandwidth $[0 \div f_{noise}]$ the noise folding will lead to an equivalent noise power in the $[0 \div \frac{f_s}{2}]$ range that can be approximated with $\frac{f_{noise}}{f_s}$ times the thermal noise source.

2.4. Mismatches and process variations

Mismatches and process variations are non idealities introduced during the fabrication process of a chip. Parameters like the dimensions of the transistors, oxide thickness or doping factors can be controlled just with a finite accuracy and random variations are always present. These variations can be approximated with a Gaussian distribution and can be divided into two main contributes:

- process variations: are alterations that affect the global characteristics of the devices due to changes in doping, oxide thickness and mobility; the main visible result of process variations is the change in the threshold voltage of the transistors that can be dozens of mV;
- mismatches: are alteration of the characteristics of two devices that should be matched (i.e. identical or scaled versions). Mismatches are mainly due to variations in the physical dimensions of the transistors and to local gradients in the physical parameters mentioned above.

The effect of process variations can be mitigated using a design with a low sensitivity on the absolute threshold voltage; for example, in a input differential pair, the threshold voltage of the input transistors influences the drain voltage of the tail current mirror; with

a careful design, it is possible to ensure that the current mirror always works in saturation region. More advanced techniques are used, like sensing V_T with a replica bias circuit and then adjusting other variables, like it could be the input common mode voltage in the example above.

The approach against mismatches is different. Since they affect devices that should be matched, their main effects can be seen in current mirrors and differential pairs. It is interesting to understand how these effects are affected by the bias point of the transistor. We can define:

- $\sigma(\frac{\Delta\beta}{\beta}) = \frac{A_\beta}{\sqrt{WL}} + B_\beta$: the variance of the mismatch on the current factor β
- $\sigma(V_T) = \frac{A_{V_T}}{\sqrt{WL}}$: the variance of the mismatch on the threshold voltage V_T

Both the variance are, as expected, inverse proportional to the area of the device.
For a current mirror, the variation in the mirroring factor can be modelled with:

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{4}{(V_{GS}-V_T)^2}\sigma^2(V_T) \qquad [1]$$

Of course, the mirroring factor is directly dependent on the current factor variation, but the effect of the variation in the threshold voltage V_T depends on the bias point of the transistor. The bigger the overdrive (low g_m/I_D), the less the contribution of $\sigma(V_T)$.
In a differential pair the parameter of interest is the effect of mismatches on the input offset voltage V_{os}:

$$\sigma^2(V_{os}) = \sigma^2(V_T) + \frac{(V_{GS}-V_T)^2}{4}\sigma^2\left(\frac{\Delta\beta}{\beta}\right) \qquad [1]$$

As expected, the effect of $\sigma(V_T)$ affects directly the input offset voltage, while the effect of current factor mismatch can be mitigated biasing the transistor with a low overdrive (high g_m/I_D).

2.4.1. FDSOI Technology

Fully Depleted Silicon on Insulator (FDSOI) is a device technology introduced with the latest sub-micron technology nodes. The key point of the FDSOI is the use of intrinsic silicon (fully depleted) in the channel area with a buried oxide insulation between the channel area and the substrate/well. The use of intrinsic silicon reduces the gate-induced leakage current and enhances the carrier mobility in the channel. Insulating the bulk contact from the channel area helps in reducing the leakage currents through the substrate but still allows threshold voltage modulations and the use of bulk driven configurations; the bulk contact is also called back gate for its similarity to the standard gate of a MOS transistor.

The technology node used in this project is the STM 28nm FDSOI that offers different types of devices for different purposes. The project has made use of the Low Threshold Voltage (LVT) transistors that are particular because they are built on flipped wells (n-type substrate for NMOS and, and p-type for PMOS transistors).

Design of the Amplifier 3

This chapter will discuss the design of the amplifier with all the steps carried out and the assumption made during this process.

3.1. Design Specifications

The amplifier requirements are listed below:

- closed loop gain $A_V = 128$;
- equivalent number of bits of the ADC $ENOB = 13$ bit;
- open loop unity gain frequency $UGF \geq 1\,\text{GHz}$;
- load capacitance $C_L = 100\,\text{fF}$;
- fully differential input and output;
- supply voltage $V_{DD} \leq 1\,\text{V}$;
- minimum power consumption.

3.2. Analysis of the required Loop Gain

The first step for the design is to calculate the low frequency loop gain L_{DC} required in order to achieve the desired accuracy of 13 bit for the entire ADC.
The analysis is made supposing a 14 bit ADC composed of two 7 bit pipelined stages. Actually, considering a two stage ADC model is not a constraint in this analysis. In fact what is important here is the equivalent number of bits upstream of the amplifier (that will set the required closed loop gain, as explained in 2.1.1) and the equivalent number of bits downstream the output side (that will set the closed loop gain error and so the loop gain L_{DC}).

The mathematical analysis is made propagating the output quantization error of the first ADC through the amplifier and the second ADC. The ADCs will be considered ideal and with an uncompensated transfer characteristic.

Calling ϵ_{q_1} the quantization error of the first ADC, its possible values will be in the range $[0 \div 2^{-7}]$. This error will be the input of the residue amplifier that will produce an output $V_{O_{RA}}$ in this form:

$$V_{O_{RA}} = V_{IN_2} = \epsilon_{q_1} \cdot (A_V + \Delta A_V)$$

where, V_{IN_2} refers to the input signal of the second ADC, A_V is the closed loop gain of the amplifier, and ΔA_V is its deviation from the ideal value.
Normally, the ΔA_V is considered negative, because a finite loop gain will lead to a closed loop gain that is less than the ideal one. In this case, however, it is interesting to consider also a positive gain error as we will see in the final result.

The expression above can be divided into an ideal term and in an error:

$$V_{IN_2} = V_{IN_{2_{IDEAL}}} + \epsilon_{V_{IN_2}} = \epsilon_{q_1} \cdot A_V + \epsilon_{q_1} \cdot \Delta A_V$$

The requirement of an overall accuracy of 13 bit can be reduced in a requirement of a 6 bit accuracy in the second ADC, since the first one will convert the 7 most significant bits. Considering also the quantization error of the second ADC $\epsilon_{q_2} \in [0 \div 2^{-7}]$ and moving it to its input side (changing the sign), we can write the simple equations below:

$$-2^{-6} < \epsilon_{V_{IN_2}} - \epsilon_{q_2} < 2^{-6} \Rightarrow \begin{cases} \epsilon_{V_{IN_2}} < 2^{-6} + \epsilon_{q_2} \\ \epsilon_{V_{IN_2}} > -2^{-6} + \epsilon_{q_2} \end{cases} \Rightarrow \begin{cases} \Delta A_V < \frac{2^{-6}+\epsilon_{q_2}}{\epsilon_{q_1}} \\ \Delta A_V > \frac{-2^{-6}+\epsilon_{q_2}}{\epsilon_{q_1}} \end{cases}$$

Substituting ϵ_{q_1} ϵ_{q_2} in order to minimize the range ΔA_V we obtain:

$$-1 < \Delta A_V < 2 \qquad \Rightarrow \qquad 127 < A_V < 130$$

The result obtained is general and shows that the amplifier could be designed for a maximum closed loop gain of 130; this would leave more room for the closed loop gain error and so it would relax the loop gain requirement L_{DC} of about a factor of 3. Since the closed loop gain is given in the specifications $A_V = 128$, the allowed loop gain error will be 1. Defining β the feedback factor, the required open loop gain of the amplifier A_{OL} can be calculated using the feedback theory:

$$\begin{aligned} &\frac{\Delta A_V}{A_V} = \frac{1}{1 + L_{DC}} \approx \frac{1}{L_{DC}} && \Rightarrow && L_{DC} = A_{OL}\beta = 128 \\ &A_V = \frac{1}{\beta} \frac{L_{DC}}{1 + L_{DC}} && \Rightarrow && \beta \approx \frac{1}{A_V} = \frac{1}{128} \\ &A_{OL} > \frac{L_{DC}}{\beta} = 2^{14} && \Rightarrow && A_{OL_{dB}} > 85\,\text{dB} \end{aligned}$$

3.3. Considerations

The design approach used in this project is entirely based on the g_m/I_D methodology because it represents a more universal way to characterize the behaviour of the different devices, based on practical simulations instead of complicated models. Every other important parameter of the design can be related to the g_m/I_D figure of merit and, then, this approach simplifies the design without introducing any limitations.

Some general consideration used in the design are listed below:

- all transistors used are Low Threshold Voltage (LVT); for the PMOS the bulk is tied

to GND and for the NMOS to V_{DD};

- the absolute values of the currents are not considered at the beginning. They will be taken into account for the bandwidth and stability requirements. When the final bias current is set, the design can be easily up-scaled without changing the low frequency gain;
- to mitigate the effect of mismatches, high g_m/I_D was used for the input differential pair (to reduce the input offset voltage) while lower g_m/I_D was used for the current mirrors to improve the current matching. The previous consideration must be made also taking care of the speed of the device f_T and its intrinsic gain g_m/g_{ds};

3.4. First Stage Design

As previously mentioned, the first stage will be based on the folded cascode configuration with the addition of the positive feedback principle described in the section 2.3.
The schematic, without the external biasing circuit, is reported in Figure 3.1.

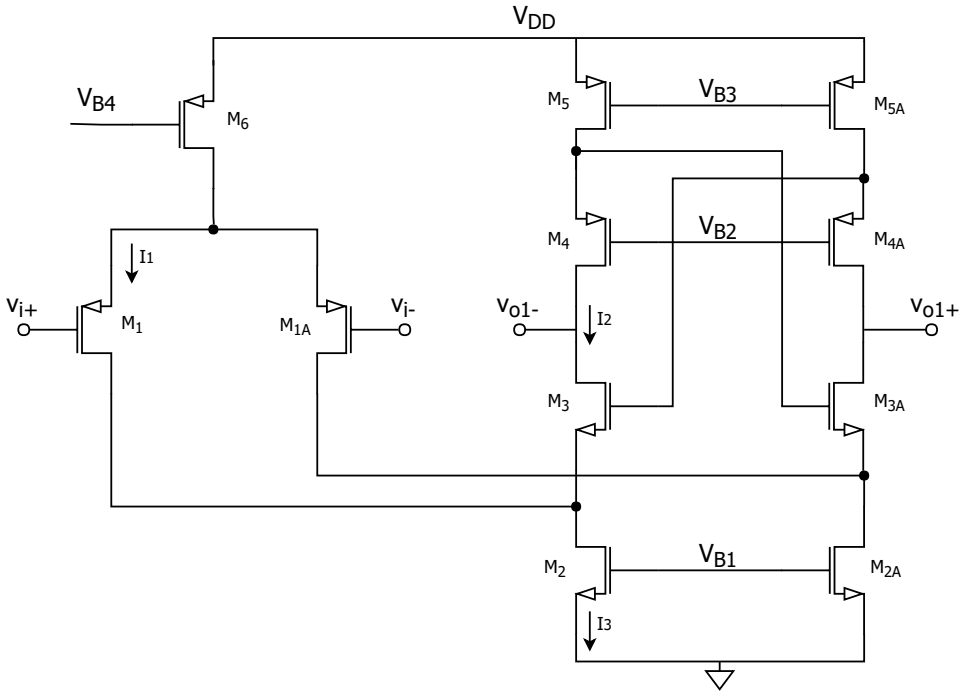

Figure 3.1.: First Stage Schematic [2]

The choice of using a PMOS input pair is mainly due to the fact that in this way the tail current mirrors $M2$, $M2A$ are NMOS. In fact we can make some considerations:

- the small signal equivalent resistance at the folding node is the parallel combination of r_{ds_1} and r_{ds_2}; both terms should contribute equally in order to maximize the parallel combination;
- the tail current mirror $M2$ is biased with the sum of the two currents I_1, I_2.
- the current mirror $M2$ is designed with a low g_m/I_D in order to lower the sensitivity of current mirroring against mismatches; the opposite consideration is done with the

input pair $M1$, $M1A$ that are designed with a high g_m/I_D to improve the input offset voltage characteristic;

These considerations leads to the fact that the tail current mirror $M2$ will be biased in the worse operating point, in terms of output resistance, than the input pair transistor $M1$. This means that better output characteristics are required for the tail transistors $M2$ $M2A$ and therefore the NMOS device are chosen for this purpose. The input pair is then made with PMOS.

As presented in the section 2.3.2, the gain of the circuit is given by:

$$A_0 = \frac{g_{m1}g_{m3}g_{m4}}{g_{ds_{12}}g_{ds_4}g_{ds_5} + g_{ds_3}g_{ds_4}g_{ds_5} + g_{ds_{12}}g_{ds_3}g_{ds_4}}$$

when the following condition is matched:

$$g_{m3}g_{ds_{12}}g_{ds_4} = g_{m3}g_{ds_4}g_{ds_5} + g_{m4}g_{ds_{12}}g_{ds_3}$$

The solution approach used in [2] is made considering $g_{m3} = g_{m4}$ and assuming an equal inverse proportional relation between the output conductance of both PMOS and NMOS transistors to the respect of the bias current I_D. The first assumption is made just to simplify the calculation and has no practical advantage since $M3$ is an NMOS and $M4$ is a PMOS and therefore they cannot be matched intrinsically. The second consideration is no longer true in such a scaled technology and therefore this approach cannot be used in this case.

For design purposes, the previous equation is difficult to handle since neither g_m nor g_{ds} are direct design parameters. The equation is then rearranged in order to write it in terms of g_m/I_D, g_m/g_{ds}, and current ratios. A Matlab script has been used to perform the design, giving as input the desired g_m/I_D and g_m/g_{ds} values, once chosen the lengths L and the drain source voltage V_{DS}. This has been a trial and error approach since different considerations must be taken into account and no simple expression can be used to model the device characteristics.

As already mentioned, a safety margin must be considered in order to ensure the stability of the closed loop amplifier to the respect of mismatch and process variations. Called the margin k, it can be written as:

$$k = g_{m3}g_{ds_4}g_{ds_5} + g_{m4}g_{ds_{12}}g_{ds_3} - g_{m3}g_{ds_{12}}g_{ds_4}, \quad k \geq 0$$

This margin has been set to be comparable to the denominator of the ideal gain expression $k \approx g_{ds_{12}}g_{ds_4}g_{ds_5} + g_{ds_3}g_{ds_4}g_{ds_5} + g_{ds_{12}}g_{ds_3}g_{ds_4}$.
The gain equation can then be written as:

$$A_0 = \frac{g_{m1}g_{m3}g_{m4}}{g_{ds_{12}}g_{ds_4}g_{ds_5} + g_{ds_3}g_{ds_4}g_{ds_5} + g_{ds_{12}}g_{ds_3}g_{ds_4} + k} \approx \frac{1}{2}\frac{g_{m1}g_{m3}g_{m4}}{g_{ds_{12}}g_{ds_4}g_{ds_5} + g_{ds_3}g_{ds_4}g_{ds_5} + g_{ds_{12}}g_{ds_3}g_{ds_4}}$$

The gain of the first stage is set to be about 65 dB.

Another important consideration that must be taken into account is that the crossed connection of the transistors $M3$ $M3A$ imposes the V_{DS} bias voltage of $M3$ and $M4$, since $V_{GS_3} = V_{DS_3} + V_{DS_4}$ (for the symmetry of the circuit in bias/common mode). This means that V_{GS_3} must be chosen in order to ensure that both $M3$ and $M4$ are biased in saturation region. Since each branch is made up with four transistors stacked on top of each other, it has been chosen to bias each transistor with a $V_{DS} \approx 250\,\text{mV}$.
The tail generator $M6$ is also biased with a $V_{DS_6} \approx 250\,\text{mV}$ and this is done by setting the input common mode voltage to be $V_{I_{CM}} = V_{GS_1} + V_{DS_6}$, while the input pair ends with $V_{DS_1} = 500\,\text{mV}$.

3.5. Second Stage Design

Beside increasing the overall gain of the amplifier, the second stage has the main purpose of increasing the output voltage swing that, in the first stage, is limited by the number of transistors stacked on top of each other.
Since a moderate gain is required in the second stage, a common source configuration is used. The schematic, without the external biasing circuit, is shown in Figure 3.2.

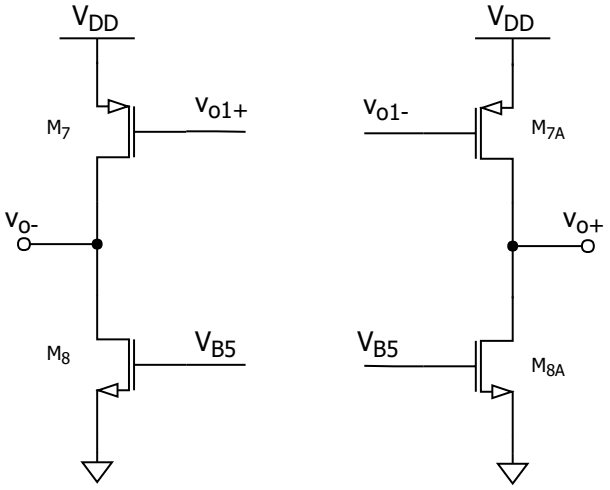

Figure 3.2.: Second Stage Schematic

The driver transistor is chosen to be a PMOS but both PMOS and NMOS driven configuration could have been used since the output common mode of the first stage is at $\approx V_{DD}/2$.

The low frequency gain of the stage can be written as:

$$A_0 = \frac{g_{m7}}{g_{ds_7} + g_{ds_8}} \propto \frac{g_m}{g_{ds}}$$

The second stage is designed for a low frequency gain of 30 dB in order to achieve an overall open loop gain of 95 dB, obtaining a 10 dB margin from the minimum loop gain

of 85 dB.

The design of the PMOS drivers must be done considering that the bias V_{GS} imposes the output common mode voltage of the first stage.
Like in the previous case, the driver has been designed with a high g_m/I_D while the active load with a relatively lower one.
Biasing the stage with an high g_m/I_D is important also for the output voltage swing since, in first approximation, it is directly dependent on the saturation voltage of the $M7$ and $M8$ transistors. In fact, setting a output common mode in the 500 mV range, therefore at half V_{DD}, and considering the saturation voltage equal on both the transistors $M7$ $M8$, the maximum output swing is given by:

$$V_{OD_{pp}} = 2(V_{DD} - V_{DS_{sat}})$$

3.6. Common Mode Feedback

A common mode feedback circuit (CMFB) is required in order to set the common mode output voltage of the amplifier. The available solution were the use of a continuous time CMFB or the switched capacitor (SC) version. The continuous time CMFB is based on active devices and is essentially made with an error amplifier that senses the output common mode voltage and compares it with a reference voltage.
The switched capacitor CMFB uses a capacitor feedback to perform the sensing and the comparing; therefore no active device is used. Since the circuit is already designed to work in a switched capacitor configuration, no limitations are introduced by the usage of a SC-CMFB. This, as mentioned, has the advantage of not adding power consumption.

The SC-CMFB circuit is shown is Figure 3.3 and two identical replicas of it are used in order to set the output common mode of the first and the second stage of the amplifier. The circuit receives as inputs the differential output voltage V_{o+} V_{o-}, the desired common mode reference voltage $V_{CM_{ref}}$ and a bias voltage $V_{B_{replica}}$, and produces the bias voltage for the current mirrors $M2$ $M2A$ (regarding the CMFB of the first stage) and $M8$ $M8A$ (regarding the CMFB of the second stage). In a periodical steady state condition the

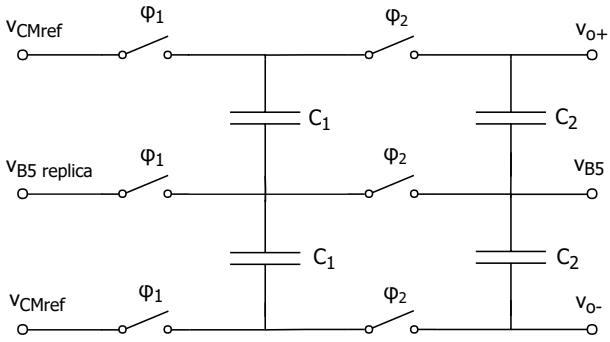

Figure 3.3.: CMFB schematic [3]

circuit will operate in such a way that [3], [4]:

$$V_{CM_{ref}} - V_{o_{cm}} = V_{B_{replica}} - V_b\,, \qquad V_{o_{cm}} = \frac{V_{O+} + V_{O-}}{2}$$

Considering a small signal common mode feedback gain $A_{CMFB} = \frac{v_{o_{cm}}}{v_b} >> 1$, it can be easily seen that $V_{o_{cm}}$ will approach $V_{CM_{ref}}$ if V_b equals $V_{B_{replica}}$. This means that $V_{B_{replica}}$ must be generated to be close enough to the real V_b value. $V_{B_{replica}}$ is therefore generated using a replica bias circuit like it happens in a standard current mirror.

The behaviour of the circuit is, in first approximation, independent from the size of both C_1 and C_2 capacitors. If parasitic capacitances, charge injection and other second order effects are taken into account, a more accurate sizing of the capacitors can be done. Since ideal switches have been used in this work, no further analysis is carried out. The value of the capacitors has been set to be 10 fF for both C_1 and C_2.
It must be kept in mind that the value of the capacitors influences the output node capacitance of both the amplifier stages and therefore this loading effect will be taken into account in the stability and compensation step.

3.7. Noise analysis and Miller Compensation

It has been described in the section 2.3.3 that a dominant pole compensation is necessary to achieve the required stability margin for the closed loop amplifier. At the same time, the band limiting capacitance is important to limit the output noise power of the amplifier. This two considerations lead to the fact that the Miller compensation must be done considering both the contributes.
The compensation of the amplifier sets also the absolute values of the currents since all the stability and bandwidth requirements can be related to a g_m/C expression.

From the first simulations of the circuit it has been ascertain that the noise constraint was the dominating contribution in setting the Miller capacitance value.
Since the flicker noise represents an important contribute to the overall output noise power, a redesign of the circuit has been done increasing the area of the main flicker noise sources (mainly due to the tail generators of the folded cascode stage since they are biased with the highest current). Increasing the area leads to an increase of the parasitic capacitances and affects the position of the non dominant poles, especially the ones introduced by the cascode nodes. This leads to and increase of the required biasing currents that, again, affects the flicker noise contribution. The final result is therefore a trade off between noise power, bandwidth and power consumption.

Once the Miller capacitance has been set, the absolute values of the biasing currents can be calculated, since the required transconductance can be derived from the stability and bandwidth specifications.

The unity gain frequency requirement is set through the previously discussed relation:

$$UGF = \frac{g_{m1}}{2\pi\, C_C} \rightarrow I_{tail} = 2I_1 = \frac{g_{m1}}{\left(\frac{g_m}{I_D}\right)_1}$$

where g_{m1} is the transconductance of the input differential pair and I_1 its bias current.
The non dominant pole of the folded cascode configuration can be approximated with:

$$\omega_{ndp_1} = \frac{g_{m3}}{C_{fn}} \rightarrow I_2 = \frac{g_{m3}}{\left(\frac{g_m}{I_D}\right)_3}$$

where C_{fn} is the parasitic capacitance seen looking into the folding node.
Since this capacitance is small compared to the the Miller capacitance C_C, this pole can be easily set to be beyond the unity gain frequency of the amplifier and then we can get rid of it in the stability analysis.
The non dominant pole ω_{ndp_2} introduced by the second stage is, instead, really important since its position is usually comparable with the unity gain frequency of the amplifier. A consideration must be done at this point since the amplifier will be designed for a closed loop gain of 128. This means that the cross-over frequency of the loop gain, the one that cares in terms of stability, will approximately be at $\frac{UGF}{128}$. Defining ω_c the cross-over angular frequency of the loop gain, the position of the non dominant pole can be set in order to achieve the desired phase margin PM:

$$PM = \arctan\left(\frac{\omega_{ndp_2}}{\omega_c}\right)$$

Knowing ω_{ndp_2} it is possible to derive the required second stage transconductance:

$$\omega_{ndp_2} \approx \frac{g_{m7}}{C_{p1} + C_{L_{eq}}}$$

where:

- g_{m7} is the transconductance of the second stage driving transistor;
- C_{p1} is the parasitic capacitance seen at the output of the first stage
- $C_{L_{eq}}$ is the equivalent capacitance at the output nodes. This capacitance is composed of the explicit load capacitance C_L, the parasitic capacitance of the output transistors and the loading effect introduced by the feedback network.

$$C_{L_{eq}} \approx C_L + (1-\beta)C_f + C_{2_{CMFB}}$$

Since C_L is the leading term, the equation above can be approximated in the form

$$\omega_{ndp_2} \approx \frac{g_{m7}}{C_L} \rightarrow I_3 = \frac{g_{m7}}{\left(\frac{g_m}{I_D}\right)_7}$$

As seen in the previous section, the Miller compensation introduces also a zero in the right half complex plane. A *nulling resistor* R_Z must be used in order to move the zero

into the left half plane. Moreover, this zero can be used to cancel the effect of the non dominant pole of the second stage ω_{ndp_2}:

$$R_Z = \frac{C_{p1} + C_{L_{eq}}}{g_{m7} C_C} \approx \frac{C_L}{g_{m7} C_C}$$

In the case of a $C_L < C_C$, the previous equation cannot be used since R_Z must be greater than $\frac{1}{g_{m7}}$ in order to the zero to be moved into the left half plane. This was not the case and the nulling resistor has been sized to cancel the non dominant pole, therefore increasing the phase margin.
The nulling resistor has been implemented in Virtuoso using an ideal resistor for simulations. A MOSFET in triode region can be used for a real implementation.

3.8. Biasing of the circuit

In the previous sections the design of the core of the amplifier has been described. No attention has been paid on the biasing circuits since they are a complementary part.

The biasing of the amplifier is made starting from a single current source and using replica bias circuits to bias the current mirrors in the amplifier. Both standard replica bias and high swing current mirrors have been used and an example of the topologies is visible in Figure 3.4.

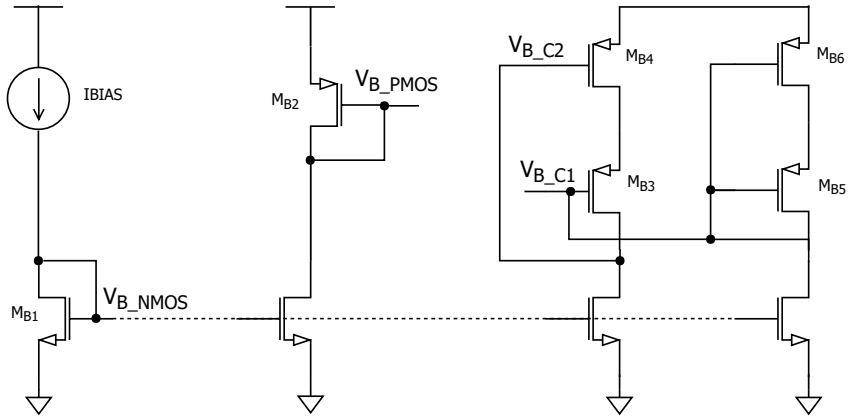

Figure 3.4.: Biasing current mirrors

The high swing configuration is used to bias the cascoded configuration in the first stage. The high swing solution is mandatory in this case because of the limited supply voltage available. The high swing bias circuit uses one more branch (M_{B5} M_{B6}) to generate the bias voltage $V_{B_{C1}}$. In this branch, the transistor M_{B6} is usually avoided and M_{B5} is designed to match the required bias voltage. If M_{B6} is used, M_{B5} is designed to be matched to M_{B3}; since $V_{GS_3} = V_{GS_5}$ (same current and same size), the drain to source voltage of M_{B6} sets the V_{DS} of M_{B4} because of the symmetry of the circuit. Analysing the circuit, M_{B6} is always biased in triode region and therefore it is designed through simulations.

In order to keep the power consumption of the biasing circuit limited to the respect of the power consumption of the amplifier, up to $1 \div 10$ current mirror ratios have been used. The power consumption of the biasing circuit is less than 10% of the total V_{DD} power. As already mentioned in the design of the amplifier, the current mirrors are biased with a low g_m/I_D in order to reduce the effect of the mismatches.

3.9. Switched capacitor feedback

The use of a switched capacitor feedback is mandatory in most of OTA based amplifiers, since a resistive feedback affects the low frequency open loop gain because of its loading effect at the output nodes.
The switched capacitor feedback can be used also to mitigate the effect of the input offset voltage of the amplifier and partially cancel the low frequency output noise. In fact, for frequencies well below the switching frequency f_S, the noise can be seen as a constant during the switching period and because of this its contribute can be seen as another offset voltage. This technique is known as *Correlated Double Sampling* (CDS).

Various CDS feedback topology can be used with two or more clock phases. The feedback network used in this design is presented in Figure 3.5. During the phase ϕ_1 the

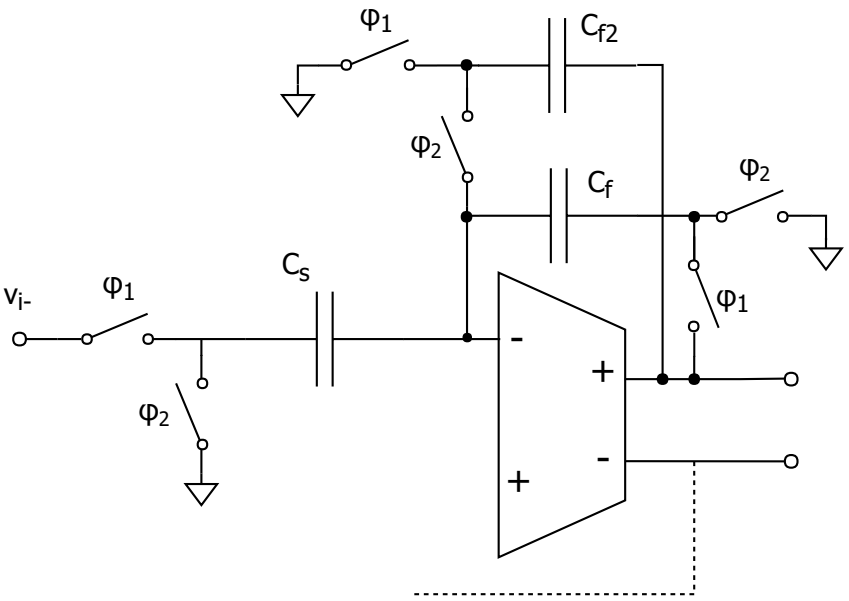

Figure 3.5.: Switched capacitor feedback

feedback is closed through the capacitor C_f and C_s and the output voltage is produced. At the same time C_{f2} is connected in parallel to the output and then the output voltage V_o is sampled in it. During ϕ_2 the input offset voltage is sampled in both C_s and C_f while the feedback is closed through the capacitance C_{f2} that still stores $V_o(\phi_1)$ voltage. This means that the output voltage of the amplifier will be $V_o(\phi_2) = V_o(\phi_1) + V_{os}$. The main advantage of this configuration lays on this property since V_o is kept close to what will be the next output voltage; this reduces the effect of the slewing of the amplifier and, at the

same time, this helps to improve the offset voltage cancellation since it is sampled with the amplifier kept in the correct working point.
The input offset voltage cancellation is really important for both the accuracy and the correct behaviour of the circuit, since its contribution onto the output voltage is multiplied by the non inverting gain of the amplifier:

$$V_o = A_V V_i + (1 + A_V)V_{os}$$

Beside the accuracy problem that can be taken into account afterwards, in such a high gain configuration, the offset voltage can compromise the working point of the amplifier, reducing the output swing or even more driving the output to saturation. The use of a CDS feedback network is therefore compulsory in this case.

The closed loop gain of the amplifier can be written as:

$$A_V = \frac{C_s}{C_f}\frac{L_{DC}}{1 + L_{DC}}$$

Since $L_{DC} >> 1$ for design, the closed loop gain is set just from the ratio of the feedback capacitance C_s/C_f. The absolute values of the capacitance cannot be set too small in order to guarantee immunity to the charge injection phenomenon, but, at the same time, they cannot be set too big in order to avoid a degradation of the performances due to the loading effect of the feedback network on the amplifier output nodes. In this project only ideal switches have been used and so a precise design is not considered.

3.10. Switching Frequency and settling time

The speed of the amplifier response is affected mainly by these contributes:

- bandwidth of the closed loop amplifier; in fact, the closed loop frequency response can be approximated with a single pole response with the pole located at the crossover frequency of the loop gain ω_c. The time response can then be considered to be an exponential with a time constant $\tau_c = 1/\omega_c$;
- finite slew-rate of the amplifier
- finite speed of the feedback network due to the poles introduced by the ON resistance of the switches. This effect, as already mentioned, is not taken into account in this project.

Considering the first term we can analyse the step response writing:

$$V_o(t) - V_O(0) = A_V(V_i(t) - V_I(0))(1 - e^{-\frac{t}{\tau_c}})$$

If we consider the settling time t_o in order to achieve a dynamic error equal to the static error, the expression can be written:

$$\epsilon_d = e^{-\frac{t_o}{\tau_c}} = \frac{1}{128} \rightarrow t_o = -\tau_c \ln\left(\frac{1}{128}\right)$$

Since the complete settling must happen during only the phase ϕ_1, the settling time t_o must be lower than half of the switching period T_S. This leads to:

$$\frac{T_S}{2} \geq -\tau_c \ln\left(\frac{1}{128}\right) \rightarrow \frac{\omega_c}{2f_S} \geq -\ln\left(\frac{1}{128}\right) \rightarrow \frac{f_c}{f_S} \geq -\frac{1}{\pi}\ln\left(\frac{1}{128}\right) = 1.55$$

We now consider the finite speed due to the slew-rate (SR) of the amplifier. The slewing is a non linear effect that is caused by a saturation of the currents in one of the two stages of the amplifier.
Considering the first stage, the limitation is introduced by the differential pair small signal current, since its maximum value is limited by the tail generator I_{tail}. The same consideration can be made on the output stage. When the current saturates, the amplifier enters in the slewing region. In this condition, the output voltages of the first or the second stage will have a constant slope behaviour that is due to a constant current charging a capacitance. The slope of the output voltage is what we call slew-rate:

$$SR_1 = \frac{\mathrm{d}V_o}{\mathrm{d}t} = \frac{I_{tail}}{C_c}$$
$$SR_2 = \frac{\mathrm{d}V_o}{\mathrm{d}t} = \frac{2 \cdot I_2}{C_2}$$

where:

- SR_1 is the slew-rate introduced by the first stage;
- I_{tail} is the tail generator bias current of the input differential pair;
- C_c is the Miller capacitance. In fact C_c is connected in parallel of a high gain stage, represented in this case by the second stage, that acts as an integrator of the small signal current coming from the input pair;
- SR_2 is the slew-rate introduced by the second stage;
- I_2 is the bias current of the second stage, doubled because of the two outputs;
- C_2 is the equivalent capacitance seen from the output node and it is composed of the parallel combination of both the total load capacitance $C_{L_{eq}}$ and the Miller capacitance C_c.

More in detail, the slew-rate due to the second stage is not symmetric to the respect of the two outputs of the amplifier. In fact, due to the PMOS driven configuration, I_2 represents the sink current limit that correspond to a turn off of the driver. The limit on the source current is instead due to the V_{GS} swing allowed at the input side of the second stage. Normally the sink current represents the most limiting contribute.
The final slew-rate of the amplifier will be the most stringent of the two slew-rates.

Since the slew-rate represents the speed limit of the output voltage variation, its contribute can be studied considering the derivative of the output signal. Considering a sinusoidal input signal $V_i(t) = V_I \sin(\omega_o t)$ we obtain:

$$V_o(t) = A_V V_I \sin(\omega_o t) \;\rightarrow\; \frac{\mathrm{d}V_o}{\mathrm{d}t} = A_V V_I \omega_o \cos(\omega_o t) \rightarrow \max\left(\frac{\mathrm{d}V_o}{\mathrm{d}t}\right) = A_V V_I \omega_o$$

This means that, if the speed required to produce the output voltage is greater than the slew-rate of the amplifier, the output voltage will be distorted.
A second boundary on the maximum switching frequency is therefore introduced by the slew-rate; to take care of it, simulation analysis are required since the amplifier operates in a switched capacitor feedback and then it must handle the fast transition occurring between the two phases. The CDS configuration used in this project helps to mitigate this problem as explained in the previous section.

Results and Discussion 4

This chapter will go through the verifications steps and the final results of the design presented above.

4.0.1. Open Loop Gain and Stability

In Figure 4.1 the open loop frequency response of the amplifier is shown. The frequency response of the first stage is also displayed to show that the design target of 65 dB is achieved. It is possible to see that the amplifier is not fully compensated since the second pole appears before the unity gain frequency. Considering a tolerated phase margin $PM = 70°$, the resulting minimum closed loop gain is about 20 dB, well below the required gain considered here.

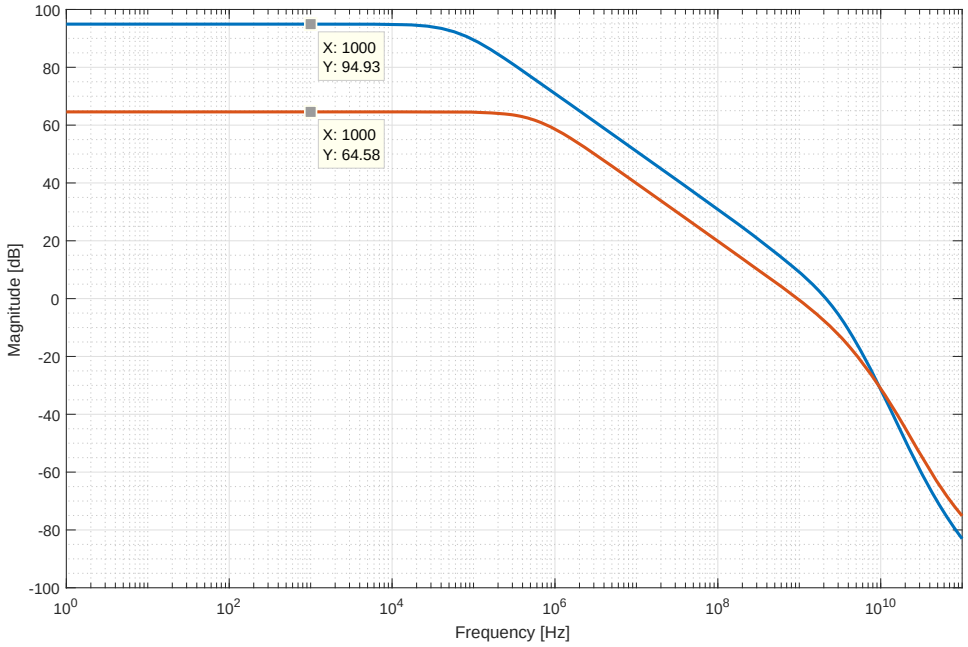

Figure 4.1.: Open Loop gain of the First Stage and the complete amplifier

Some attention must be paid on the loop gain of the positive feedback configuration. The simulation is shown in Figure 4.2 in both gain and phase response. The negative loop gain shows that the positive feedback loop is stable; the more the loop gain approaches 0 dB the more the gain boost is introduced, but this will make the amplifier prone to instability when mismatches and process variations are considered.

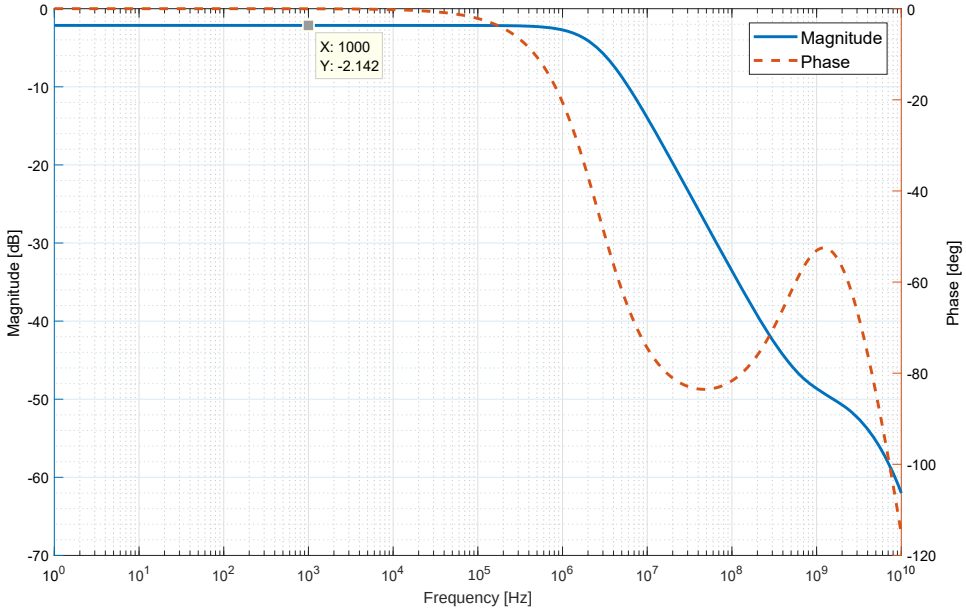

Figure 4.2.: Positive Feedback - Loop Gain

A Monte Carlo simulation (50 simulation with both process and mismatches) of the open loop gain was performed in order to make sure that the minimum gain target is respected. The result is displayed in Figure 4.3 and it shows that a the low frequency gain is the only thing affected by mismatches and process variation, while the GBW and the phase response are not heavily affected at the frequencies of interest:

$$A_{OL_{MIN}} = 87.8\,\text{dB} \; > 85\,\text{dB}$$
$$GBW \in [3.1 \div 3.9]\text{GHz}$$

.

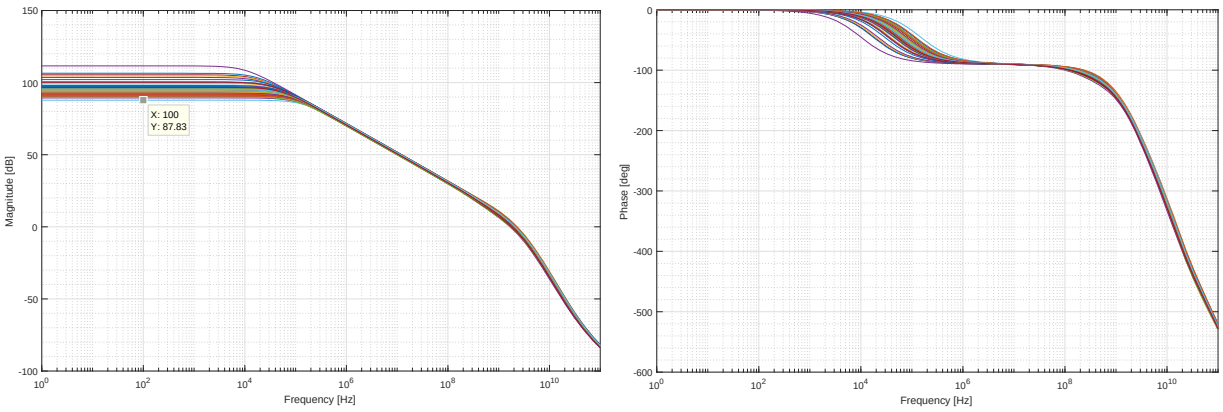

Figure 4.3.: Open Loop Gain and Phase response - Monte Carlo Simulation

The input offset voltage is also characterized with a Monte Carlo simulation:

$$\sigma(V_{os}) = 3.8\,\mathrm{mV}_{RMS}$$

Even though the result can be considered relatively low, the proper working of the amplifier is ensured by the usage of a CDS feedback as explained in the design section.

To check the stability of the closed loop amplifier a continuous time feedback was used. The loop gain is shown in Figure 4.4 and highlights a closed loop bandwidth $f_c = 27.3\,\mathrm{MHz}$ and a phase margin of almost 90°; a Monte Carlo simulation was considered also in this case but, as already said, the phase response is not affected, maintaining a $PM > 85°$. The same happens for the closed loop bandwidth that is kept in a range $f_c \in [24.8 \div 29.8]\,\mathrm{MHz}$.

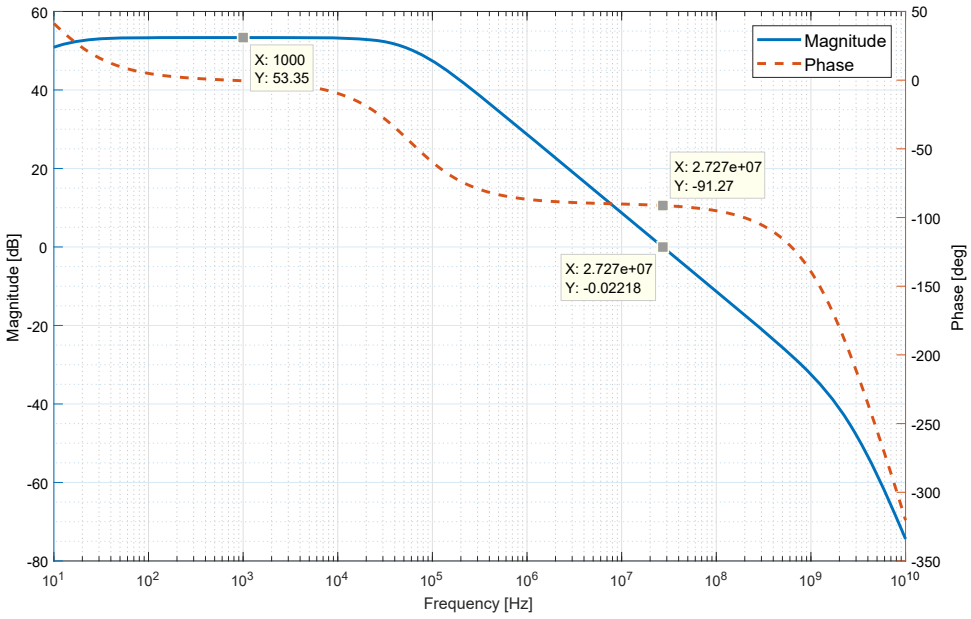

Figure 4.4.: Closed Loop Amplifier - Loop Gain

4.0.2. Slew-Rate and Switching Frequency

In Figure 4.5 the simulation of the slew-rate of the amplifier is presented. The simulation is done giving a wide input step in order to completely unbalance both the input pair and the output stage. The result is a slew-rate $SR \approx 220\,\mathrm{V/\mu s}$. As expected, the result shows that the slew-rate limitation is introduced by the bias current of the second stage of the amplifier. In fact, the theoretical values for the two slew-rates are:

$$SR_1 = \frac{\mathrm{d}V_o}{\mathrm{d}t} = \frac{I_{tail}}{C_c} = \frac{130\,\mu\mathrm{A}}{40\,\mathrm{fF}} = 3250\,\mathrm{V/\mu s}$$

$$SR_2 = \frac{\mathrm{d}V_o}{\mathrm{d}t} = \frac{2 \cdot I_2}{C_{L_{eq}} + C_c} = \frac{2 \cdot 20\,\mu\mathrm{A}}{160\,\mathrm{fF}} = 250\,\mathrm{V/\mu s}$$

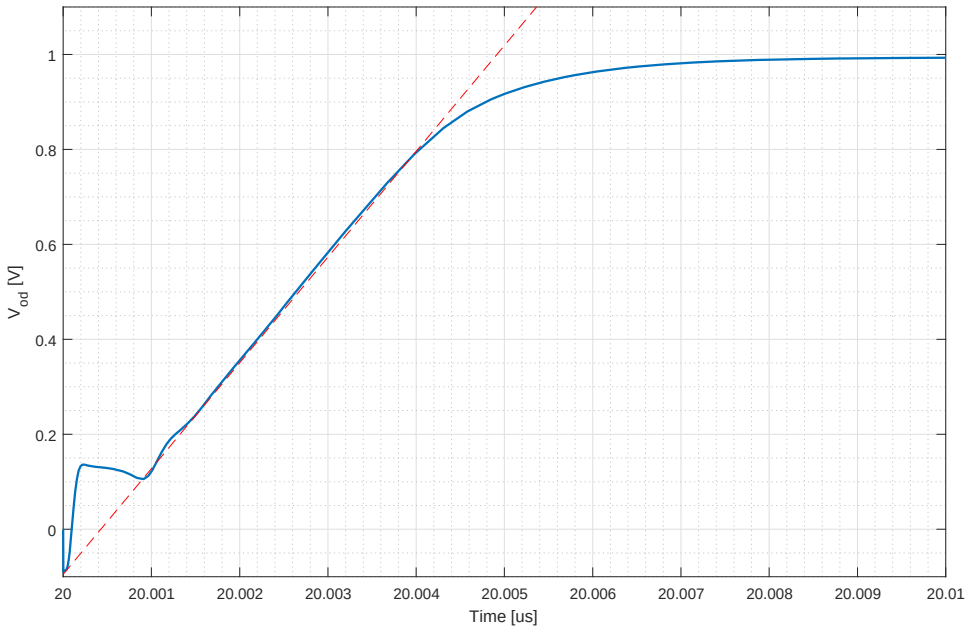

Figure 4.5.: Slew Rate

where $C_{L_{eq}}$ is the effective load capacitance at the two output nodes (explicit load capacitance, feedback network loading, common mode feedback loading and parasitics):

$$C_{L_{eq}} = C_L + (1-\beta)C_f + C_{2_{CMFB}}$$

From the result it is possible to calculate the upper bandwidth limit introduced by the slew-rate, also know as *Power Bandwidth*, that indicates the maximum allowed sinusoidal input frequency considering a full swing output voltage:

$$f_{MAX_{SR}} = \frac{SR}{2\pi V_{O_{FS}}} = 19.5\text{MHz}$$

The result shows that the most strict boundary on the maximum switching frequency is due to the closed loop bandwidth of the amplifier f_c. Previously it was demonstrated that a ratio $f_c/f_s = 1.55$ is necessary in order for the dynamic error to be equal to the required accuracy. In this case, the switching frequency is set at $f_c/f_s \approx 5 \rightarrow f_s = 5\,\text{MHz}$. With this choice, we can get rid of the dynamic error since it will be $< 0.1\% \rightarrow << 1/128$

4.0.3. Closed loop amplifier - SC Feedback

After the characterization of the continuous time behaviour, the amplifier is now tested with the switched capacitor feedback and including the SC-CMFB. The main behaviour of the amplifier does not change when the SC feedback is applied, but some differences are introduced and must be tested.

Figure 4.6 shows the full swing sinusoidal output waveform, strobed at the end of the sampling phase ϕ_1 (i. e. when the output is ready). A Monte Carlo simulation is

then performed in order to include the effects of mismatches (in particular the second harmonic distortion). An FFT is then computed on all the output waveforms with the purpose of calculating the output distortion power. The worst case of the Monte Carlo simulations is reported in Figure 4.7 and it shows a second and third harmonic distortion respectively $HD_2 \approx -64.5\,\text{dB}$, $HD_3 \approx -49.7\,\text{dB}$. Considering all the harmonics, the signal to distortion power ratio is $SDR = 46.3\,\text{dB}$, that is equivalent to a 7.4 bit accuracy. The result shows that a pk-pk output swing of $V_{O_{FS}} = 1.8\,\text{V}_{pp}$ fulfills the requirements on the output distortion power. At first, the swing was set to be $1.6\,\text{V}_{pp}$ that is a more common input swing of a SAR ADC with this supply voltage. The choice of increasing the output swing was taken considering also the contribute of output integrated noise. From the specifications:

$$V_{N_{RMS}} \leq \frac{V_{O_{FS}}}{128}$$

Two considerations can be made:

- increasing the output swing allows more headroom for the output integrated noise and this leads to a smaller compensation, with benefits on bandwidth and power consumption;
- the distortion power should be comparable to the noise power in order to use the amplifier more efficiently;

After this considerations, the output swing was increased to $V_{O_{FS}} = 1.8\,\text{V}_{pp}$ with the purpose of increasing the distortion power and set it close to the minimum required $SDR = 42.1\,\text{dB}$.

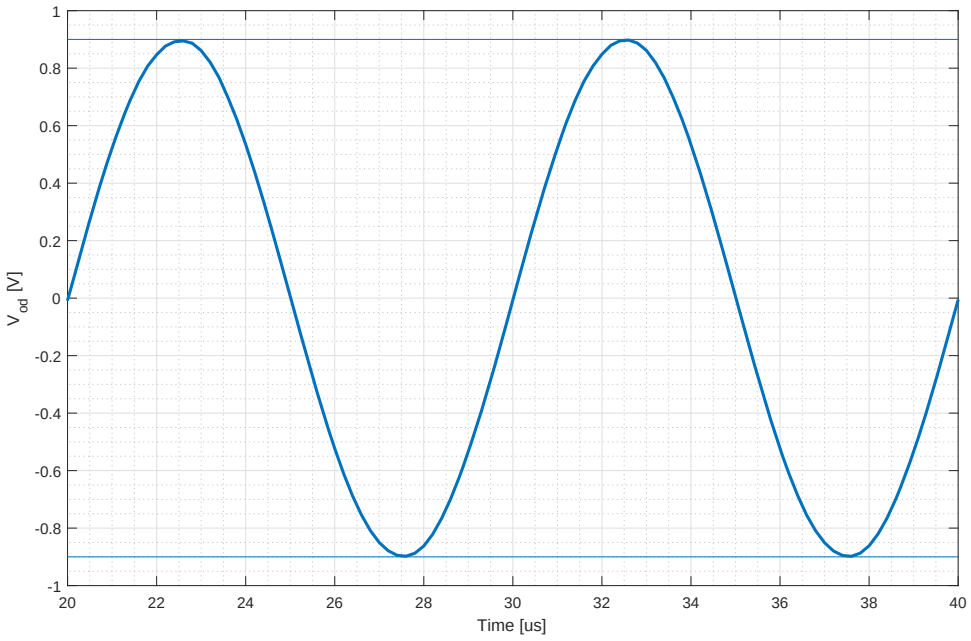

Figure 4.6.: SC Feedback Amplifier - Full Swing transient (Strobed)

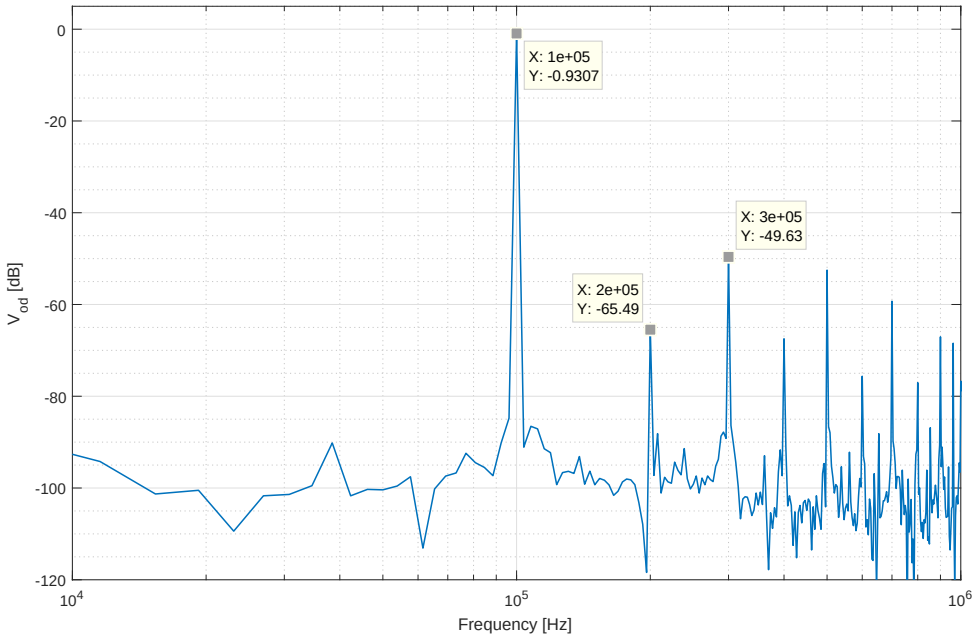

Figure 4.7.: SC Feedback Amplifier - Worst case distortion at full swing

Regarding the output noise, the first tests were done using the continuous time feedback. This has been helpful in locating the main noise sources and then in lowering their contributions. In fact the main contribution was due to the flicker noise of the transistors with the highest bias currents (the input differential pair and the two tails in the folding nodes). To reduce these components, the dimensions of the transistors were increased, since the flicker noise is inverse proportional to the area of the device.
For the final result, the SC feedback must be used in order to take into account also the noise folding contribution as explained in 2.3.4. The noise simulation is performed with a transient analysis, with a noise bandwidth of $[1\,\text{kHz} \div 1\,\text{GHz}]$ and without any input signal (worst case condition). The result is:

$$V_{N_{RMS}} = 12.4\,\text{mV}_{RMS} \quad < \frac{V_{O_{FS}}}{128} = 14.0\,\text{mV}_{RMS}$$

As final test, a step response of the amplifier was performed and the result is shown in Figure 4.8. The main purpose of the test was to measure the settling time of the amplifier in a non slewing condition. The input signal, in fact, is set to be 1 mV in order to maintain both the differential pair and the second stage in a linear condition. The result shows a 0.1% settling time of about 50 ns that is in accordance with the predicted settling given by the closed loop bandwidth f_c:

$$t_s = \frac{1}{2\pi f_c} \ln \epsilon_d = 43\,\text{ns}$$

In the figure it is also shown the sampling phase ϕ_1 with the purpose of comparing it to the settling time. As expected, the switching frequency could be pushed further up but, in this case, the slewing of the amplifier should be taken into account with more detailed

simulations.

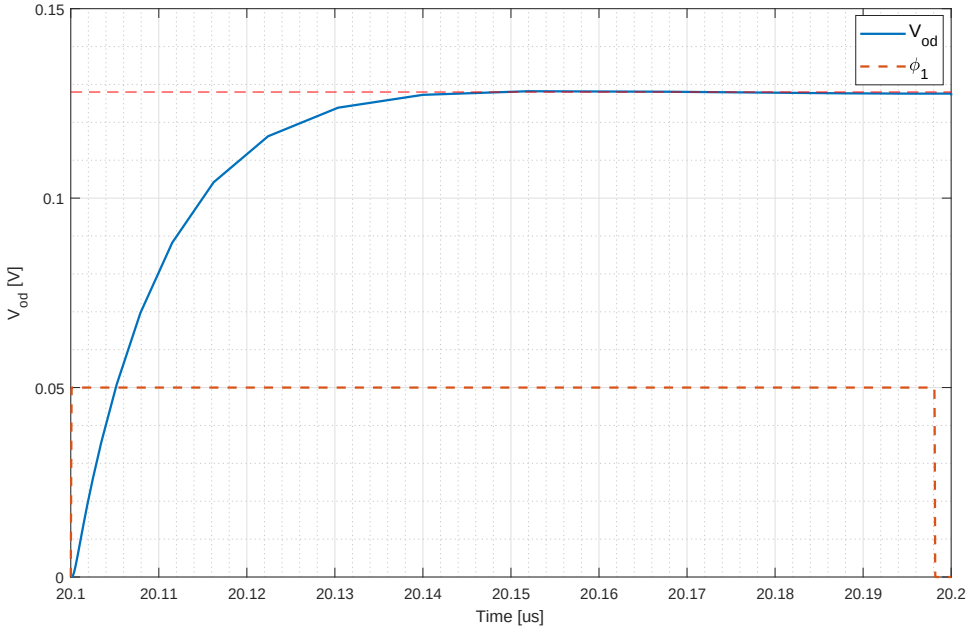

Figure 4.8.: SC Feedback Amplifier - Step Response

4.0.4. Power Consumption

The power consumption was not a defined target but the design was done taking care of keeping it as low as possible.
The consumption of the only amplifier is about 215 µW while the biasing circuits require about 25 µW.
As previously seen from the results, both the GBW and the slew-rate are overkilled compared to the design requirements. This means that the bias current of both stages can be reduced. A careful redesign should also be targeted to a noise reduction approach in order to shrink the Miller capacitance and therefore reduce the power consumption.

4.0.5. Summary and final discussions

A summary of the results is visible in Table 4.1

Result / Value	Min	Typ	Max	σ	Unit
Open Loop Gain	87.8	94.9	-	-	[dB]
GBW interpolated	3.1	3.5	3.9	-	[GHz]
Minimum gain ($PM = 70°$)	-	20	-	-	[dB]
Slew-rate	-	220	-	-	[V/µs]
Loop Gain	46.1	53.4	-	-	[dB]
Closed Loop BW	24.8	27.2	29.8	-	[MHz]
Phase Margin	88	89	-	-	[°]
Settling Time 0.1%	-	50	-	-	ns
Output Swing Pk-Pk	-	1.8	-	-	[V_{pp}]
Output Common mode voltage	-	500	-	-	[mV]
Input Offset Voltage	-	-	-	3.8	[mV_{RMS}]
Output RMS Noise	-	-	-	12.4	[mV_{RMS}]
SDR	46.3	-	-	-	[dB]
Supply Voltage	-	1	-	-	[V]
Amplifier power consumption	-	215	-	-	[µW]
Overall power consumption	-	240	-	-	[µW]

Table 4.1.: Summary of the result

Conclusions and Further work 5

This project went through most of the main steps required for the design of an integrated circuit block, starting from the derivation of the requirements, through the understanding and the comparison of different solutions, and ending with the final design that was done taking care of most of the aspects, like mismatches and process variations, distortion, noise and power consumption. The main target was the design of the open loop amplifier, but to really be able to characterize it, a closed loop configuration was required. Therefore, the choice of using a switched capacitor feedback allowed a more in depth study of the most common implementation of a feedback loop, with its drawbacks and side effects. No considerations were done on the Layout of the circuit since it requires knowledge and, moreover, time to mature experience and get confidence with the rules and the practical approach.
The project was carried out with an extensive use of the Spectre simulator included in Virtuoso Analog Design Environment, starting with the basic analysis and ending with the lately introduced periodical steady state simulations that are getting more and more common nowadays.

The positive feedback solution used in this work has turned out to be a modestly efficient gain boosting technique. Its main problem lays on its robustness against mismatches and process variations. A lot of effort was put in this problem in order to ensure the stability of the amplifier, paying, of course, on the gain boosting factor. The main benefit of this configuration is that it doesn't increase the power consumption of a standard folded cascode stage. Even though the gain boosting achievable is not comparable with an active cascode configuration, it comes "for free" in terms of power consumption and complexity of the circuit. Moreover, the positive feedback principle can be applied also locally, for example in the input differential pair or in the second stage. This would lead to a higher gain boosting factor with a more robust circuit.

The noise requirement represented another difficulty in the design. Large area transistors have been used in order to reduce the flicker noise component. Increasing the size of the devises brings also benefits to the robustness against mismatches, but at the same time, increases the parasitic capacitances, hence a trade off between all these components must be considered.

Although all the requirements have been fulfilled, many improvements can be done to the proposed configuration. For sure the power consumption can be reduced with

a more careful design, focusing on lowering the noise contributions at first, as well as improving the positive feedback gain boosting factor to the respect of mismatches and process variations.
Introducing real switches, a more accurate design of the feedback network can be made and the switching frequency can be pushed up to the speed limit of the amplifier. In terms of power consumption, an adaptive biasing technique [5] can be used in order to control the bias current of the stages proportionally to the input voltage, therefore increasing the overall efficiency of the circuit.

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[3] Paul R. Gray Paul, J. Hurst Stephen, H. Lewis Robert, G. Meyer, "Analysis and Design of Analog Integrated Circuits, 5th Edition", *John Wiley & Sons*, 2009. vii, 20, 21

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[5] Giuseppe Ferri, Vincenzo Stornelli, and Angelo Celeste, "Integrated Rail-to-Rail Low-Voltage Low-Power Enhanced DC-Gain Fully Differential Operational Transconductance Amplifier", *ETRI Journal*, December 2007. 38

Appendix A

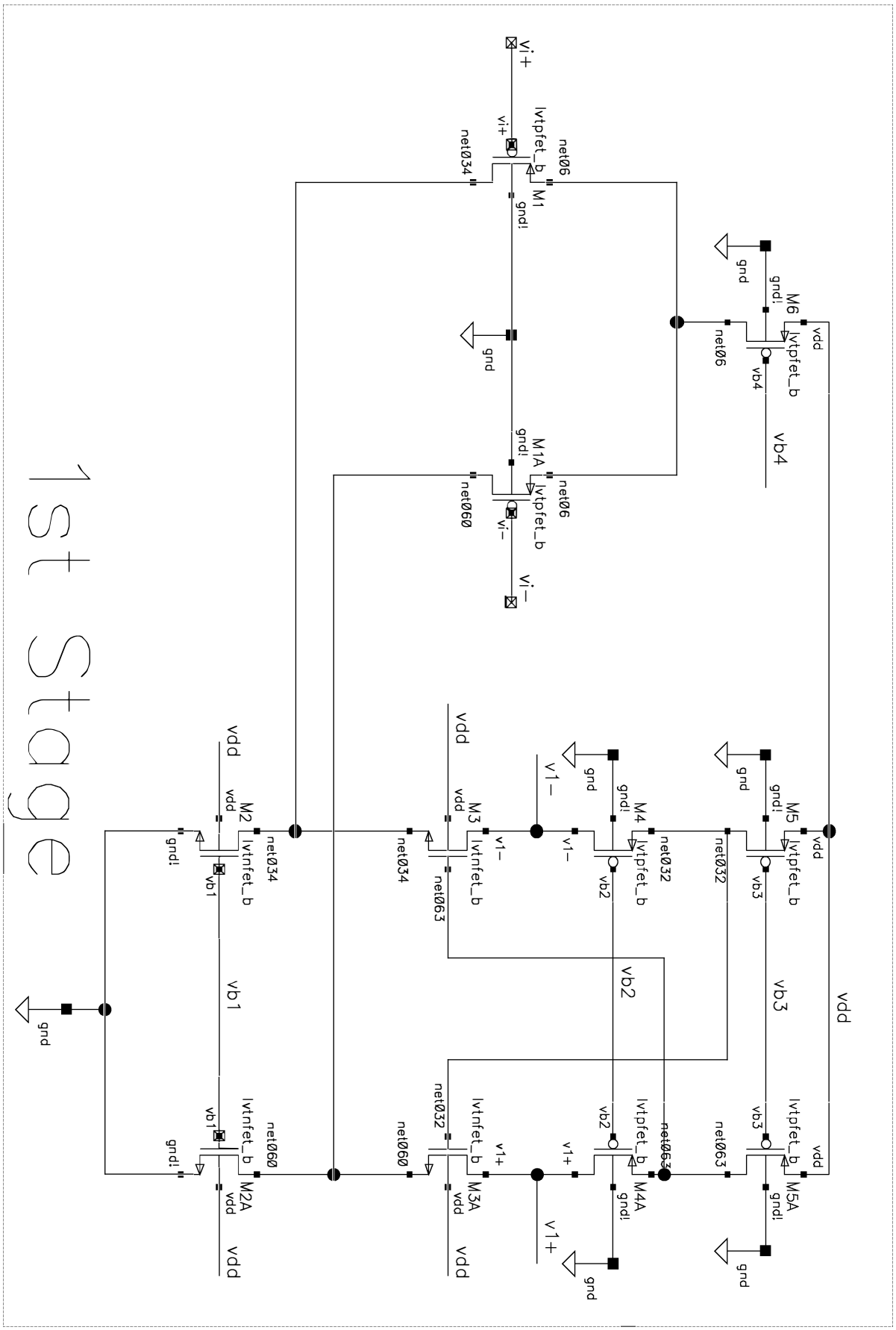
The following tables report the dimensions of the transistors and of the other components used for the amplifier and the SC-feedback; the biasing circuit is omitted. The names are related to the schematics attached below

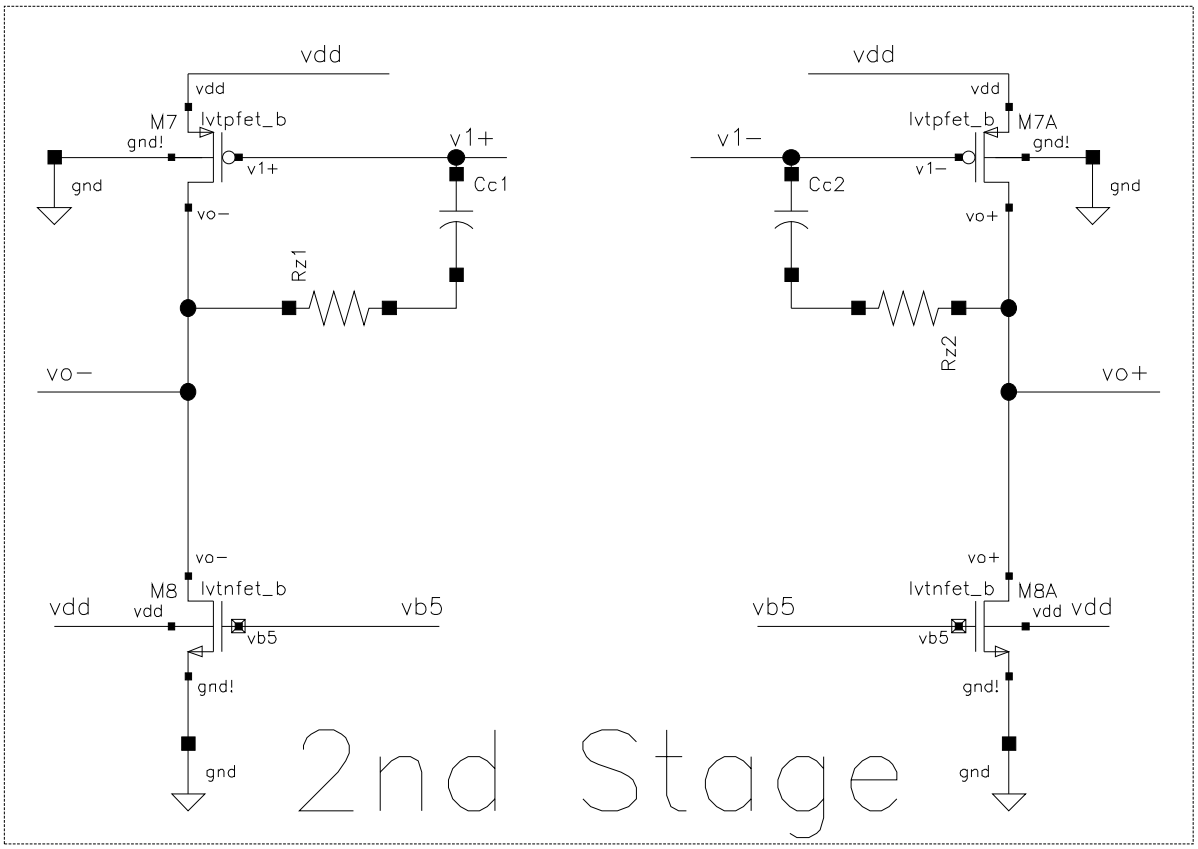
Transistor	Length [nm]	Width [µm]	I_D [µA]	g_m/I_D
M1, M1A	$2.5 \cdot 30$	10.5	67	15.9
M2, M2A	$8 \cdot 30$	2.5	88	9.6
M3, M3A	$4 \cdot 30$	0.6	22	10.9
M4, M4A	$4 \cdot 30$	2.3	22	12.4
M5, M5A	$4 \cdot 30$	1.2	22	9.1
M6	$4 \cdot 30$	6.0	135	8.5
M7, M7A	$3 \cdot 30$	4.2	18	16.9
M8, M8A	$8 \cdot 30$	0.57	18	9.6

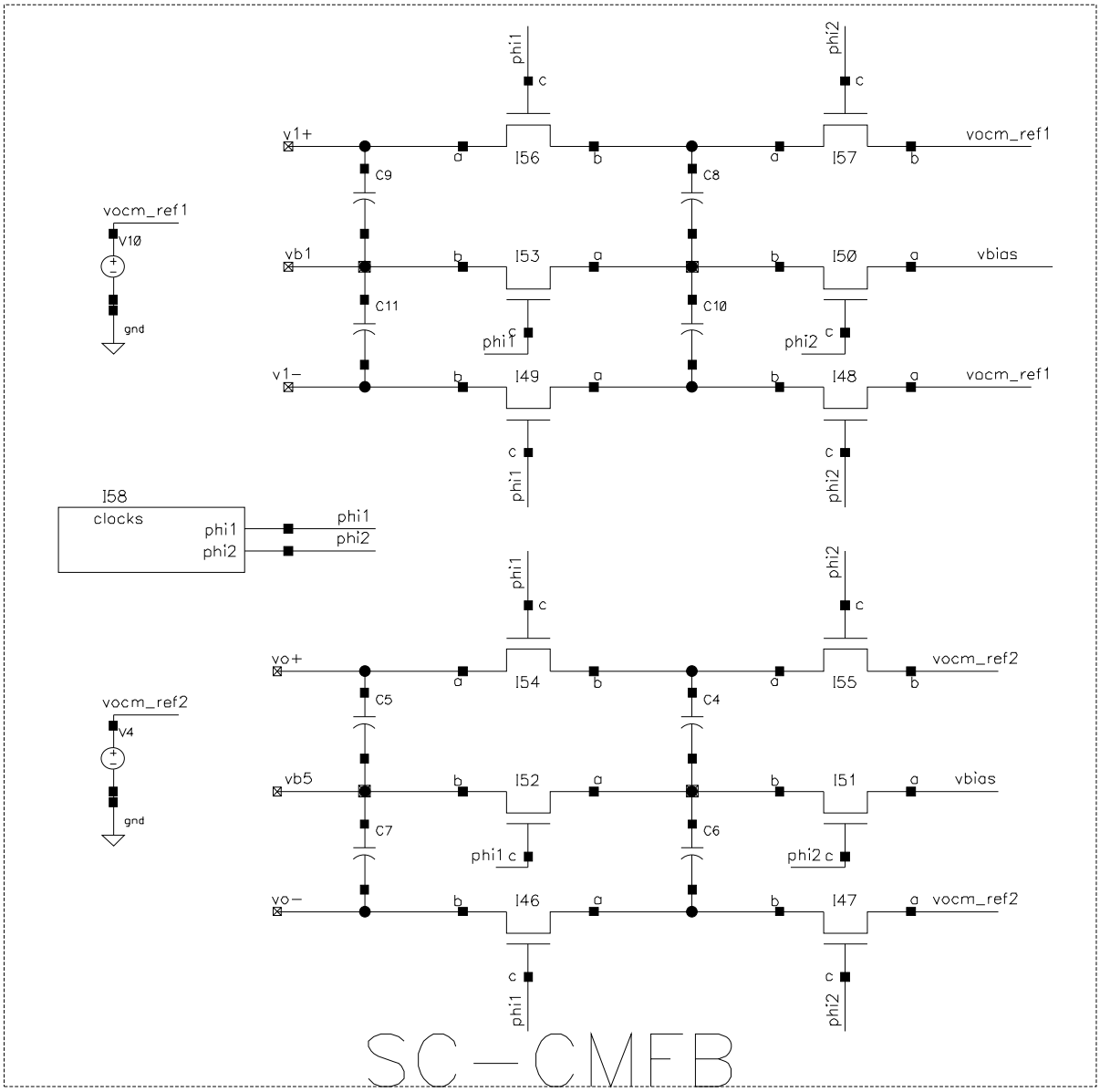
Table A.1.: Dimensions of the transistors of the two stages (bias circuit is omitted)

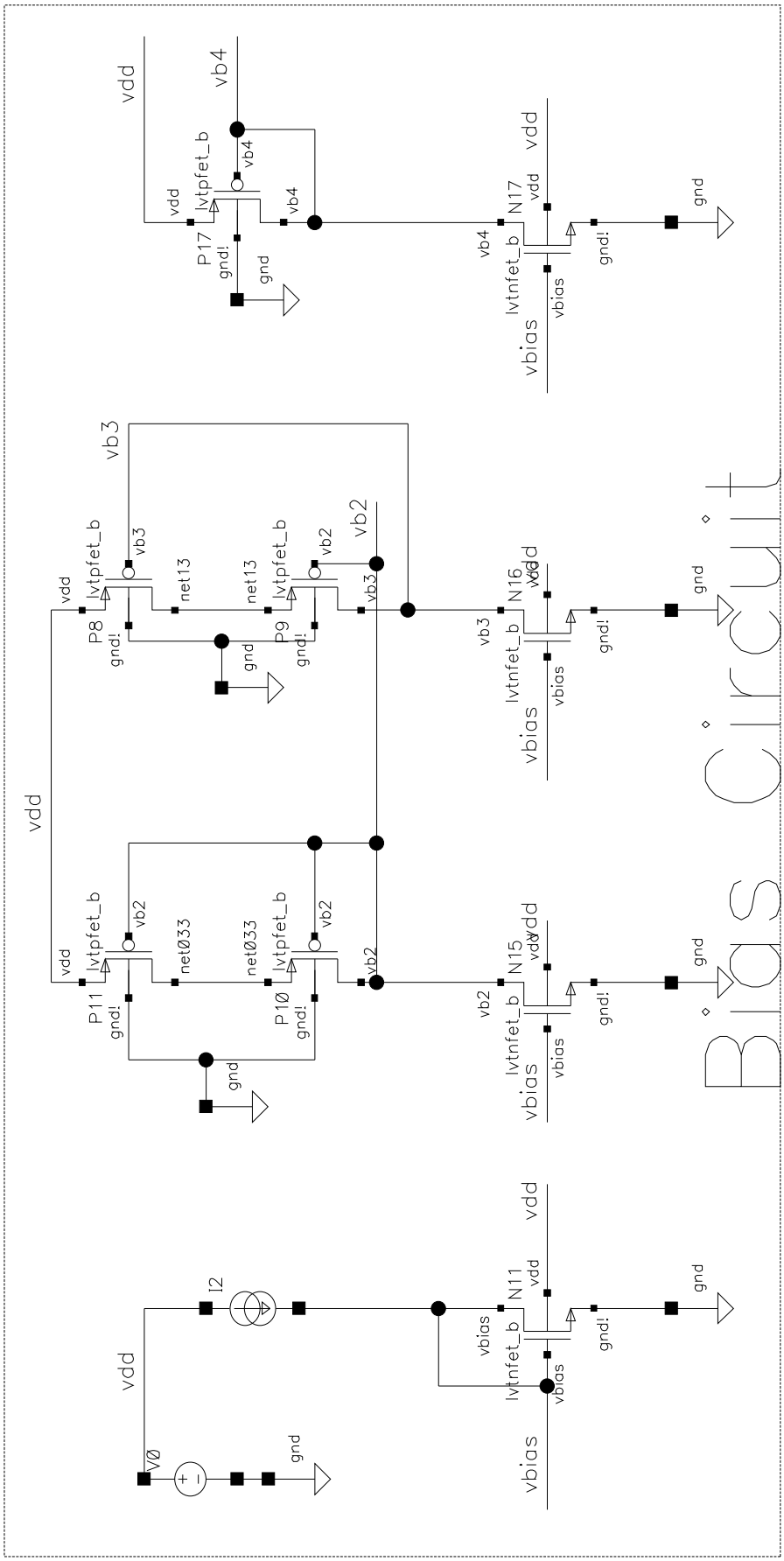
Component	Value	Unity
C_c, C_{c_1}	40	fF
R_z, R_{z_1}	12	kΩ
C_s, C_{s_A}	1.28	pF
C_f, C_{f_A}, C_{f2}, C_{f2_A}	10	fF
C_4, C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}	10	fF
C_{45}, C_{46}	100	fF
I_2	10	µA
V_{ref_1}	550	mV
V_{ref_2}	500	mV

Table A.2.: Component values


1st stage
vi+
vi−
lvtpfet_b
lvtnfet_b
M1
M1A
M2
M2A
M3
M3A
M4
M4A
M5
M5A
M6
net06
net034
net060
net032
net063
vb1
vb2
vb3
vb4
v1−
v1+
vdd
gnd
gnd!


vdd
vdd
M7
lvtpfet_b
gnd!
v1+
gnd
v1+
Cc1
vo−
Rz1
vo−
vo−
M8
lvtnfet_b
vdd
vdd
vb5
vb5
gnd!
gnd
2nd Stage
vdd
vdd
lvtpfet_b
M7A
v1−
gnd!
v1−
Cc2
gnd
vo+
Rz2
vo+
vo+
lvtnfet_b
M8A
vb5
vdd
vdd
vb5
gnd!
gnd


SC—CMFB
v1+
v1−
vb1
vo+
vo−
vb5
vocm_ref1
vocm_ref2
vbias
V10
V4
gnd
C9
C8
C11
C10
C5
C4
C7
C6
I56
I57
I53
I50
I49
I48
I54
I55
I52
I51
I46
I47
I58
clocks
phi1
phi2


Bias circuit
vdd
gnd
V0
I2
vbias
vb2
vb3
vb4
lvtpfet_b
lvtnfet_b
P11
P10
P8
P9
P17
net033
net13
N11
N15
N16
N17
gnd!