A Survey of A/D-Converter Performance Evolution

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***Abstract*— This paper presents the performance evolution over time for monolithic ADC implementations reported in scientific publications. The survey is based on an exhaustive search of IEEE journals and conferences central to the field from 1974 to 2010 and thus represents a near-exhaustive survey of reported scientific ADC data. Based on the full set of historical data, empirically observed evolution trends are extracted. The trends are used to predict the state-of-the-art specifications of future ADCs and also form a valuable reference and complement to theoretical performance limits derived in other works.**

Keywords*— *Analog-digital conversion, ADC

I. INTRODUCTION

Over a period of approximately 36 years, the field of monolithic A/D-Converter (ADC) integration has evolved at an exponential rate from the delta-modulator reported by Baldwin, et al. [1] in 1974. The evolution of ADC technology has been an essential enabling factor for a wide range of applications, spanning from low power *system-on-chip* (SoC) solutions for consumer electronics to high-performance front-ends in digital communication nodes. From a systems point-of-view, it is therefore crucial to understand the rate of ADC performance evolution, so that system-level roadmaps can be adapted to what can be realistically expected from ADC technology at any given time. Several authors have presented work, combining to various degrees performance evolution surveys and derivations of theoretical and practical limits. Walden's survey [2] analyzed the performance evolution as defined by 150 commercial and scientific ADCs reported between 1978 and 1997. It was the first to be based on a larger set of empirical data, and the trends detected in the data was compared to a set of derived theoretical limits including thermal noise, jitter, comparator metastability, and Heisenberg's principle of uncertainty. Le et al. reviewed performance data from nearly 1000 commercial ADCs [3], and the survey by Murmann [4] is a recent contribution to the analysis of empirical performance data covering around 260 scientific ADCs reported 1997-2008. Other relevant work is found in [5]-[8]. This paper is based on a data set extracted from more than 1400 scientific publications published from 1974 to present day (March 2010), thus representing a near-exhaustive survey of the entire body of experimental ADC performance data reported in major IEEE publications. Data was collected from an exhaustive survey of papers reporting measured ADC performance in the *IEEE J. of Solid-State Circuits* and *IEEE Transactions on Circuits and Systems*, as well as seven major conferences. To the best of the author's knowledge, this makes it the largest and most comprehensive survey of scientific ADC implementations to this date. The results presented in this paper focus on general performance trends over time, and parameters of relevance to a broad range of architectures.

II. PROCESS TECHNOLOGY

ADC performance is limited to a large degree by the available device technology. Evolution of ADC performance is therefore correlated with the simultaneous evolution of process technology. Recent designs benefit from the scaled device geometries and higher bandwidth, but suffer in dynamic range and sampling linearity due to reduced supply voltages and available swing. With the increasing interest in one-chip solutions, the demand for SoC-compatible ADCs implemented in current digital processes is high [9]. This is reflected in an accelerated adoption rate for new CMOS nodes.

A. Device scaling

Fig. 1 shows the CMOS technology nodes used for scientific ADC implementations over time, thus illustrating the adoption rate for new CMOS nodes within the ADC field. Flash ADC implementations in 0.30 and 0.25 µm SOS/CMOS using focused-ion-beam implants as part of the processing were reported by Walden et al. 9-10 years before any other ADCs in similar geometries [10]-[11]. Apart from these designs by Walden, the lowest reported channel length L was halved every 5.4 years according to a log-fit of the highlighted state-of-the-art data until 1995. The increase in adoption rate after 1997 is clearly seen, and a fit of the state-of-the-art data for 1995-2010 reveals that L has been halved every 3.7 years for the last 15 years. The current trend would suggest *ADCs implemented in 5 nm CMOS by 2020*. This is, however, significantly below the ~10 nm predicted for digital in [12]. A slowdown in the adoption rate is therefore to be expected as the gap between ADCs and digital ICs close.

B. Supply voltage reduction

As a consequence of device scaling, the power supply voltages are also reduced. The supply voltage (VDD) reported for ADCs over time is shown in Fig. 2. Until 1985, the low-voltage state-of-the-art remained fixed at 5 V. During the 22 years from 1985 to 2007, it was in average reduced by half every 5.1 years although in rather coarse steps. The lowest reported VDD to this date, 0.2V, was first used in a VCO-

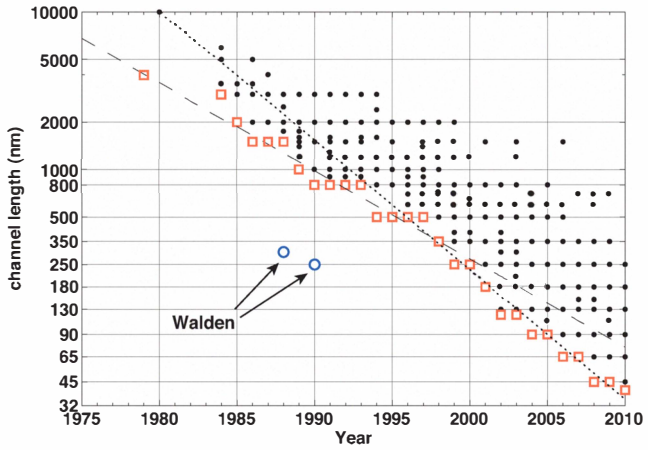

Figure 1. CMOS technology nodes reported for scientific ADC implementations over time. Adoption rates until 1995 (dashed), and from 1995 to present-day (dotted).

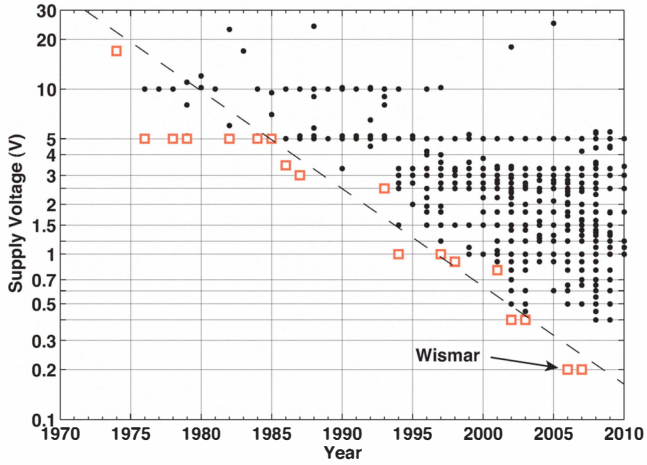

Figure 2. Supply voltage for scientific ADCs over time. Trend line fit to state-of-the-art evolution data points 1985-2007.

based delta-sigma modulator design by Wismar et al. [12]. Following the current trend, *ADCs operating with 40 mV supplies will have been reported around 2020.*

III. Noise

While non-linear distortion, memory effects, and device mismatch can to a certain extent be modeled and calibrated for, thermal white noise can not, and is therefore one of the most fundamental limitations of ADC performance [8]. It must be addressed by circuit-, architecture-, or system-level design. Since it is easier to achieve a high *signal-to-noise ratio* (SNR) in a narrow bandwidth, the relative noise-floor n_r in dB/Hz

$$n_r = -\left(\mathrm{SNR} + 10\log_{10} BW\right) \tag{1}$$

was used as the noise parameter for this study. This enables noise performance comparison between widely different ADCs. Fig. 3 shows that ADC noise-floor has improved at an average rate of 2 dB/year until year 2000, after which it has remained in saturation. A likely explanation for this trend is the lower signal swing, and thus higher relative noise-floor implied by the continuous technology scaling [14]. Although the *absolute* noise-floor may remain intact [15], the *relative* noise-floor is raised when signal swing is reduced. New technologies allow higher bandwidths, but the *simultaneous combination of SNR and bandwidth* has not improved for a decade due to this inherent dynamic-range limitation of nanometer technology. This is an expected, yet significant result of the study as it clearly confirms the commonly raised concerns regarding analog design in nanometer technologies, e.g., in [4], [6], [14]-[15]. With a further reduction in signal swing, *future ADCs could very well fail to maintain even the current state-of-the-art in noise performance*.

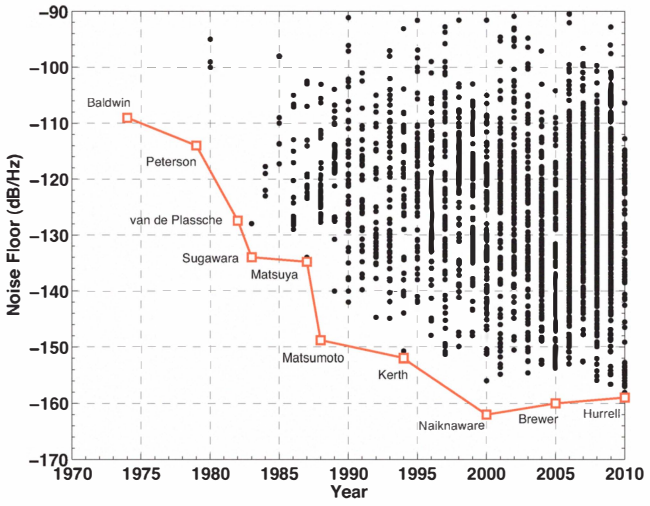

Figure 3. Evolution of relative noise-floor. Saturation is evident

IV. Sampling Rate and Resolution

Two key parameters for ADCs are *Nyquist sampling rate* (f_s) and *resolution* (N). The *effective number-of-bits* (ENOB) calculated from *signal-to-noise-and-distortion-ratio* (SNDR) [4] is commonly used instead of N as a measure of the actual resolution. Since a high resolution is readily achieved at low sampling rates, and a high sampling rate is less of a challenge with relaxed resolution requirements, the evolution of f_s and ENOB should be observed simultaneously. It was chosen to observe the evolution of peak ENOB achieved at a number of speed grades ranging from 10 kS/s to 1 GS/s, and the peak sampling rate at a number of effective resolution grades ranging from 4 to 14-b. The results are shown in Fig. 4 and Fig. 5. As an example, Fig. 4 shows that, during the first 15 years, the sampling rate of an ADC with at least 4-b ENOB increased by 5 orders of magnitude, while during the last 22 years it has improved by only one order. Similar signs of saturation are visible at all levels of ENOB in Fig. 4. If this trend remains *it can be anticipated that the peak sampling rate at any given resolution will increase by less than 5X until 2020*. Similarly, from Fig. 5 it is seen that ADCs of all speed grades from 100 MS/s and below seem to have saturated at an improvement rate of 0.1 ENOB/year, or less. Of the six curves, the curve for GS/s ADCs is the only one that does not show signs of saturation. These trends were estimated using visual inspection.

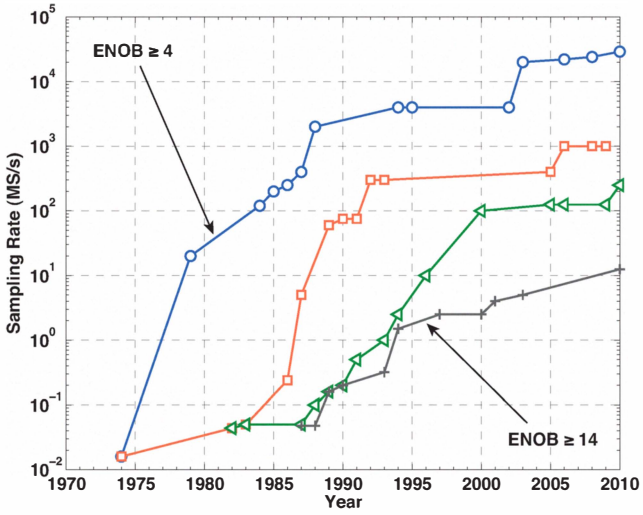

Figure 4. Evolution of peak fs over time for minimum ENOB of 4, 8, 12, and 14 bits respectively.

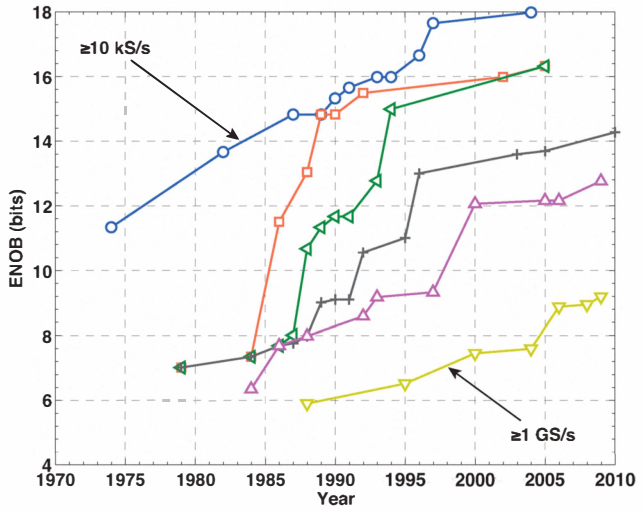

Figure 5. Evolution of peak ENOB over time for minimum sampling rates of 10k, 100k, 1M, 10M, 100M, and 1GS/s respectively.

If they hold, *ADCs below 100 MS/s will not increase their ENOB by much, while GS/s ADCs will go from currently 9-b to around 11-b ENOB by 2020.*

V. Power Efficiency (Figure-of-Merit)

When comparing ADCs with different specifications, two or more parameters can be combined into a single *figure-of-merit* (FOM). One of the most widely used FOM is defined as

$$F = \frac{P}{2^{ENOB} f_s} \qquad (2)$$

and relates the ADC power dissipation to its performance in terms of conversion rate and error *amplitude*. It is based on SNDR rather than SNR, but otherwise similar to the FOM used in [2], and therefore sometimes referred to as the "*Walden-FOM*". Fig. 6 shows the evolution of the Walden-FOM over

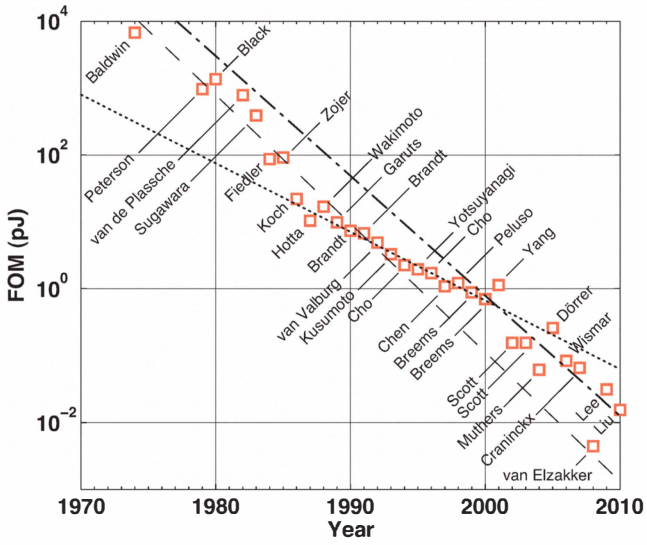

Figure 6. Best reported "Walden-FOM" over time. Log-fit lines indicate the average improvement rate until 1986 (dashed), between 1986-2000 (dotted), and from 2000 to present day (dash-dotted).

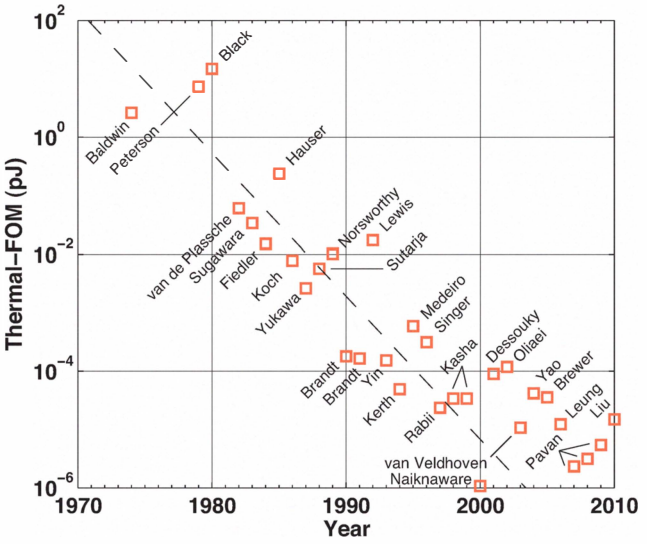

Figure 7. Best reported "Thermal-FOM" over time. The graph shows that this FOM has not improved during the last decade. Trend line (dashed) fitted to data from 1974-2000 shows an average improvement of 2X every 15 months until 2000.

time. The overall rate is ~2X every two years, but there are distinct breakpoints at approximately 1986 and 2000, in between which the evolution showed a significant slowdown to 2X/35months. This can be compared with the nearly identical rates before 1986 (2X/19 months) and after 2000 (2X/20 months). At the current rate of improvement *we could anticipate ADCs with a FOM = 0.2 fJ by 2020.* Current state-of-the-art (4.4 fJ) was reported by van Elzakker, et al. [16]. As pointed out by Bult in [9], there is currently a strong focus on this FOM within the scientific ADC community. The scientific competition has to a large extent been targeting this FOM, and together with a clear trend to leave out certain parts of the total power dissipation [9], that may explain the accelerated rate of

improvement. Another explanation is that this FOM has a preference for low-power designs over high-resolution, and thus potentially benefits more from the scaling of CMOS technology. A closer inspection of the underlying data revealed that, for the best FOM every year, the trajectories for ENOB and f_s are fairly random whereas P follows a distinct path towards consistently lower power. In other words, you achieve better results with this FOM by lowering the power dissipation than by improving resolution. In order to compare high-resolution ADCs limited by thermal noise it has therefore been proposed to use a slightly different FOM – the "*Thermal-FOM*" [17]-[18].

$$F_2 = \frac{P}{2^{2ENOB} f_s} \tag{3}$$

The thermal-FOM considers error *power* rather than amplitude and thus improves by 4X (rather than 2X) for every effective bit of resolution – a fact that is balanced by the corresponding theoretical minimum 4X increase in power if ENOB was limited by *kT*/*C*-noise [4] and the architecture remains otherwise unchanged [9]. As seen in Fig. 7, the thermal-FOM has improved by 2X every 15 months until year 2000, after which it has remained in saturation. This coincides with the breakpoint in Fig. 3 where the noise floor – which approximately defines the denominator in (3) – also goes into saturation. It can further be noticed from Fig. 6 that it coincides with the accelerated evolution of the Walden-FOM as well. The overall picture would therefore suggest that scientific ADC research first focused on SNR/SNDR performance and related design optimization, and since around year 2000 has moved on to focus on power efficiency.

VI. Conclusions

Data from a near-exhaustive survey of reported scientific ADC performance were analyzed, and past and present trends were estimated. Empirically observed trends form an important complement to theoretical performance predictions derived in other works, and can also be used as a reference in order to refine such theory. *If all the trends discussed in this paper would hold for the next decade*, we would have ADCs by 2020 that are implemented in 10–11 nm CMOS, and ADCs that are operating from 40 mV supplies. 1 GS/s ADCs with 11-b ENOB will be reported, but ADCs from 100 MS/s and below will not have much better resolution than today. The relative noise-floor for reported designs will remain at the –162dB/Hz where it is today, or even degrade slightly. The thermal-FOM of 1 aJ reported by Naiknaware and Fiez in 2000 [19] remains the state-of-the-art also in 2020 while the most power-efficient ADCs will have a Walden-FOM of approximately 0.2 fJ.

Acknowledgment

The author thanks Dr. Nick Tan of *AnaLutions, Inc.*, Laguna Niguel, CA, USA for many valuable comments and suggestions.

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