The Race for the Extra Decibel

A Brief Review of Current ADC Performance Trajectories

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IMAGE LICENSED BY GRAPHIC STOCK

At the turn of this century, there was widespread concern that the performance of analog-to-digital converters (ADCs) might have reached a saturation point and would, in fact, deteriorate as we began to scale into deep submicron CMOS technology. The past 15 years of innovation have clearly refuted such fears. Driven by a combination of application pull, architectural modifications, and relentless optimization, we have seen steady improvements in several key performance metrics.

The purpose of this article is to enumerate some of the pertaining progress slopes, explain their possible foundations, and speculate about their remaining lifetime. In this context, it is important to note that this general subject has received a great deal of attention over the years, as evidenced by the large number of ADC surveys and trend papers (see, e.g., [1]–[20]). The advanced reader is referred to these contributions for a deep dive.

Conversion Energy

The first aspect that we will investigate is the persistent trend toward lower conversion energy. To visualize the progress made over the past five years, we consider the scatter plot shown in Figure 1(a).

Digital Object Identifier 10.1109/MSSC.2015.2442393
Date of publication: 15 September 2015

1943-0582/15©2015IEEE

In this chart, the *y*-axis is the conversion energy (power dissipation, *P*, divided by the conversion rate, *fs*) and the *x*-axis is the peak signal-to-noise-and-distortion ratio (SNDR), a metric commonly used to quantify a converter's output signal fidelity. The data points in this chart are taken from [20], which tabulates results reported at the IEEE International Solid-State Circuit Conference and the VLSI Circuits Symposium. The markers with solid fill represent time-interleaved designs.

From the data points added between 2010 and 2015 (drawn in red), one can immediately see that there has been significant progress in lowering the conversion energy within the past five years. For further orientation and interpretation, we include two trend lines representing the commonly used Walden figure of merit (FoM_W) and the SNDR-based Schreier figure of merit (FoM_S). These metrics quantify an ADC's energy efficiency against its SNDR and are discussed further in "ADC Figures of Merit."

We note that as of 2015, there are 15 publications reporting a FOM_W below 10 fJ/conversion-step. In 2010, there was only one such design. Second, while we see improvements across the board, the successive approximation register (SAR) architecture stands out and now clearly dominates the low-energy design space. Third, and most importantly, we observe that the leading-edge designs for an SNDR greater than 50 dB align well with the slope of 4x per 6 dB (1 bit). This trade-off forms the basis for FoM_S and corresponds to circuits that are mainly limited by thermal noise. An important conclusion to draw from this is that we have pushed our designs closer to thermal limits, indicating a higher degree of optimization.

The fact that most leading-edge designs (with SNDR > 50 dB) now align along the thermal slope has led to the widespread adoption of FoM_S for designs with moderate to high resolution. The bold dashed line in Figure 1(a) corresponds to $\text{FOM}_\text{S} = 175\,\text{dB}$, which can be viewed as the state of the art. The Walden FOM assumes a slope of 2x per 6 dB, which remains useful mostly for lower resolution designs.

Conversion Speed

To get a feel for progress in raw speed (regardless of power dissipation), we consider the "aperture" plot shown in Figure 1(b). Here, the *y*-axis is the conversion bandwidth or, more precisely, the upper input frequency (f_in) for which the plotted SNDR was measured. This frequency is typically taken equal to $f_s/2$, and exceptions are noted in [20].

At first glance, we observe that while the improvements in raw speed are significant, they are not as pronounced as those for conversion energy. The reason for this is that the speed–resolution product tends to be limited by our ability to make a low-jitter clock [1], [24]. The data point with the best combination of bandwidth and SNDR is [25], located at an equivalent aperture jitter of $\sigma_\text{j} = 127\ \text{fs}_\text{rms}$. This number is based on the following classical expression [24], modified to estimate the approximate equivalent jitter using the converter's SNDR:

$$\text{SNR}_\text{jitter} = \frac{1}{(2\pi f_\text{in})^2 \cdot \sigma_j^2}$$
$$\Rightarrow \sigma_j^2 \cong \frac{1}{(2\pi f_\text{in})^2 \cdot \text{SNDR}}. \qquad (1)$$

This estimate is clearly pessimistic, since all nonidealities (jitter, thermal noise, quantization noise, distortion, etc.) are counted as jitter. This yields good estimates only when a converter is truly jitter-limited, which can be a reasonable approximation for leading designs. In the analysis of [19], which uses a much larger data set than considered here, it was found that careful de-embedding of

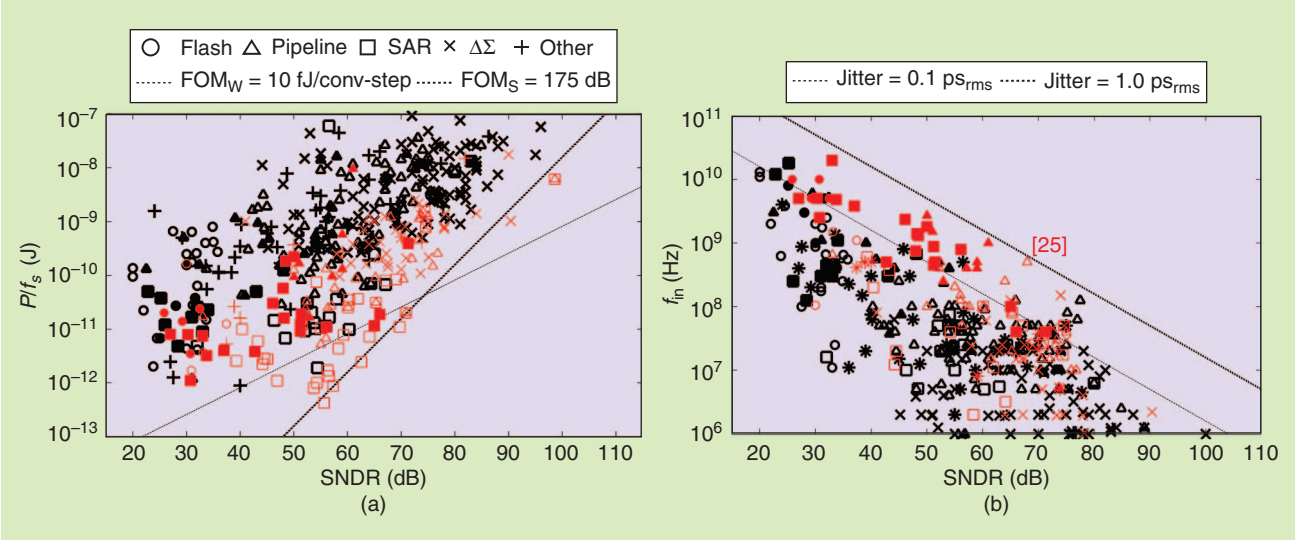

FIGURE 1: ADC performance data (ISSCC 1997–2015 and VLSI Circuits Symposium 1997–2014): (a) conversion energy and (b) conversion bandwidth versus SNDR. The red markers indicate data reported after 2010. Points with solid fill mark time-interleaved designs.

ADC FIGURES OF MERIT

A figure of merit (FoM) lumps several performance metrics into a single number, thereby creating a proxy for the overall efficacy of a circuit or device. For ADCs, the construction of a "fair" FoM is non-trivial, not only because an ADC is a rather complex device with dozens of specifications (see Figure S1),

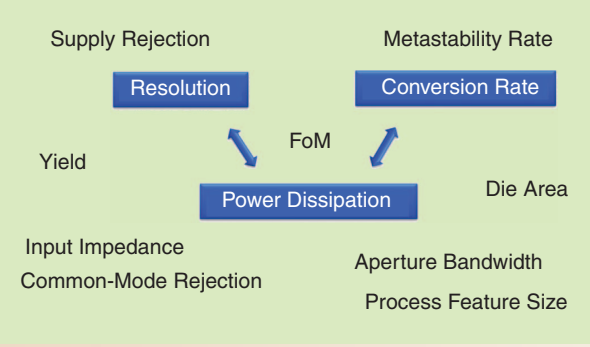

FIGURE S1: ADC specifications.

but also because the exact trade-off between the relevant metrics can be non-obvious. Most of the commonly used FoMs for ADCs share two basic properties: 1) they are purposely kept simple and mainly focus on power dissipation, conversion rate, and resolution (or a related metric); 2) they are constructed using first-order, physically-grounded trade-offs and avoid empirical fitting parameters as much as possible. More complex FoMs (considering area, supply voltage, process technology, etc.) have been proposed in the literature [4], [21], but their empirical and data-driven nature makes them difficult to use. Ultimately, it is important to realize that a FoM does not (and is not meant to) capture all there is to know about a specific converter. A direct comparison between two converters should always be made using a table, where the FoM is just one of several entries. Other usage scenarios include broad-stroke comparisons between different architectures or trend tracking (as this article does).

One of the first widely used FoMs for quantifying the trade-off between ADC speed, resolution, and power dissipation is the so-called Walden FoM (see Table S1). This FoM asserts that power (P) grows linearly with conversion rate (f_s). This is justified from first-order physics (power = energy/time) but tends to fall apart as speed is pushed toward technology limits (see discussion in the body of this article). In terms of resolution, FoM_W assumes that each added "effective" bit (ENOB: effective number bits) doubles the power dissipation. This trade-off was chosen empirically and tended to match experimental outcomes reasonably well for a number of years. Recently, however, we have seen that moderate- to high-resolution converters tend to follow a power quadrupling per effective bit, a trade-off that is consistent with noise-limited analog circuits [9].

To capture the 4x per bit trade-off, one could simply modify the denominator of FoM_W and replace 2^{ENOB} with $2^{2\text{ENOB}}$. However, a different way of formulating the same trade-off in logarithmic units has caught on. The Schreier FoM in its original form takes the dynamic range (DR) of the converter in dB and adds ten times the logarithm of the bandwidth (BW) to power ratio. A 6 dB DR increase is thus assumed to inflict a 4x increase in power at the same efficiency. Also note that the proper unit of this FoM is dB/J, but the unit "Joule" is typically dropped in the literature. What we call FoM_S in this article is a modified version of this logarithmic metric. DR is replaced with SNDR (to capture distortion) and BW is replaced with $f_s/2$. While it is certainly true that the power dissipation of a converter depends on its actual acquisition bandwidth (which may be different from $f_s/2$), it is difficult to argue that there should be a strict proportionality. To overcome this issue, the survey of [20] uses $f_s/2$ as a proxy for BW and takes the SNDR value from measured data at that input frequency (where possible). This creates a level playing field among the different converters and avoids assumptions about the scaling of power with true acquisition bandwidth; the trade-off is instead reflected in the achieved SNDR.

TABLE S1. ADC FIGURES OF MERIT.

WALDEN FoM [1]	SCHREIER FoM (DR) [22]	SCHREIER FoM (SNDR) [23]
$\text{FoM}_W = \frac{P}{f_s \cdot 2^{\text{ENOB}}}$ $\text{ENOB} = \frac{\text{SNDR(dB)} - 1.76}{6.02}$	$\text{FoM}_{S,\text{DR}} = \text{DR(dB)} + 10\log\left(\frac{BW}{P}\right)$	$\text{FoM}_S = \text{SNDR(dB)} + 10\log\left(\frac{f_s/2}{P}\right)$

some of the non-jitter imperfections gives approximately 100 fs_{rms} as the state of the art.

While it is possible to create clocks with lower jitter than stated above, their distribution to the sampling switch is what will often limit us. The design of [26] achieves a total jitter of 70 fs_{rms}, with equal parts contributed by the clock source and the subsequent distribution to the sampling switch. The latter contribution comes from several sources [27]. The first is thermal noise, which can be overcome by investing more power. The second is supply noise and other forms of coupling noise, which are hard to tame, given that most of the popular sampling circuits ultimately require single-ended clocking. To first order, a 1% variation on the supply voltage of an inverter that buffers a single-ended clock causes a 1% change its rise time. Even for advanced technologies with 10 ps rise time, this amounts to a 100 fs change in timing. Improvements on these numbers will be hard to come by, and future progress threatens to be incremental.

To investigate further, we consider Figure 2, which plots the speed–resolution product of the top three designs in each year versus time (1997–2015). A fit to these data reveals that the speed–resolution

performance has so far doubled approximately every four years, which is relatively slow compared to other progress rates that one may extract (as, for instance, ADC energy efficiency; see below). Also note that only two designs reported after 2010 surpass the performance of [28] (which is the peak point for 2010). This may, indeed, be indicative of an imminent speed–resolution performance saturation, which is also the conclusion of [19]. It is interesting to note, however, that such saturation was already seen by Walden in 1999 [1], and we have since moved to much higher levels of performance (thanks to technology scaling). It is likely that the data converter community will eventually find ways to march on for a number of years, especially if there are important applications that demand further progress.

From an application standpoint, it is important to note that the situation may actually not be as bleak as often portrayed. The jitter requirement of an ADC strongly depends on the spectral composition of the ADC input signal or, equivalently, its autocorrelation function [24], [29]. In [30], it was shown that for a typical wideband signal seen in high-speed serial links, the jitter requirement is relaxed by about 12 dB compared to the above formula that assumes a sinusoid at $f_s/2$. The difference is due to the wideband and low-pass nature of the signal. In yet another scenario involving wideband digitization for satellite and cable receivers [31]–[33], it can be argued along similar lines that jitter is less important than other nonidealities due to the subsequent digital channel filtering. The proper benchmarking and FoM comparison for such application-specific ADCs remains an open topic, and metrics involving sinusoidal characterization are often too pessimistic to be useful.

As a final remark, we note that it is unlikely that ADCs will ever be affected or limited by Heisenberg's uncertainty principle. This reference point was created in [1], suggesting

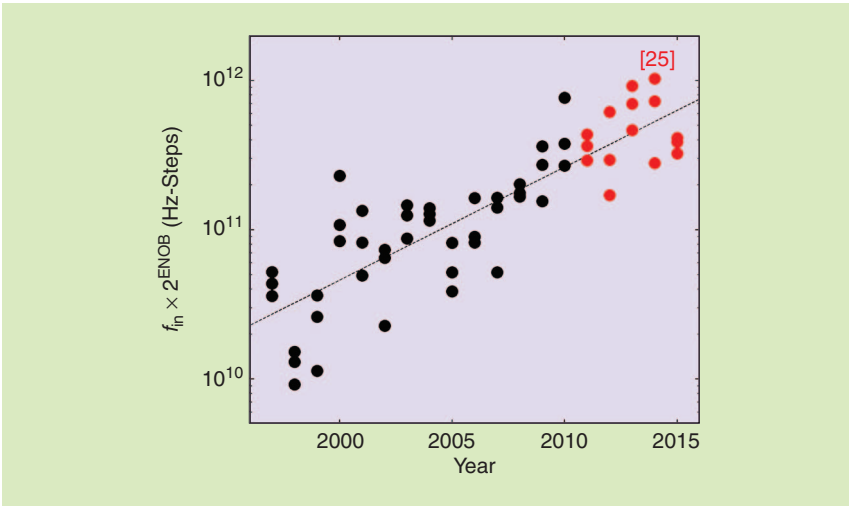

FIGURE 2: Fit to speed–resolution product of the top three designs in each year. The red markers indicate data reported after 2010. The fit line has a slope of 2x/4 years.

an "ultimate" aperture limit of about 0.1 fs_{rms}. The applicability of such a quantum-theoretical limit for ADCs has been questioned in the meantime [34], and there is no evidence that we can produce and distribute clocks with such purity by electrical or optical means at room temperature.

Figure of Merit Trends

Turning our attention back to energy efficiency, we now investigate trends in FoM_S versus conversion rate and also over time. We select FoM_S here because 1) it fits the leading-edge data points in Figure 1(a) remarkably well and 2) it is a metric that is cleanly justified via the fundamental thermal noise trade-off in analog circuits.

Figure 3 plots FoM_S against conversion rate. Similar to Figure 1, we mark the data points from the past five years in red to give a feel for recent advances. First, we note that the achieved FOM_S is highest for low conversion rates. This is expected since it is generally harder to make a fast ADC energy efficient. At frequencies

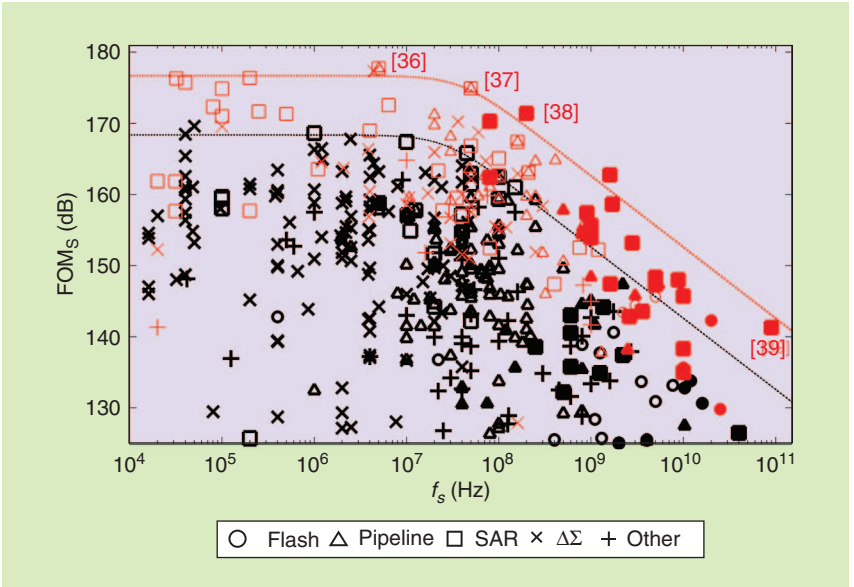

FIGURE 3: FOM_S versus conversion rate (f_s). The red markers indicate data reported after 2010. Points with solid fill mark time-interleaved designs.

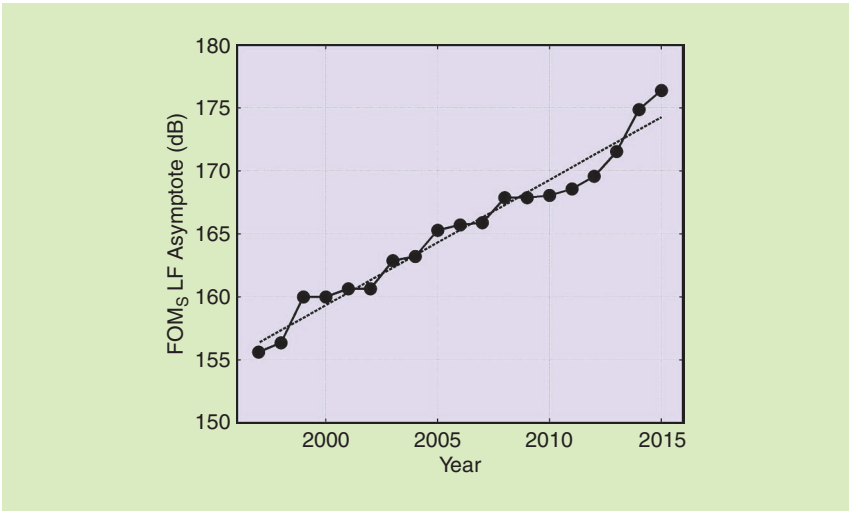

FIGURE 4: FOMS trend over time (low-frequency asymptote). The fit line has a slope of about 1 dB per year.

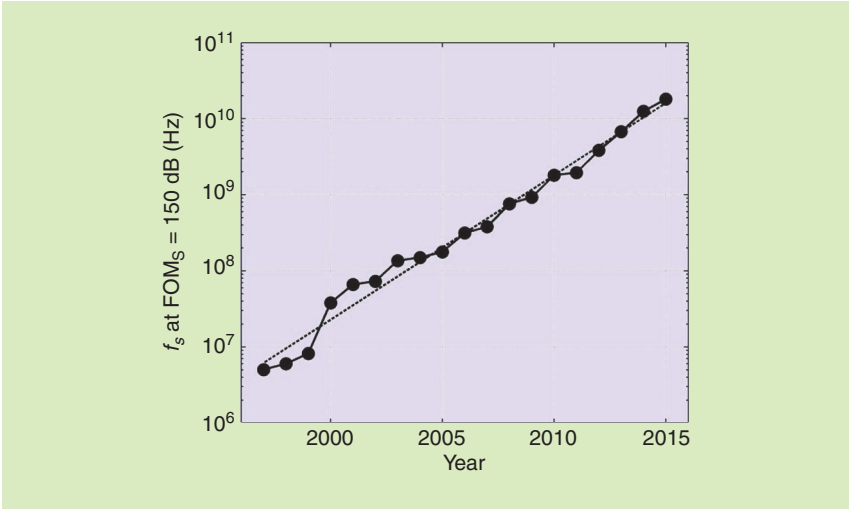

FIGURE 5: FOMS trend (high frequency asymptote). The fit line indicates doubling of the conversion rate (f_s) for every 1.8 years.

between 10 and 100 MHz, the efficiency begins to deteriorate and rolls off with a slope of approximately –10 dB per decade. As discussed in [35], this indicates that the power dissipation scales with the square of the conversion speed in this regime.

Also notice from the plot that recent pipelined SAR designs ([36]–[38]) set the peak performance near the corner. The time-interleaved SAR ADC reported in [39] marks the fastest design and interestingly lies almost exactly on the –10 dB/decade roll-off portion of the envelope. The envelope is positioned by taking the average of the top five data points to define the horizontal asymptote, and the average of the top five designs along a –10 dB slope.

As we can see from Figure 3, the contributions of the past five years have pushed the asymptotes up and to the right. It is interesting to quantify the rate of this movement. This is done for the location of the low-frequency asymptote in Figure 4. We observe that the improvements have followed a steady pace with minor variations (likely due to the finite size of the data set) from year to year. Interestingly, the overall progress rate comes out almost exactly to 1 dB per year (or doubling of energy efficiency every three years). In this context, it is worth noting that $\mathrm{FoM_W}$ tends to improve significantly faster, since it de-emphasizes noise limits and is thus catered toward technology-limited designs that benefit more directly from feature size scaling. The work of [19] extracted a $\mathrm{FoM_W}$ improvement rate of 2x every 2.5 years for delta-sigma converters and only 1.8 years for Nyquist converters. These numbers align well with the 2x energy improvement for every 1.9 years that was observed in [16]. The key take-home here is that the composition of the figure of merit plays an important role in the observed trends.

It is sometimes suggested that part of the above-quantified improvements come from ever more "creative" reporting of results and leaving out significant power contributors (e.g., off-chip calibration units, I/O, etc.) [10]. While this may certainly play a role, it cannot explain the steady improvements observed in Figure 4, which sum to an aggregate progress of over 20 dB in less than two decades.

In the context of ever-improving efficiency, it is useful to revisit the fundamental limit discussion of [9]. There, we noted that a useful bound on conversion energy is given by the minimum energy it takes to drive a sampling capacitor using an ideal (class-B) amplifier [40], [41]:

$$\left(\frac{P}{f_S}\right)_{\min} = 8\,\mathrm{kT} \times \mathrm{SNR}\,. \tag{2}$$

Approximating $\mathrm{SNDR} \cong \mathrm{SNR}$, assuming room temperature, and inserting this expression into the definition of $\mathrm{FoM_S}$ gives:

$$\begin{aligned}\mathrm{FOM_{S,max}} &= \mathrm{SNR(dB)} \\ &\quad + 10\log\left(\frac{1}{16\,\mathrm{kT}\times\mathrm{SNR}}\right) \\ &= -10\log(16\,\mathrm{kT}) = 192\,\mathrm{dB}.\end{aligned} \tag{3}$$

Since this bound considers only the sampling energy, it is clear that we will likely never reach this number. A more practical limit may be around 186 dB, which would be

reached in about 11 years, assuming that we can maintain the progress rate of 1 dB per year.

To extract the rate at which the high-frequency asymptote of Figure 3 moves to the right, we use FOM_S = 150 dB as an arbitrary reference point and measure (for each year) up to which conversion rate this level of efficiency is maintained. This yields the plot of Figure 5, from which we observe doubling every 1.8 years, or 60x every ten years. A good portion of this progress slope can be explained by technology scaling. The transit frequency of CMOS transistors has improved by about a factor of ten over the last decade. This leaves about a factor of six that was likely gained by "clever design."

Note that the above number quantifies the rate of power efficiency improvement for high-speed designs, and it is therefore not surprising that the improvement rate is quite similar to that of FoM_W. Lastly, note that since the low- and high-frequency asymptotes in Figure 3 shift at different rates, the corner shifts to the right over time. While it was located at about 1.4 MHz in 1997, the roll-off now occurs at about 42 MHz.

Architectural Trends

As speculated above, at least part of the progress seen over the years has certainly been due to pure process technology scaling. However, scaling alone would not have been sufficient. As we shall discuss in this section, there were a number of innovations in circuit and architecture design that not only made further scaling possible, but led to new topologies that made better use of scaled transistors. With this relentless and concurrent optimization involving technology, circuits, and architectures, it is not surprising that we have seen increasing competition among previously disjoint ADC options.

While it was relatively straightforward to make architectural decisions in the past, today's ADC designer is confronted with an overlapping design space offering multiple solutions that are difficult to differentiate in their suitability. For example, the design space for pipelined ADCs has been encroached on by time-interleaved SAR converters. Similarly, wideband delta-sigma converters such as [42] now offer bandwidths that were previously only achievable with Nyquist converters.

Figure 6 gives an indication of architectural trends. As is commonly known, the SAR topology continues to be actively researched and conforms to the general trend toward minimalistic, op-amp–less architectures. In order to extract high speed from the SAR topology, time interleaving is typically needed. This explains, in part, an up-tick in the number of reported designs that use time interleaving, illustrated in Figure 7. More generally, this trend is, of course, also supported by the increasing integration density available in silicon, which has also enabled multicore microprocessors.

SAR ADCs

The SAR ADCs discussed in the literature in recent years show great versatility and range from ultralow-power to ultrahigh-speed designs (using time interleaving). To see this, contrast the 10-bit 200 kS/s converter of [43] with the 8-bit 90 GS/s part of [39]; both use very similar circuitry in their converter core. Somewhere in between, we see 10-bit 2.6 GS/s time-interleaved SAR ADCs that can digitize the entire cable TV spectrum [44], as well as highly efficient 100-MS/s, 11-ENOB converters [45] that meet the demands of typical wireless receivers. While much of the progress in SAR converters is enabled by technology scaling, there have been a number of important circuit and architecture innovations as well. These include the combination of SAR conversion with pipelining [46] and the use of dynamic residue amplification in such hybrid topologies [45]. Other recent advancements include the judicious use of redundancy and digital-to-analog converter (DAC) replica timing [47], majority voting for noise reduction [48], and integrated buffering to ease the input drive requirements [49].

Pipelined ADCs

Challenged by the impressive energy efficiency and scaling robustness of SAR converters, the designers of pipelined ADCs have continued their search for op-amp–less residue amplification techniques. We have seen intriguing innovations in fully-dynamic amplification [50], ring-amplifier–based amplification [51], [52], and comparator-based amplification [53], as well as bucket-brigade

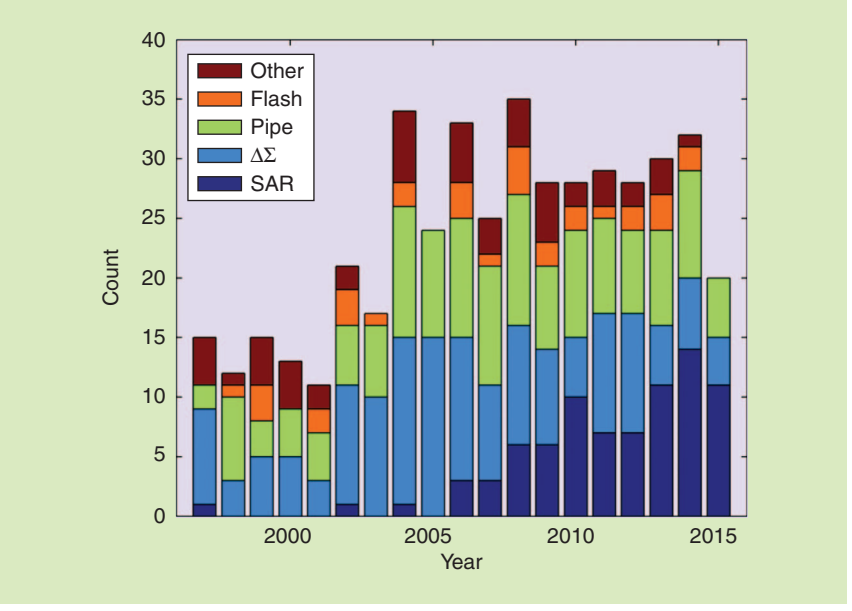

FIGURE 6: Architectures of ADCs described in the literature (ISSCC 1997–2015 and VLSI Circuits Symposium 1997–2014).

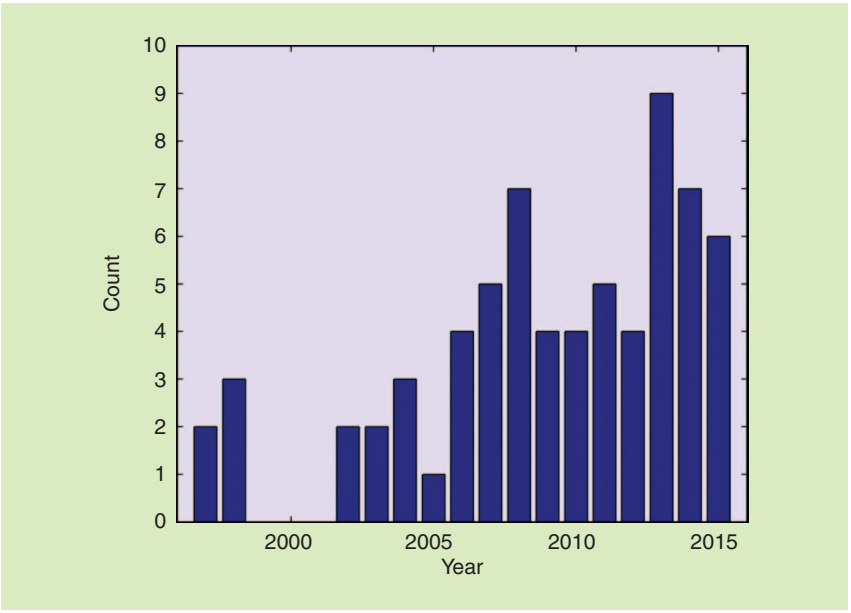

FIGURE 7: The number of time-interleaved ADCs described in the literature (ISSCC 1997–2015 and VLSI Circuits Symposium 1997–2014).

processing [54], [55]. This has been accompanied by a push for low stage count [56], leading to significant reductions in power and complexity.

Architecturally, the work of [57] reported an intriguing modification to the typical pipeline by splitting the amplifier into a coarse and fine path. This change extends the available settling time in each stage and may prove to be a valuable concept going forward.

2-level to 4-level pulse-amplitude modulation signaling in high-speed data links. The time interleaved flash design of [58] operates at 10.3 GS/s and thereby enables a multi-standard transceiver. As shown in the 32-nm SOI design of [59], the speed can even be extended to 20 GS/s while maintaining outstanding power efficiency. Key to maintaining high efficiency in flash ADCs is to identify a proper

A more practical limit may be around 186 dB, which would be reached in about 11 years, assuming that we can maintain the progress rate of 1 dB per year.

In the context of high-speed conversion for wireless infrastructure, pipelined ADCs are still the only topology that can meet the stringent application requirements. With proper calibration, we have seen that the pipelined architecture can be pushed to 1 GS/s at 14 bits [25], a performance level that is hard (if not impossible) to reach with any other topology.

Flash ADCs

Flash ADCs have regained some interest due to the imminent shift from

offset calibration/mitigation scheme and to minimize the circuit complexity as much as possible. In that vein, the design of [60] introduced a technique that generates extra decision levels using dynamic interpolation at the comparators' regenerative nodes. These and other innovations are strongly linked to the unprecedented speed and integration density that is now at the disposal of the designers.

In terms of concept innovation, the approach described in [61] points toward an intriguing new direction. Instead of designing flash ADCs with near perfect thresholds, this work proposes to adaptively control the decision levels to minimize the system's bit error rate, which is the ultimate specification of interest. Broadly speaking, this approach also falls into the category of analog-to-information conversion (see "Where Analog Meets Digital" by Marian Verhelst and Ahmad Bahai in this issue).

Oversampling ADCs

In oversampling delta-sigma ADCs, CMOS feature size scaling has enabled an increase in sampling frequency from several hundreds of MHz up to 6 GHz in recent work [42], [62], [63]. Signal bandwidth has scaled proportionally, now exceeding 100 MHz. In addition to technology scaling, a number of important circuit and architecture innovations have played a critical role in advancing the state of the art. Examples include refinements on continuous-time loop filter design and multi-bit DAC implementation, excess-loop–delay compensation [64], integrator-loss compensation [65], sturdy multi-stage noise shaping [66], [67], and filtering topologies [68], [69].

Digitally Assisted Design

At the forefront of digitally assisted design, we have seen a variety of ideas applied to all of the above architectures. Perhaps the most complex and sophisticated scheme was implemented in the time-interleaved pipeline ADC of [70], which leverages two million logic gates to reach the unprecedented performance level of 14 bits at 2.5 GS/s. The digital logic is used to correct a variety of analog imperfections including dynamic sampling nonlinearity and signal-dependent self-heating. Similarly, digital equalization concepts are used in [32] to alleviate the residue amplifier speed requirements and achieve 5.4 GS/s with only two interleaved slices.

In the context of background calibration for pipelined ADCs, another noteworthy development was the introduction of algorithms with short

convergence times [71]. Another area where digital assist has been pushed to new levels is in the correction of time-interleaving artifacts [72]. The time-interleaved SAR converter of [73] uses fully digital compensation of timing skew, which was previously thought to be prohibitively complex. In flash ADC design, digital assist was shown to be effective in reducing the comparator offset trim range by employing a fault-tolerant encoder [58], leading to significant savings in complexity and power. Another area where digitally assisted techniques have found their use is in emerging topologies, such as voltage-controlled-oscillator–based Nyquist converters [74], [75]. Here, digital calibration is not an add-on, but often required to make these approaches practical. In oversampling ADCs, we have seen advancements on digital calibration for multi-bit feedback DACs [76].

Conclusions

Innovation in ADC design is alive and well. We have seen remarkable improvements in all relevant performance metrics (only a subset of which are discussed here), and architectures continue to morph and refine to address application pull and process technology push. In this race for the extra decibel, we always seem to be at the edge of what is possible, and we are always tempted to conclude that progress will have to stall soon. If the above assertions turn out to be accurate, we would reach the end of ADC energy efficiency improvements in about 11 years (going from $FOM_S = 175$ dB to 186 dB, in steps of 1 dB per year). Progress in the speed–resolution product appears to have already stalled due to jitter limitations, but at the same time it seems that we have not yet exhausted all options for mitigating this issue. Going forward, it is best to err on the optimistic side and assume that the data converter community will deliver the "impossible." Ultimately, this may involve the complete rethinking of the analog–digital interface, as articulated in the article by Verhelst and Bahai elsewhere in this issue.

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