## ADC 架构 VIII: 积分 ADC

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## 简介

在发现基本计数 ADC 架构(参见<u>教程 MT-026</u>)后,通过结合集成和计数技术就能实现更高精度,进而推动了高精度双斜率、三斜率和四斜率 ADC 的开发。随着高分辨率  $\Sigma$ -Δ型 ADC 的迅速普及,集成架构不再像以前那样流行,不过仍用于各种精密应用,例如数字电压表等。

## 多斜率 ADC

1950 年代推出的"双斜率" ADC 架构,对高分辨率应用中的 ADC (例如数字电压表)确实是一大突破(参见参考文献1至4)。简单示意图如图1所示,积分器输出波形如图2所示。

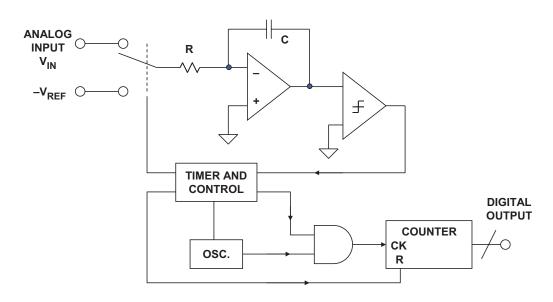
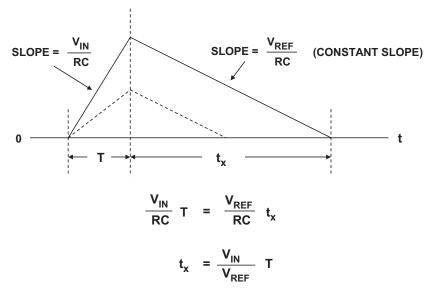


图 1: 双斜率积分 ADC

计数器开始计算时钟脉冲的同时,输入信号施加于积分器。经过预定时间 (T) 后,具有相反极性的基准电压施加于积分器。此时,积分电容上的累积电荷与输入在间隔 T 内的平均值成正比。基准电压积分是反向斜坡,斜率为  $V_{REF}/RC$ 。同时,计数器重新从零计数。当积分器输出到达零,计数停止,模拟电路复位。由于所得电荷与  $V_{IN} \times T$  成正比,且相等数量的丢失电荷与  $V_{REF} \times t_x$  成正比,因此相对于满量程计数的计数次数与  $t_x/T$  或  $V_{IN}/V_{REF}$  成正比。如果计数器输出是二进制数,那么就是代表输入电压的二进制形式。



HIGH NORMAL MODE REJECTION AT MULTIPLES OF  $\frac{1}{T}$ 

图 2: 双斜率 ADC 积分器输出波形

双斜率积分具有许多优点。由于转换精度以相同比率影响上行斜率和下行斜率,所以与电容和时钟频率均无关。

固定输入信号积分周期抑制了模拟输入(其周期等于积分时间 T 或为其约数)上的噪声频率。因此,只要正确选择 T,就能实现对 50 Hz 和 60 Hz 线路纹波的极佳抑制,如图 3 所示。

利用额外充电/放电循环测量"零"和"满量程",并借助测量结果对初始测量值进行数字校正,可以消除由偏置电流、积分放大器的失调电压和比较器造成的误差以及增益误差,如参考文献 5 所述的四斜率架构。

三斜率架构(参见参考文献6至8)保留了双斜率的优点,同时大幅提升了转换速度,但是增加了复杂性。提升转换速度通过在两个不同速率下完成基准电压积分(斜降)来实现,即高速速率和"游标"低速速率。计数器同样分成两部分,一部分用于 MSB,一部分用于 LSB。在正确设计的三斜率转换器中,可以实现速度的大幅提升,同时保留双斜率 ADC 固有的线性度、微分线性和稳定性特性。

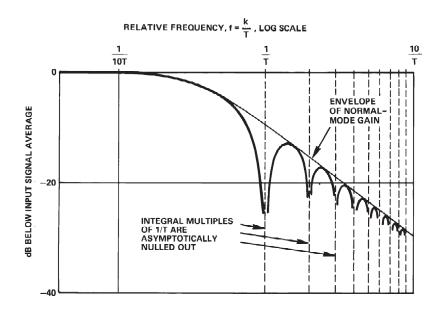


图 3: 积分 ADC 的频率响应

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