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Paper ID [CS205]

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MAy. 08

B.Tech. (Sem. - 3rd)
DIGITAL CIRCUITS & LOGIC DESIGN (CS - 205)

Time : 03 Hours   **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.

2) Attempt any **Four** questions from Section - B.

3) Attempt any **Two** questions from Section - C.

Section - A

Q1) a)   Choose the correct or best alternative in the following: *(6 × 2 = 12)*

   (i)   8 is equal to signed binary number
         (A) 10001000.   (B) 00001000.
         (C) 10000000.   (D) 11000000.

   (ii) De-Morgan's first theorem shows the equivalence of
         (A) OR gate and Exclusive OR gate.
         (B) NOR gate and Bubbled AND gate.
         (C) NOR gate and NAND gate.
         (D) NAND gate and NOT gate.

   (iii) The digital logic family which has the lowest propagation delay time is
         (A) ECL.   (B) TTL.
         (C) CMOS.   (D) PMOS.

   (iv) The device which changes from serial data to parallel data is
         (A) COUNTER.   (B) MULTIPLEXER.
         (C) DEMULTIPLEXER.   (D) FLIP-FLOP.

   (v)   A device which converts BCD to Seven Segment is called
         (A) Encoder.   (B) Decoder.
         (C) Multiplexer.   (D) Demultiplexer.

     (vi) In successive-approximation A/D converter, offset voltage equal to $\frac{1}{2}$ LSB is added to the D/A converter's output. This is done to

        (A) Improve the speed of operation.
        (B) Reduce the maximum quantization error.
        (C) Increase the number of bits at the output.
        (D) Increase the range of input voltage that can be converted.

b)   (i)   Convert 2222 in Hexadecimal number.   **[2]**

     (ii)   Subtract -27 from 68 using 2's complements.   **[3]**

    (iii) Divide $(101110)_2$ by $(101)_2$.   **[3]**

Section - B

(4 × 5 = 20)

Q2) State and prove De-Morgan's theorems.

Q3) Prove the following identities using Boolean algebra:

   (a) $(A + B)(A + \overline{AB})C + \overline{A}(B + \overline{C}) + \overline{A}B + ABC = C(A + B) + \overline{A}(B + \overline{C})$.

   (b) $\overline{A(\overline{\overline{A \cdot B}})} \cdot \overline{B(\overline{A \cdot B})} = A \oplus B$.

   (c) $\overline{\overline{AB} + \overline{A}} + AB = 0$.

Q4) A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations
A is False, B is True
A is False, C is True
A, B, C are False
A, B, C are True
   (a)   Write the Truth table for F. Use the convention True = 1 and False = 0.
   (b)   Write the simplified expression for F in SOP form.
   (c)   Write the simplified expression for F in POS form.
   (d)   Draw logic circuit using minimum number of 2 - input NAND gates.

Q5) Minimise the logic function
F (A,B,C,D) = Π M (1,2,3,8,9,10, 11,14)· d (7,15)
Use Karnaugh map. Draw the logic circuit for the simplified function using NOR gates only.

Q6) What is the necessity of Interfacing in digital ICs and what are the points to be kept in view, while interfacing between TTL gate and CMOS gate?

Section - C

Q7) a) What is a Multiplexer Tree? Why is it needed? Draw the block diagram of a 32:1 Multiplexer Tree and explain, how is input directed to the output in this system.

b) What is a Decoder? Compare a decoder and a demultiplexer with suitable block diagrams.

Q8) a) Draw the logic diagram of 4 - bit Twisted Ring counter and explain its operation with the help of timing diagram.

b) Design a MOD - 3 synchronous counter using J-K Flip-Flops.

Q9) a) Differentiate between static MOS and Dynamic MOS RAM. Draw the circuit of a static MOS RAM cell and explain its working.

b) The capacity of 2K x 16 PROM is to be expanded to 16 K x 16. Find the number of PROM chips required and the number of address lines in the expanded memory.

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