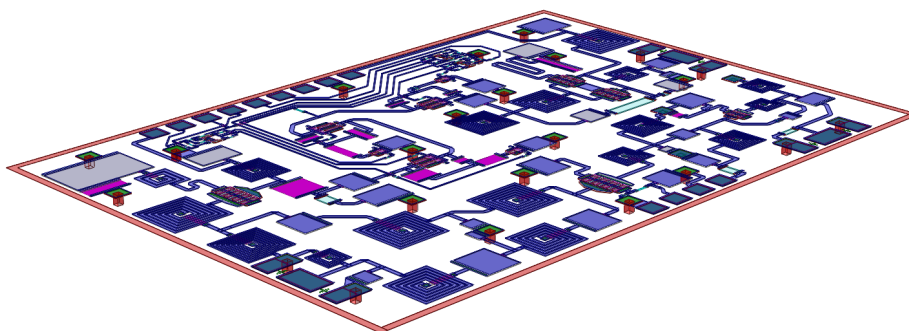


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S Band Multi-function Down-converter GaAs MMIC

Master's Thesis
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Abstract

An S band, high-linearity down-converter is implemented using a 0.25 μm GaAs MMIC pHEMT-process. Using UMS' PPH25 process, an unbalanced FET resistive mixer with a lumped diplexer and an integrated square-wave LO-drive performs the down-converting. The produced single-frequency IF-signal is then amplified twice, first in an LNA and then in a highly linear amplifier. The chip has a dynamic attenuation range of 10.5 dB and offers a maximum gain of 15 dB. The input 1 dB-compression point at nominal gain is 10 dBm which estimates input IP_3 to 20 dBm. The noise figure at nominal gain is 11 dB.

The chip offers down-converting of RF-frequencies between 2.9 and 3.4 GHz for input LO-signals of -4-0 dBm and an image rejection of 40 dBc. The chip size is 2.9x3.4 mm, is designed to fit in a 4x5 mm QFN-capsule and consumes 1.0 W of DC power. Three control signals govern the dynamic attenuation with an LSB of 1.6 dB.

Comparative studies regarding mixer topologies and process technologies are performed. The choice of a single cold FET resistive mixer type is motivated by its linearity, small size and simplicity. A medium-power pHEMT process is chosen, as this provides improved linearity of the amplifiers as well as acceptable noise features given the requirements.

Sammanfattning

En linjär blandare för S-bandet har implementerats med en 0.25 μm GaAs MMIC pHEMT-process. För nedkonvertering används en obalanserad resistiv FET-mixer, som bygger på en diplexer och en integrerad fyrkantig LO-signal. Den nedblandade IF-signalen förstärks två gånger, först i en lågbrusförstärkare och sedan i en effektförstärkare. Chippet har en dynamisk dämpning på 10.5 dB och ger 15 dB maximal förstärkning. Ingångs- P_{1dB} är 10 dBm, vilket ger ett uppskattat ingångs- IP_3 på 20 dBm. Vid nominell förstärkning är brusfaktorn 11 dB.

Chippet klarar nedblandning av RF-frekvenser mellan 2.9 och 3.4 GHz för LO-effekter -4-0 dBm och dämpning av spegelfrekvenserna med minst 40 dBc. Chippet är designat för montering i en 4x5 mm QFN-kapsel och förbrukar 1.0 W. Tre kontrollsignaler styr den dynamiska dämpningen med 1.6 dB LSB.

Jämförelsestudier av blandartopologier och processval har genomförts. Blandaren är vald på grund av dess linjäritet, lilla storlek och enkelhet. UMS PPH25 process har valts då den erbjuder hög effekt och därmed mer linjära förstärkare såväl som acceptabla brusförhållanden givet designspecifikationen.

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Preface

This report concludes our master's thesis work on monolithic microwave integrated circuit down-converter design. It is the degree project for our Master of Science in Engineering Physics at Chalmers University of Technology. The work has been carried out at Saab Electronic Defence Systems (former Saab Microwave) in Mölndal, Sweden, in the fall of 2010.

First and foremost we would like to thank our supervisor at Saab, Niklas Billström, for his guidance during our project and for an unceasing patience. We thank our boss, Karin Adebahr, for her early faith in our abilities. We would also like to thank Simon Kristiansson, Joakim Nilsson, Peter Karlsson and the rest of the IC-design department at Saab for input during our work.

Moreover, we would like to thank our supervisor and examiner at Chalmers Microwave Electronics Laboratory, Christian Fager, for his support during the project.

Richard Abrahamsson
Anders Bennehag
Göteborg January 22, 2011



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Chapter 1

Introduction

1.1 Active electronically scanned array

Radars of today often utilize a phased array function which permits steering of the antenna lobe by use of constructive and destructive interference. This removes the need for mechanical constructions that rotates the radar. By not having any movable parts, the reliability and performance vastly outperforms the properties of rotating radars. For example, because the angular speed of the electronically steered antenna array, the antenna lobe can simultaneously keep track of several targets while also scanning the skies for new ones. This type of radar is an electronically steered antenna, or ESA.[1]

An ESA-antenna consists of many small antenna elements, or transmit/receive-modules. The signal's phase and amplitude are controlled individually for each TRM while other signal processing is common for groups of modules. It is therefore to one's advantage to create small antenna elements as well as small circuits controlling them. This can be done with monolithic microwave integrated circuits (or MMICs). MMICs are small, efficient and reliable, making them well-suited for radar applications.[2]

Older ESA's were usually passive (PESA); all TRMs operating at the same frequency and powered by a common source. If small groups of antenna elements are powered individually the array is active, an AESA. This gives the flexibility of being able to transmit over different frequencies at the same time and thus, amongst other things, decrease the likelihood of discovery.[3]

Common modern radars transmit at frequencies from 1 GHz up to tens of GHz. Early digital sampling of the analogue signal enables more processing to be done in software, extending the radar's applications and utility. To perform analogue-to-digital conversion with today's technology, the frequency must be in the order of 100 MHz. This is at least one order of magnitude less than the transmit frequencies.

Figure 1.1 presents a usual setup of an AESA-system. The signal is received in a large number of TRM-modules where amplification and phase steering

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are performed. In the next step, the signal is prepared for AD-conversion by down-converting the frequency. In the third step, the signal is digitized and processed in software.

In this thesis work, the first in a chain of necessary down-converters is designed on a GaAs MMIC. The chip is called multi-functional because it contains additional components such as amplifiers and variable attenuators. Due to the tailored performance with strict specifications and the inclusion of many components, the chip cannot be bought of the shelf. The main reason for implementing on an MMIC is the need for miniaturisation to be able to fit an as big part of the receiver as possible close to the antenna.

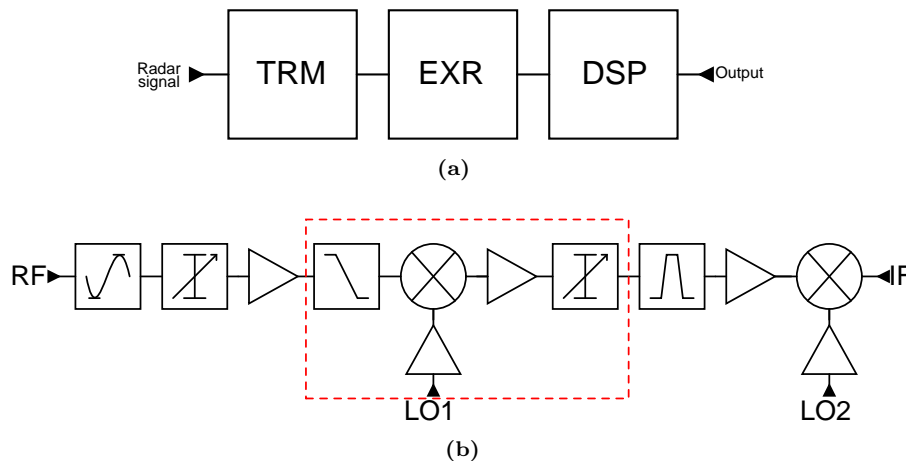


Figure 1.1: Schematic view of the AESA receiver system. (a) The signal is picked up by the antenna in the transmitter receiver module (TRM), processed in the exciter receiver subsystem (EXR) and finally converted to a digital signal in the DSP-unit, where digital beam forming is performed. (b) A detailed view of the EXR-unit. It contains a series of down-converters and filters. The down-converters are necessary to provide the analogue-to-digital converter with the correct frequency. This master's thesis covers the implementation of the first down-converter and a dynamic gain on an MMIC (components enclosed by a red dashed line). The chip is designed for the S band and contains image reject features. RF, LO and IF are explained in Mixer principles 1.5.

1.2 Design specifics

As just mentioned there is a need for a custom, very small, mixing circuit. Implementation as an integrated circuit is clearly beneficial because of the small size. In Appendix B the full specification of the MMIC is listed. Most important are the demands on linearity, noise and gain. The gain is set to $\sim 4\text{--}14\text{ dBm}$. This means that the gain is variable and that the chip needs amplifiers and some means to control the gain. The linearity, measured using the input third-order



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intercept point, should be at least 15 dBm at nominal gain. The noise figure should for nominal gain be less than 15 dB. These quantities are explained later on in this chapter.

1.3 GaAs monolithic microwave integrated circuit

1.3.1 Properties

MMICs offers miniaturization of electric circuits and can be constructed with different materials having different properties. Gallium arsenide (GaAs) has been used as a semiconductor material since the 70's. When it was introduced it was a minor revolution; the high electron mobility permitted frequencies in excess of 200 GHz and greater breakdown voltages increased the power levels. GaAs circuits are less sensitive to heat compared to ordinary silicon semiconductor materials and offers good noise-performance.[4]

1.3.2 HEMT-technology

The active components of MMICs are usually FETs and different processes offer different kinds of FETs. The High Electron Mobility Transistor-, or HEMT-technology uses the quantum well created in the conduction band in the interaction between two semiconductors. The electrons in the well form a two-dimensional electron gas that can be used to form the channel region of the FET.[5] The two semiconductor-materials usually must have the same lattice constants.

Pseudomorphic HEMTs, or pHEMTs, have a very thin second layer which allows that layer to "stretch" over the first layer. This avoids the requirement of having the same lattice constant allowing greater band gap differences, giving greater power handling capabilities.

1.3.3 Foundry process

Foundry processes differ, both in the size of components and in the performance features, such as power capability, noise, etc. The size of a process usually refers to the gate length in its active device.

The two processes considered for this chip are PH25 and PPH25 from UMS. United Monolithic Semiconductors (UMS) is an MMIC fabrication plant in France. Both processes utilize pHEMT-technology and have a 0.25 μm gate length. The difference is that PPH25 (power pHEMT) allows higher power density while PH25 has better noise performance. Another thing to consider is that UMS holds test runs for PH25 (not for PPH25) which is a cheap way of verifying a design prior to large volume orders.



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An evaluation is conducted to compare the MMIC performance for the two UMS processes. The results are found in Appendix C and they are based on the designs detailed in the report. From this comparison PPH25 is chosen.

1.4 Circuit simulations

This project governs the design of the MMIC and does not include measurements made on an actual chip. All results documented are thus simulated results. The simulations are initially based on mathematical models of UMS' components. However, as the design matures the accuracy of these models becomes insufficient. Full electromagnetic (EM) simulations are therefore performed on all passive structures on the chip. The results in the report are all calculated using EM-simulations. More information on specifics regarding EM-simulations are found in Appendix E.

1.5 Mixer principles

1.5.1 Mixing

The mixer supplies the fundamental function of down- or up-converting a signal's frequency and is principally a simple component; it receives a radio signal and together with a local oscillator an intermediate frequency is created, as seen in Figure 1.2. The mixer utilizes the fact that multiplication of two signals creates a signal with new frequencies

$$\omega_{IF} = |\omega_{RF} \pm \omega_{LO}| \quad (1.1)$$

This is used for converting signals between different frequencies. The new signal is called the intermediate frequency and it contains the two frequencies resulting from Equation 1.1. The components are called the upper and the lower sideband. There is usually a filter after the multiplication as only one of the frequency components is desired. An example is shown in Figure 1.3. More details are presented in chapter 3.

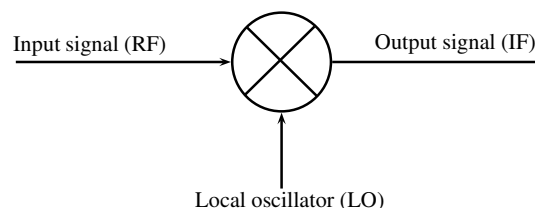


Figure 1.2: Schematic component of a mixer.

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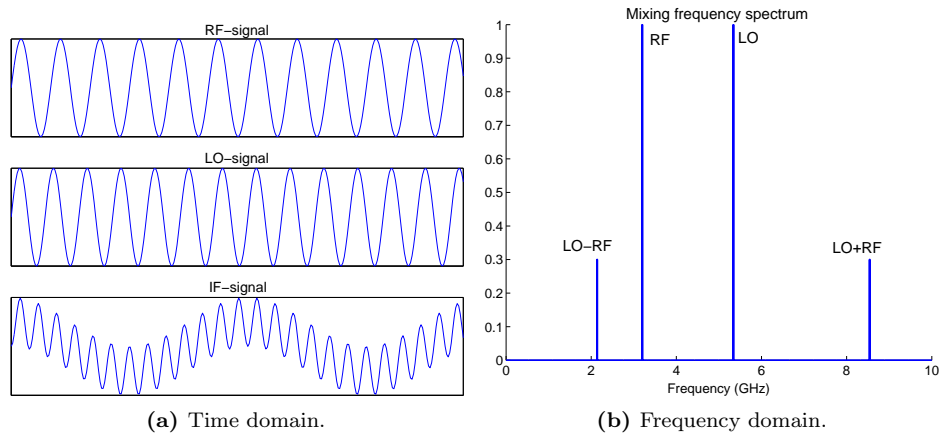


Figure 1.3: The resulting signals from multiplication of RF- and LO-signals. The IF-signal contains both the upper and the lower sidebands.

1.5.2 Image rejection

An incoming signal in the frequency band that converts to the same IF-frequency as the desired signal is called an image. Once this signal has been down-converted it becomes indistinguishable from the desired signal. To avoid this the mixer has an image reject specification of 30 dBc. This means that the conversion gain of the image should be at least 30 dB lower than that of the desired band.

1.6 Intermodulation products

1.6.1 Linearity and intermodulation

The operation of a mixer, or downconverter, should be as linear as possible. Linearity in the mixer ensures that as few unwanted signals as possible arise from the mixing procedure. The frequencies of these spurious signals are calculated in the same manner as the downconverted intermediate frequency:[6]

$$f_{mix} = |k_1 f_1 \pm k_2 f_2 \pm \dots \pm k_n f_n| \quad (1.2)$$

The order of the intermodulation products are $O = \sum_{m=1}^n |k_m|$ and the amplitude of a signal rapidly decreases as the order gets higher. The intermodulation products that are most harmful are thus low-order signals at frequencies close to the IF. The signal of interest, the IF-signal, will in a non-linear mixer become mixed up with many of these spurious signals. The source of spurious signals are not only different orders of RF and LO signal mixes but also mixes of multiple input RF signals along with the LO. Even though this creates infinite combinations of mixing frequencies, there are a few of special interest. See Kundert for a thorough theoretical treatment[7].



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Table 1.1: Spurious signal frequencies, within 1.5 GHz of the IF, originating from single-tone excitation. The frequencies are mixed according to $f_{mix} = mf_{RF} + nf_{LO}$ and the orders are $O = |m|$. $f_{RF} = 3.2$ GHz and $f_{LO} = 5.34$ GHz.

m	n	Frequency (GHz)	Order
2	-1	1.06	2
-3	2	1.08	3
4	-2	2.12	4
-1	1	2.14	1
-6	4	2.16	6
-6	-3	3.18	6
1	0	3.2	1
-4	3	3.22	4

In order to find out which spurious frequencies are present, all low-order mixing products for the system have been calculated, using frequencies valid for the project (Table 1.1). The order of intermodulation by convention only counts the sum of the coefficients of the RF-signals.

A similar calculation of mixing products using two-tone excitation results in more spurious frequencies. The frequencies are mixed according to $f_{mix} = mf_{RF1} + nf_{RF2} + pf_{LO}$, where f_{RF1} and f_{RF2} are placed some tenth of MHz apart. Of special interest are the of m and n low odd-order signals with a low-order LO ($p = 1$), and in particular the third-order intermodulation product.

1.6.2 Intercept point

Usually the third-order intermodulation products from multiple input signals cause most distortion. The third-order intercept point is an observable used to quantify the linearity in a component. Although it measures the third-order product in particular, it represents the overall linearity of a system.

The general n^{th} -order intercept point, or IP_n , is calculated by exciting the system with two tones, as described above. The intercept point is the theoretical intercept point between the fundamental frequency and the n^{th} -order intermodulation product, had the gain (or loss) in the system been linear.[6, 8] That is, for small input (system in linear region) the output of the fundamental signal increases 1 dB/dB, and n dB/dB for the n^{th} -order IM product. The intercept point value is referenced either to the input power (IIP_n) or to the output power (OIP_n). The two values are determined as illustrated in Figure 1.4.

1.6.3 1 dB compression point

The 1 dB compression point (P_{1dB}) is another measure of linearity. It is the point at which the output power is compressed 1 dB compared to the linear case (Figure 1.4). This measure is also referenced to either the input or the output power.

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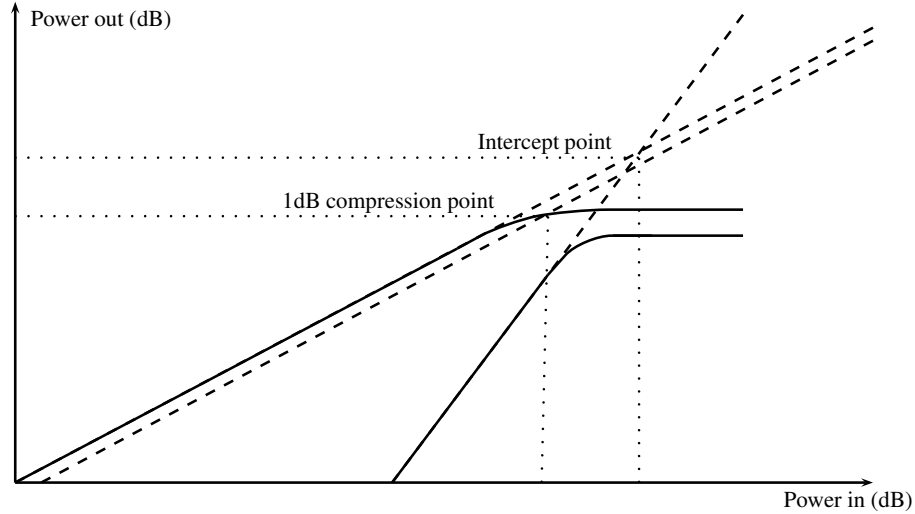


Figure 1.4: The theoretical intercept point between the fundamental frequency component and an intermodulation product. The 1 dB compression point (P_{1dB}) is marked as well.

P_{1dB} is shown to be approximately 10 dB lower than IIP_3 . [7] It can therefore be used as a second parameter to estimate and verify the linearity of a component in the design phase.

1.6.4 Cascaded components

As circuits usually contain multiple components, such as amplifiers, mixers, filters etc, it is preferable to treat the linearity of each component individually in the design process. The total IIP_3 for two components is then given by [8]

$$I_T = \left(\frac{1}{G_2 I_1} + \frac{1}{I_2} \right)^{-1} \quad (1.3)$$

I_1 , I_2 and I_T are the IIP_3 for the first component, second component and the two together, respectively. G_2 is the gain of the second device in the cascade. It's here evident that the order of the components are important for the total linearity.

1.6.5 Linearity simulations

In order to simulate a mixer's IIP_3 a three-tone setup is required (LO and two input RF tones). Necessary simulation accuracy for all three tones and their mixing products is very high, too high for the simulation software Microwave Office to handle. In contrast to the simpler two-tone setup required for calculating IIP_3 in an amplifier, the result becomes unreliable.



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The theory that results in the rule of thumb $IIP_3 = P_{1dB} + 10 \text{ dBm}$ is based on a power series expansion of the transfer characteristics. A simplification to the calculations is made to only consider the the first three terms. This approximation is empirically shown to work well with amplifiers. In mixers are however much more harmonics present and they cannot be as easily discarded. A quick look at different papers and commercial mixers show that IIP_3 can be anything from 6 dBm to 14 dBm higher than P_{1dB} .

This means that neither an estimate of IIP_3 from P_{1dB} nor a simulation of IIP_3 directly are reliable methods for the mixer. The two combined gives the best hint available to a correct IIP_3 value.

1.7 Noise

1.7.1 Noise sources

Thermal noise arise due to collisions between electrons. As temperature increases, the particles will move faster and collide more often, thus increasing the thermal noise. The mean-square thermal noise voltage generated in a resistance R over a bandwidth Δf is[6]

$$\langle v_{\text{thermal}}^2 \rangle = 4k_B T R \Delta f \quad (1.4)$$

This type of noise is introduced in passive, resistive components such as resistors and inductors.

A second type of noise present in active structures such as the FETs is shot noise. Shot noise occurs when there are not enough electrons to successfully approximate the current as continuous. The statistical variations in the electron's speed result in the sum of all electrons having variations as well. The mean-square shot noise voltage for a current i which flows through resistance R is given by

$$\langle v_{\text{shot}}^2 \rangle = 2q_e i R^2 \Delta f \quad (1.5)$$

1.7.2 Noise in a system

When designing electrical circuits in general and receivers in particular, the noise must be considered at every step. Without proper design, it will be problematic to differentiate signals from the background noise. Noise has all kinds of origins; it is part of the original transmission and it is introduced while processing the signal.

An important measure when dealing with noise is the signal to noise ratio, or SNR, which is the ratio between the useful signal and the underlying noise. It is defined as

$$\text{SNR} = 20 \log \left(\frac{A_{\text{signal}}}{A_{\text{noise}}} \right) \quad (1.6)$$

where A is the amplitude of the signal. In Figure 1.5, examples with different SNR are shown.

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1.7.3 Noise figure

The noise figure, or NF , measures how much noise a subcircuit introduces. Introducing noise is inevitable and in order to minimize the noise it is important to amplify the signal as early as possible and thereby raising the signal higher above the background noise. Otherwise, every subsequent attenuation of the signal will raise the noise figure just as much. NF is defined as

$$NF = 10 \log \left(\frac{SNR_{in}}{SNR_{out}} \right) = SNR_{in,dB} - SNR_{out,dB} \quad (1.7)$$

For example, in Figure 1.5a, the SNR is 67 dB. If the same ratio were to be 47 dB after some passing through some component as in Figure 1.5b, the noise figure for this component would be 20 dB.

1.7.4 Cascaded components

The total noise figure (NF) for a system with two components is given by [8]

$$NF_T = NF_1 + \frac{1}{G_1} (NF_2 - 1) \quad (1.8)$$

where NF_1 , NF_2 and NF_T are the noise figures of the first component, the second component and the total system respectively. G_1 is the gain of the first component. Just as for IIP_3 the order of the components plays a big part of the final noise figure. In the next chapter different permutations of components are analysed for the purpose of finding which components and what order give the best trade-off between noise and linearity.

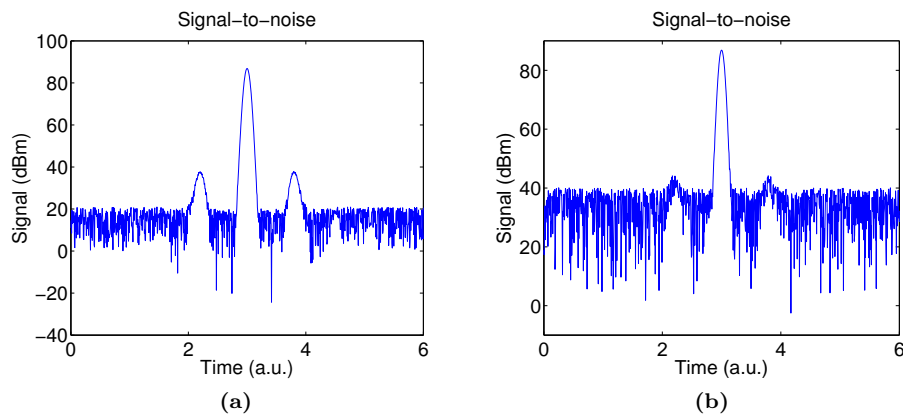


Figure 1.5: (a) An example of how noise makes it difficult to measure anything but the very strong signals. The noise level and the strongest signal are found at 20 dBm and 87 dBm, respectively. This results in a SNR of 67 dBm. In (b) the environment is noisier. The side lobes are barely visible.

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Chapter 2

Chip Design

The required functionality of the chip can be realized in many ways. This chapter aims at explaining and choosing an appropriate setup of sub-circuits given the requirements from SAAB.

2.1 Overall performance

The required performance of the down-converter is listed in Appendix B. These specifications list requirements that the chip is expected to achieve. Besides these there is a list for targeted performance. That is, a list of important parameters of the chip that should be improved upon given the possibility. These are the bandwidth, the noise, the linearity and the power efficiency. The chip design takes all these parameters into account.

A system's noise and linearity are counterparts. To see this dualism a two-component system composed of a component with low attenuation and an amplifying component is considered. If the amplifier is placed before the attenuator the system's overall noise figure (NF) will be only the few decibels of noise present in the amplifier. The IIP_3 will on the other hand be limited by the amplifier's output power. In a reversed system, with the attenuator first, the NF will become the loss in the attenuator plus the noise in the amplifier. The IIP_3 however, will be higher, benefiting from the initial loss according to Equation 1.3.

Naturally there is a minimum of components necessary to achieve the specified performance. The mixing circuit needs a dedicated amplifier to amplify the LO-signal to an appropriate power level. Unless an image reject mixer is used there is a need for a filter to remove the image frequencies which an opponent could use for jamming the system. The RF-to-IF chain needs amplifiers and a variable attenuator block. The nominal chip gain is set to be 8–10 dB with a ± 5 dB gain control. This means that the signal must be amplified at least 13 dB plus losses in the entire circuit. If the losses in the mixer and the attenuator block are 10 dB then the gain of the amplifiers must be at least 23 dB.

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2.2 Component performance

To estimate the performance of different layouts, typical performance of the individual components are needed. However, as this is an analysis made prior to the design, the performance is only estimated. In Table 2.1 the estimates are presented.

Table 2.1: Estimated performance of the chip's components.

	Mixer	Amplifier	Attenuators
Gain	-8 dB	< 13 dB	-2-12 dB
NF	8 dB	1-2 dB	2-12 dB
IIP_3	20-27 dBm	14-22 dBm	30 dBm

The mixer losses are due to the two sidebands and to the reactive circuits. The inherent splitting of the signal into two sidebands effectively reduces the gain with 3 dB (subsection 3.1.1). Depending on the type of mixer the losses in the filters and/or baluns usually amounts to about 3-7 dB, depending on complexity. The estimates are based on the properties of resistive mixers. As explained in subsection 3.2.5, a resistive mixer is chosen since they are very linear. The IIP_3 of a mixer is the most difficult property to estimate. One of the main topics of the thesis is to evaluate the linearity of different mixer topologies. The estimate used here for mixer IIP_3 (25 dBm) as well as for losses in diplexer and mixer (8 dB) are therefore made in the initial mixer study reported in chapter 3.

UMS, the foundry producing the MMIC chips, have amplifiers in PPH25 with an unconditionally stable gain up to about 13 dB, depending on the other characteristics.[9]

Attenuator blocks from previous works have been studied and even though there are different ways to realize them, the performances are more or less the same.[10]

2.3 Budget analysis

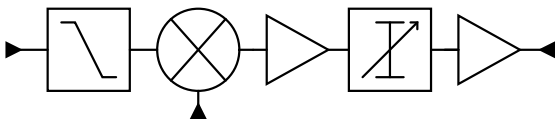
The purpose of the budget analysis is to estimate the performance of the MMIC based on the estimates made of each individual component. With the noise target $NF < 12$ dB and linearity target $IIP_3 > 17$ dBm it is evident that the priority is high linearity and that the signal chain thus needs to start out with an attenuating device. All components placed before the mixer in the signal path need to have a 0.5 GHz bandwidth, while components placed after only need performance for a 20 MHz narrow band. Estimates of full chip performance are made for some different component permutations at different gain states. This way, the effect on the performance due to different gain settings is taken into account.

The performance of a chip layout starting out with the gain block (Table 2.3) has two inherent problems. The first is that all components prior to the mixer



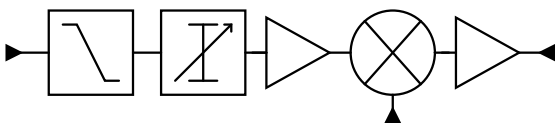
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Table 2.2: Estimated performance of chip setup 1. The order of the components is: Filter, mixer, amplifier, attenuators and amplifier.



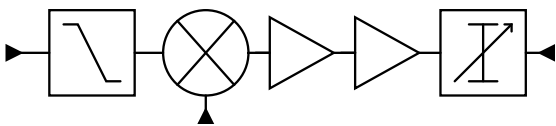
	Nominal gain	Gain: +5 dB	Gain: -5 dB
Gain	9 dB	14 dB	4 dB
NF	10.7 dB	10.0 dB	12.4 dB
IIP_3	18.5 dBm	16.4 dBm	19.4 dBm

Table 2.3: Estimated performance of chip setup 2. The order of the components is: Filter, attenuators, amplifier, mixer and amplifier.



	Nominal gain	Gain: +5 dB	Gain: -5 dB
Gain	9 dB	14 dB	4 dB
NF	12.0 dB	7.0 dB	17.0 dB
IIP_3	18.4 dBm	13.6 dBm	22.8 dBm

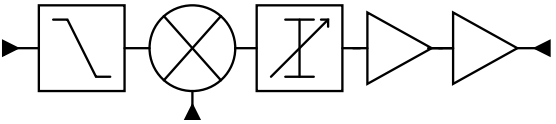
Table 2.4: Estimated performance of chip setup 3. The order of the components is: Filter, mixer, amplifier, amplifier and attenuators.



	Nominal gain	Gain: +5 dB	Gain: -5 dB
Gain	9 dB	14 dB	4 dB
NF	9.9 dB	9.9 dB	10.1 dB
IIP_3	10.5 dBm	10.5 dBm	10.5 dBm

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Table 2.5: Estimated performance of chip setup 4. The order of the components is: Filter, mixer, attenuators, amplifier and amplifier.



	Nominal gain	Gain: +5 dB	Gain: -5 dB
Gain	9 dB	14 dB	4 dB
NF	16.9 dB	11.9 dB	21.9 dB
IIP_3	21.4 dBm	18.0 dBm	23.4 dBm

must be wideband and the second is that the entire chip becomes very sensitive to the gain setting (compare with Table 2.2). Due to these, only chip layouts starting out with the mixer are considered feasible. Also, if the mixer is placed first there are possibilities to integrate the filter with the input networks existing in most mixer designs.

Considering the three setups starting with a mixer, the layout in Table 2.4 gives a good noise figure but too low IIP_3 and the layout in Table 2.5 gives high IIP_3 but too much noise. The layout in Table 2.2, starting out with a mixer and then alternating amplifier and attenuator, gives the best trade-off in performance and low sensitivity to different gain states. With this design it should be possible to reach the required performance as stated in the specifications. Also the targeted performance will be met at most gain states.

2.4 Realization

The components are designed individually based on the above plan. Specific performance demands on individual components are discussed in depth in each section. The report is segmented to separate different classes of components such as amplifiers and mixers into different chapters.

The mixer circuit and the image reject low-pass filter are detailed in chapter 3. It starts out with a theoretical treatment of the mixing process and the importance of the LO drive. Decisions regarding topology and other design aspects follow. The design of a FET-mixer is then reported along with simulated results.

Three different types of amplifiers are designed and reported in chapter 4. The first one is the LO-amplifier running in compression to provide an amplified and stable LO signal to the mixer. The second and third amplifiers are placed on the IF path, to provide the necessary chip gain. The first is designed to minimize the noise contribution while the second is designed to maximize power output and thereby chip linearity.

Chapter 5 contains the design and results of a variable attenuator block needed to control the chip gain.

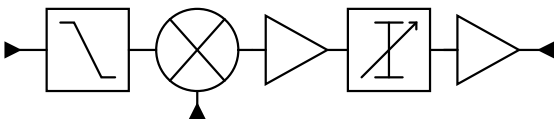


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2.5 Comparison to final result

The figures above are based on prior estimates. Table 2.6 lists the results achieved with the layout in Table 2.2 and shows a good agreement.

Table 2.6: Achieved simulated performance with chip setup 1. The results are in agreement with the prior estimates detailed in Table 2.2.



	Nominal gain	Gain: +4.4 dB	Gain: -6 dB
Gain	10.6 dB	15.0 dB	4.6 dB
NF	11 dB	10 dB	13 dB
IIP_3	20 dBm	17 dBm	21 dBm

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Chapter 3

Mixer Design

The system design chapter shows the importance of having the mixer sub-circuit first. Here we examine more in-depth how a mixer functions, different ways of realizing them, and the chosen topology in particular.

3.1 Introduction

3.1.1 Signal multiplication

The mixer down-converts a signal by means of multiplication. The input radio frequency (RF) is multiplied with a local oscillator (LO), an external sinusoidal signal with frequency f_{LO} . f_{LO} is selected such that one of $f_{IF} = |f_{RF} \pm f_{LO}|$ (3.1) becomes the desired down-converted signal. f_{IF} is called the intermediate frequency.[11]

$$V_{RF} \cos(\omega_{RF}t) V_{LO} \cos(\omega_{LO}t) = \frac{V_{RF}V_{LO}}{2} \left[\cos((\omega_{RF} - \omega_{LO})t) + \cos((\omega_{RF} + \omega_{LO})t) \right] \quad (3.1)$$

The result from Equation 3.1 requires a completely ideal multiplication device. A component with non-linear I/V-characteristics can be used for mixing, which brings about more spectral products:[6]

$$i = a_0 + a_1v + a_2v^2 + a_3v^3 + \dots + a_Nv^N \quad (3.2)$$

The current i through the device depends on the sum of the two input signals $v = V_{RF} \cos(\omega_{RF}t) + V_{LO} \cos(\omega_{LO}t)$. The mixing products then become

$$\begin{aligned} i = & a_0 + a_1 [V_{RF} \cos(\omega_{RF}t) + V_{LO} \cos(\omega_{LO}t)] \\ & + a_2 [V_{RF} \cos(\omega_{RF}t) + V_{LO} \cos(\omega_{LO}t)]^2 + \dots \\ & + a_N [V_{RF} \cos(\omega_{RF}t) + V_{LO} \cos(\omega_{LO}t)]^N \end{aligned} \quad (3.3)$$



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The output current $i = i_{DC} + i_{IN} + i_{SPUR}$ contains a DC current term ($i_{DC} = a_0 + a_2(V_{RF}^2 + V_{LO}^2) + \dots$), the original signals ($i_{IN} = a_1(V_{RF} \cos(\omega_{RF}t) + V_{LO} \cos(\omega_{LO}t))$) and the mixing products (i_{SPUR}). The second-order terms are the primary mixing products and contains the upper ($\omega_{RF} + \omega_{LO}$) and the lower ($\omega_{RF} - \omega_{LO}$) sidebands:

$$i_{2nd} = a_2 \left[\frac{1}{2} V_{RF}^2 (1 - \cos(2\omega_{RF}t)) + V_{RF} V_{LO} (\cos((\omega_{RF} - \omega_{LO})t) + \cos((\omega_{RF} + \omega_{LO})t)) + \frac{1}{2} V_{LO}^2 (1 - \cos(2\omega_{LO}t)) \right] \quad (3.4)$$

In this design the lower sideband is the desired intermediate frequency ω_{IF} .

3.1.2 LO drive

Regardless of topology and design choice all mixers need an LO reference signal. This signal, or drive, is usually very large in comparison to the RF and IF signals in order to increase mixer linearity. A large LO drive will, from the RF signal's point of view, switch the mixer between on- and off-states faster, making the multiplication of the signals digital. The larger the LO drive the faster the transition between on and off states takes place. This results in more linear operation.[11]

For the P_{1dB} measure, not only fast on- and off-transitions are important but also the power of the LO. As explained in subsection 1.6.3 P_{1dB} is simulated by noting at which power the gain of a component has dropped 1 dB. When the power of the RF-signal becomes the same order of magnitude as the power of the LO drive, the LO-signal will no longer be able to switch the mixing-FET as desired. This will cause the gain to drop and thus limit P_{1dB} . As IIP_3 is closely coupled to P_{1dB} this will also be limited.[7]

3.2 Topologies

3.2.1 Overview

The mixing functionality can be realized with a number of different mixing devices and different balanced or unbalanced designs. The literature presents two preferred devices used to multiply two signals; the diode and the transistor.[12]

3.2.2 Balanced and unbalanced mixers

An ordinary unbalanced mixer exhibits the behaviour where all spurious products from Equation 1.2 are present. By utilizing a balanced layout with two or more mixing elements, it is possible to suppress some of these spurious responses. There are many kinds of balanced mixers and the type determines what spurious responses are suppressed.[11, 13]



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The downside is that additional elements must be introduced in the form of hybrids or baluns and these are often relatively large on MMICs, depending on frequency. These elements either phase shift or convert the signal between balanced and unbalanced signals.

3.2.3 Image reject mixers

Two mixers can be designed as an image reject mixer which cancels out the image frequency. That is the frequency that converts to the exact same IF-signal as the RF and is almost always an unwanted product. See subsection 3.1.1.

The image reject functionality is achieved, in short, when the LSB and USB (lower and upper sideband respectively) are subjected to different phase shifts in the hybrids. This makes it possible to cancel out or suppress one of the sidebands depending on the quality of the hybrids and mixers. The image reject performance is very dependant on the precision of the baluns, more specifically the degrees of phase-shift and amplitude difference.[14]

These constructions are most useful in situations when the image band lies close to the IF. In this case the IF-signal has the frequency 2.14 GHz and the image band starts at 7.18 GHz. With this large distance in frequency the image is easily filtered and an image reject topology is therefore not considered.

3.2.4 Diode mixers

Diode mixers are realized with Schottky diodes because of their switching speed. Today diode mixers are more prevalent for high frequencies, where FETs are less potent. An advantage with diode mixers is that they do not need a bias voltage.

3.2.5 FET mixers

FET mixers generally have lower noise and higher gain compared to diode mixers. There are in general two approaches to designing a FET-mixer; active or resistive mixer. MMIC processes are optimized for FET-structures, not diodes. A major advantage with FET-mixers is the inherent isolation between the LO and the IF provided by the FET.

Active FET mixers are biased like an amplifying element and thus have a positive conversion gain while resistive mixers are biased with zero v_{ds} and v_{gs} below pinch-off such that the drain-source resistance is linear to the applied gate-voltage. When considering linearity, resistive mixers are superior.[11, 15]

3.2.6 Conclusion

Almost all MMIC mixers designed for the S band are today FET mixers. Diodes are common only when designing mixers with frequencies at least one order of magnitude higher or using discrete components. Since high linearity is important, a FET resistive mixer is designed. To decide whether to implement it as single-ended or as singly balanced, both types are initially designed with



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simple ideal components. The single-balanced mixer is eventually disregarded due to its complexity and to the fact that the single-ended mixer shows adequate performance. The comparison is detailed in Appendix D.

3.3 Design of single-ended FET resistive mixer

3.3.1 Device

As described in subsection 3.3.3 higher LO power will result in a more linear mixer. The greater the gate width, the more LO power the FET can handle. The largest FET in the UMS process has a $8 \times 75 \mu\text{m}$ gate width. As it turns out, this is also the FET which gate is easiest to match to 50Ω . [10]

A shunt inductance is placed at the gate to the mixing FET in order to ensure that the FET bias point remains fixed at high LO power. The inductance is part of the matching network in the LO-amplifier.

3.3.2 Diplexer

The overall simplicity of the FET resistive mixer makes the diplexer the most sophisticated part and also crucial to the performance (Figure 3.1). Between the RF input and the mixer FET, the network has to band-pass filter the signal in order to both inhibit the IF-signal from leaking out and to suppress the radar image at $f_{image} = f_{LO} + f_{IF}$. Once the image frequency has passed this filter it will mix down to f_{IF} and from there be indistinguishable from the original signal:

$$|f_{image} \pm f_{LO}| = |f_{LO} + f_{IF} \pm f_{LO}| = \begin{cases} 2f_{LO} + f_{IF}, & \text{Easily filtered} \\ f_{IF}, & \text{Harmful} \end{cases} \quad (3.5)$$

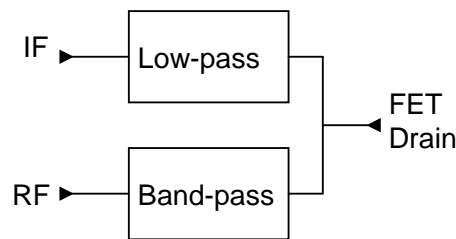


Figure 3.1: This diplexer consists of a low-pass filter and a band-pass filter. The signal is band-pass filtered, mixed at the FET and then low-pass filtered. Both filters are designed to match the signal to the port at the appropriate frequencies.

Between the mixer FET and the IF output, the diplexer must low-pass filter to reject any signals above the down-mixed lower sideband frequency at f_{IF} . Additional filtering is done in the subsequent amplifiers.

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Besides filtering, the diplexer has to match both the input signal and the output signal. The input RF port is matched to $50\ \Omega$ at 2.9 – 3.4 GHz and the output IF port is matched to $50\ \Omega$ at 2.14 GHz.

The diplexer is implemented using non-resistive L-C circuits with the number of poles required to fulfil the chip specifications. The losses in the inductors add directly to the overall noise figure of the chip. The result is therefore a trade-off between filter characteristics and network simplicity.

3.3.3 Bias scheme

The principle of the mixer is to set the gate-source voltage v_{gs} below pinch-off and then control the FET with the LO-signal. Pinch-off for the FET is $v_p \approx -0.7\text{ V}$. A low distortion mixer is achieved by having high LO power and thereby reducing the rise-time when the FET switches on and off. This way less time is spent operating in regions where v_{gs} is close to v_p (operation at gate voltages close to v_p are more non-linear). However, an LO powered too high will cause the gate to rectify and this will in turn lead to non-linear operation.[15] By lowering v_{gs} even more below v_p this can be avoided. The gate will also start to break down for too large negative gate voltages, providing a lower limit for v_{gs} .

As the chip is fed a +5 V DC, the source and drain are both raised to $|v_{gs}|$ for the mixer to experience an effective negative gate voltage and $v_{ds} = 0\text{ V}$. The bias network is placed at the source and two large value resistors divide the voltage appropriately. No DC-current will pass through the resistors.

3.4 Schematics and layout

The schematic of the final resistive FET mixer is shown in Figure 3.2. The corresponding layout is found in Figure 3.3.

3.5 Simulation results

3.5.1 Overview

A summary of the mixer's performance is listed in Table 3.1. Simulations are made using the LO-amplifier to provide the LO-signal. This amplifier is explained in section 4.2 but knowing it amplifies the system's LO-signal is enough to understand this mixer-chapter. All sub-circuits apart from the FETs are simulated with EM-models, see Appendix E for an explanation of the EM-simulations. Yield simulations are found in Appendix F.

3.5.2 Filter characteristics

The most important part of the diplexer filter characteristics is shown in Figure 3.4. The figure shows the EM simulated diplexer as well as a spread analysis made on the circuit model. How the spread analysis is performed is explained



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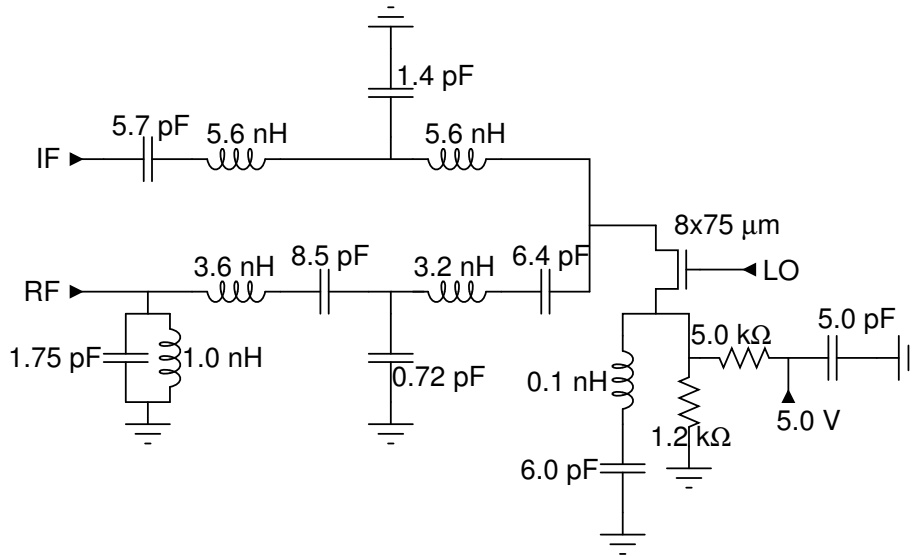


Figure 3.2: Schematic of the mixer.

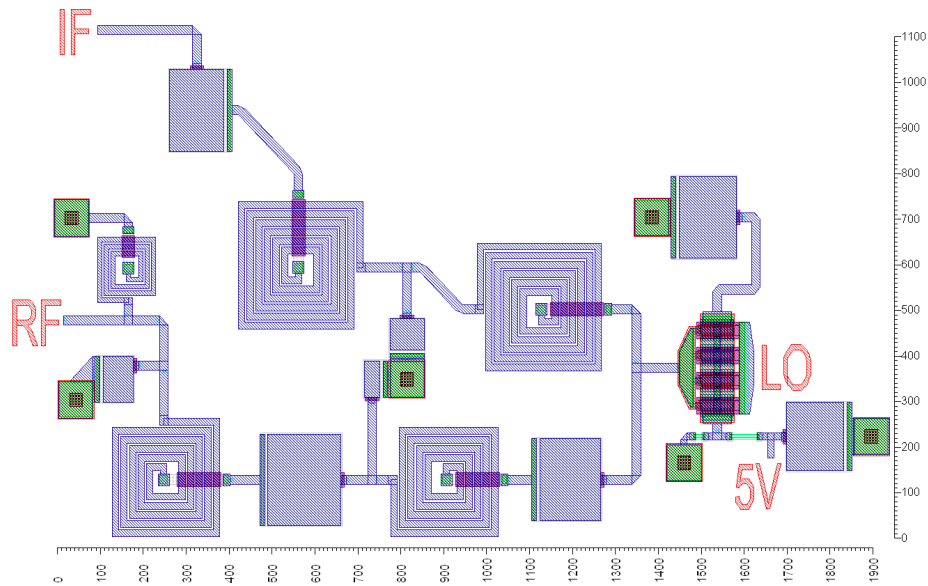


Figure 3.3: Layout of mixer. Dimensions in μm .

in-depth in Appendix F. For the full 0–10 GHz frequency characteristics see Figure F.4c.

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Table 3.1: Simulation results of the mixer for $LO = -2$ dBm and $v_{gs} = -0.95$ V. Temperature at 25 °C and no parameter spread applied.

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Frequency range RF		2.9–3.4		3.1–3.3			GHz
Frequency range LO		5.04–5.54		5.24–5.44			GHz
Frequency IF		2.14		2.14			GHz
Return loss RF	14	16		20	21		dB
Return loss Out		16			16		dB
Conversion loss		7.7	7.9		7.5	7.6	dB
Gain Variation		0.45	0.45		0.05	0.05	dB
Image Rejection	48	50		50	51		dB
P_{1dB} (input)	12.7	13		12.7	13		dBm
IIP_3 (estimate)	23	23		23	23		dBm
Noise figure		7.7	7.9		7.5	7.6	dB

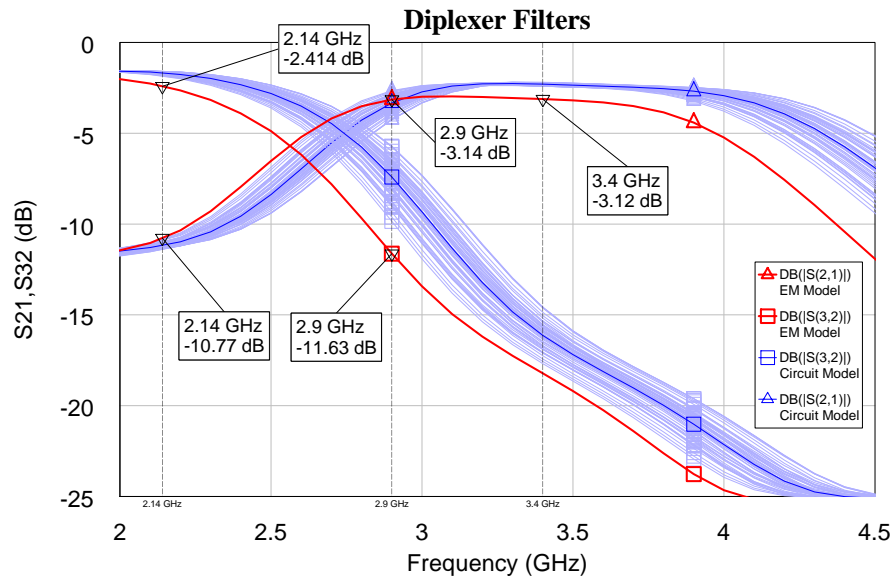


Figure 3.4: Diplexer filter characteristics. The red (thick) line is the EM simulation and the blue lines correspond to the spread analysed with the circuit model. The curves marked with triangles Δ details the bandpass filter between the RF input and the mixer-FET drain. The curves marked with squares \square details the low-pass filter between the mixer-FET drain and the IF output.

3.5.3 Conversion gain and matching

Mixer gain (Figure 3.5) and input matching (Figure 3.6) are calculated with the final LO-amplifier connected and using large signal analysis. The bias point



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does not effect neither the conversion gain nor the input matching much. The matching of the RF-port is quite independent of the LO power. The gain depends on the LO-signal which in turn depends on the LO input power. Different settings on the chip's gain block located after the first IF amplifier does not to affect the performance of the mixing part, which is why simulations with varied chip gain are not displayed. The final bias point is chosen to $v_g = -0.95$ V.

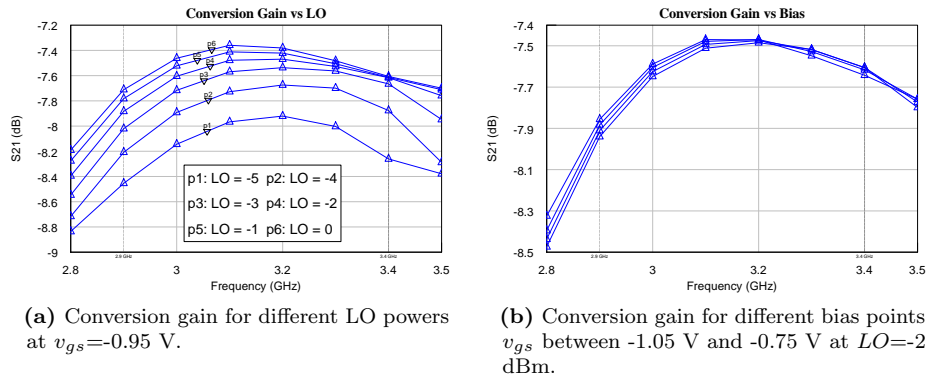


Figure 3.5: Mixer conversion gain.

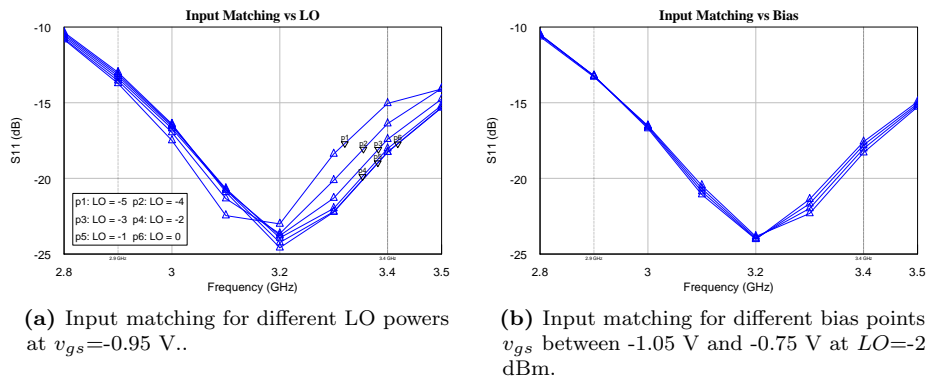


Figure 3.6: Mixer RF-input matching.

3.5.4 Linearity

Figure 3.7 illustrates the compression of the conversion gain for different bias points v_{gs} . P_{1dB} is the point where the conversion gain has dropped 1 dB and is usually referenced to the input power. P_{1dB} as a function of frequency and LO input power are plotted in Figure 3.8.

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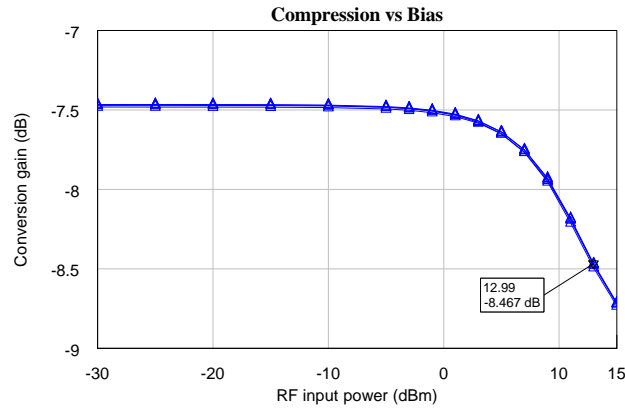


Figure 3.7: Mixer conversion gain compression for different bias points v_{gs} . Here $LO = -2$ dBm and $f = 3.2$ GHz. The compression does not vary with the bias point.

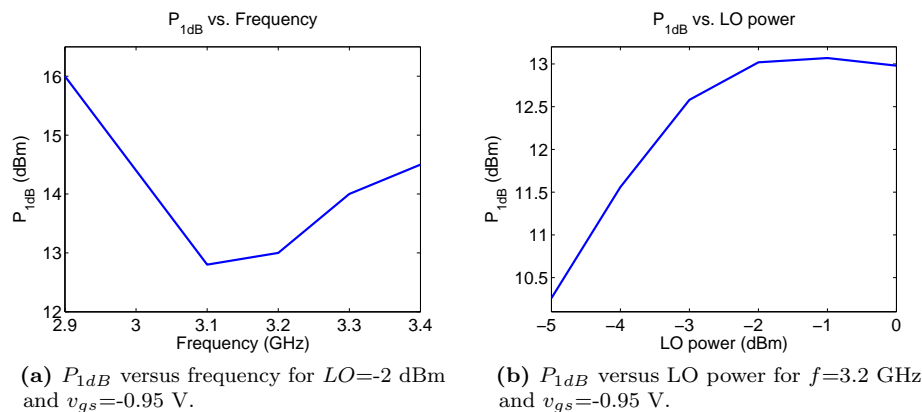


Figure 3.8: Mixer P_{1dB} versus frequency and LO power.

3.5.5 Image reject

The conversion gain of the RF image at $f_{LO} + f_{IF} = 7.18$ – 7.68 GHz is displayed in Figure 3.9.

3.6 Discussion

As discussed in the performed topology study there are a few sophisticated designs that may give very good mixer performance. The achieved performance and the simple design of the single-ended resistive FET mixer is however undeniable. Not only does this save design effort but also space on the chip and thereby also



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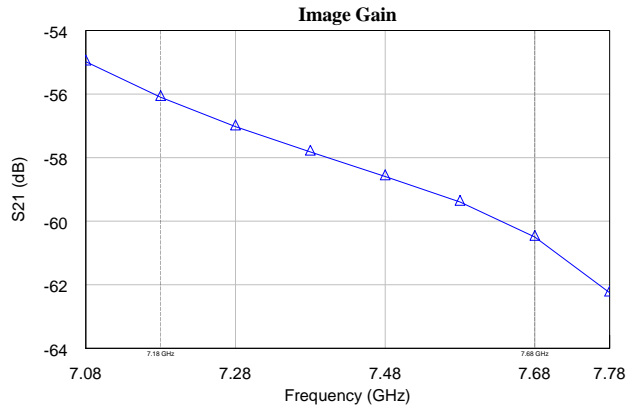


Figure 3.9: Conversion gain with the RF-image as the input signal.

money in yield and wafer costs. It is not surprising that the industry in general chooses this topology for high linearity mixers at these frequencies.[16]

The noise figure in the mixer is casually considered equal to the losses. Even though this is a popular approach there are some ways to take noise generated in the mixer into account.[17] However, since the noise figure is generally somewhat lower than the losses, the conversion loss is taken as a high estimate of the noise, disregarding the more accurate noise calculations.

Low accuracy three-tone IIP_3 simulations yield a result 2–3 dBm higher than the estimates made from P_{1dB} . Due to their uncertainty, these results are not reported here and are only mentioned in this discussion for reference.

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Chapter 4

Amplifier Design

After down-conversion, the signal must be amplified twice according to the chip design in chapter 2. Furthermore, the LO-signal controlling the mixer also needs amplification. The function and purpose of these three amplifiers are explained in this chapter.

4.1 Introduction

4.1.1 Function

The purpose of an amplifier is to amplify electric signals. In a radar receiver setup the amplifier is often, after a limiter and a filter, the first element an incoming signal sees. Any degradation of the signal's power before the first amplification increases the noise (see Figure 1.5). The main goal of such an amplifier is to provide gain without adding noise, and is called an LNA (low noise amplifier).

The last amplifier in a transmitter-setup is more focused on providing as much gain and output power as possible without consuming too much power. For most amplifiers it is also of concern to operate linearly. This is measured with $IIP3$ and P_{1dB} as explained in subsection 1.6.2.

An amplifier designed with FET-technology needs a drain-supply voltage v_{ds} (drain-source), see Figure 4.1. The current through the FET, i_{ds} (drain-source) depends on the gate-source voltage v_{gs} . The incoming signal, which is fed to the gate-terminal, controls the current through the FET which amplifies the signal.

4.1.2 Bias point

When operating the FET there are in general four different bias points corresponding to different classes of amplifiers.[18] For example, see Figure 4.2. For low noise operation, bias point A is common and for high output-power and class A operation, bias point C is more prevalent.

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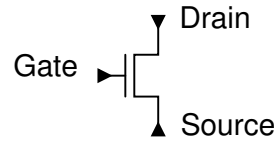


Figure 4.1: The ports of a FET. The voltage v_{gs} (gate-source) controls how much current i_{ds} can flow through the FET.

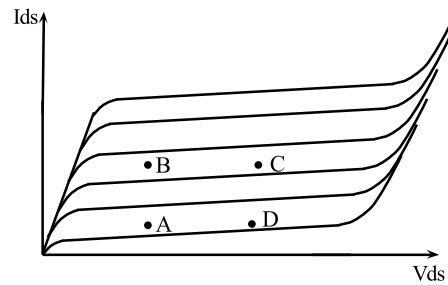


Figure 4.2: Different bias points for a FET.

4.1.3 Bias scheme

The amplifiers in this project are biased using a self-biasing scheme according to Figure 4.3.[6] This limits the size and complexity of the bias network as only one (positive) DC source is supplied. The PPH25 process, contrary to PH25, can handle a higher drain-source voltage v_{ds} over the FET. This further simplifies the biasing as the supplied 5 V DC voltage can be applied without the need of a resistor on the drain, given that this constitutes an appropriate bias point.

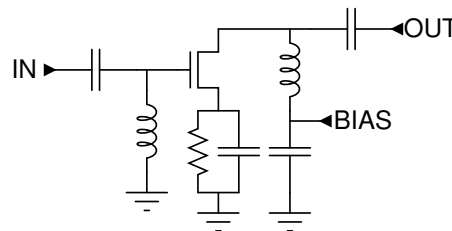


Figure 4.3: The principle of the self-biasing scheme. The FET's drain is raised to V and the gate is DC-grounded. The resistor on the source controls the gate-source voltage v_{gs} and thereby also the bias-current i_{ds} .

4.1.4 Stability

A stable amplifier ensures that there is no oscillation.[19] The amplifiers on this chip are all designed to be unconditionally stable at all frequencies. Generally

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an amplifier with higher gain is harder to make stable. The stability measure K in Equation 4.1 is used to quantify the stability. The amplifier is unconditionally stable if $K > 1$ for all frequencies.

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \quad (4.1)$$

4.1.5 Power utilization

As the DC-power consumption of a amplifier increases, the linearity (P_{1dB} and IIP_3) increases. This is evident as compression will occur at higher power (subsection 1.6.3). The LO amplifier is designed to operate in compression and as such it does not benefit from high power. The remaining available DC-power is divided between the first and the second IF amplifier. As the IIP_3 for the second amplifier affects the system more than that of the first one, the power utility here is higher.

4.2 Constant power LO-amplifier

4.2.1 Introduction

The system's LO-signal is specified to -5-0 dBm and therefore there is a need to amplify this signal. The purpose of the amplifier is to provide a high and constant input power to the mixer, not depending on fluctuations in the system's LO-signal. This is achieved by operating the amplifier in compression so that the mixer always sees the same LO. Also, by running the amplifier into compression, i.e. outputting a square-waved pulse, the mixer will switch faster between the on- and off-states, behaving more like an ideal switch. This results in a more linear mixer as explained in subsection 3.1.2.[20]

4.2.2 Design

Principle

When designing an LO-amplifier for a resistive FET mixer it is important to minimize reflections from the very reactive mixer-gate. However, attaining a well-matched gate is difficult.[21] At first, a bias-point is chosen, so that proper gain and compression is achieved. The dependence on frequency was considered too large and a weak feedback loop (500Ω) was implemented. A too strong feedback is undesirable because of the reduced gain and stability. A schematic and the actual layout of the amplifier are seen in Figure 4.4 and Figure 4.5, respectively.

The FET is self-biased by applying a voltage to the source, while having $v_{DC} = 0$ V on the gate (see 4.1.3 Bias scheme). This requires having an inductance to ground close to the gate.

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As noise is not of much concern for the LO, it can be traded for stability, compression, ease of tuning and frequency independence. Since linearity is actually to be avoided and the amplifier never enters high-linearity bias-regions such as for class A-operation, the amplifier consumes small amounts of power, around 100 mW.

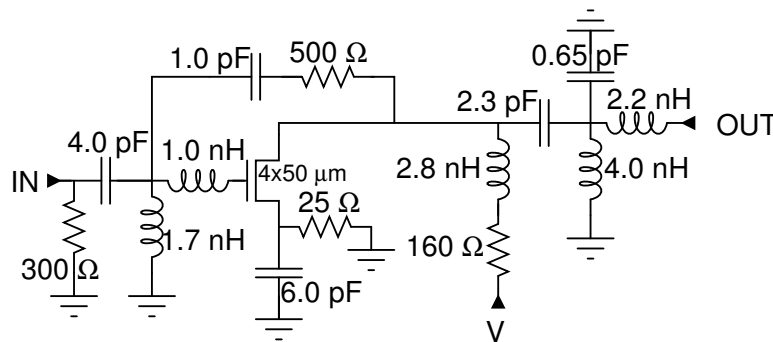


Figure 4.4: Schematic of the LO-amplifier.

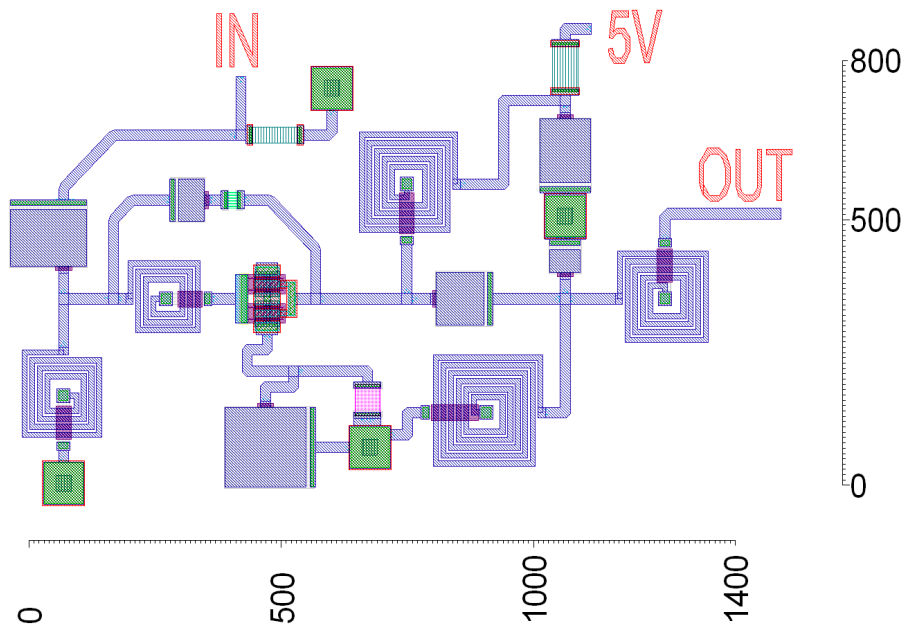


Figure 4.5: The layout of the LO-amplifier with a weak parallel feedback, slightly elongated source for input matching and a self-biasing scheme. Dimensions in μm .

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FET-configuration and matching networks

Using large FET's results in a relatively linear operation which is to be avoided for the compression technique to work.[15] In Figure 4.6 the drain impedance for different FET-sizes is simulated. It shows that a smaller FET such as $4 \times 25 \mu\text{m}$ is a better conjugate match for the mixer since only reactive matching networks would be needed. However, such a small FET does not provide enough gain. Therefore a FET-size of $4 \times 50 \mu\text{m}$ is chosen.

The input matching network consists of an L-shaped inductor-inductor network and a shunt-resistance. The length of the source is chosen to create small input reflections. The output matching network needs to match the reactive gate of the mixing FET. This is done with a shunt capacitance and an inductance in series. The inductance to ground keeps the gate of the mixing FET at $v_{DC} = 0 \text{ V}$.

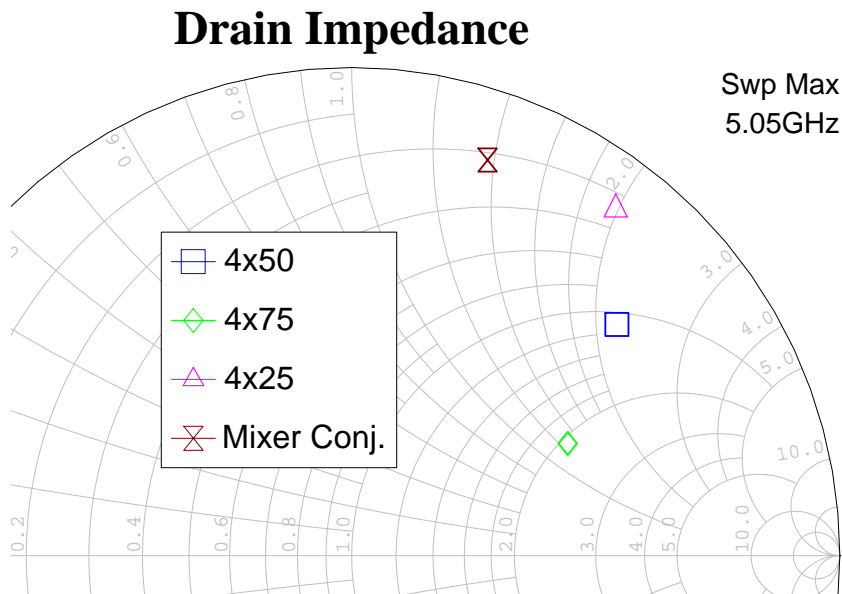


Figure 4.6: The drain impedance for different FET-sizes. The $4 \times 50 \mu\text{m}$ and the $4 \times 25 \mu\text{m}$ FET-sizes make a good conjugate match for the mixer. However, $4 \times 25 \mu\text{m}$ does not provide enough gain.

Bias point

The amplifier enters compression when applying a low v_{ds} as seen in Figure 4.7. The output power is shown versus input LO-power for different FET-bias points. A good bias point seems to be $v_{gs} = -0.4 \text{ V}$, $v_{ds} = 2 \text{ V}$ which provides a signal in compression.



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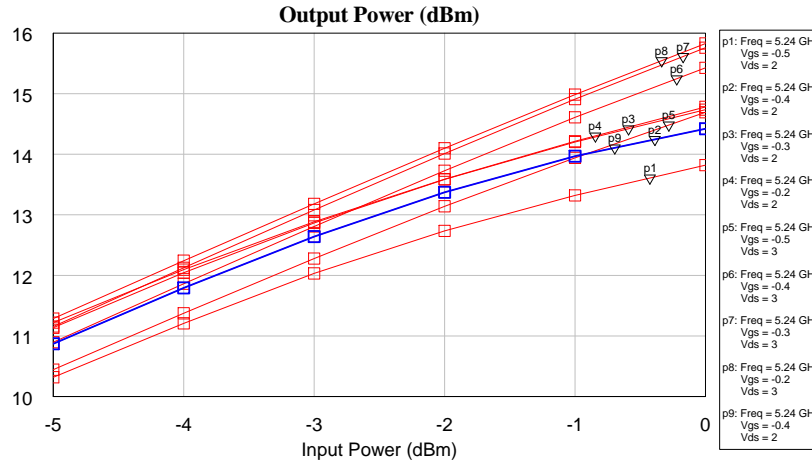


Figure 4.7: Output power for different bias points for the $4 \times 50 \mu\text{m}$ FET. The blue line represents the chosen bias-point $v_{gs} = -0.4$ V, $v_{ds} = 2$ V.

4.2.3 Simulation results

The simulation results for the LO-amplifier are presented in Table 4.1 for two ranges of input powers. The amplifier is operating in compression for input powers of -2 – 0 dBm and less so for weaker input powers. The power delivered into the mixing FET is shown in Figure 4.8 and input reflections in Figure 4.9. The reflections become a problem at higher frequencies and input powers around -4 dBm. Good input matching is hard to achieve with the current amplifier design. As the load is changing depending on input power it is difficult to match for all input powers. Emphasis has been placed on achieving a good match for $P_{lo} = -2$ dBm which is considered to be the most likely input power. The square-wave pulse is seen in figure Figure 4.10.

The spread analysis, Figure F.1, suggests that the LO-amplifier is sensitive to variations. The delivered power may drop as much as 2 dB for input powers of -2 dBm. However, when spreading the LO- and mixer-FET which seem to cause most of the spread, the mixer conversion gain and compression are hardly affected, Figure 4.11. This suggests that the power supplied to the mixer is above some threshold-power where it is fair to assume that stronger LO is less important[21]. However, for $P_{LO} = -4$ dBm, the mixer P_{1dB} is being affected, it drops on one occasion to 9.7 dBm.

4.2.4 Gain versus compression

It is possible to increase the amplifier's gain by increasing v_{ds} a little but this would not compress the signal as much. As seen in Figure 4.12, the mixer gain for the compressed LO-signal has the same frequency dependence for different

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Table 4.1: Simulation results of the LO-amplifier. Temperature at 25 °C and no parameter spread applied.

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Frequency range	5.04–5.54			5.24–5.44			GHz
Delivered Power							
@LO=−2–0 dBm	4.0	4.8	5.5	4.6	5.0	5.4	dB
@LO=−4– −2 dBm	2.4	3.7	5.0	3.3	4.0	5.0	dB
Return loss input							
@LO=−2–0 dBm	13.5	17		17	18		dB
@LO=−4– −2 dBm	10.5	15		13	16		dB
Stability K @0–80 GHz	>1	>1		>1	>1		
Power consumption		100			100		mW

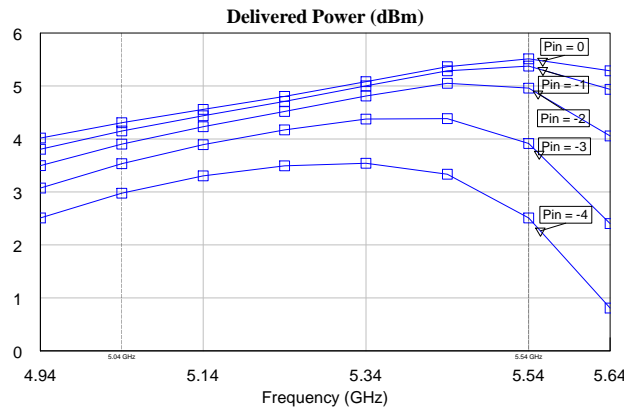


Figure 4.8: The power delivered into the mixer from the LO-amplifier for different frequencies and LO-input powers. Measured in between amplifier and mixer. The active frequencies are 5.04 to 5.54 GHz.

LO-powers. If the gain is increased, i.e. not so strong compression, the LO-signal will vary for different input signal and this causes the mixer-gain to behave badly, Figure 4.12d. When the LO-drive to the mixer becomes too large, the mixer-gain suffers.

4.2.5 Discussion

The key feature with the LO-amplifier is the square-waved pulse which helps to achieve a more linear mixer. The gain of the amplifier is somewhat low, this is attributed to the compression technique and the matching to the very reactive mixer FET. But due to the system layout with two IF-amplifiers, having a more powerful LO and thereby increasing the mixer's P_{1dB} -point would not yield a great increase in the complete chip's compression point as the IF-amplifiers



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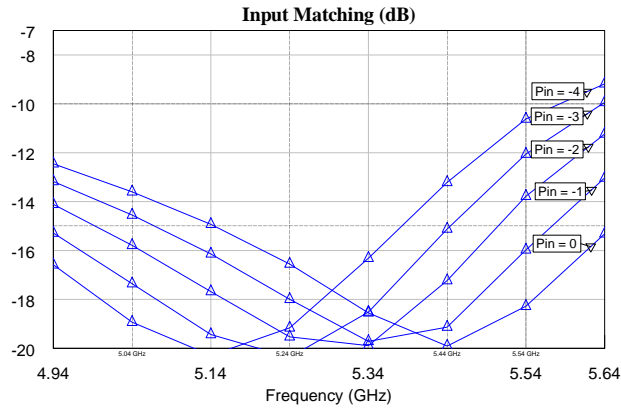


Figure 4.9: Input reflections of LO-amplifier, weaker input-powers and higher frequencies give larger reflections. The active frequencies are 5.04 to 5.54 GHz.

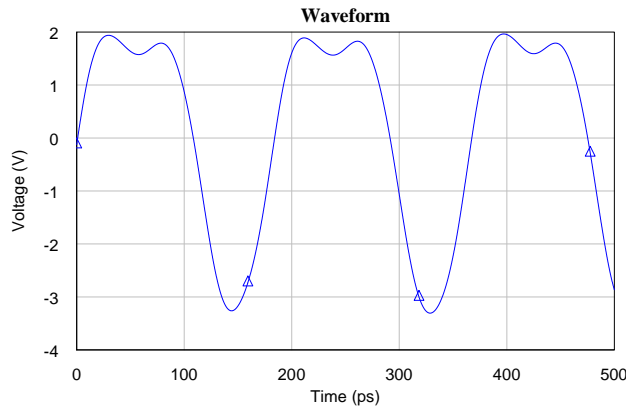
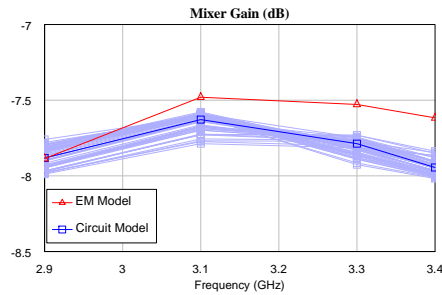


Figure 4.10: Amplifier LO running in compression, producing a square-shaped output voltage waveform.

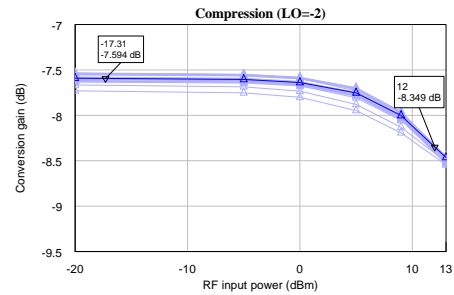
then become the limiting factor. Also, a stronger LO-drive would be harder to filter out in the diplexer and the LO-isolation would suffer, see Figure 6.6. The interaction between mixer conversion gain and LO-amplifier is difficult to foresee which is why the matching network was modified many times and some adjustments to the diplexer's RF-bandpass were made before acceptable performance was achieved.

The amplifier can deliver some more gain in exchange for compression by increasing v_{ds} a notch, see Figure 4.12. However, there are repercussions on the mixer gain if the LO becomes too strong. Therefore it might be of future interest to vary the 5 V-bias voltage to achieve the desired bias-point. It is also possible to increase the gate-source voltage, v_{gs} , for some gain and increased power consumption.

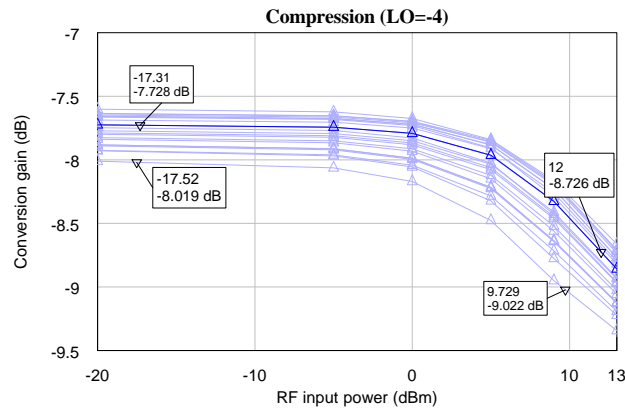
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(a) Mixer gain when spreading LO-FET at LO=-2dBm.



(b) Mixer compression when spreading LO- and mixer-FET for LO=-2dBm.

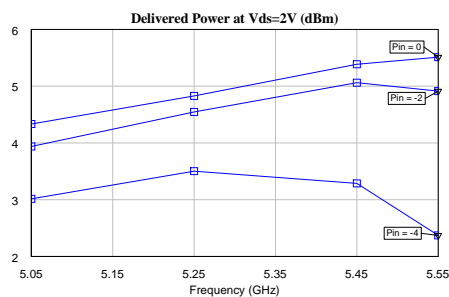


(c) Mixer compression when spreading LO- and mixer-FET for LO=-4dBm.

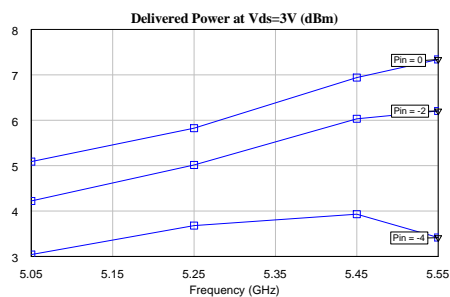
Figure 4.11: Conversion gain and compression point for the mixer when applying spread to the mixer- and LO-amplifier-FET. Using EM-models at $f_{rf} = 3.2$ GHz. The observed spread in delivered LO-power is not present in (b) ($P_{lo} = -2$ dBm) suggesting some threshold power is reached. For $P_{lo} = -4$ dBm, (c), the mixer's compression point is being affected by spread in the FETs.



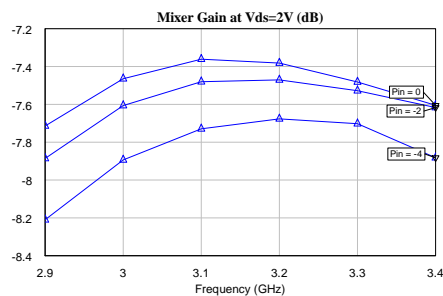
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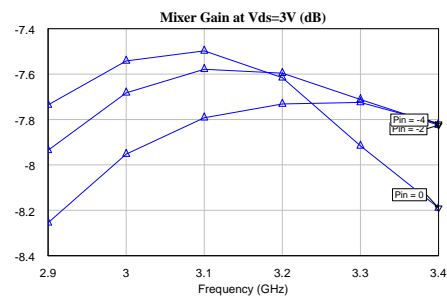
(a) Delivered power for LO-amplifier in compression (drain-source voltage is 2 V).



(b) The delivered power for LO-amplifier in less compression (drain-source voltage is 3 V).



(c) Mixer-gain for LO-amplifier in compression.



(d) Mixer-gain for LO-amplifier in less compression. For LO=0 dBm the mixer-gain is starting to offset and drops drastically at higher frequencies.

Figure 4.12: Comparison between a compressed and not as compressed LO by varying V_{ds} .

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The literature states that a single ended FET resistive mixer has a P_{1dB} -point approximately 4 dB above the LO-drive[22] and the result for this LO-mixer construct applies approximately to that rule. A P_{1dB} of 12 dBm at $P_{LO} = -4$ dBm, at center frequency and a 3 dB attenuation in the diplexer says that the required LO should be 5 dBm. The LO-amplifier outputs 3.5 dBm at these conditions and it is thought that the square-shaped LO-drive accounts for the extra linearity.

The reflections were tuned for an input power of -2 dBm but as the load changes for different input powers, it is difficult to achieve low reflections on all frequencies and for all input powers. Especially input powers of -4 dBm and high frequencies results in the input reflections being -10 dB.

The yield analysis, Figure F.1a, shows a large spread in delivered power especially at higher frequencies. The spread at $P_{lo} = -2$ dBm hardly affects the mixer conversion gain and compression point, suggesting that the delivered power is enough for this mixer. As the amplifier is much less in compression for $P_{lo} = -4$ dBm, the spread starts to affect the mixer performance, Figure 4.11.

Future work could investigate if it is possible to choose another bias-point with more gain and still maintain good compression and matching to the mixer. It may be the case that the parallel feedback could be removed for some additional gain. One solution to the large spread in the FET may be to use another bias-scheme which could be adjusted after production on a per-chip basis. For other MMIC-designs where the mixer requires a much stronger LO-drive, a two-stage LO-amplifier might be justified. The first stage would then supply strong gain while the second stage compresses the signal.

4.3 Low noise IF-amplifier

4.3.1 Introduction

All components of the MMIC should be as linear as possible. However, the noise figure in the system also requires attention. Together with the conversion loss in the mixer the first IF amplifier contributes with the most noise. This amplifier is therefore designed as a low noise amplifier (LNA). Linearity is still of high importance, which is why the amplifier should also have high P_{1dB} and high IIP_3 . As the IF-signal is a single frequency, the amplifier's bandwidth is very narrow.

4.3.2 Design

Principle

The principle design of a LNA is to find the input matching network that minimizes the noise of the FET and at the same time matches to S_{11} . The first part of this would be finding the best FET size. In order to match to both S_{11} and optimum noise series feedback is implemented.[23] The final noise figure of the amplifier is primarily the combination of both the losses in the input



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matching network and the noise inherent to the FET. The amplifier is biased according to the self-biasing scheme detailed in subsection 4.1.3.

Noise

There is no noise model for the PPH25 FET. The only data available are measurements of a $4 \times 75 \mu\text{m}$ FET provided by UMS. To estimate the amplifier's noise the PH25 model is used. This model together with the similarity in behaviour between the PH25 and the PPH25 FET gives a crude estimate of the noise figure. The position of the Γ_{opt} is approximately the same for the different processes. The noise increases faster in the PPH25 case as mismatch increases (see Figure 4.13). Approximately 0.5 dB is added to the noise simulated with the PH25 FET to get the PPH25 noise, provided the mismatch is not too large.

Minimum FET Noise

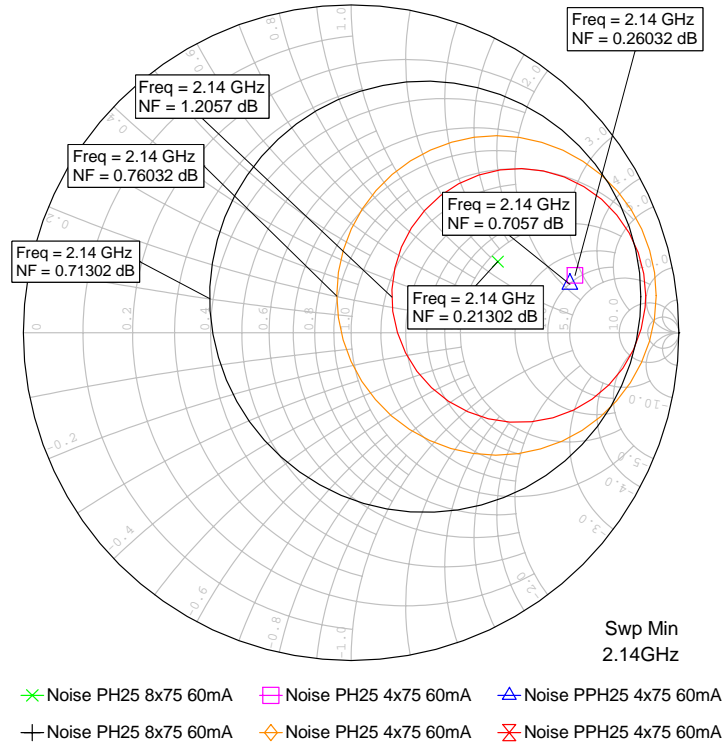


Figure 4.13: Γ_{opt} and constant noise circles for different UMS FET, both PH25 and PPH25. Both the absolute noise and the noise increase with mismatch is greater for PPH25. The $8 \times 75 \mu\text{m}$ is the biggest FET available. It has the lowest inherent noise, the most conveniently placed Γ_{opt} and is the most linear device (see subsection 3.3.1).

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FET selection and input network

Based on the noise properties of the FETs (Figure 4.13) and previous work with the PH25 process[10], the $8 \times 75 \mu\text{m}$ FET is chosen for the amplifier. Fortunately both low noise and linear operation favours a large device. The input network is a simple L-shaped inductor-inductor impedance matching network.

Attenuator

The system design requires the amplifier to have a certain gain. If the gain of this amplifier is higher, the total IIP_3 will suffer and if it is lower the final noise will increase. As the amplifier's gain is higher than the specified 12 dB an attenuator consisting of two resistors is placed at the end. It is designed to optimize the input and output matching as well as add to the stability.[24] An alternative to an attenuator is parallel feedback (as in IF amplifier 2). This design would however degrade the noise figure and has therefore been discarded.

4.3.3 Schematics and layout

The schematic of amplifier IF1 is shown in Figure 4.14. The corresponding layout is found in Figure 4.15.

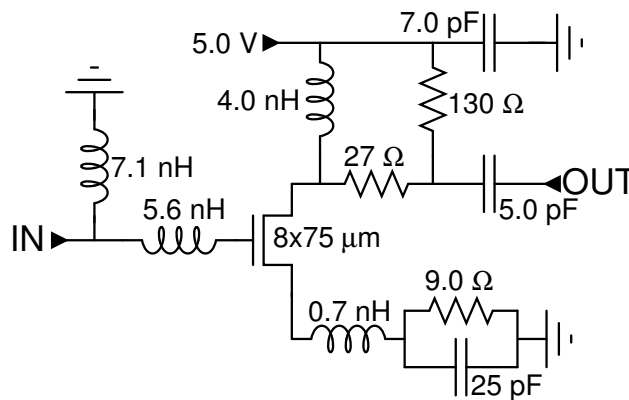


Figure 4.14: Schematic of amplifier IF1.

4.3.4 Simulation results

The simulated performance of amplifier IF1 is found in Table 4.2. Spread analysis is reported in section F.3 together with plots of the simulation data. The full spectrum gain is plotted in Figure 4.16.

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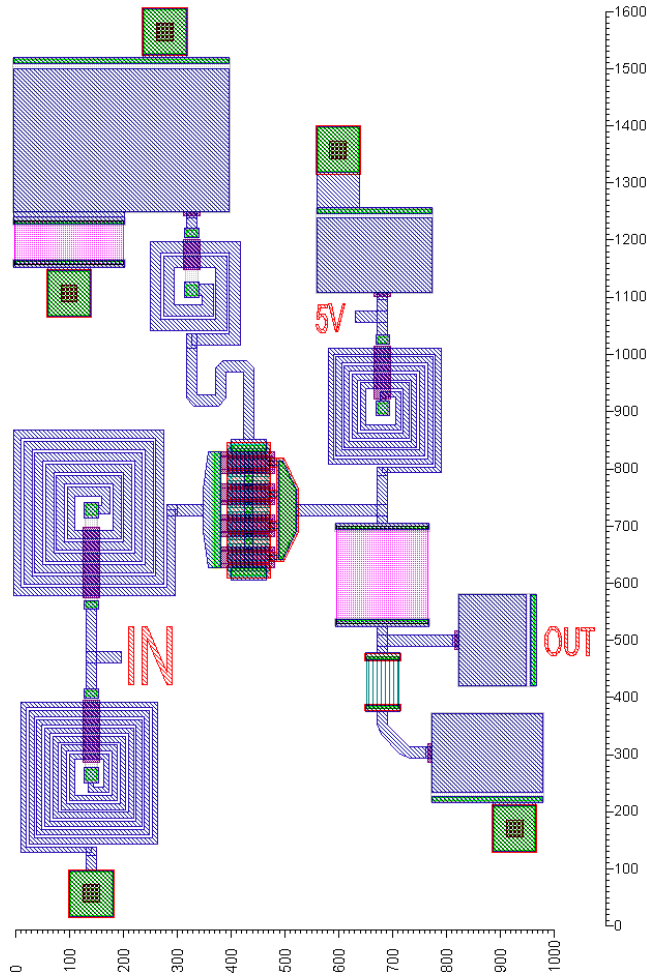


Figure 4.15: Layout of amplifier IF1. Dimensions in μm .

4.3.5 Discussion

The narrowband property of the amplifier enables a design in which parallel feedback can be omitted. This has a good impact on the noise figure but it also gives a steep gain slope and a gate that is hard to match. One consequence is that the matching inductors become very large which in turn increases the noise figure as the UMS inductors have a somewhat low quality factor Q . Another consequence is that would the frequency characteristics shift only 100 MHz during fabrication the performance of the amplifier will change dramatically. Detailed frequency dependence can be found in section F.3.

A noise figure of 1.5 dB can by LNA-standards not be considered low. In the PH25 process this value could very well be cut in half.[25] Still, amplifier IF1 is

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Table 4.2: Simulation results for amplifier IF1. Temperature at 25 °C and no parameter spread applied.

Parameter	Min.	Typ.	Max.	Unit
Frequency range		2.04–2.24		GHz
Gain	11.2	11.5	11.8	dB
Return loss input	12.1	14.4		dB
Return loss output	16.5	16.9		dB
Stability $K@0-80$ GHz	>1	>1		
P_{1dB} (input)	5.7	6.5		dBm
IIP_3	19.0	19.5		dBm
Power consumption		290	290	mW
Noise figure (estimate)		1.5	1.8	dB

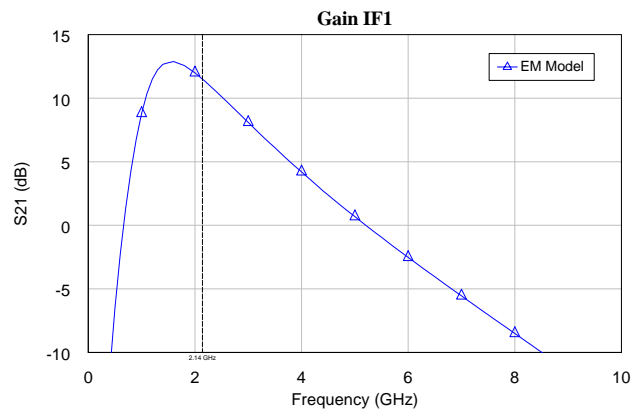


Figure 4.16: Gain of amplifier IF1.

not designed only to produce low noise, but also to have linear operation. This leads to a compromise in which the power-PH25 process without noise models is used.

4.4 High-power IF-amplifier

4.4.1 Introduction

The last amplification stage has together with the mixing component the biggest impact on the overall chip linearity. As discussed earlier, the more DC-power provided, the more linear the operation becomes. Because the signal has already been amplified once the overall noise figure is not very sensitive to the noise here. High power devices generate a lot of heat and this has to be taken into consideration.



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4.4.2 Design

Principle

To design a high linearity amplifier a method similar but opposite to the one used to design a LNA is used. Instead of matching the input to the noise optimum the output is matched to peak P_{1dB} . The first step is to create a stable and input-matched circuit. Feedback circuits are used to control the gain and the linearity of the amplifier. Using this amplifier load-pull simulations are made for different bias points. This way it's possible to see which bias point and output matching network give the most linear operation.[26]

Thermal considerations

Calculations performed on the FETs' junction temperatures show that in order to handle the available power and the specified ambient temperature there has to be two FETs. With only one $8 \times 75 \mu\text{m}$ FET the junction temperature T_j exceeds 170°C which is the maximum rating for a GaAs FET. T_j is calculated using thermal resistance models[27], where T_0 is set to 100°C :

$$T_j = T_0 + P_{FET} R_{TH} \quad (4.2)$$

P_{FET} is the power dissipated over the FET and R_{TH} is the FETs thermal resistance according to the models. T_0 , the temperature on the backside of the chip, is the sum of the ambient temperature and the estimated thermal resistance in the circuit board and the chip package. If the total thermal resistance is 15°C , the chip can handle an ambient temperature of $100^\circ\text{C} - 15^\circ\text{C} = 85^\circ\text{C}$.

With two $6 \times 75 \mu\text{m}$ FETs the maximum T_j becomes $\approx 150^\circ\text{C}$, which is a high although manageable temperature. Two FETs placed in parallel can be viewed as one big FET with the number of gate fingers equal to the sum of the parts, thus resulting in an equivalent $12 \times 75 \mu\text{m}$ FET.

Feedback and bias

The second IF-amplifier is biased in the same manner as the first one, described in subsection 4.1.3. This amplifier has both series feedback and parallel negative feedback. Though very small, the inductor on the source creating the series feedback is needed for stability and gain control. The parallel feedback that connects the drain to the source has an attenuating resistance and a capacitance for DC blocking. The purpose of this feedback is to simplify matching and to provide high bandwidth. Although the signal is of a single frequency it is preferable if not both amplifiers' gain are frequency sensitive. The parallel feedback also makes the amplifier less stable.

The FET's decrease in gain slightly as the temperature rises. To compensate for this loss a resistor of GaAs type is chosen for the parallel feedback. This resistor has a positive temperature gradient. This way the decrease in gain is reduced by the smaller feedback.

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4.4.3 Schematics and layout

The schematic of amplifier IF2 is shown in Figure 4.17. The corresponding layout is found in Figure 4.18.

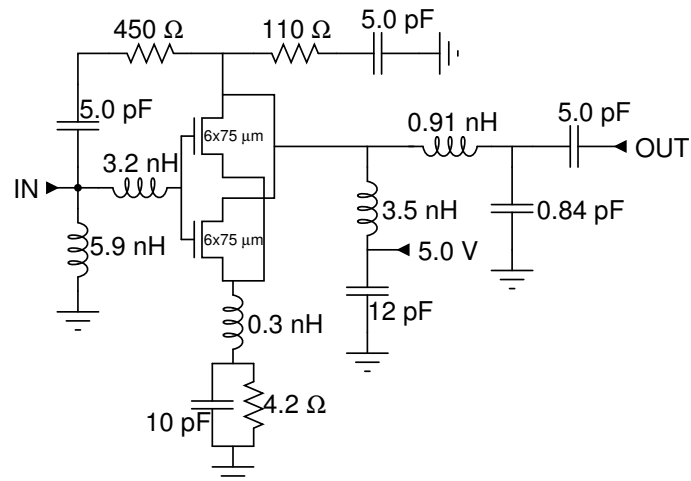


Figure 4.17: Schematic of amplifier IF2.

4.4.4 Simulation results

Performance overview

The simulated performance of amplifier IF2 is found in Table 4.3. Spread analysis is reported in section F.4 together with plots of the simulation data. The gain is plotted in Figure 4.19.

Table 4.3: Simulation results of amplifier IF2. Temperature at 25 °C and no parameter spread applied.

Parameter	Min.	Typ.	Max.	Unit
Frequency range		2.04–2.24		GHz
Gain	12.0	12.1	12.1	dB
Return loss input	24.9	25.5		dB
Return loss output	18.0	19.7		dB
Stability $K@0-70$ GHz	>1	>1		
P_{1dB} (input)	10.4	10.4		dBm
IIP_3	22.0	22.5		dBm
Power consumption		550	550	mW
Noise figure (estimate)		2.0	2.3	dB



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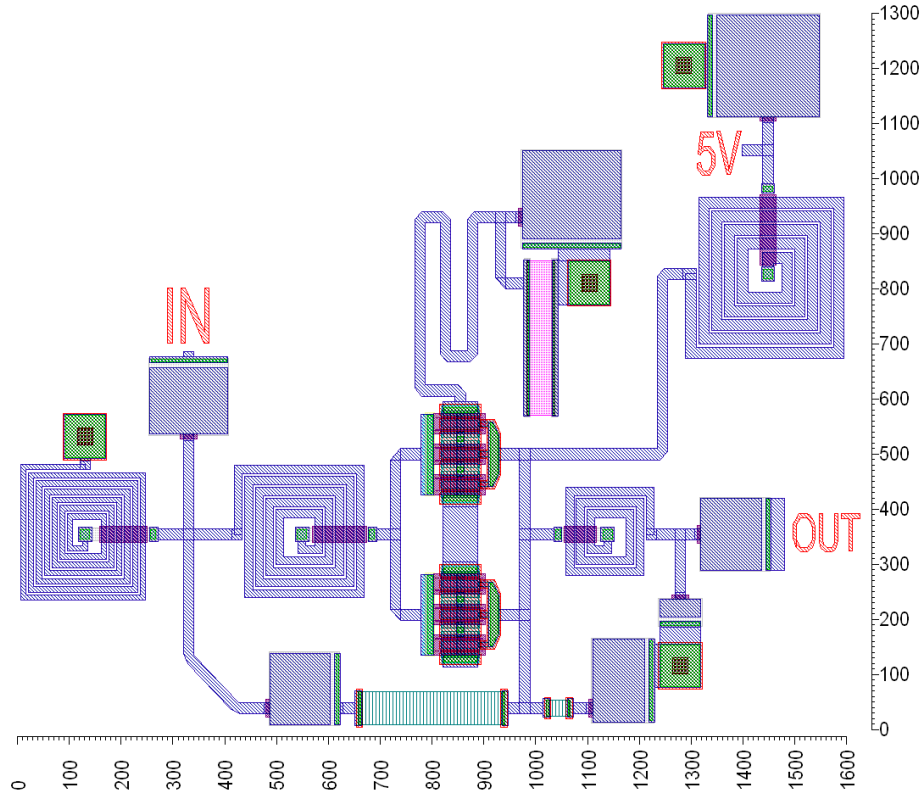


Figure 4.18: Layout of amplifier IF2. Dimensions in μm .

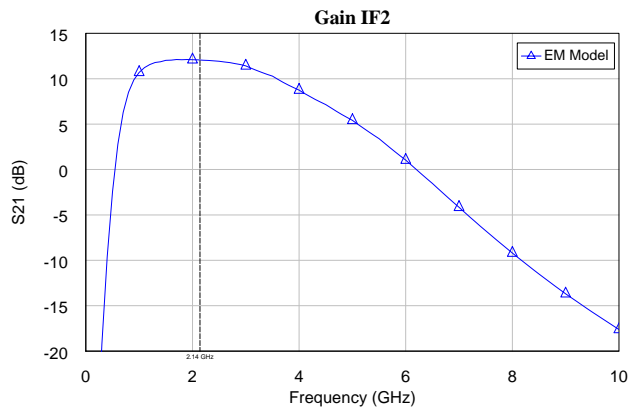


Figure 4.19: Gain of amplifier IF2.

Linearity analysis

The 1 dB-compression point, P_{1dB} , is simulated for different i_{ds} (Figure 4.20). A load pull analysis with both the output matching and P_{1dB} analysed is shown

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in Figure 4.21. The analysis shows the importance of choosing a correct, and in this case high power, bias point to optimize the two quantities. From the three plots combined it can be seen that the linearity increases dramatically with increased power until peak P_{1dB} is aligned with optimum output match. After that, the increase is only linear. This overall linearity increase agrees with the discussion about power utilisation in the introduction subsection 4.1.5.

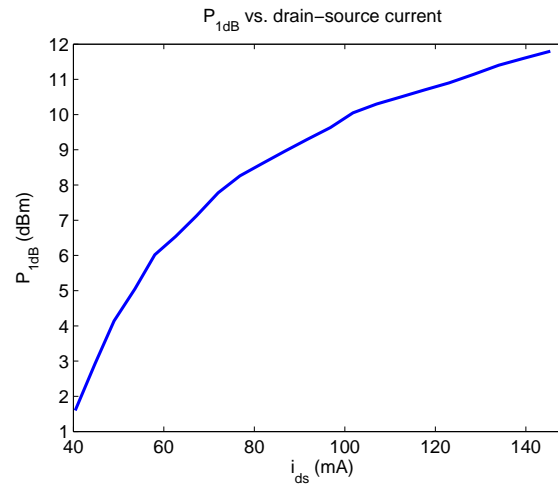


Figure 4.20: Amplifier IF2 P_{1dB} versus i_{ds} . The increase with increased power is non-linear in the beginning. From approximately 90 mA the increase is linear.

4.4.5 Discussion

The thermal limitations forced a two-FET amplifier design. This requires more space but effectively splits the source-drain current for each device in half. Another interesting observation is that the amplifier's linearity increased in the process. P_{1dB} increased with 4 dBm keeping the power consumption unchanged. The reason for this increase is attributed the same general reason why large devices are preferred over small when designing high-linearity class A amplifiers.

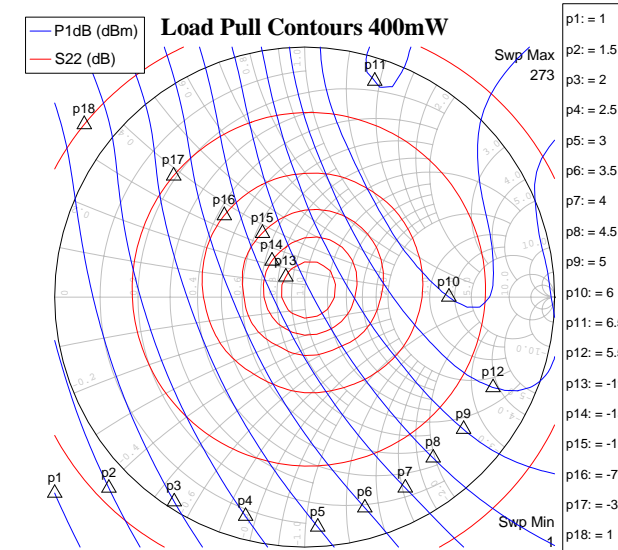
Even though the junction temperature in the FETs has been reduced dramatically with the dual-FET design, the asymmetric design with only one source network causes a large current to flow through the upper transistor. The FET connected to the source has the DC-current of the other transistor in the source. In these UMS FETs the source layers are connected with 14 μm air bridges. According to the maximum ratings these layers can only handle 7.5 mA/ μm . This gives a total of 105 mA and the design is just above that (110 mA). The three alternatives are either to reduce the current 5 mA, to widen the air bridge 1 μm or to route a common source for both FETs from the middle strip via an air bridge.

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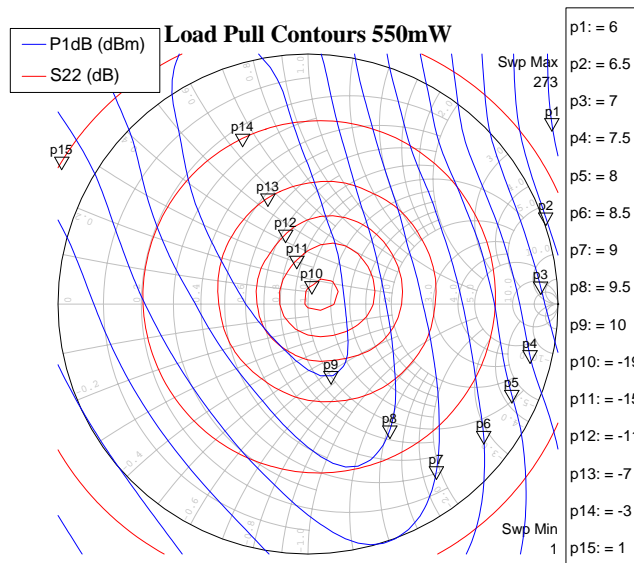
The implemented negative parallel feedback provides wider bandwidth and easier matching. The bandwidth may seem unnecessary considering the single frequency operation. However, as amplifier IF1 is designed with a steep gain slope it is preferable that this amplifier is not. This is due to the possibility of process variation in the frequency dependence. A variation within the current design limits most damage in performance to amplifier IF1.

The noise figure in the amplifier is approximately 0.5dB higher than in amplifier IF1. This shows that even though the input network is simpler, the parallel feedback will result in an increase in noise. Also, no effort has been made to match noise optimum with the input match in this amplifier.

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(a) Power consumption 400 mW corresponding to drain-source current 80 mA.



(b) Power consumption 550 mW corresponding to drain-source current 110 mA.

Figure 4.21: Load pull diagrams for optimal linearity (deformed contours) and optimal output matching (circular contours). The analysis is applied to a stable and matched amplifier with two $6 \times 75 \mu\text{m}$ FETs. The load pull diagrams show that devices biased in the most linear and high power region of the iv-curve (point C in Figure 4.2) not only give a higher 1 dB compression point overall but also a better match of the maximum P_{1dB} with the optimal output impedance match.



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Chapter 5

Variable attenuators

5.1 Introduction

The IF-signal output should preferably be fixed in power as well as in frequency for later digital to analog-converters to be effective. In order to adjust the signal to a given level, the gain from the amplifiers is slightly higher than needed which, combined with variable attenuators, creates a variable gain circuit.

5.2 Topologies

The simplest attenuator consists of a resistance that somehow interacts with the main RF line. Usually transistors are used to dynamically divert power into an attenuator, either into ground or back to the main line. This crude technique will however lead to relatively large reflections which is why slightly more sophisticated topologies are used. T- and Π -attenuators are common and offer small reflections, see Figures 5.1 and 5.2.

A fairly thorough discussion by Gustafsson and Westlund concludes that due to compact size and ease of control, the T-structure makes the best choice of attenuator.[10] The same arguments are valid for this circuit and process and thus the same type of attenuator is implemented. No notable differences are seen between PH25 and PPH25.

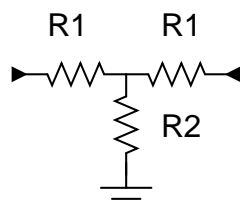


Figure 5.1: A tee-attenuator.

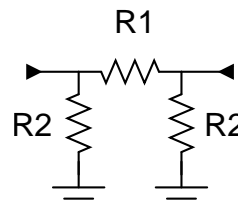


Figure 5.2: A pi-attenuator.

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5.3 Design

The values of the resistances R_1 and R_2 for the T-attenuator are given as [28]

$$R_1 = Z_0 \left[\frac{10^{A/20} - 1}{10^{A/20} + 1} \right]$$

$$R_2 = 2Z_0 \left[\frac{10^{A/20}}{10^{A/10} - 1} \right]$$

In order to control the attenuator, two FET's are added between the tee-pad and ground and in parallel with the tee-pad, see Figure 5.3. When V1 is closed and V2 open, there is no attenuation. Opening V1 and closing V2 forces the current to go through the resistances and partly into ground resulting in an attenuation.

The attenuators are biased by giving the source +5 V and switching the gate voltage between 3 V and 5 V. Therefore a DC-block must be added between V2 and ground in Figure 5.3.

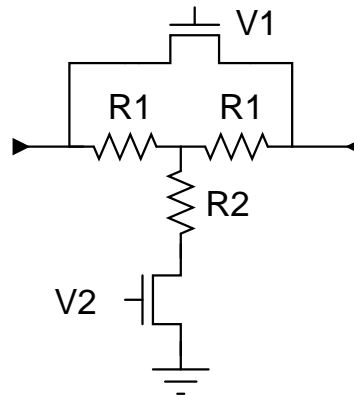


Figure 5.3: A tee-attenuator schematically. By switching the FETs, the gain is changed. When V1 is shorted and V2 open, the attenuator is not active. By reversing the voltages, the attenuator is activated.

The values of R_1 and R_2 are optimized to account for the extra capacitor and FET parasitics. The gates of the FETs are connected via high-value resistors to the control blocks. The high-value resistors are added to increase the FET's S_{21} in its closed state, see Figure 5.4. A $6\text{ k}\Omega$ resistance is chosen, as in the PH25-process.

5.4 Combining attenuators

Several techniques are available when combining attenuators to achieve a spectrum of discrete points. Attenuators can be connected in parallel or in series. A parallel connection results in a smaller total loss when all attenuators are

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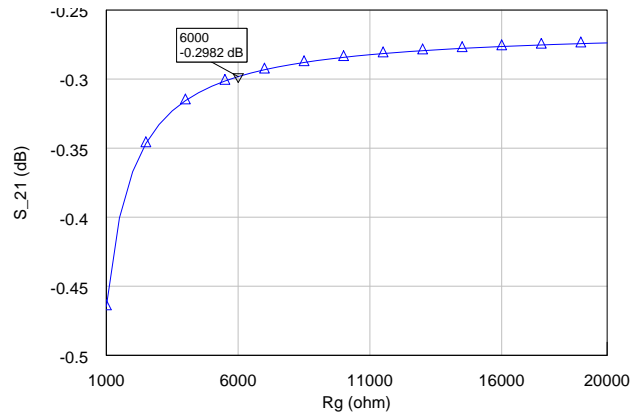


Figure 5.4: The inherent attenuation of the FET in its closed state, depending on gate impedance for the switching FET (PPH25SSW).

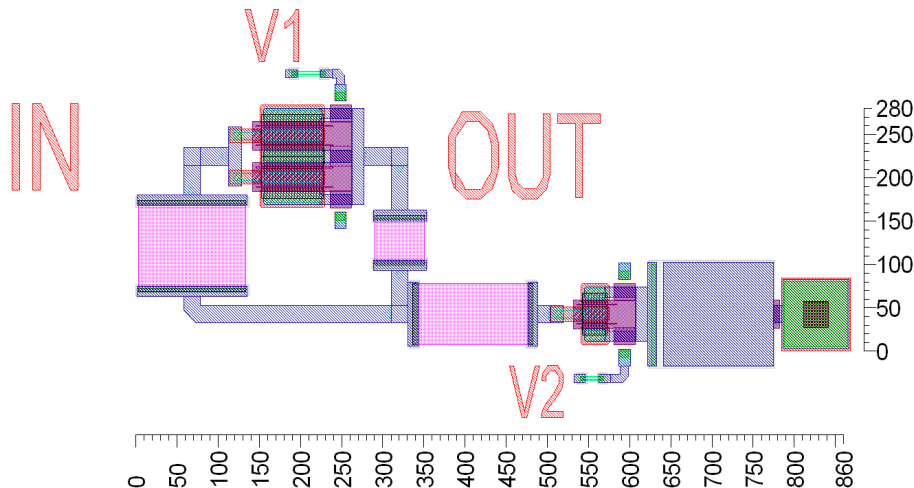


Figure 5.5: Layout of the 6dB-attenuator. A high-value resistor is connected to the gate of the FETs. Dimensions in μm .

inactive, i.e. when maximum gain is sought. This is because of the inherent drain-source resistance in the transistors used for overriding the attenuators. When connecting attenuators in parallel, the total loss is smaller in their inactive state but there are fewer possible states of attenuation.

As maximizing the number of controlling bits and thereby saving chip-size is deemed important, it is decided to use a series design of the attenuators. Furthermore, a resolution of 1.5 dB and a total of 3 bits suffices. This gives $2^3 = 8$ steps and a maximum attenuation of $1.5 + 3 + 6 = 10.5$ dB.

The entire attenuator-circuit must be properly biased. Therefore there are

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DC-blocks before and after the attenuators. The entire line is raised to +5 V by connecting the bias-voltage through a high-resistance element serving as IF-block (Figure 5.6).

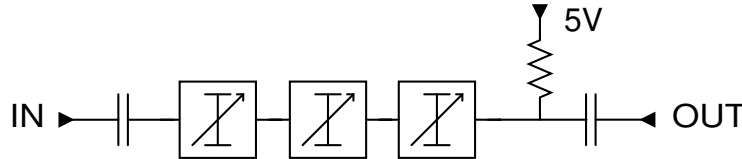


Figure 5.6: The three attenuators with DC-blocks raised to 5 V so that the FETs are properly biased. The attenuators are controlled by level-shifters as explained in the following chapter.

5.5 Results

When simulating the attenuators, there is the option of using a linear model of the switching FET called PPH25SSW or the non-linear cold FET called PPH25NCF. The non-linear models are more powerful in that they can be used in non-linear simulations but the linear switching FET models approximate linear operation better. The simulations are performed with PPH25SSW as far as possible.

The attenuation values and reflection coefficients for all attenuators are displayed in Table 5.1. All attenuation states, including spread are seen in Figure 5.7. The compression point, P_{1dB} , for the complete variable-gain-circuit (three attenuators in series) is calculated to 22 dB using PPH25NCF when all attenuators are in their inactive state. All other states result in higher P_{1dB} .

Table 5.1: Simulated attenuator data for PPH25SSW.

Attenuator	$S_{21,\text{diff}}$	$S_{21,\text{off}}$	S_{11}, S_{22}
1.5 dB	1.5 dB	0.36 dB	>25 dB
3 dB	3.0 dB	0.34 dB	>25 dB
6 dB	6.1 dB	0.35 dB	>21 dB

5.6 Attenuator control

5.6.1 Introduction

The attenuators are controlled by applying either 5 V or 3 V to the FET's gates, thereby switching them between completely on and completely off. This is the task of the so called level shifters. The level shifters take as input a binary zero (0-4 V) or one (1.8-5 V), adhering to the standardized LvTTL-logic.[29]



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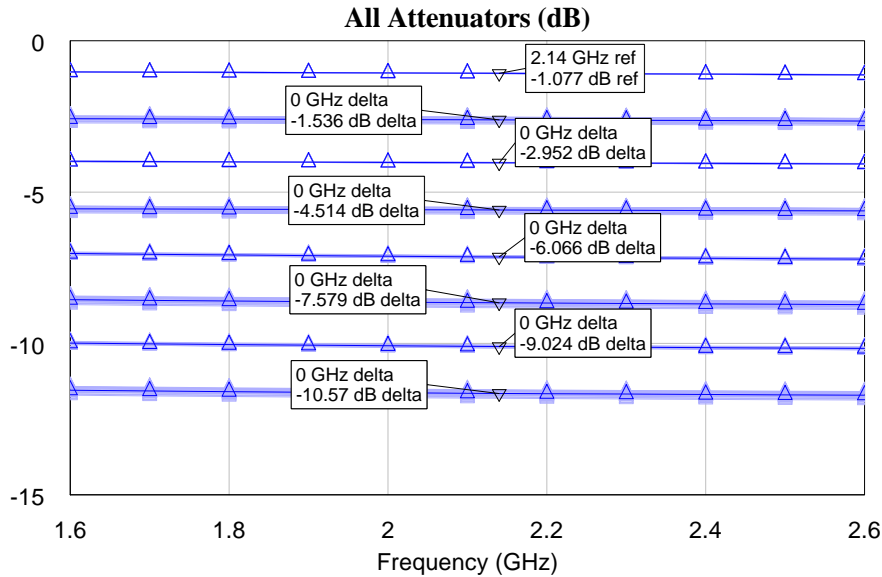


Figure 5.7: Spread for all gain states using PPH25SSW.

This technique is well established at SAAB and there are existing models for the PH25-process[10]. The level shifters are implemented again in PPH25 without any major changes.

5.6.2 Design

The schematic and real layout for the level shifter are seen in Figure 5.9 and Figure 5.10, respectively. In short, $v_{control}$ directly controls T_1 . When T_1 is closed, $v_1 = 3\text{ V}$ as the bias voltage will split over R_2 and R_6 . This in turn will cause T_2 to open, making $v_2 = 5\text{ V}$. As $v_{control}$ is decreased, T_1 will eventually open, making $v_1 = 5\text{ V}$. As there will no longer be any current over R_6 , v_{gs} over T_2 will decrease, and T_2 will close, making $v_2 = 3\text{ V}$.

The level shifter's output is shown in Figure 5.11a. By adjusting the two resistances between $V_{control}$ and ground in the circuit, the voltage at which the attenuator is turned on, V_{shift} is adjusted. Also, the current consumption can be decreased by increasing the remaining resistances. However, there comes the penalty in the form of increased size. See Figure 5.11b for the current consumption.

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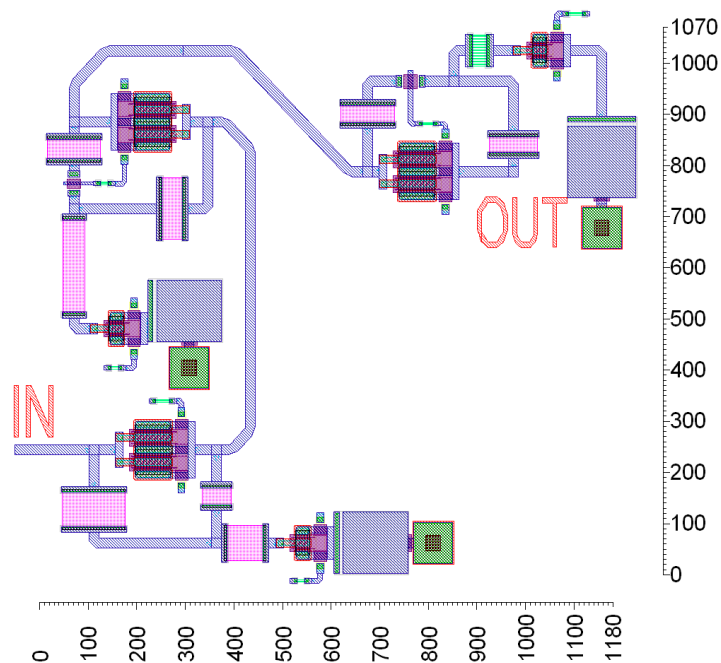


Figure 5.8: The complete attenuator circuit. Dimensions in μm .

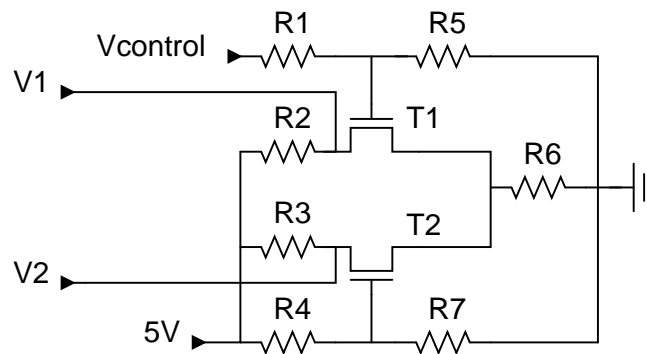


Figure 5.9: Schematic of the level-shifter used for biasing the attenuators. $T_1, T_2 = 1 \times 25 \mu\text{m}$, $R_1 = 1.0 \text{ k}\Omega$, $R_2 = 2.1 \text{ k}\Omega$, $R_3 = 3.3 \text{ k}\Omega$, $R_4 = 20 \text{ k}\Omega$, $R_5 = 6.2 \text{ k}\Omega$, $R_6 = 3.0 \text{ k}\Omega$ and $R_7 = 5.0 \text{ k}\Omega$.



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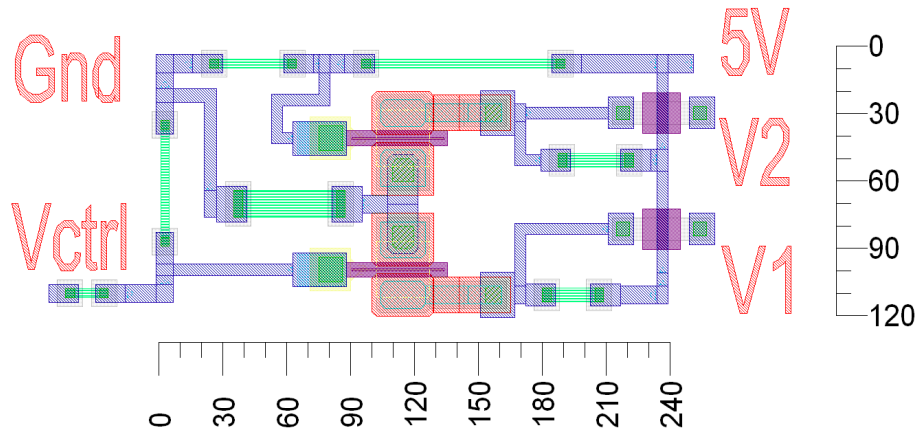
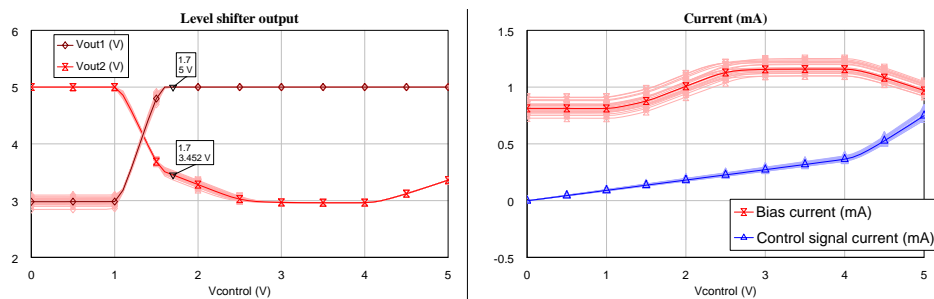


Figure 5.10: The layout on-chip for the level shifter used for biasing the attenuators.



(a) Level shifter output with yield analysis.

(b) Level shifter current consumption with yield analysis.

Figure 5.11: (a) Voltages generated by the level shifter and (b) current consumption as a function of the control signal.



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Chapter 6

Chip Summary And Final Conclusions

The complete circuit design is the final product of this work. It is based on the three previous chapters explaining the design of the chip's individual components. This chapter explains the final layout with connecting pads and lists the final full-chip simulations. The chip is compared to design specifications and potential improvements are discussed. The report is wrapped up with some final conclusions.

6.1 Layout

The complete chip is designed to fit into a 4×5 mm QFN-package (Figure 6.1). The chip components are placed according to a few requirements:

First of all, the incoming RF- and outgoing IF-port should ideally be placed on opposite sides of the chip. In order to avoid interference, it would be preferable to have the LO-port on one of the remaining sides. Early on, a straight signal path was favored over more complex choices although this wasn't really a requirement and was relaxed as the chip-layout matured.

The diplexer is a big sub-circuit and rather significant to the entire chip-function and at large decides the placement of other circuits on the chip. The LO-amplifier is quite small and connects straight to the mixer. The remaining subcircuits: Two IF-amplifiers and three attenuators are adjusted to fit together.

The final layout has the RF-port and IF-port on opposite short sides of the chip coupled with ground-pads. No other pads are placed on the short sides to keep the bonding wires isolated. The LO-signal and two bias-signals for the mixer and LO-amplifier respectively are connected on one of the long sides. The bias-signals for the two circuits are separated and isolated with two grounded pads. This gives the possibility of biasing the mixer and/or the amplifier with signals different from 5 V in the future.



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On the remaining long side, three 5 V bias-signals for the IF1-, IF2-amplifiers and the attenuator-circuit enters, as well as three control-signals for the attenuators.

Grounded pads are placed next to the major bias-pads. They are put there in order to make accurate measurements of the naked chip. These pads are however not connected to exterior bonding pads for the packaged chip.

6.2 Performance

6.2.1 Summary

Summary of simulated chip performance at nominal gain (Table 6.1), maximum gain (Table 6.2) and minimum gain (Table 6.3).

Table 6.1: Summary of chip performance at nominal gain. LO drive at -2 dBm. Temperature at 25 °C and no parameter spread applied.

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Frequency range RF		2.9–3.4			3.1–3.3		GHz
Frequency range LO		5.04–5.54			5.24–5.44		GHz
Frequency IF		2.14			2.14		GHz
Return loss RF	14	16		20	21		dB
Return loss LO	13.5	17		17	18		dB
Return loss IF	23	24		23	24		dB
Conversion gain	10.3	10.6	10.8	10.7	10.8	10.8	dB
Gain variation		0.45	0.45		0.05	0.05	dB
Image rejection	48	50		50	51		dB
P_{1dB} (input)	9.8	10.0		9.8	10.0		dBm
IIP_3 (estimate)	20	20		20	20		dBm
Noise figure (estimate)		11	11		11	11	dB
Power consumption		1.0	1.0		1.0	1.0	W

6.2.2 Return loss

The return losses at the RF- and LO-ports are simulated and found to be very similar as those simulated for the individual components. The results are listed in the chip summary but for detailed frequency characteristics see Figure 3.6 for the RF-port and Figure 4.9 for the LO-port. The IF-port's return loss depends on the gain setting and is found to be at least 21 dB in all cases with a 100 MHz bandwidth.

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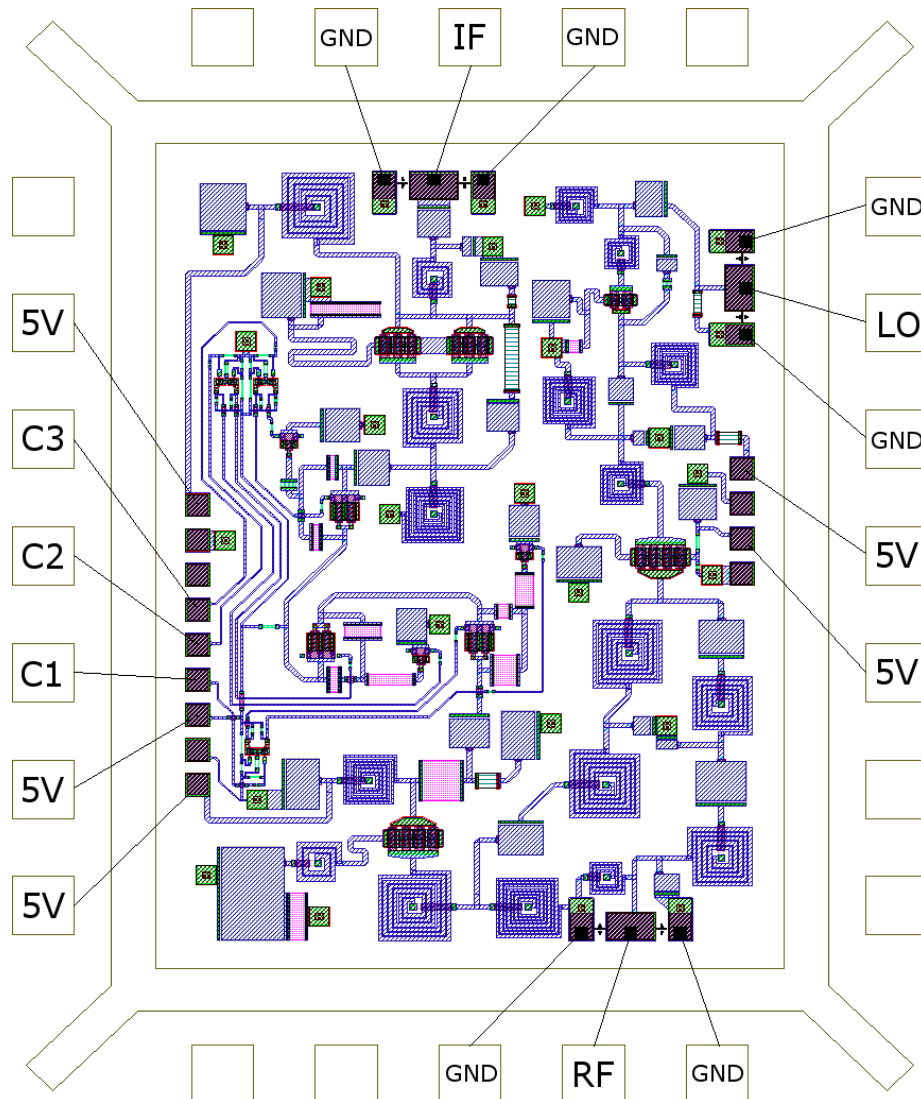


Figure 6.1: Layout of the MMIC and labels of the bonding pads. The size of the final package is 4×5 mm. The effective chip area containing all components is 2.3×3.3 mm. C1, C2 and C3 provide the control signals for the 6 dB, 3 dB and 1.5 dB attenuators respectively.

6.2.3 Conversion gain

The chip's conversion gain is simulated for all gain states in Figure 6.2 and for different LO drives in Figure 6.3.

The IF signal has a narrow bandwidth. Even so, the 20 MHz on the MMIC



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Table 6.2: Summary of chip performance at maximum gain (+4.5 dB). Only parameters which performance has changed compared to the case with nominal gain are presented. LO drive at -2 dBm. Temperature at 25 °C and no parameter spread applied.

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Frequency range RF		2.9–3.4			3.1–3.3		GHz
Return loss IF	29	31		29	31		dB
Conversion gain	14.7	15.0	15.2	15.1	15.2	15.2	dB
P_{1dB} (input)	6.6	6.7		6.6	6.7		dBm
IIP_3 (estimate)	17	17		17	17		dBm
Noise figure (estimate)		10	10		10	10	dB

Table 6.3: Summary of chip performance at minimum gain (-6.0 dB). Only parameters which performance has changed compared to the case with nominal gain are presented. LO drive at -2 dBm. Temperature at 25 °C and no parameter spread applied.

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Frequency range RF		2.9–3.4			3.1–3.3		GHz
Return loss IF	21	22		21	22		dB
Conversion gain	4.3	4.6	4.8	4.7	4.8	4.8	dB
P_{1dB} (input)	11.3	11.5		11.3	11.5		dBm
IIP_3 (estimate)	21	21		21	21		dBm
Noise figure (estimate)		13	13		13	13	dB

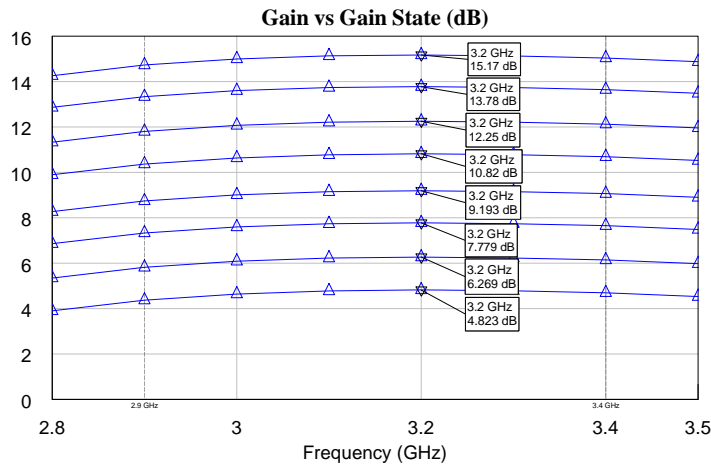


Figure 6.2: Chip gain versus frequency for all gain states. $P_{Lo} = -2$ dBm. The least significant bit (LSB) is 1.55 dB and the dynamic gain is 10.3 dB.



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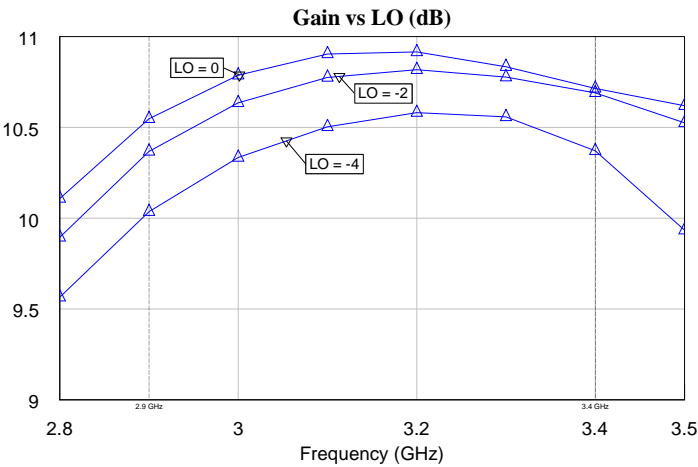


Figure 6.3: Chip gain versus frequency for different LO drives at nominal gain. The gain variation is kept below 0.6 dB between 2.9 and 3.4 GHz for $P_{lo}=-4$ to 0 dBm.

that it does occupy exhibits a frequency dependent gain according to Figure 6.4. This plot is also interesting, should the frequency characteristics in the IF-path shift.

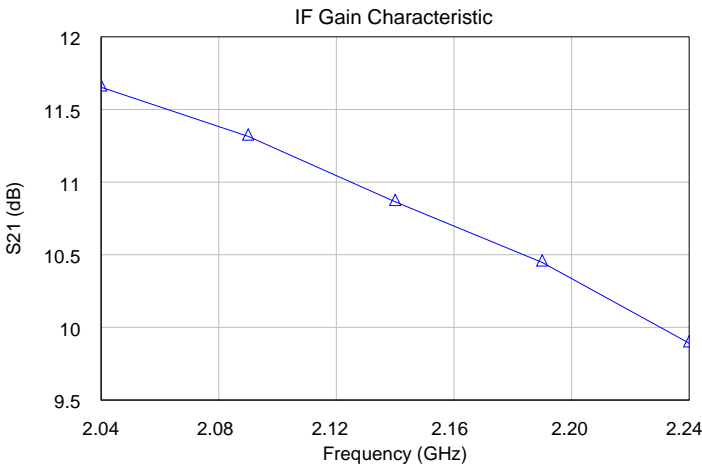


Figure 6.4: IF-frequency dependent chip gain. The gain variation in the 20 MHz wide IF band is 0.2 dB



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6.2.4 Linearity

Chip P_{1dB} for different gain states and LO drives are plotted in Figure 6.5. The linearity is as expected highest for minimum gain and lowest for maximum gain. P_{1dB} tends to drop for smaller LO-drives.

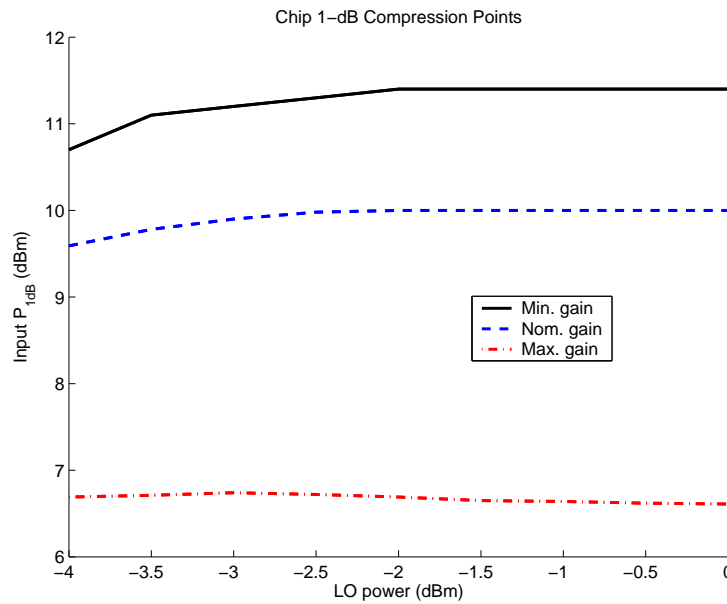


Figure 6.5: Chip P_{1dB} for different gain states versus input LO power.

6.2.5 Spectrum and spurious frequencies

The frequency spectrum from 0 to 10 GHz at the output IF port is shown in Figure 6.6.

6.2.6 Maximum rating

All the components are scaled to survive a maximum input power level of $P_{RF} = 17$ dBm. This is the maximum power the circuit prior to this mixer chip is able to deliver. The major concerns are the resistors' widths and the width of the microstrips. The sizes are scaled according to UMS specifications.[9]

Transistors may not survive if the junction temperature becomes too high. The FETs in the IF-amplifiers run the risk of overheating due to their large current consumption. They are designed to survive a maximum chip backside temperature of 100 °C which is thought possible in the event of starting the system in a warm dessert for example.

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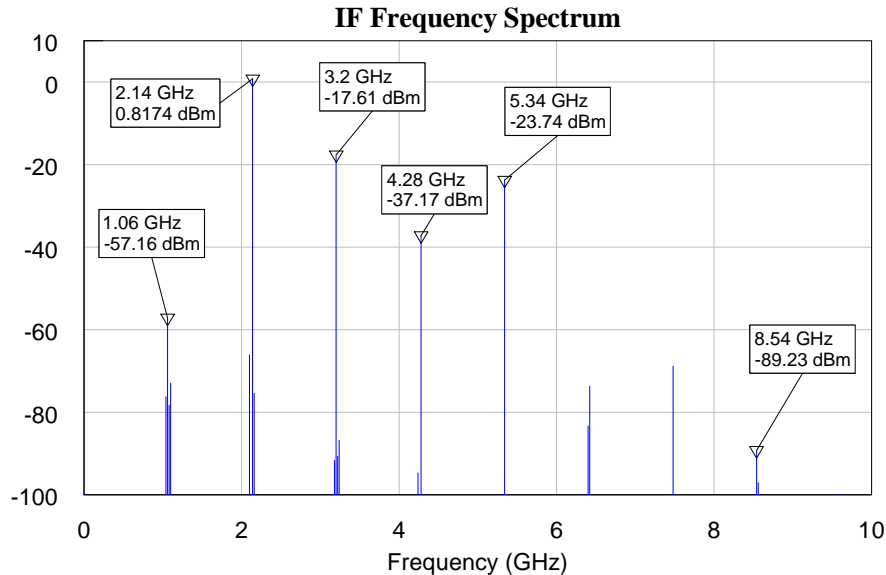


Figure 6.6: Frequency spectrum at the output IF-port for input frequency 3.2 GHz, $P_{io} = -2$ dBm and nominal gain. Noteworthy components are: IF (2.14 GHz), RF (3.2 GHz), LO (5.34 GHz), $2 \times$ IF (4.28 GHz), RF-IF (1.06 GHz) and RF+IF (8.54 GHz). The LO isolation is 21 dB, which is just above the required level of 20 dB. The $2 \times$ IF-signal suppression is 38 dBc, which is 2 dB below the required value. The RF-signal has only 7.6 dB isolation. Some of the smaller components are spurious frequencies predicted in Table 1.1.

6.3 Temperature and yield analysis

6.3.1 Components

Components are affected by temperature as well as production spread. An analysis of the chip performance for different temperatures and yields has been performed. The chip is required to keep its performance between -40°C and 55°C and to function up to 85°C .

The temperature dependence arise mostly in the TiWSi- and GaAs-resistors where the resistance differs $\sim 10\%$ as temperature goes from 20°C to 85°C . The FETs have a temperature dependence as well but the PPH25 models only allow simulations at 20°C . Some qualitative arguments can be made by reviewing PH25 FET performance. The gain in PH25 FETs have approximately a $-0.2\%/K$ dependence and this is believed to hold for PPH25 as well considering how similar the processes are. This gives an extra gain of 0.5 dB at -40°C and decreases the gain of each FET with 0.25 dB at 55°C .



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6.3.2 Conversion gain

The entire chip's conversion gain is simulated for temperatures between -40°C and 85°C (Table 6.4). The conversion gain increases slightly as temperature increases to 85°C . It is believed that the unaccounted temperature dependence of the FET's gain has a reverse effect on the increased chip gain.

By taking temperature, yield and the FET's temperature dependence into account, the minimum and maximum chip conversion gain is 9.4 dB at 55°C and 12 dB at -40°C , respectively. This is at the nominal gain state.

Table 6.4: Chip conversion gain with yield analysis at nominal gain. The simulation is performed with circuit models where the resistors are adjusted for temperature. PPH25 FET models can only be simulated at 20°C and the decreased gain of the FETs at higher temperatures is therefore not included.

Temperature	Conversion gain
-40°C	$10.0 \pm 1 \text{ dB}$
20°C	$10.6 \pm 1 \text{ dB}$
55°C	$10.9 \pm 1 \text{ dB}$
85°C	$11.3 \pm 1 \text{ dB}$

6.3.3 Compression point

The 1 dB-compression point could not be successfully simulated using circuit-models and therefore a qualitative argument must be made using performance of subcircuits and theory.

Since the gain of the FETs decrease with temperature, it can be argued that the IF-amplifiers' compression-points will not decrease at higher temperatures. The LO-amplifier loses 0.4 dB of gain at 55°C due to its TiWSi-feedback loop and reduced FET-gain which may affect the mixer P_{1dB} with as much. This does not affect the chip compression point by more than -0.1 dB at nominal gain. It is therefore probable that higher temperatures will not affect the chip compression point more than -0.1 dB.

At temperatures close to -40°C , the gain of each FET increases with 0.5 dB. As a side effect, the IF-amplifiers' compression-points decrease with 0.5 dB which decreases the chip compression point with -0.2 dB according to the cascade formulas, Equation 1.3. The positive effect of having a larger LO drive is unaccounted for. This analytical approach results in the chip's compression point being rather temperature-invariant. The yield analysis shows a smallest mixer P_{1dB} of 10 dB at $P_{lo} = -4 \text{ dBm}$. With a 0.5 dB and 0.5 dB decrease in P_{1dB} for the IF-amplifiers respectively, the effect on the chip's 1 dB-compression point is a decrease of 1 dB at nominal gain.

By using the yield analysis of sub-circuits and an analytical temperature analysis, the chip P_{1dB} is believed to lose $\sim 1 \text{ dB}$ at -40°C .

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6.4 Discussion

6.4.1 Comparison to design specifications

In Tables 6.5 and 6.6 is a comparison between design specifications and the simulated chip performance shown. The nominal gain is approximately 1 dB higher than specified. This is acceptable, considering that the dynamic gain range is 10.5 dB and that the gain empirically is lower than simulated.

Table 6.5: Achieved performance compared to design specifications for frequencies 3.1–3.3 GHz. For many parameters there is no target specification and the entry is left blank. Explanations and exceptions are listed at the bottom.

Parameter	Specification		Result	
	Required	Target		
Temp. function	-40–+85 °C		-40–+85 °C	✓
Temp. performance	-40–+55 °C		-40–+55 °C	✓
LO input power	-5–0 dBm		-4–0 dBm	–
Nominal gain	8–10 dB		10.5 dB	✓
Gain variation	≤ 0.6 dB		0.05 dB	✓
Gain control	≥ ±5 dB		-6.0 to +4.5 dB	✓
Noise figure	≤ 15 dB	≤ 12 dB	11 dB [*]	✓
Return loss RF	≥ 15 dB		21 dB	✓
Return loss IF	≥ 15 dB		24 dB	✓
Return loss LO	≥ 15 dB		14 dB [†]	–
IIP_3	≥ 15 dBm	≥ 17 dBm	20 dBm [‡]	✓
LO to IF isolation	>20 dB		21 dB	✓
Image rejection	>30 dBc		40 dBc	✓
RF+LO suppression	>40 dBc		90 dBc	✓
Other mixing spurs	>40 dBc		38 dBc [§]	–
Max input power RF	17 dBm		17 dBm	✓
Bias	+5 V		+5 V	✓
Power consumption	<1.5 W	<1.0 W	1.0 W	✓
Control signals	2.5–3.3 V		2.5–3.3 V	✓
Package	4×4, 4×5 or 5×5 mm		4×5 mm	✓

^{*} For nominal gain. $NF = 13$ dB at minimum gain.

[†] For $P_{LO} = -4$ –0 dBm.

[‡] For nominal gain. $IIP_3 = 17$ dB at maximum gain.

[§] 2×IF at 4.28 GHz.

6.4.2 Linearity

The chip linearity at nominal gain is measured to $P_{1dB} = 9.8$ dBm with the RF-signal at 3.2 GHz. This frequency, the center frequency, has the lowest conversion



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Table 6.6: Achieved performance compared to design specifications. Parameters listed have different result for frequencies 2.9–3.4 GHz compared to the narrower band 3.1–3.3 GHz. The others are listed in Table 6.5.

Parameter	Specification		Result
	Required	Target	
LO input power	-5–0 dBm		-4–0 dBm –
Gain variation	≤ 0.6 dB		0.6 dB ✓
Return loss RF	≥ 15 dB		16 dB ✓
Return loss LO	≥ 15 dB		10 dB* –

* For $P_{LO} = -4-0$ dBm.

loss and noise and therefore also the lowest P_{1dB} (as shown in Figure 3.8). Using the estimate that $IIP_3 = P_{1dB} + 10$ dBm the final IIP_3 becomes approximately 20 dBm. This is far above the target set at 17 dBm.

The high P_{1dB} is needed to provide linear operation even when there is little or no attenuation in the gain block. In the worst case (maximum chip gain) P_{1dB} becomes 6.6 dBm. Using the same estimate, IIP_3 turns out to be slightly less than 17 dBm.

Furthermore, the full chip simulations resulted in a P_{1dB} 2 dBm higher than the one calculated using the results from the individual components. This discrepancy is explained by the dynamics of the entire chip working together. Spurious and harmonic frequencies earlier only simulated in the mixer component are now present everywhere. Also, if there is a mismatch between two components this loss will increase P_{1dB} . This will unfortunately also increase the noise figure.

The simulation software cannot provide high enough accuracy needed to perform the three-tone simulation (f_{RF1} , f_{RF2} and f_{LO}) necessary for IIP_3 , why estimates from P_{1dB} -simulations are used instead. Some full-chip, low accuracy IIP_3 simulations are however made for reference and they show a ~3 dBm better result than the estimates using P_{1dB} . Due to their uncertainty, these results are not listed above. It is interesting to see which results the manufactured chip will adhere to.

6.4.3 Noise

As PPH25 noise models are unavailable, the noise figure for the individual components are estimated using various methods. The reliability of these noise figures is quite high. Contrary to measuring P_{1dB} on the full chip, noise cannot be simulated but must instead be calculated using a formula similar to the one used for IIP_3 (subsection 1.6.4). Calculating IIP_3 this way gives a 2 dB discrepancy from the complete chip simulation. There is a possibility that this discrepancy in present also in the case of the noise. It is therefore hard to say if the final noise figure result is as reliable as the individual components'.



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6.5 Conclusions

6.5.1 Achievements

The simulations show that the chip performs well, comparing performance to the specifications. Except for some input matching and input power issues at the LO port all required and targeted goals are met. Chip IIP_3 is 3 dB above the targeted performance and the noise figure NF is 1 dB below the target.

6.5.2 Possible improvements

RF-to-IF isolation in the chip is rather weak, only 7.6 dB at nominal gain. There is no required level of isolation specified but a RF-signal at the output only 18 dB lower than the IF-signal can be considered large. In order to increase the isolation the filtering structure after the mixing FET has to be improved. Components part of this structure are the low-pass filter in the diplexer and the two IF-amplifiers. This is not an easy task as the RF lies close to the IF in frequency. The isolation would be even worse if the first IF amplifier would have wider bandwidth and thus higher gain at the RF frequency (which is possible with parallel feedback).

The high linearity can be traded for lower DC power consumption, if such an interest exists. The present DC power consumption is just below the target of 1.0 W. The final IF-amplifier is the part consuming most power in order to achieve high linearity. Decreasing i_{ds} and thereby the power consumption for this amplifier will reduce overall chip IIP_3 . Since the IIP_3 is as high as it is, it might therefore be interesting to cut back on the power.



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Appendix A

Glossary

AESA	Active electronically scanned array.
Balun	Balanced to unbalanced transition.
dBc	Decibels relative to the carrier.
dBm	Power in decibels relative to 1 mW.
DC	Direct current.
EXR	Exciter receiver. Middle part of the receiver system.
FET	Field effect transistor.
GaAs	Gallium arsenide.
IF	Intermediate frequency. Name of the down-mixed frequency.
IIP_3	Third-order intercept point referenced to the input power.
IP_3	Third-order intercept point. A linearity measurement.
MIM capacitor	A metal-insulator-metal capacitor.
MMIC	Monolithic microwave integrated circuit.
NF	Noise figure. A measure of a component's noise.
LO	Local oscillator. The outside signal the RF mixes with to produce the IF.
LVTTL	Low voltage transistor-transistor logic.
OIP_3	Third-order intercept point referenced to the output power.
P_{1dB}	1 dB compression point. Referenced to either the input or the output power.
PH25	Low noise pHEMT 250 nm UMS foundry process.
PPH25	Power pHEMT 250 nm UMS foundry process.
pHEMT	Pseudomorphic high electron mobility transistor.
RF	Radio frequency. The incoming radar signal.
S band	Frequencies 2–4 GHz in the electromagnetic spectrum.
TaN resistor	Tantalum nitride resistor.
TiWSi resistor	Titanium(IV) tungstosilicate resistor.
TRM	Transmitter receiver module.
TTL	Transistor-transistor logic.
UMS	United monolithic semiconductors. A GaAs foundry.



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Appendix B

Design Specifications

Table B.1: Specification of the MMIC's features.

Parameter	Requirement	Comment
Radio frequency (RF) range	3.1–3.3 GHz	Study: 2.9–3.4 GHz
Temperature range (function/performance)	-40–+85 °C/ -40–+55 °C	
Intermediate frequency (IF)	2.14 GHz	
Local oscillator (LO) range	RF+IF	
LO input power	-5–0 dBm	
Nominal gain	8–10 dB	
Gain variation over frequency	≤ 0.6 dB	
Gain control	≥ ±5 dB LSB: * ≤ 2 dB	3 or 4 bits
Noise figure (nominal gain)	≤ 15 dB	Target: ≤ 12 dB
Return loss (all gain states)	≥ 15 dB	
IIP_3 (nominal gain)	≥ 15 dBm	Target: ≥ 17 dBm
LO to IF isolation	> 20 dB	
Image rejection	> 30 dB	
RF+LO product (@RF=-10 dBm)	<-40 dBc	
Other mixing spurs (@RF=-10 dBm)	<-40 dBc	
Max input power RF	17 dBm	Survival
Bias	+5 V	Single bias
Power consumption	≤ 1.5 W	Target: ≤ 1.0 W
Control signals	2.5–3.3 V	Parallel interface
Package	Plastic mold QFN [†] (4×4, 4×5 or 5×5 mm)	

* Least significant bit

[†] Quad flat no leads

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Appendix C

UMS Process Evaluation

C.1 Introduction

The system design motivated in chapter 2 is chosen as the design most likely to meet the target specifications (Appendix B). As UMS is the foundry service that the chip is designed for, a lot of the input data for the system design is based on empirical knowledge from earlier designs with the same foundry. UMS does however have several processes to choose from. Of interest are the PH25 (low noise pHEMT; $0.25\ \mu\text{m}$ gate length) and PPH25 (power pHEMT; $0.25\ \mu\text{m}$ gate length) processes.

Initial design is based on the low noise PH25 process. As high linearity is prioritized and because the performance profit from high power, PPH25 is considered. To determine the most suitable process an evaluation is carried out to compare the two.

C.2 Estimated performance

C.2.1 Mixer

Ideal mixers using FETs from both processes are simulated. The purpose of using an ideal setup is to have the FET as the only parameter affecting the outcome. Both the conversion gain and P_{1dB} are calculated. It turns out that the conversion gain is unaffected by the choice of process while P_{1dB} is generally 1 dB higher for PPH25 than for PH25 (Figure C.1).

C.2.2 Amplifier LO

Since neither low noise nor high power is of importance for the LO-amplifier, the choice of process has little effect.



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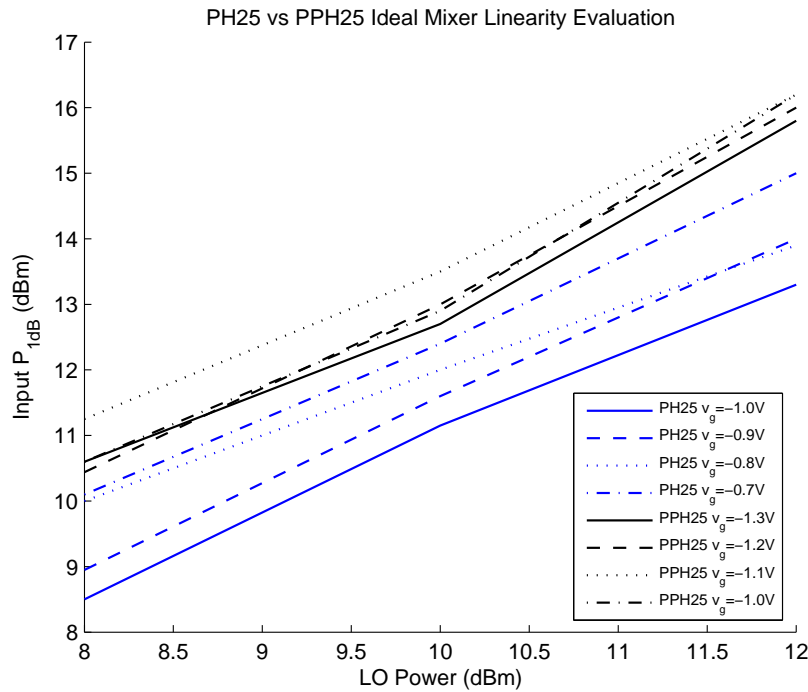


Figure C.1: P_{1dB} for an ideal FET resistive mixer for both PH25 and PPH25. P_{1dB} is generally 1 dB higher for PPH25.

C.2.3 Amplifier IF1

Amplifier IF1 does not use the amount of power that motivates the use of PPH25. The noise does however depend on the process choice. As explained in section 4.3.2 there are no noise models for the PPH25 process. However, the noise level is through measurements estimated to be approximately 0.5 dB higher for PPH25 than for PH25.

C.2.4 Attenuators

The loss in the attenuator-FETs are marginally less for PPH25 than for PH25. The difference is at most 0.1 dB per FET. As the attenuators are placed after the first amplifier the affect of these losses on the system's total noise figure is small.

C.2.5 Amplifier IF2

The main reason for considering PPH25 is to increase power of the last amplifier (subsection 4.4.1). The maximum DC current in an inductor for PH25 is merely

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44 mA.[30] The same value for PPH25 is 130 mA.[9] The RF-choke in the bias network requires an inductor to prevent the RF-signal from escaping. A work-around for PH25 would be to create an inductor out of a long microstrip. This is however space inefficient as an inductor of this kind at 2.14 GHz would become large.

A PH25 amplifier biased at $i_{ds} = 44$ mA gives $P_{1dB} \approx 3$ dBm. The equivalent PPH25 amplifier used in the final design biased at $i_{ds} = 110$ mA gives $P_{1dB} \approx 10$ dBm. Both have gain ≈ 12 dB.

C.2.6 System summary

Table C.1 states the final performance for a system with PH25 and for a, besides the FET, equivalent system with PPH25. Estimates are made for both the extreme gain cases as well as the nominal gain. The system design i.e. the choice and order of components are the same as the one chosen for the project (Table 2.2).

Table C.1: System performance for PH25 and PPH25 at different gain states. As the UMS components don't support multi-tone (IIP_3) analysis it is assumed that $IIP_3 = P_{1dB} + 10$ dBm for the mixer and $IIP_3 = P_{1dB} + 11$ dBm for the amplifiers. These estimates are considered conservative.

	Nominal Gain		Gain: +5 dB		Gain: -5 dB	
	PH25	PPH25	PH25	PPH25	PH25	PPH25
Gain	9 dB	9 dB	14 dB	14 dB	4 dB	4 dB
NF	11.4 dB	11.8 dB	10.5 dB	11.0 dB	13.3 dB	13.6 dB
IIP_3	15.8 dB	19.7 dB	12.2 dB	17.7 dBm	18.2 dBm	20.6 dBm

C.3 Conclusion

From Table C.1 one can see that even though the PPH25 process suffers from ~ 0.5 dB higher noise figure it is vastly more linear.

For the first component in a receiver chain, where low noise is of utter importance, PH25 is the better choice. At least until the noise level in the PPH25 process can be confirmed and real noise models can be used in the design process. In this stage however, the first downconverter, the noise is not that important and the PPH25 power features makes it a better option.

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Appendix D

Singly Balanced Versus Single-ended FET Mixer

D.1 Introduction

This topic is not easily covered and strict limitations are made to only consider the circumstances in this project. Both a single-balanced and a single-ended FET resistive mixer are implemented using ideal components to form a groundwork to decide which mixer topology is the best choice. The main focus is the linearity (IIP_3) of the mixers. From the implementations the single-ended mixer is eventually selected. This is due to its simplicity and sufficient performance.

D.2 Single-ended mixer

A single-ended cold FET mixer is the simplest version of a FET mixer possible. It is simply a FET with the LO connected to the gate and the RF and IF connected to the drain. Besides the FET there is need for a bias network and for a diplexer to separate the two signals on the drain.

The single-ended mixer is implemented with an ideal frequency split, acting as the diplexer separating the RF and the IF on the drain of the mixing FET. The gate of the FET is biased via an ideal RF-choke to $v_{gs} = -1\text{ V}$. The FET model used is the UMS PPH25 NCF (non-linear cold FET), which is the only non-ideal component in the design.

D.3 Balanced mixer

D.3.1 Concept

Balanced mixers promise better linearity and suppression of spurious responses. There are different topologies but all of them require at least one balun, and

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usually a stronger LO drive since two or more FETs are used. The performance of balanced mixers largely depends on the baluns. Thus, large effort is put into the design of these. An obvious drawback is the bulky nature of these balanced to unbalanced transition.

The ideal implementation of a balanced mixer uses perfect 180° baluns, with the ability to control the loss and the phase imbalance. The two NCF FETs required in a balanced setup are both biased with $v_{gs} = -1\text{ V}$, just as the unbalanced mixer. No filters are used.

D.3.2 Baluns

The purpose of baluns is to convert an unbalanced signal (a single signal in reference to ground) into its balanced counterparts (in which there are two signals, usually described as positive and negative) or vice versa. As such, they are usually three-ports, receiving a signal relative ground on one port and outputs the balanced signal on the two remaining ports.

Baluns can be either active, lumped or distributed. Because of the size of distributed baluns at these frequencies, they are not considered for this project. Active baluns use FETs and have gain.

The layout and performance of an implemented lumped element balun is shown in Figure D.1.[31] The construction is quite simple, but the bandwidth is not large enough for the LO-signal. The amplitude difference is rather large as f_{LO} increases, which impacts on the performance of a balanced mixer.

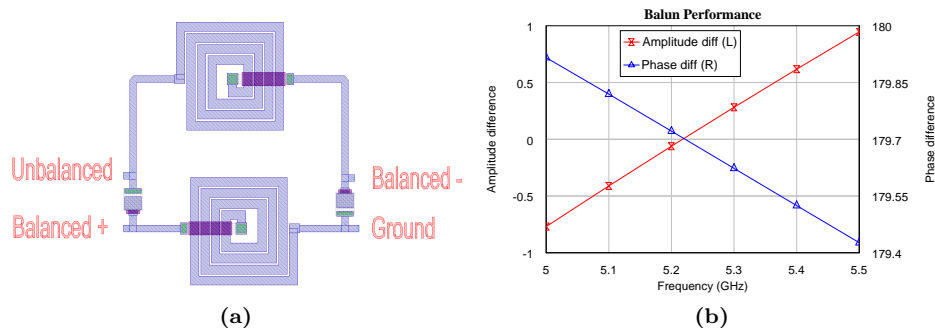


Figure D.1: (a) The layout and (b) the simulated performance of a simple lumped element 180° balun.

D.4 Results

A phase shift in the baluns of a singly balanced mixer does not have as big an impact on linearity as expected. IIP_3 is almost constant for a 10° phase difference in the balanced signal. The linearity is however very sensitive to the



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loss in the baluns, as shown in Figure D.2. No component in the single-ended mixer has been observed to affect the IIP_3 in a similar manner.

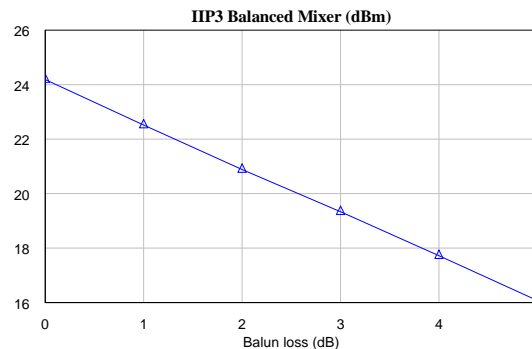


Figure D.2: IIP_3 of the singly balanced mixer versus the loss in one of the two baluns. The affect on IIP_3 is the same regardless of in which balun the losses are present. In this case the other balun is set to zero loss. The LO power is 12 dBm and the signal is matched to 50Ω (not the impedance of the gate).

Is Figure D.3 the IIP_3 is compared between the two topologies. For the balanced mixer there is a 2 dB loss applied to both baluns. This is a loss that is considered reasonable in a non-ideal implementation. No comparison in conversion gain between the topologies has been performed, as the filter structures that produce most losses are ideal and different for the two mixers.

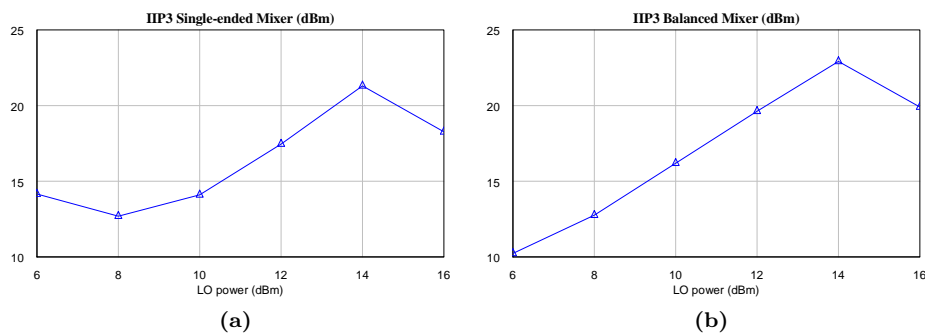


Figure D.3: IIP_3 for (a) the single-ended mixer and (b) the singly balanced mixer. Here the balanced mixer has a realistic 2 dB loss in each of its two baluns. The FET linearity decreases in both cases, as the LO power exceeds 14 dBm. The LO is matched to 50Ω , and not to the gate impedance.



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D.5 Conclusion

From the simulation results of the ideal mixers it is evident that a balanced structure gives the highest IIP_3 . However, for small losses in the baluns the performance drop rapidly and becomes comparable to the single-ended mixer. As the LO-signal has 500 MHz bandwidth it is probable that a balun that can handle such a bandwidth becomes rather complex and thus have considerable losses. An IF-balun would also have some losses, although not as much as the LO-balun would. Another important issue to take into consideration is the large space that baluns take on an MMIC.

This leads to the conclusion that the simple unbalanced single-ended design provides good enough performance and at the same time being very space efficient and easy to implement.

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Appendix E

Electromagnetic Simulations

The length scales when designing integrated circuits are very small. This together with gigahertz frequencies cause the electric design models to be inaccurate. Unexpected electric fields can cause a circuit to behave very erratic. To model this behaviour realistically finite element analysis is used. The electric structures are defined as meshes and the Maxwell equations are solved numerically. This is the most accurate way available to predict the properties and performance of a circuit. However, the simulations are computationally heavy and are mainly used as a final step to verify and adjust a design initially based on electric circuit models.

Besides not treating coupling between elements the electric models are unreliable at high frequencies (Figure E.1). Even though the fundamental frequencies in this project reside within the accurate range there are higher frequency harmonics that will be calculated erroneously.

In Figure E.2 the passive structure of amplifier IF2 is modelled and meshed. This is an example of a structure used in the final electromagnetic simulations.

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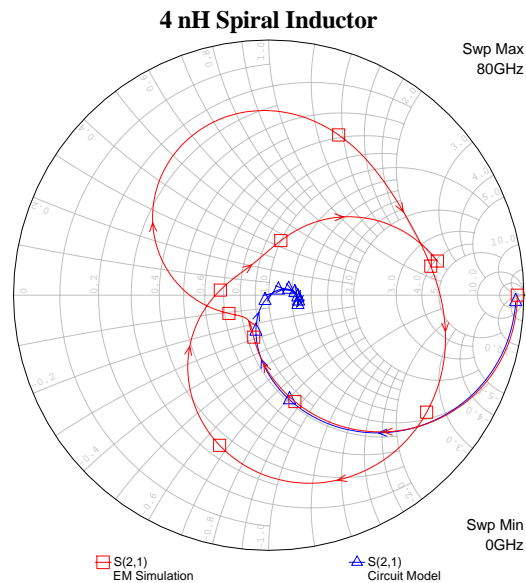


Figure E.1: Comparison of S_{21} between the electric model of the PPH25 spiral inductor and its EM simulation. For low frequencies the results are approximately the same. The electric circuit model is not trustworthy above ≈ 12 GHz for a 4 nH inductance.

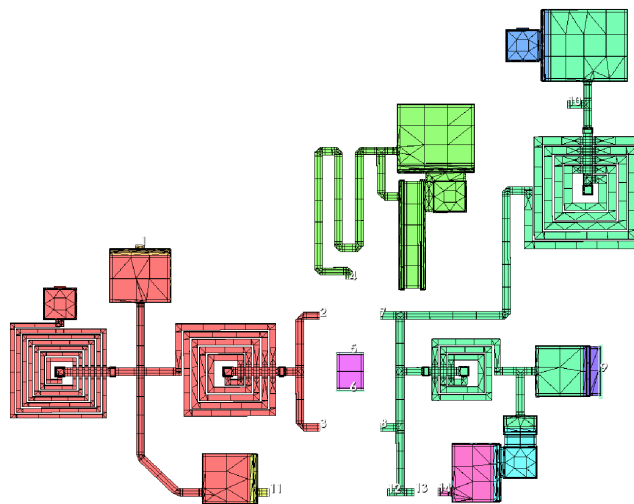


Figure E.2: Meshed EM structure of the passive components in amplifier IF2. Bias, input, output and active components (including the GaAs resistors) are connected with edge ports. Areas of the same colour are DC-connected.



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Appendix F

Yield Analysis

F.1 Introduction

All components on the GaAs wafer have parameter spread. That is, the performance of both the passive and active structures have an uncertainty interval.[9] The uncertainty is due to minor variations within the wafer and to larger variations between wafers. Yield analysis is performed to estimate the possible impact that these variations can cause. The analysis randomly varies parameters in the design according to their specifications (Table F.1). Of interest are especially gain and stability of amplifiers as well as the frequency characteristics of sensitive filters.

Table F.1: Different components' spread parameters. The values are spread uniformly. Some of the values are taken from PH25 as they aren't defined in the PPH25 manual.

Component	Parameter	Spread
FET transistor	dV_t^*	$\pm 0.2 \text{ V}$
GaAs substrate	Height	$\pm 10 \mu\text{m}$
Spiral inductor	Inductance	$\pm 5 \%$
MIM capacitor	Capacitance	$\pm 5.6 \%$
TaN resistor	Resistance	$\pm 3.6 \%$
GaAs resistor	Resistance	$\pm 6 \%$
TiWSi resistor	Resistance	$\pm 8 \%$

* An internal parameter affecting the FET's pinch-off voltage and thus the current i_{ds} .

While all final results stated in the report are calculated using electromagnetic (EM) simulations, the yield calculations are performed on the electric models. This is because yield analysis with EM simulations would be too computationally intensive. However, the results from the electric models can be very far from

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the EM results. The yield analysis should therefore be regarded as a measure of how the result can vary due to process spread and not as the actual result.

F.2 Amplifier LO

Yield analysis of amplifier LO is shown in Table F.2, Figure F.1.

Table F.2: Amplifier LO typical performance with spread at $P_{LO} = -2$ dBm.

Parameter	Performance
Delivered Power	5 ± 2 dB
Return Loss Input	15 ± 2 dB
Stability	$K > 1$
Power Consumption	100 ± 5 mW

F.3 Amplifier IF1

Yield analysis of amplifier IF1 is shown in Table F.3 and Figure F.2.

Table F.3: Amplifier IF1 typical performance with spread.

Parameter	Performance
Gain	11.5 ± 0.75 dB
Return Loss Input	14.4 ± 5 dB
Return Loss Output	16.9 ± 1.5 dB
Stability	$K > 1$
P_{1dB} (Input)	6.2 ± 1 dBm
Power Consumption	290 ± 40 mW

F.4 Amplifier IF2

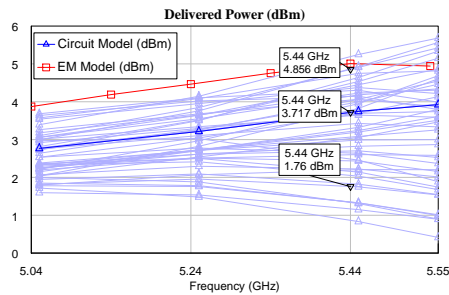
Yield analysis of amplifier IF2 is shown in Table F.4 and Figure F.3.

F.5 Mixer

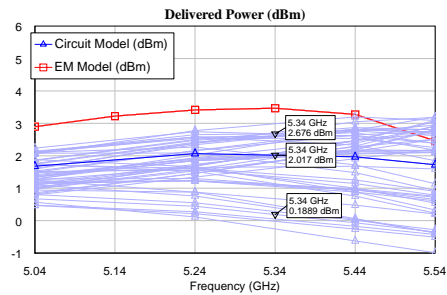
Yield analysis of the mixer's input matching and conversion gain as well as the stand-alone diplexer are shown in Figure F.4. All yield results are concluded in Table F.5.



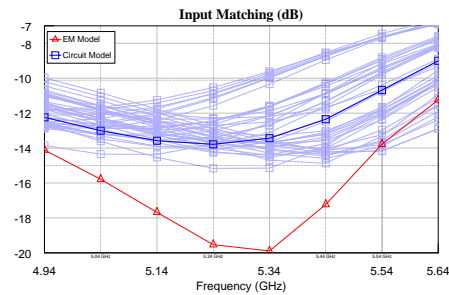
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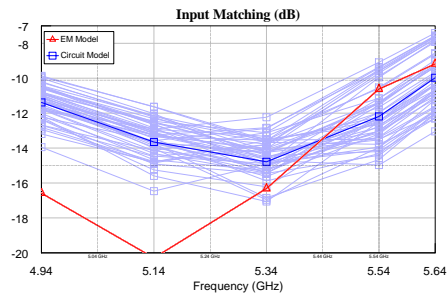
(a) Delivered power at input power -2 dBm.



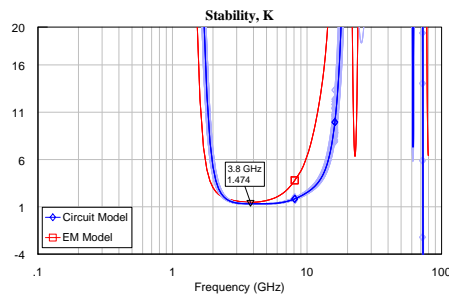
(b) Delivered power at input power -4 dBm.



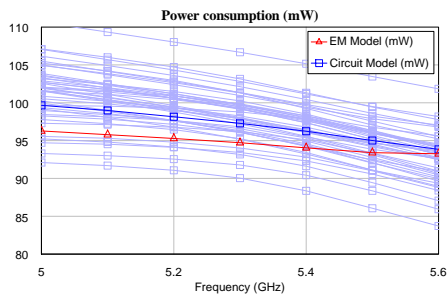
(c) Input reflection coefficient S_{11} at input power -2 dBm. Active frequency range is 5.04 to 5.54 GHz



(d) Input reflection coefficient S_{11} at input power -4 dBm. Active frequency range is 5.04 to 5.54 GHz



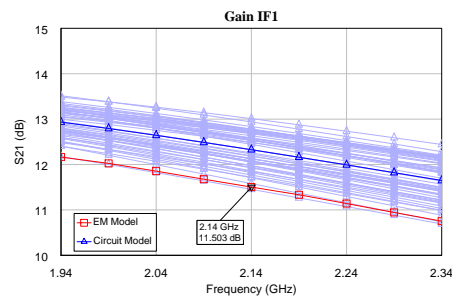
(e) Stability measure K. Note that even though the electric model has $K < 1$ at 70 GHz the EM model is stable.



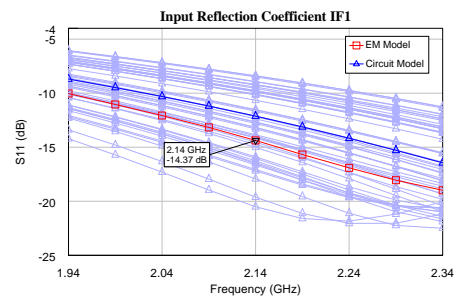
(f) Power consumption at input power -2 dBm.

Figure F.1: Yield analysis of amplifier LO at input power -2 and -4 dBm. The spread analyzed with the electric circuit model gives a hint of the spread for the more accurate electromagnetic simulation.

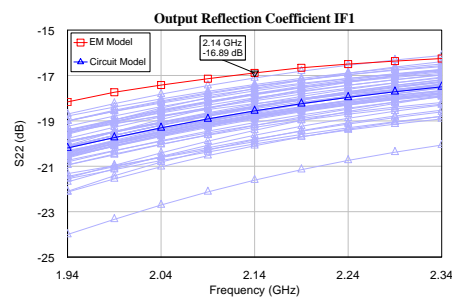
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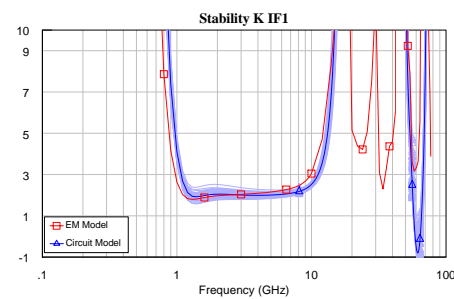
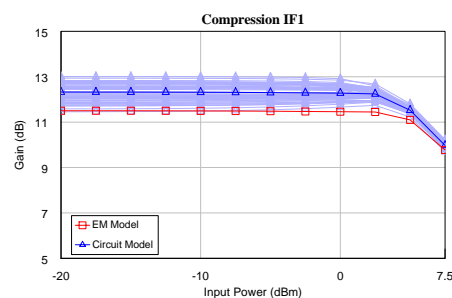
(a) Gain.



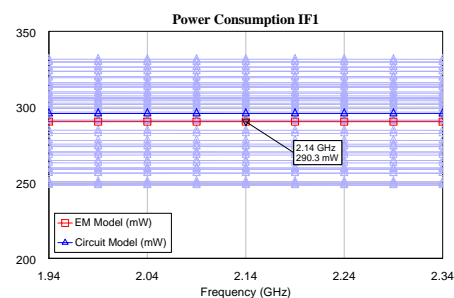
(b) Input reflection coefficient S11.



(c) Output reflection coefficient S22.

(d) Stability measure K. Note that even though the electric model has $K < 1$ at 60 GHz the EM model is stable.

(e) Power compression.



(f) Power consumption.

Figure F.2: Yield analysis of amplifier IF1. The spread analyzed with the electric circuit model gives a hint of the spread for the more accurate electromagnetic simulation.

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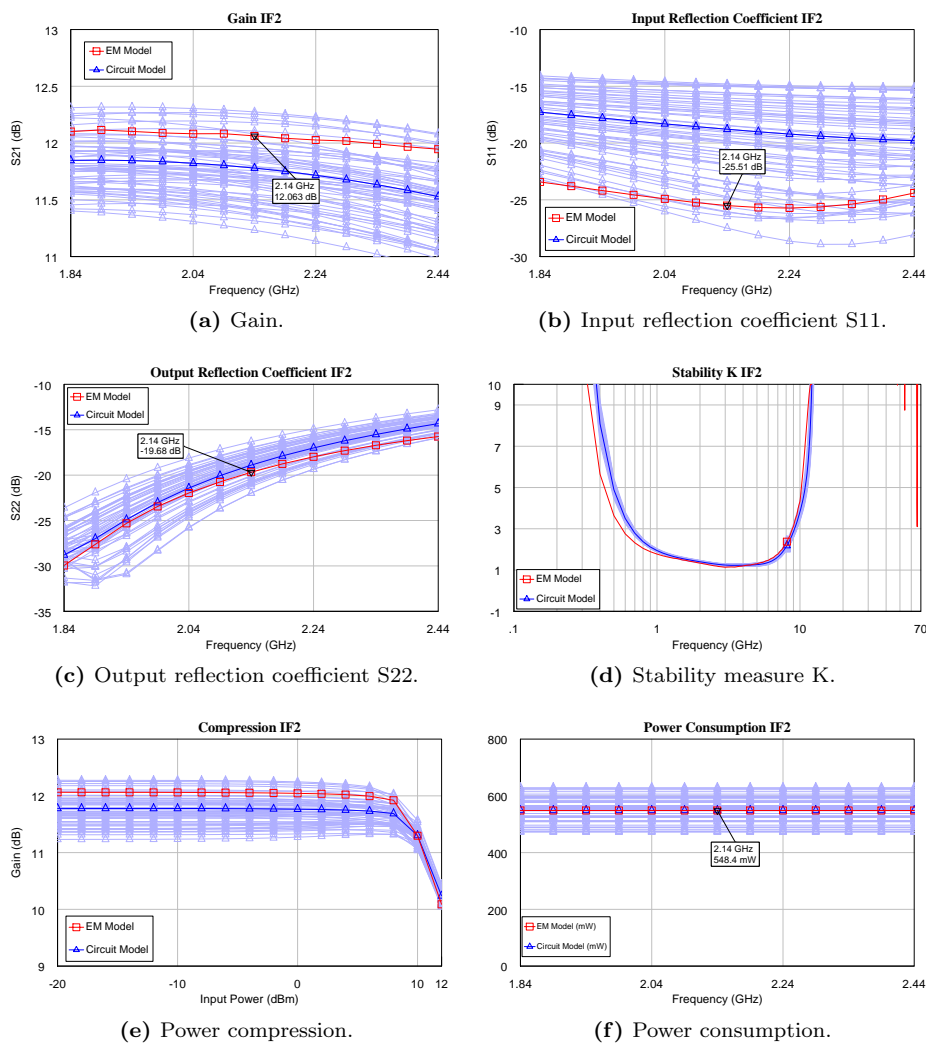


Figure F.3: Yield analysis of amplifier IF2. The spread analysed with the electric circuit model gives a hint of the spread for the more accurate electromagnetic simulation.



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Table F.4: Amplifier IF2 typical performance with spread.

Parameter	Performance
Gain	12.1 ± 0.5 dB
Return Loss Input	25.5 ± 6 dB
Return Loss Output	19.7 ± 3 dB
Stability	$K > 1$
P_{1dB} (Input)	10.4 ± 1 dBm
Power Consumption	550 ± 70 mW

Table F.5: Typical mixer performance with spread at input power -2 dBm.

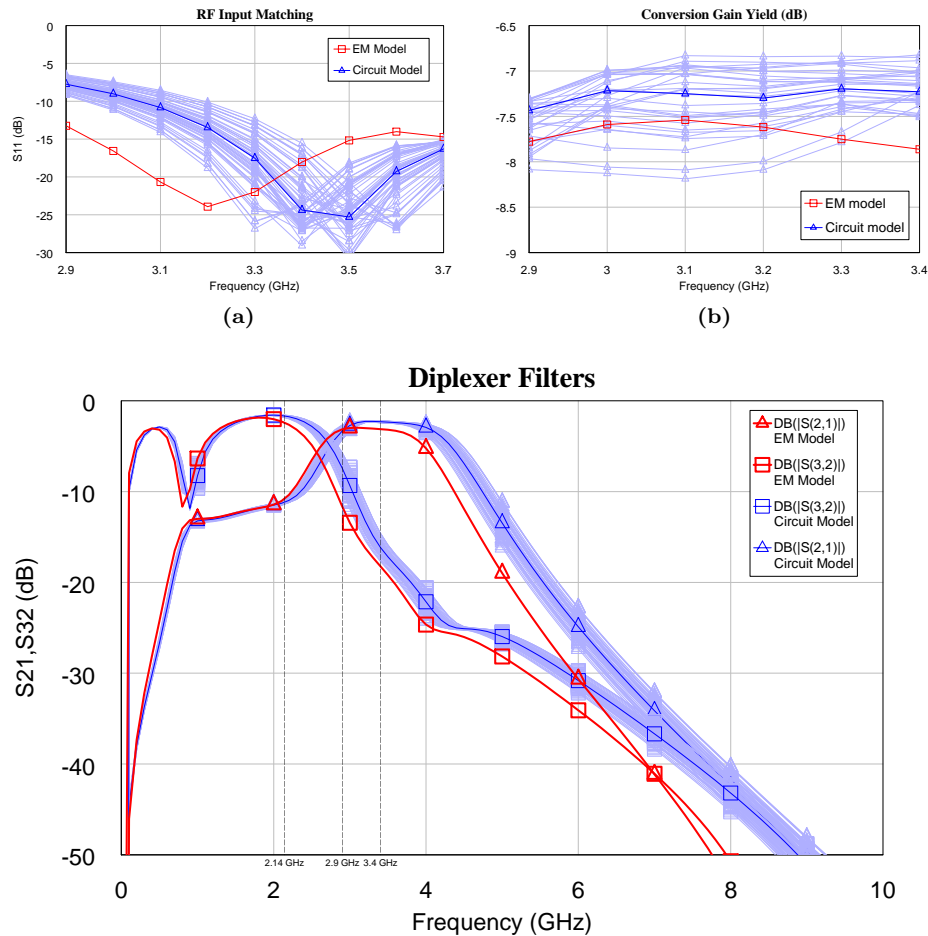
Parameter	Performance	Performance	Unit
Band	2.9–3.4	3.1–3.3	GHz
Conversion loss	7.7 ± 0.8	7.5 ± 0.8	dB
Gain variation	0.45 ± 0.4	0.05 ± 0.3	dB
Return loss input	16 ± 3	21 ± 5	dB
Return loss output (@2.14 GHz)	16 ± 2	16 ± 2	dB
P_{1dB} (input)	13 ± 0	13 ± 0.5	dBm

F.6 Chip

Yield analysis of chip conversion gain is shown in Figure F.5.



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(c) Yield analysis of the diplexer. The red (single) lines are the EM simulations and the blue (broad) lines correspond to the spread analysed with the circuit model. The curves marked with triangles Δ details the bandpass filter between the RF input and the mixer-FET's drain. The curves marked with squares \square details the low-pass filter between the mixer-FET's drain and the IF output.

Figure F.4: Yield analysis of (a) the RF input matching (b) the mixer's conversion gain and (c) the diplexer. The spread analysed with the electric circuit model gives a hint of the spread for the more accurate electromagnetic simulation.



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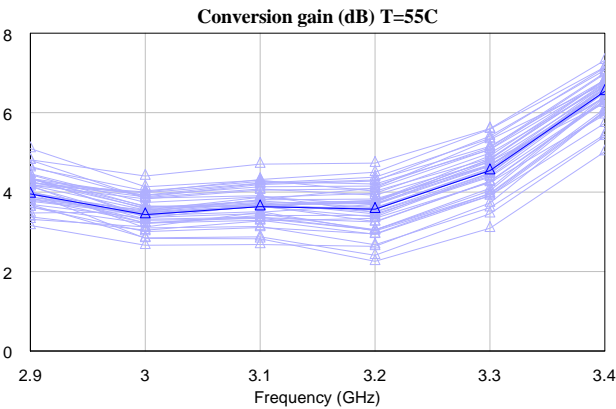


Figure F.5: Yield analysis on chip conversion gain at 55 °C and nominal gain. Circuit models are used. The yield is ±1 dB. Other temperatures show similar spread.