EOPC2205 DIGITAL SYSTEM DESIGN (0-0-3)

Course Objectives

1. To familiarize students with the basic concepts of digital logic gates and Boolean function minimization.
2. To enable students to design, assemble, test, and implement combinational and sequential digital circuits.
3. To develop skills in hardware implementation and Verilog/VHDL programming for digital circuit simulation and testing.
4. To provide hands-on experience in using programmable logic devices and analyzing the behavior of memory units and digital components.

List of Experiments

(At least 10 experiments should be conducted. Experiment Nos. 1 and 2 are compulsory. Out of the remaining 8 experiments, at least 3 must be implemented using both Verilog/VHDL and hardware as per the student's choice, totalling 6. The remaining 2 experiments can be implemented either through Verilog/VHDL or hardware.)

1. Digital Logic Gates: Investigate the logic behavior of AND, OR, NAND, NOR, EX-OR, EX-NOR, Inverter, and Buffer gates, and demonstrate the use of the Universal NAND gate.
2. Gate-Level Minimization: Implement and verify two-level and multi-level Boolean functions.
3. Combinational Circuits: Design, assemble, and test adders and subtractors, code converters, gray code to binary converters, and 7-segment displays.
4. Minimal Gate Designs: Design, implement, and test a given example using (i) NAND gates only, (ii) NOR gates only, and (iii) the minimum number of gates.
5. Multiplexers and De-Multiplexers: Design circuits using multiplexers and de-multiplexers.
6. Flip-Flops: Assemble, test, and investigate the operation of SR, D, and J-K flip-flops.
7. Shift Registers: Design and analyze the operation of various types of shift registers with parallel load.
8. Counters: Design, assemble, and test various ripple and synchronous counters, including decimal counters and binary counters with parallel load.
9. Clock-Pulse Generator: Design, implement, and test a clock-pulse generator circuit.
10. Parallel Adder and Accumulator: Design, implement, and test a parallel adder and accumulator.
11. Binary Multiplier: Design and implement a circuit to multiply two 4-bit unsigned numbers to produce an 8-bit product.
12. Verilog/VHDL Simulation and Implementation: Simulate and implement experiments from Sl. Nos. 3 to 11 using Verilog/VHDL.

Course Outcomes

After the completion of this lab course, students will be able to:

CO1: Investigate the logic behavior of digital gates and implement universal gates in digital circuits.

CO2: Simplify and implement Boolean functions at the gate level using two-level and multi-level minimization techniques.

CO3: Design and test combinational circuits, including adders, subtractors, code converters, and 7-segment displays.

CO4: Implement sequential circuits such as flip-flops, counters, and shift registers, and analyze their operation.
CO5: Develop and simulate digital circuits using Verilog/VHDL and implement them in hardware.
CO6: Analyze the behavior of memory units and programmable logic devices.