Experiment 1: Verification of Kirchhoff's Laws (KCL & KVL)

1. Introduction

In the field of electrical engineering, analyzing complex circuits often goes beyond the capabilities of Ohm's Law alone. Gustav Kirchhoff formulated two fundamental laws in 1845 that govern the conservation of charge and energy in electrical circuits. These are:

1. **Kirchhoff's Current Law (KCL)**
2. **Kirchhoff's Voltage Law (KVL)**

This experiment aims to verify these laws experimentally using a DC circuit.

2. Objective

To configure a DC circuit on a breadboard and verify Kirchhoff's Current Law and Kirchhoff's Voltage Law by measuring currents and voltages across various elements.

3. Apparatus Required

S.No	Apparatus	Quantity
1.	Breadboard	1
2.	DC Power Supply (0-30V)	1
3.	Resistors (Various values, e.g., R_1, R_2, R_3)	3
4.	Digital Multimeter (DMM)	1 or 2
5.	Connecting Wires	As required

4. Theory

A. Kirchhoff's Current Law (KCL)

Statement: KCL states that the algebraic sum of currents entering a node (or junction) is equal to the algebraic sum of currents leaving it. Alternatively, the algebraic sum of all currents meeting at a junction is zero.

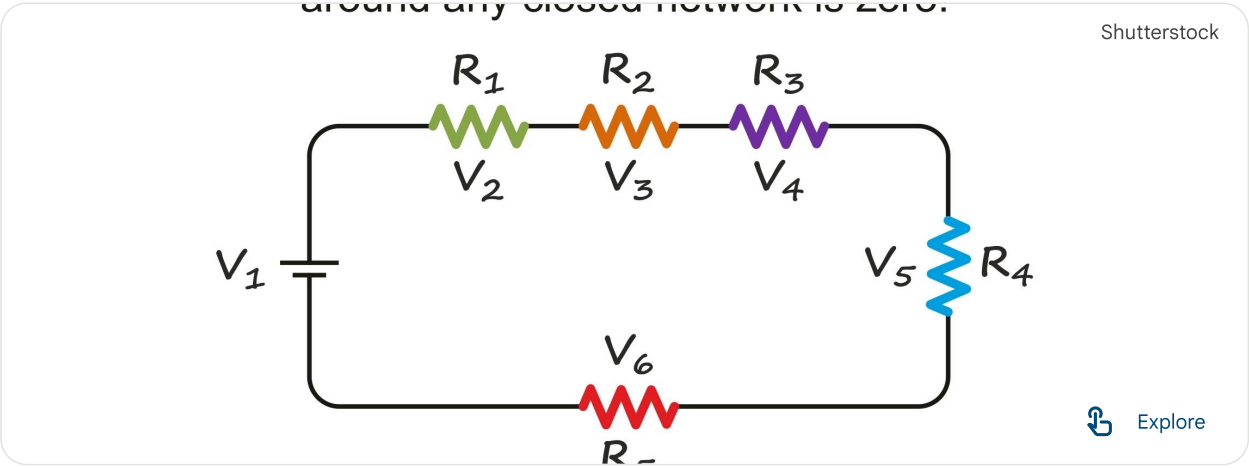
Mathematical Expression:

$$\sum I_{\text{entering}} = \sum I_{\text{leaving}}$$

OR

$$\sum_{k=1}^{n} I_k = 0$$

Principle:



This law is based on the **Law of Conservation of Charge**. Charge cannot be created or destroyed at a node; whatever charge flows in must flow out.

Example: Consider a node where current I_1 enters, and currents I_2 and I_3 leave. According to KCL:

$$I_1 = I_2 + I_3$$

B. Kirchhoff's Voltage Law (KVL)

Statement: KVL states that in any closed loop (or mesh) of an electrical circuit, the algebraic sum of all voltages (EMFs and potential drops) is equal to zero.

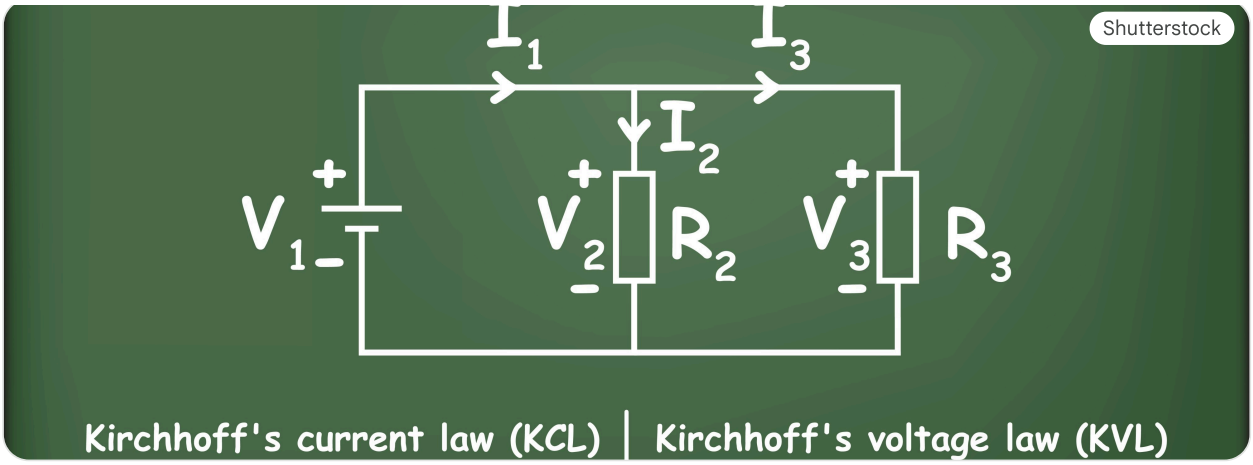
Mathematical Expression:

$$\sum V_{\text{rise}} = \sum V_{\text{drop}}$$

OR

$$\sum_{k=1}^{n} V_k = 0$$

Principle:



This law is based on the **Law of Conservation of Energy**. The energy supplied by the source in a closed loop is completely consumed by the passive elements (like resistors) in that loop.

Sign Convention (Crucial for Verification):

- **Voltage Rise (Gain):** Moving from Negative (-) to Positive (+) terminal. Treated as **Positive (+)**.
- **Voltage Drop (Loss):** Moving from Positive (+) to Negative (-) terminal (direction of current flow). Treated as **Negative (-)**.

Example: For a simple loop with a voltage source V_s and two series resistors R_1 and R_2:

$$V_s - IR_1 - IR_2 = 0$$

$$V_s = V_1 + V_2$$

5. Circuit Diagram

(Note: Below is a standard T-network often used for this experiment)

- **Resistors:** R_1, R_2, R_3 connected in a T-shape.
- **Source:** DC Voltage V_{in} connected to R_1.
- **Nodes:** Point A (Input), Point B (Junction of R_1, R_2, R_3).
- **Ground:** The other ends of R_2 and the source are grounded.

(Imagine a circuit where current I_{total} flows through R_1 and splits into I_2 through R_2 and I_3 through R_3.)

6. Procedure

Part A: Verification of KCL

1. **Setup:** Connect the circuit on the breadboard as per the diagram. Ensure the power supply is initially OFF.

2. **Measure Total Current (I_{in}):** Break the circuit before the main junction node and connect the Ammeter in **series** to measure the total incoming current. Record this as I_{total}.
3. **Measure Branch Currents (I_1, I_2):**
    - Reconnect the main branch.
    - Break the first branch (e.g., resistor R_2) and connect the Ammeter in series to measure I_1.
    - Repeat for the second branch (e.g., resistor R_3) to measure I_2.
4. **Calculation:** Verify if $I_{total} = I_1 + I_2$.

Part B: Verification of KVL

1. **Setup:** Use the same circuit.
2. **Measure Source Voltage (V_s):** Connect the Voltmeter in **parallel** to the power supply terminals.
3. **Measure Voltage Drops (V_1, V_2, V_3):** Connect the Voltmeter in **parallel** across each resistor (R_1, R_2, R_3) individually.
4. **Loop Selection:** Identify a closed loop (e.g., Source -> R_1 -> R_2 -> Ground).
5. **Calculation:** Verify if $V_s = V_{R1} + V_{R2}$ (or whichever components form the closed loop).

7. Observation Table

For KCL: | S.No | Applied Voltage (V) | Total Current I_{in} (mA) | Branch Current I_1 (mA) | Branch Current I_2 (mA) | Error ($I_{in} - (I_1 + I_2)$) | | :--- | :--- | :--- | :--- | :--- | :--- | | 1. | 5V | ... | ... | ... | ... | | 2. | 10V | ... | ... | ... | ... |

For KVL: | S.No | Loop Chosen | Supply Voltage V_s (V) | Drop V_1 (V) | Drop V_2 (V) | Verification ($\sum V = 0$) | | :--- | :--- | :--- | :--- | :--- | :--- | | 1. | Loop 1 | ... | ... | ... | $V_s - V_1 - V_2 \approx 0$ |

8. Precautions

1. **Ammeter Connection:** Always connect the ammeter in **series**. Connecting it in parallel will blow the fuse due to low resistance.
2. **Voltmeter Connection:** Always connect the voltmeter in **parallel**.
3. **Loose Connections:** Ensure breadboard wires are inserted firmly to avoid contact resistance errors.
4. **Heat:** Do not keep the power supply ON for too long to prevent resistors from heating up, which changes their resistance value.

9. Conclusion

The algebraic sum of currents at the node was found to be approximately zero, verifying KCL. The