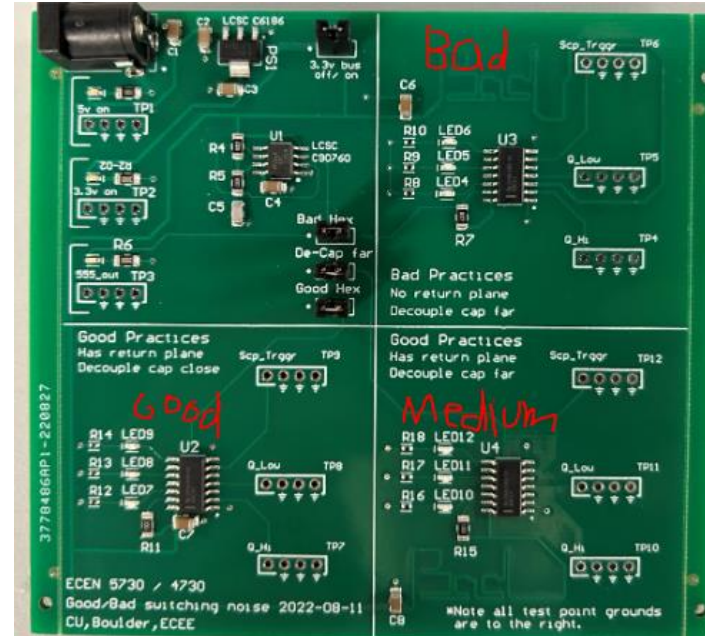
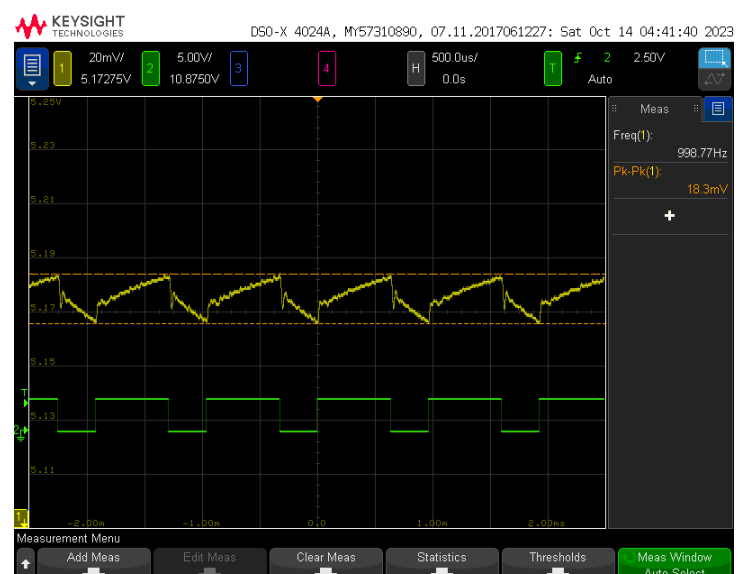
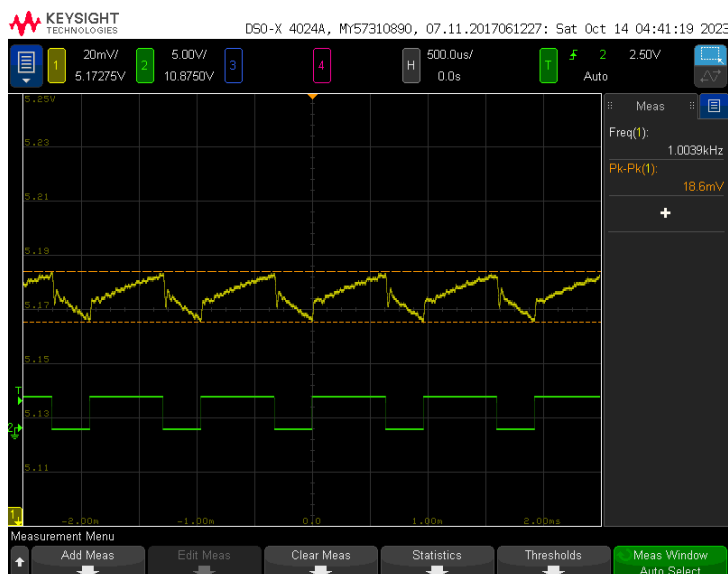


## Lab 15 Report

In this lab, I used a board provided by my course instructor to measure the effects of various PCB design best practices, a return plane and a decoupling capacitor near the IC, on noise experienced throughout the board. I used the board on the right to test a 555 timer circuit connected to a hex inverter without a return plane and nearby decoupling capacitor, a circuit with return plane and a far decoupling capacitor, and a circuit with a return plane and nearby decoupling capacitor. I will refer to the circuits at the bad, medium, and good circuit respectively. I measured the outputs of a quiet high inverter, quiet low inverter, and the 5V power rail to observe the noise.

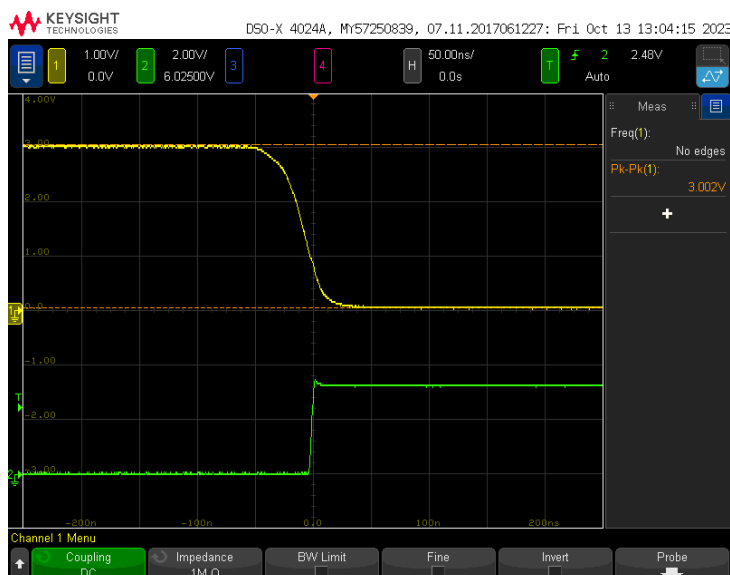
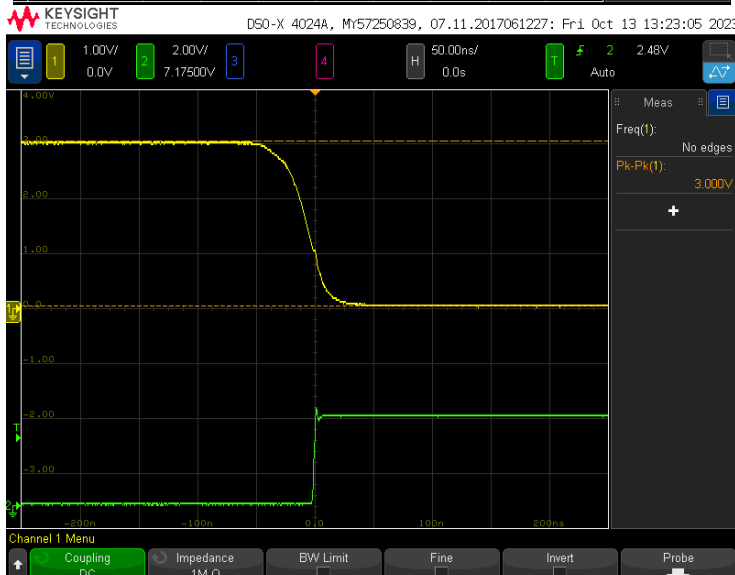
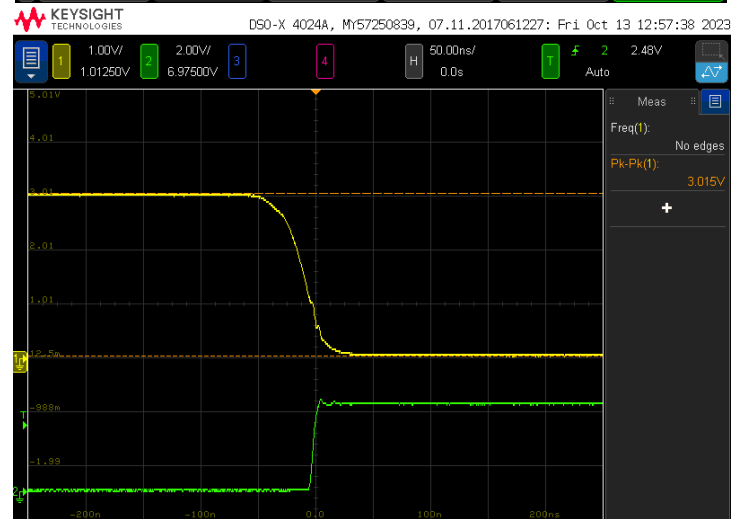


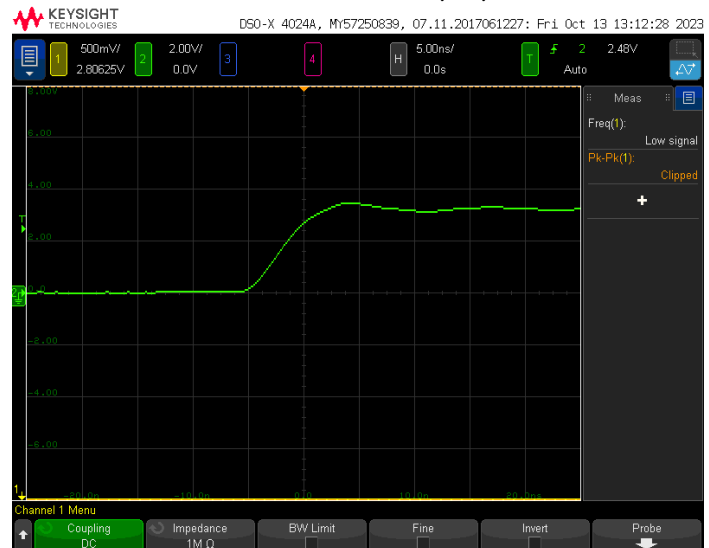
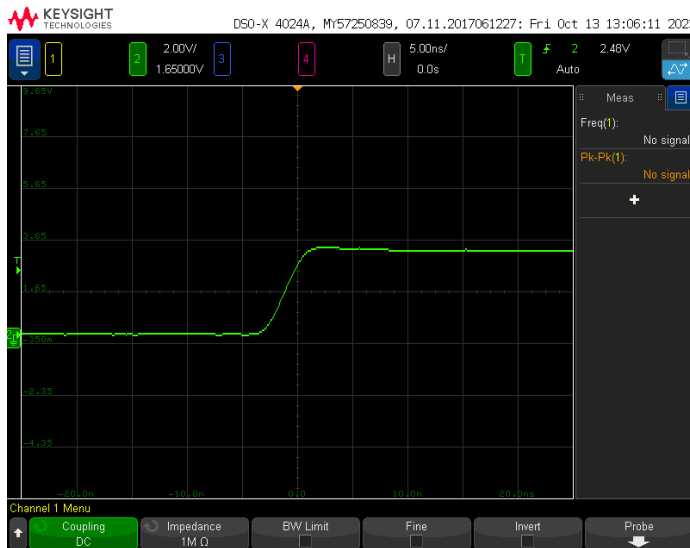
To start, I measured the noise on my power rail while each inverter was running on its own. The 2 images below show the noise that I measured on the 5V power rail from the bad, left, and the medium, right, circuit. The noise on the rail is very similar, between 18 and 19mV peak to peak. The noise from the good circuit was much smaller



with about 13mV of noise. This is because the purpose of that nearby decoupling capacitor is to reduce this noise on the power rail by discharging the capacitors during the switch to compensate for the sudden change in current draw.

I also measured the fall time of the 555 timer and the rise time of the inverter. The 2 are shown in the next set of images, with the yellow showing the 555 timer and the green showing the inverter. The top right image is the bad circuit, the left image is the medium circuit and the bottom right image is the good circuit. The rise times of the 555 timer between the 3 circuits are almost identical, being about 75ns. The rise times of the inverter, however, are different. The next three images show just the rise of the inverter and are in the same orientation.

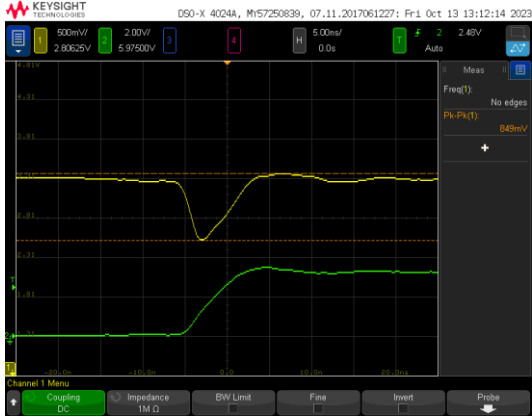

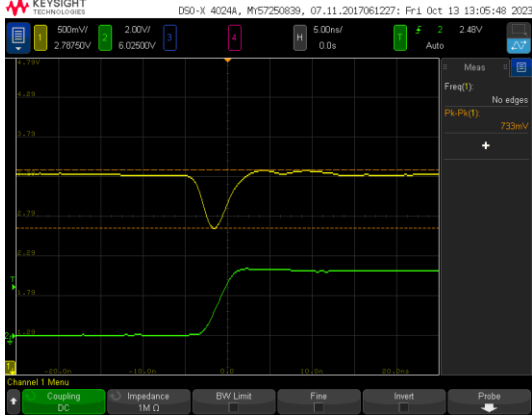
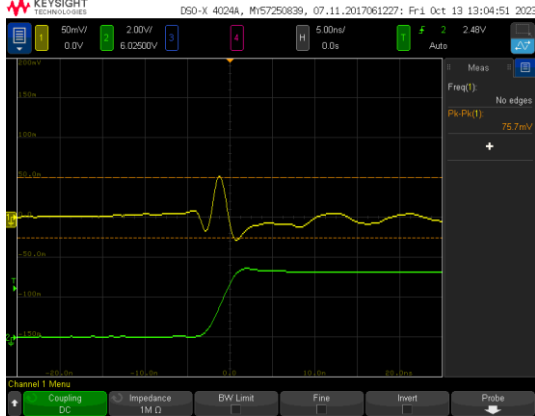






The rise time for the bad inverter is about 10ns, 5ns for the medium circuit and 3.75ns for the good circuit. The differences are result of the differing inductances of each circuit design. The bad circuit experiences a relatively high inductance due to the long traces and the lack of a return plane and the medium circuit only experiences the higher inductance due to the long traces. With these rise times, I can conclude that adding the return plane roughly halves the loop inductance and moving the decoupling capacitor closer to the IC reduces the inductance by about 25%. The estimation isn't perfect, but with the change in voltage and current being roughly the same, increases in rise time mean an increase in inductance according to the equation  $V = L \left( \frac{di}{dt} \right)$ .



I next measured the outputs of a quiet high output and a quiet low output from each inverter. The chart below shows the findings from each circuit for the quiet high and quiet low outputs.

	Quiet High	Quiet Low
Bad Circuit		
Med Circuit		
Good Circuit		

The quiet high inverter was an inverter whose input was tied to ground, so the output should always be high, and any fluctuations in the voltage are the result of noise. In the images above, there was a fluctuation in voltage of the quiet high during the switch of the 555 timer, and the inverter as a result. While the noise can never be truly

removed, the noise gets better in the good circuit. The noise in the bad and medium circuit is about a 700-800mV drop in voltage while the good circuit only experiences a 300mV drop. This large difference is due to the distance between the hex inverter IC and the decoupling capacitor. Because the output of the quiet high output is tied to the power rail, any fluctuations in the power rail will cause a fluctuation in the output. The decoupling capacitor is placed close to the IC to minimize the switching noise on the power rail, so when the capacitor is far from the IC, the noise will be larger.

The quiet low inverter was an inverter whose input was tied high, so its output should remain at 0V, which any fluctuations being due to noise. This noise is a result of a phenomenon called ground bounce which can cause the ground to fall below fluctuate, possibly below 0V. This is a result of the inductance created from a shared return trace. Again, a shared return plane will heavily reduce this inductance, which is evident with the reduction in noise from a 400mV spike above ground to a 25mV drop in current followed by a spike to about 50mV.

From this lab, it is clear that it is best practice to use a common return plane along with decoupling capacitors near the ICs to reduce switching noise in a circuit. Not all circuits will be at risk of having problems due to the switching noise created by not using these practices, but it will often cost nothing to implement these practices. It is an easy way to remove large amounts of noise from a circuit.