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ECEN 3730
Professor Blum
9/29/2023

Board 2: Switching noise with good and bad layouts

The purpose of this board was to both get practice designing a board with 2 PCB best practices and impact of those best practices on the noise experienced in the board. In particular, I measured the effects of a common return plane and a decoupling capacitor near the IC. To make this board, I made a plan of record to guide the development, and it is included below.

1. Convert 5 V in to 3.3 V.
2. Create a clock signal of about 500 Hz and about 50% duty cycle.
3. Drive four of the inputs of a hex inverter used to demonstrate good layout and bad layout.
4. Add a switch to selectively connect the 555 output to the various inputs of the good and bad layout hex inverters. When not connected to the timer output, all the switching inputs should be tied HIGH so they do not switch.
5. Use red LEDs and 50 ohm resistors as the load to three of the switching outputs of each hex inverter.
6. Connect the output of the fourth switching inverter to a test point to act as a trigger for the scope.
7. Set up one output of each hex inverter as a quiet HIGH and one output as a quiet LOW.
8. Use indicator LEDs, test points, and isolation switched to allow for debugging of the board and testing
9. Engineer the layout on one side of the board with best design practices and the other side of the board with bad layout practices. In the bad layout, move the decoupling capacitors far away from the Vcc pin.
10. Keep the part placement and routing identical for the two regions of the board, except for the location of the decoupling capacitor.
11. Plan test points for these signals:
    a. The scope trigger output
    b. Voltage across one of the 50 ohm resistors
    c. Voltage across the output of one of the inverters driving the LED and resistor
    d. The quiet high
    e. The quiet low
    f. The 555 output signal
    g. The 3.3. V rail on the board
    h. The 5 V rail on the board

Using these I made a sketch to plot out what my circuit should generally look like and I've included it below. The good circuit is on the left, and the bad is on the right.

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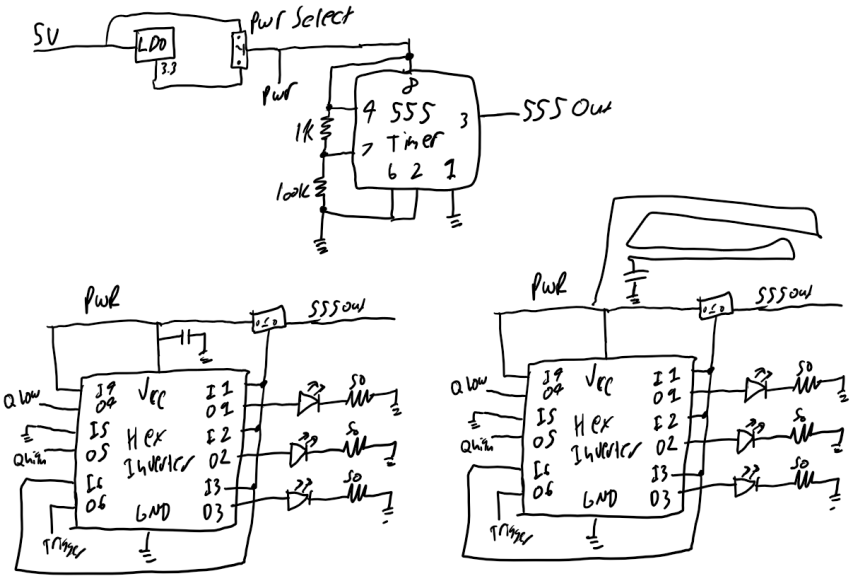
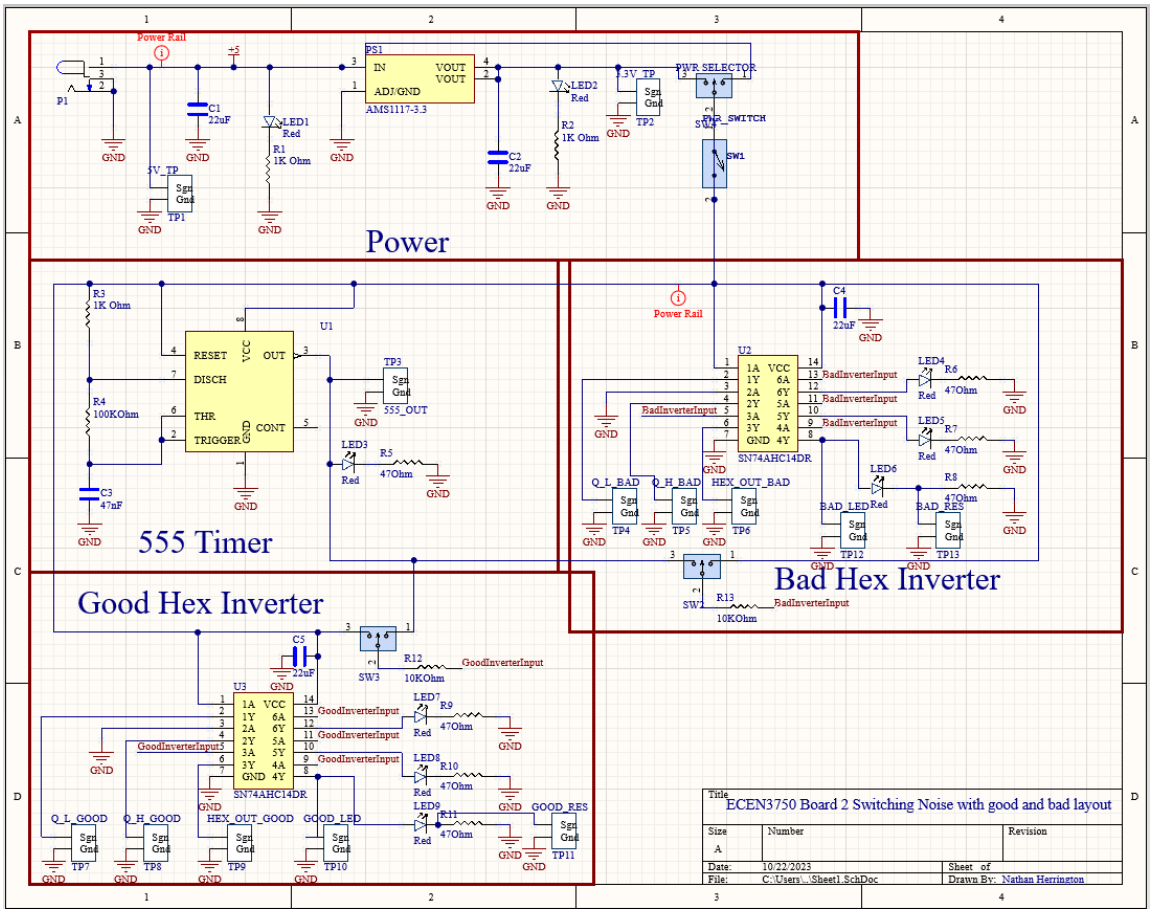


From past labs, I found that a 22uF capacitor will suffice to decouple the IC. From here I created my schematic in Altium and have added it below.



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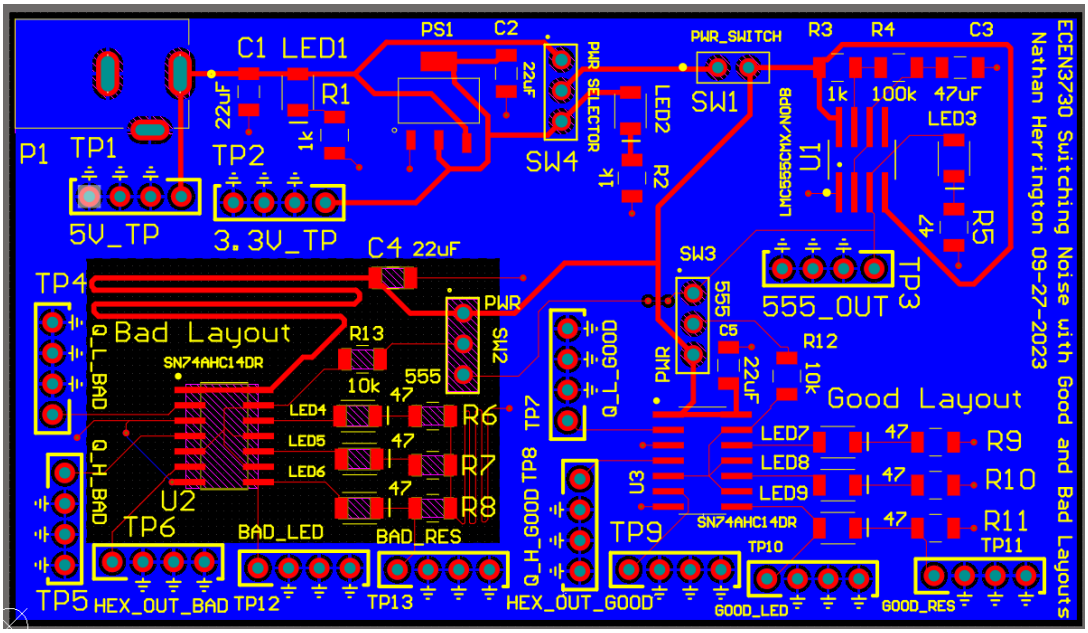
In this schematic, I also added several indicator LEDs to provide an easy visual indication when there is power to each part of the board. There is a 5V led, 3.3V led, a 555 timer output led, and leds for each hex inverter. There are also test points to test the 5V power rail, 3.3V power rail, the output of the 555 timer along with quiet high, quiet low, an inverter trigger, a testpoint for across the led, and a testpoint for the resistor for both the good and bad layouts. The resulting board is added below.



From here I ordered the board from JLCPCB, assembled it, and included pictures of the board below.

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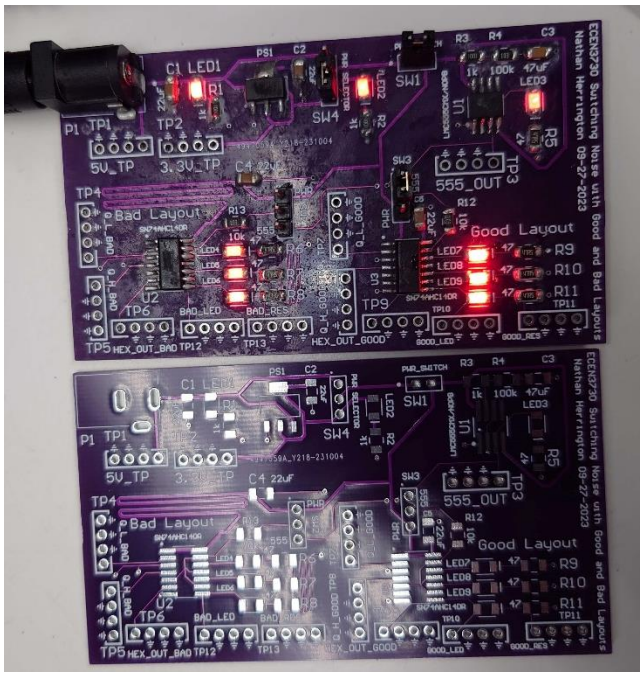

With the assembled board, I took many measurements to verify both the function of the board and to measure the impact of the best practices on the switching noise.

Based on my POR, my board is functional in all means except for the fact that my board did not have a 500Hz duty cycle. I forgot to measure the duty cycle of the 555 timer at its test point, but I have measurements of the duty cycle of the inverter output, which will have the same duty cycle, but with a steeper rise time. That measurement is to the right. The green is the inverter output and the signal has a frequency of about 75Hz. From a visual inspection, the signal is very close to a 50% duty cycle as well. I also tested that my board had a functioning 3.3V rail. The next image shows my power rail, and the switching noise from the good side of my board. As

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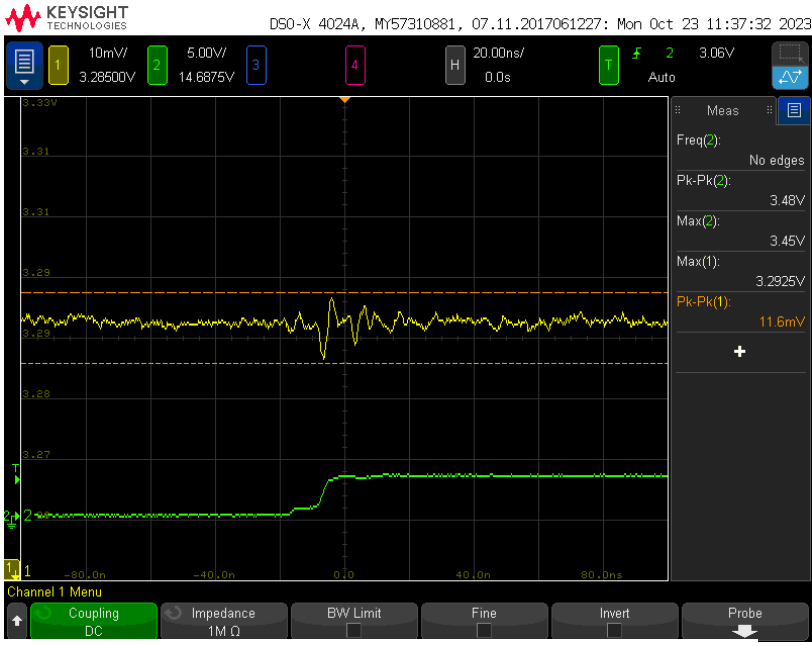
expected, there is a 3.3V power present on my board. The rest of the POR points are confirmed through visual inspection of the board.



With a functional board, I proceeded to measure the noise at the quiet high and quiet low outputs of the good and bad layouts at 5V and 3.3V. This chart below shows the noise experienced on the quiet high output of each inverter.

	Good Layout	Bad Layout
5V		
3.3V		

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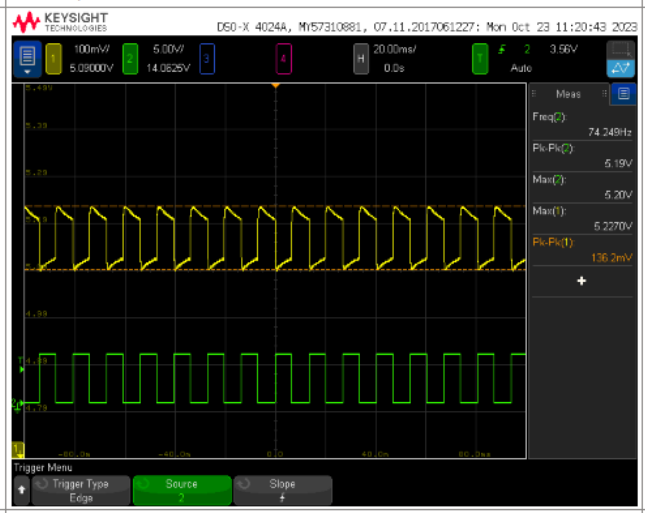
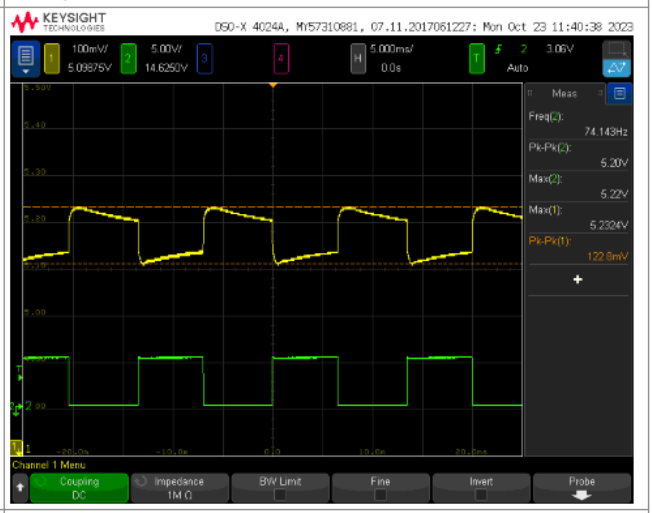
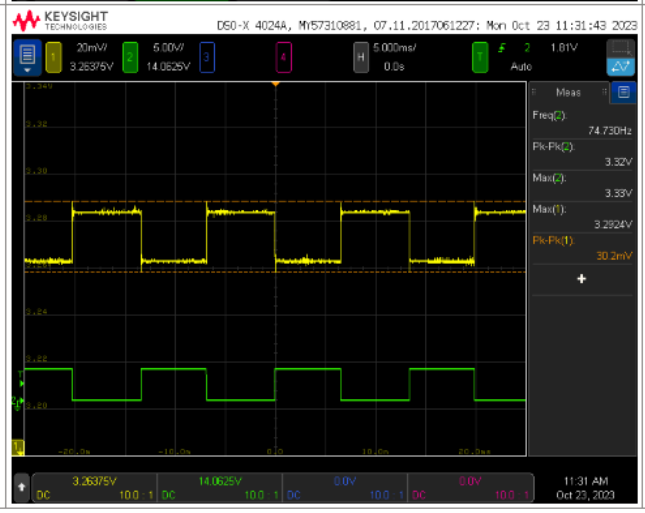
The quiet high output is supposed to be tied to the power rail, so any fluctiations measured must be noise. In this case, it is a switching noise caused by fluctuating current draws on the power source. The decoupling capacitor near the IC is meant to reduce this noise, and the measurements above support that. When powered by 5V, the good layout has an about 400mV peak to peak noise while the bad layout has almost 1.2V of noise. The 3.3V noise is similar, with the good layout having about 270mV peak to peak of noise while the bad layout had 350mV. However, over the longer duration of the increased current draw, the decoupling capacitor no longer aids in noise reduction. I measured the noise experienced over the duty cycle of the quiet high output and included it below.

	Good Layout	Bad Layout
5V		
3.3V		

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Over this longer period, there is no discernable difference in noise between the 2 layouts. This is largely due to the fact that my circuit has a frequency of about 75Hz while the intended frequency was 500Hz. Ideally, the decoupling capacitor will discharge during the switches to reduce the large changes in voltage when switching, but the period is too large and the capacitor fully discharges before the circuit switches back.

Finally, I measured the quiet low output. This output should be tied directly to ground and any fluctuations are due to noise, and in this case it is due to ground bounce. Those measurements are below.

	Good Layout	Bad Layout
5V		
3.3V		

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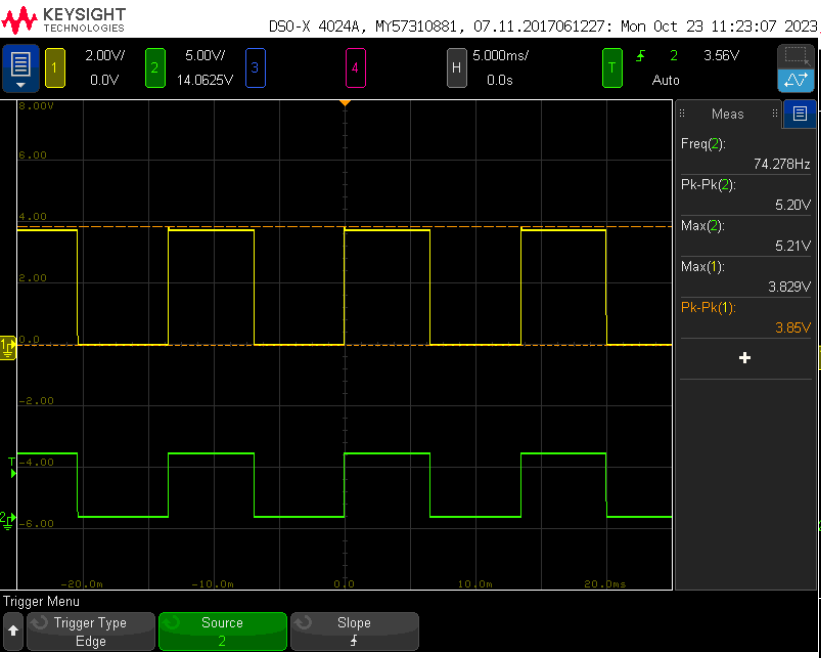
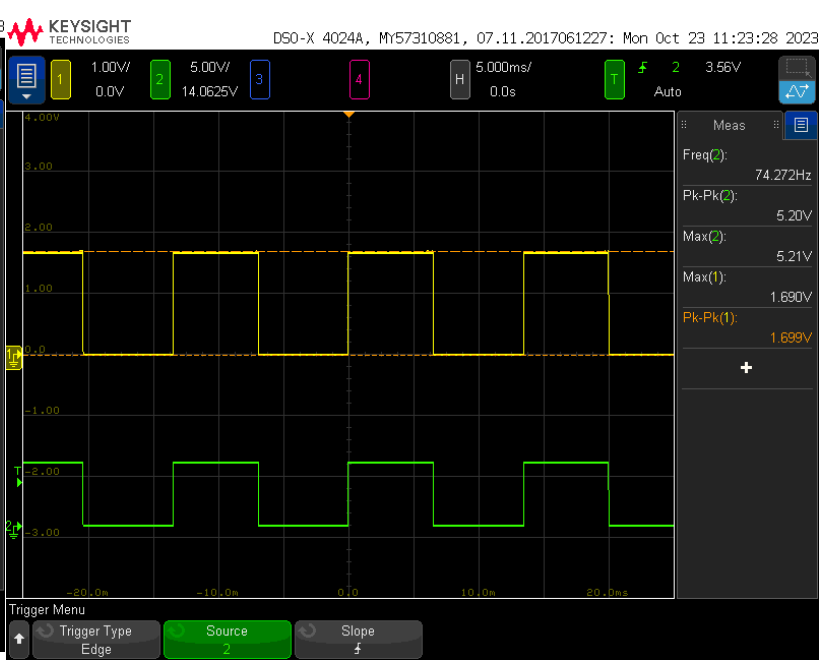
Interestingly, my measurements found that the noise was greater with the good layout than the bad layout. A common return plane is the best practice that this board minimizes the ground bounce with, but my design of the bad layout likely isn't bad enough to cause significant noise compared to the good layout, and the increased distance to the good layout may be why the good layout experiences larger ground bounce. If I really wanted maximize the effect of the lack of a return plane, I should have increased the length of trace I used to ground the hex inverter, and I should have routed the hex inverters ground directly to the 5V plug's ground instead of the ground plane. For this part of the experiment, I didn't do a good enough of a job at making the bad layout bad.

Next, I calculated the thevenin resistance of the hex inverter. To do this, I needed the voltage of an unloaded output, the voltage of a loaded output, and the voltage drop across the resistor of a loaded output. The recorded values for all 3 are below. The yellow signal in the left image shows the loaded output voltage, the yellow signal in the right image shows the voltage drop across the loaded resistor, and the green in both shows the unloaded output.





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Using these measurements, I calculated a thevenin resistance of 37Ω and included my math below.

$$R_{TH} = R_{load}\left(\frac{V_{TH} - V_{load}}{V_{load}}\right)$$

47Ω = load resistor

$$I_{load} = \frac{1.7}{47} = .036$$

$V_{TH} = 5.2\ V$

$V_{load} = 3.85\ V$

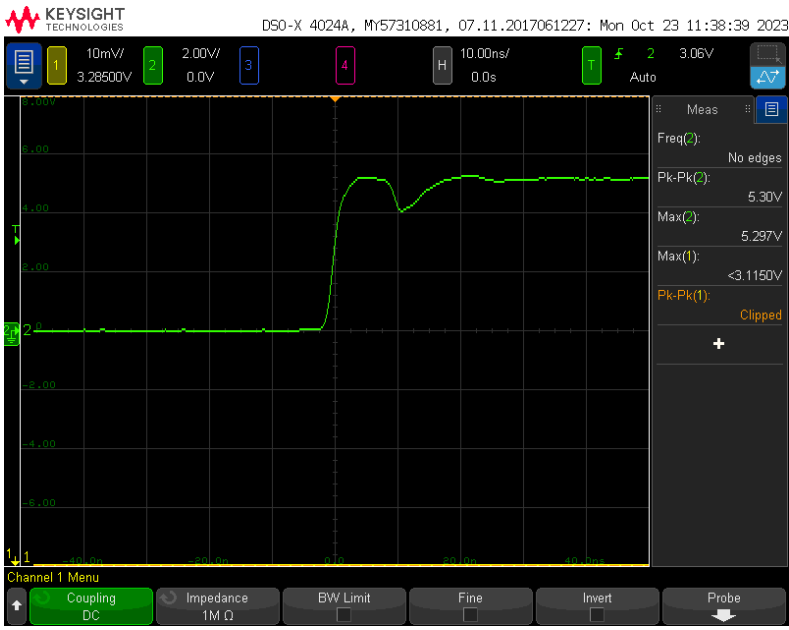
$R_{load} = 107\Omega$

$$R_{load} = \frac{V_{load}}{I_{load}} = \frac{3.85}{.036} = 107$$

$$R_{TH} = 107\left(\frac{5.2 - 3.85}{3.85}\right) = 37\Omega$$

$R_{TH} = 37\Omega$

Finally, I measured the rise time of each layout and included those measurements below, the left image is the good and the right is the bad. They both had similar rise times of 7.5ns, which is expected.



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Overall, the development of this board went smoothely but I made some errors in the design that were only realized when testing the final board. The bad side of my board wasn't bad enough to make the noise impact noticeable and my design for the 555 timer produced a slower frequency that would have been useful to see the benefits of a decoupling capacitor. The resistors I was provided to construct the board weren't what I calculated to be needed to make my 555 timer run as I wanted. I planned on a 1k and 100k resistor for my timer but got a 1k and 10k resistor. In the future, if this output frequency is critical to the success of the board, then I need to guarantee that I get resistors closer to what I calculated.

I found that seperating both the schematic and board layout into sections based on their function made it much easier to design and debug. Unfortunately, this won't be possible on more complex boards, but it is something helpful to try to do when possible. Based on my measurements, it is an almost costless addition to any board to add a nearby decoupling capacitor to the ICs to minimize noise. Based on my outside knowledge of PCB design, a common return plane is also an almost free addition to any board to reduce noise, though my measurements here fail to support that.