PROJECT REPORT
ON
FLASH ADC IMPLEMENTATION ON FPGA

EEN-360: EMBEDDED SYSTEMS

Submitted by:

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PREFACE

This project report has been prepared in partial fulfilment of the course project for the course EEN-360: Embedded Systems of the program Bachelors of Technology in the autumn semester of academic year 2019-20.

For completing the project and preparing the report, we have gone through various research papers in the field of Analog to Digital converters,priority encoding and comparators from various reliable sources such as IEEE and Research gate, etc. during the suggested period of four months to avail the necessary information. The blend of learning and knowledge acquired during our practical and theoretical studies for this project is presented in this report.

The rationale behind working on Analog to Digital Converter(ADC) is to enhance the conversion speed, power loss and area occupied on the chip. This helped us learn a lot about the various algorithms used for ADC Implementation, decoding techniques and comparator circuits.

The Project Report starts with the basic introduction of ADCs and various types of it with performance comparisons followed by different techniques used for generating thermometer code leading to the multiplexer based decoding circuitry.

The information presented in this report is obtained from sources like Institute of Electrical and Electronics Engineers(IEEE) , Research Gate, etc.

ACKNOWLEDGEMENT

We have taken efforts in this project. However, it would not have been possible without the kind support and help of many individuals and organizations. I would like to extend my sincere thanks to all of them.

I am highly indebted to Dr. Vishal Kumar for his guidance and constant supervision as well as for providing necessary information regarding the project and also for their support in completing the project.
I would like to express my gratitude towards my parents & teaching assistants for their kind cooperation and encouragement which helped us in completion of this project.

My thanks and appreciations also go to my colleagues in developing the project and people who have willingly helped me out with their abilities.

ABSTRACT

With increasing use of digital systems in the electronics field, it is required to have a converter to interface with the analog world. Such converters are popularly know as Analog to Digital Converters(ADCs). Analog converters on a very fundamental note consists of two stages. First, **Comparator Stage** conversion of analog input voltage into digital signal and secondly, **Decoding Stage** producing valid digital output corresponding to the input voltage from the obtained digital signal.

These stages can be executed by various techniques for example comparator stage can be developed by using different types of analog comparators like Resistor-Ladder and operational amplifiers combination, TIQ Comparators, etc. and Decoding Stage by priority encoding, fat tree encoding, mux-based encoding etc.

In this project we have used **R-Ladder Comparators** for generating Thermometer code from the analog input and **MUX-based decoding scheme** for obtaining binary equivalent from Unary code. Decoding with Multiplexers is the best scheme in terms of speed of conversion. Comparison using R-Ladder and dual output differential comparators is highly effective.

The low cost and easily market available discrete analog components are employed. The digital part is kept configurable with FPGA(Field Programmable Gate Array) based implementation and is done via VHDL. the system implementation is described, Testing results are also presented. These results assure near proper functionality of the designed ADC.

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INTRODUCTION

As Digital Signal Processing(DSP) is replacing analog processing, Analog to Digital Converters(ADCs) have become a critical component as it has a major impact on the system performance.Designers choose different types of ADCs as per their design specifications. Though, Flash ADC has limited resolution and high cost, this is preferred because of its high conversion speed.

The focus of this work is to design and develop an ADC with high conversion speed and accuracy. The following section briefly describes the basic conversion principle of ADC.

A/D CONVERSION PRINCIPLE:

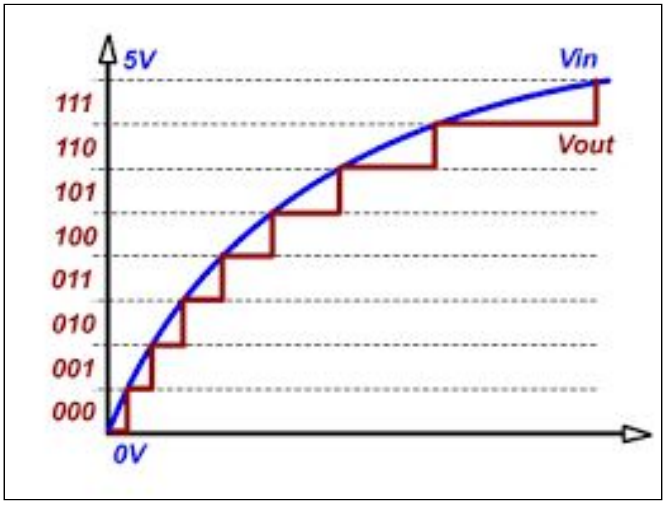


Figure1: Basic concept of Analog to digital conversion.

Basic ADC samples the input data compares it with a reference voltage and then gives the output by making each bit of output low or high based on comparison.

For a N-bit ADC, voltage ranging between [0,Vmax], step size is given by:

$$S = \frac{V\,max}{2^N - 1}$$

FLASH ADC ARCHITECTURE
(Proposed Solution)

Block diagram of proposed Flash ADC is shown in figure2.

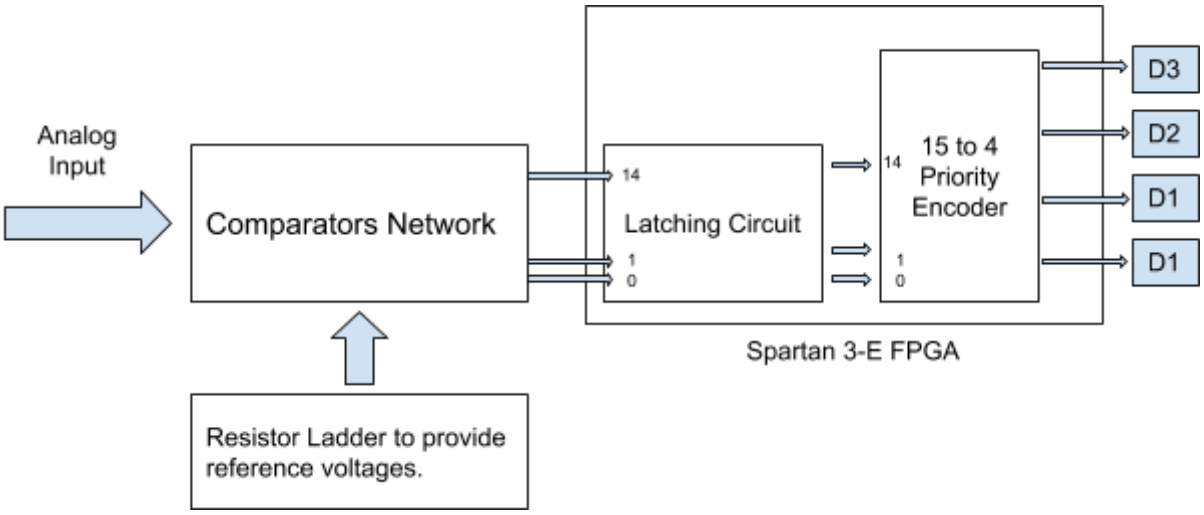


Figure-2: Flash ADC Architecture

COMPARATOR SCHEME:

The first module in the ADC Implementation is the **Comparators Network.** For an N-bit ADC $2^N - 1$ number of comparators are required. Therefore, here for 4-bit ADC, $2^4 - 1 = 15$ analog comparators are used each of which compares the input signal to a unique reference voltage. The LM7382, having low offset voltage , dual comparators are employed for this purpose.

The comparator gives a logic ’1’ when its analog input voltage is higher than the reference voltage applied to it, otherwise gives logic ‘0’.

The 15 equispaced reference voltages for each comparator are generated by a network of resistors each of value 1K ohm and having high precision.

The above explained principle is demonstrated in figure3 with the help of spice model simulation in Tina-T(software tool provided by Texas Instruments for simulation of analog circuits).

Decoding Scheme:

The output from the comparator is a thermometer code, which is fed to the mux based decoder[1]. There are various types of Decoder to convert thermometer code output of the comparator to binary code. Some of the decoder are Rom Based Decoder, Ones Counter Decoder, Fat Tree Decoder, Wallace tree based encoder and Multiplexer based decoder. Each one of them have their pros and cons.This decoder result in short critical path and small area while fabricating on the chip. It requires less hardware cost. The others are good in eliminating bubble code error but requires large encoding circuitry as in the case of Wallace tree encoder[2]. This design based on the mux(2 to 1) is also able to reduce the bubble error to a certain limit.

This decoder uses iterative technique so it can be used for more and more resolution. For N bit flash ADC most significant bit (MSB) of the thermometer to binary decoder output is logic one if more than half of the output in the thermometer scale is 1. Hence the MSB is same as thermometer output at level 2N - 1. To find MSB-1 the appropriate partial thermometer scale must be decoded. If the value of MSB is 1 then upper partial thermometer scale is chosen otherwise the lower partial thermometer scale is chosen. The MSB-1 bit is decoded in the same as MSB. This is repeated to get all the bits.

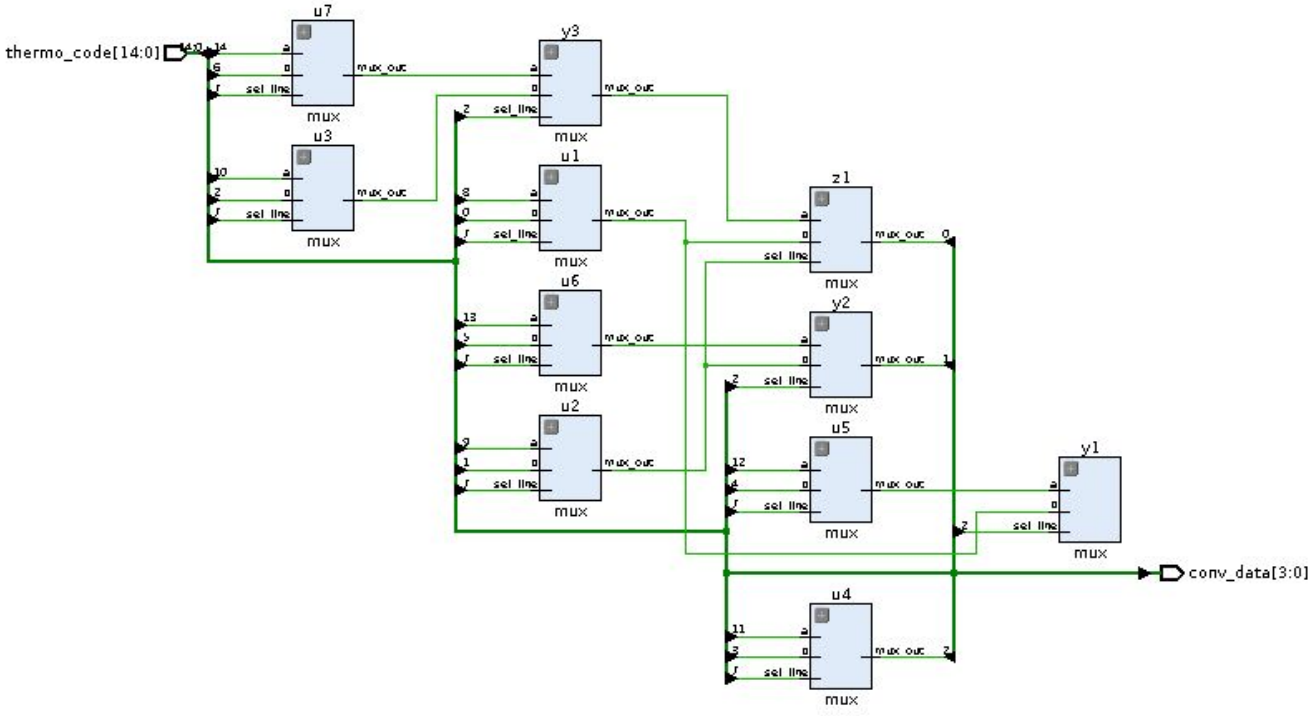


Fig4: Mux Based Decoder

Thermometer to Binary Conversion:

The basics of thermometer to binary code conversion can be understood by table1. In simple terms, the number of ones from the right of Thermometer code till the first zero is the decimal equivalent of the binary number to be obtained.

T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	B4	B3	B2	B1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0
1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table1: Thermometer to Binary Conversion

RESULTS AND ANALYSIS

The above described ADC has been tested for various values of input voltage and results of simulation for one input voltage has been shown in figure3 and figure5.
In the shown tested case, reference input has been taken as +5V and input voltage is equal to +3V.

Mathematical Conversion:

V_{in} = 3V
V_{ref} = 5V
N =4

For B3(MSB):

V' = 5/2 = 2.5 < 3 (V_{in})
=> B3 = 1

For B2:

V'' = $5/2^2$ = 1.25
V' = 2.5+1.25 = 3.75 > 3 (V_{in})
=> B2 = 0

For B1:

V'' = $5/2^3$ = 0.625
V' = 2.5+0.625 = 3.125 > 3 (V_{in})
=> B1 = 0

For B0(LSB):

V'' = $5/2^4$ = 0.3125
V' = 2.5+0.3125 = 2.8125 < 3 (V_{in})
=> B0 = 1

Desired Output is 1001
But from simulations the Output received = 1010
Voltage corresponding to 1010 = 3.125V
Error in output = 3.125-3.0 = 0.125V

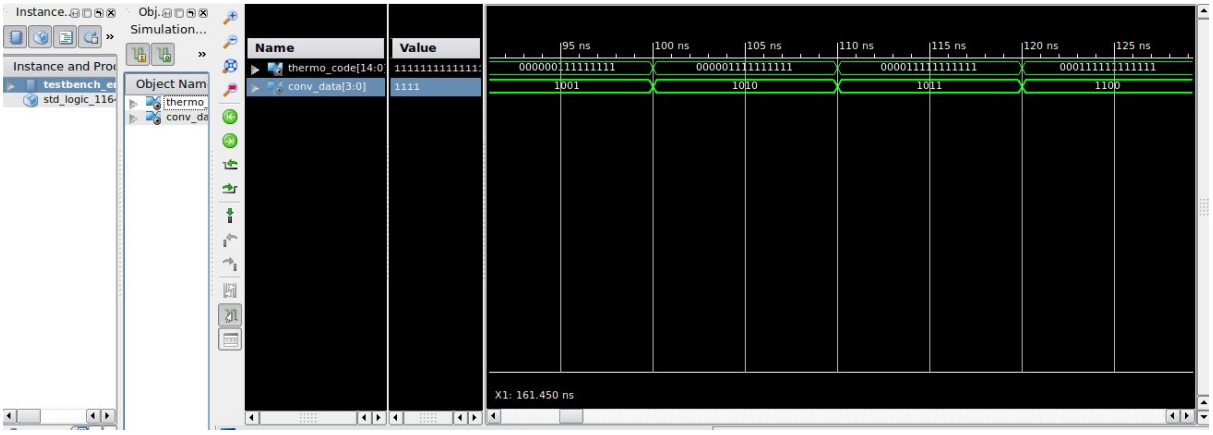


Figure5: Simulation results of thermometric output received from comparator stage

CONCLUSION

The above simulations shows that the proposed ADC design is accurate within the range of one step which is for this 4-bit ADC design is

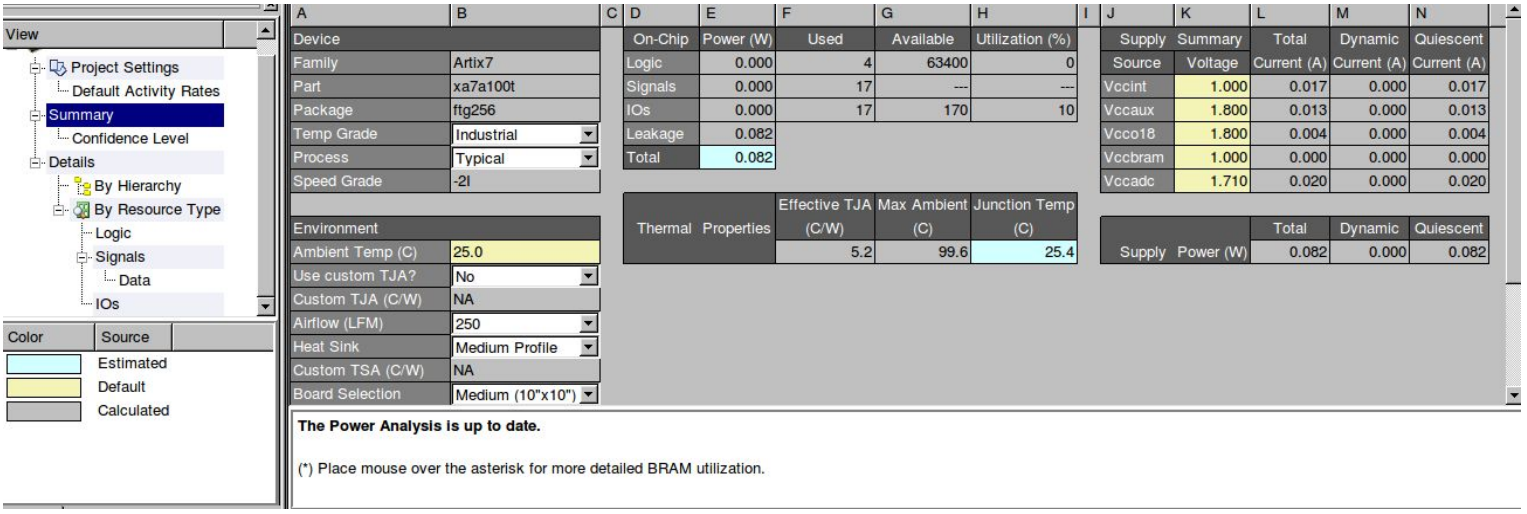
$$\varepsilon = [5/(2^4-1)] = 0.3333V$$

FUTURE SCOPE

The proposed design can further be improved by using Threshold Inverter Quantization(TIQ) Comparators for generating thermometer code. They improve the performance in terms of lesser area requirement on chip and low power dissipation with a constraint of having reference voltage of about 1V. Also, there is a scope for improving the encoding scheme by adding bubble error correction circuits. Also, resolution of the system can be improved by using 2 step ADC scheme with flash ADC in each step.

References

1. Sail, E., and Mark Vesterbacka. "A multiplexer based Decoder for flash analog - to - digital converters." TENCON 2004. 2004 IEEE Region 10 Conference.
   Vol.500. IEEE, 2004.
2. https://www.researchgate.net/publication/274713910_Thermometer_to_Gray_Encoders
3. Design and Implementation of a 5-Bit Flash ADC for Education
4. Design of Flash ADC using Improved Comparator Scheme.




```
*                            Design Summary                                   *
================================================================================

Top Level Output File Name         : Design_encoder.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 6
#      LUT3                        : 2
#      LUT5                        : 3
#      MUXF7                       : 1
# IO Buffers                       : 17
#      IBUF                        : 13
#      OBUF                        : 4

Device utilization summary:
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Selected Device : xa7a100tftg256-2i


Slice Logic Utilization:
 Number of Slice LUTs:                  5  out of  63400     0%
    Number used as Logic:               5  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    5
   Number with an unused Flip Flop:     5  out of      5   100%
   Number with an unused LUT:           0  out of      5     0%
   Number of fully used LUT-FF pairs:   0  out of      5     0%
```