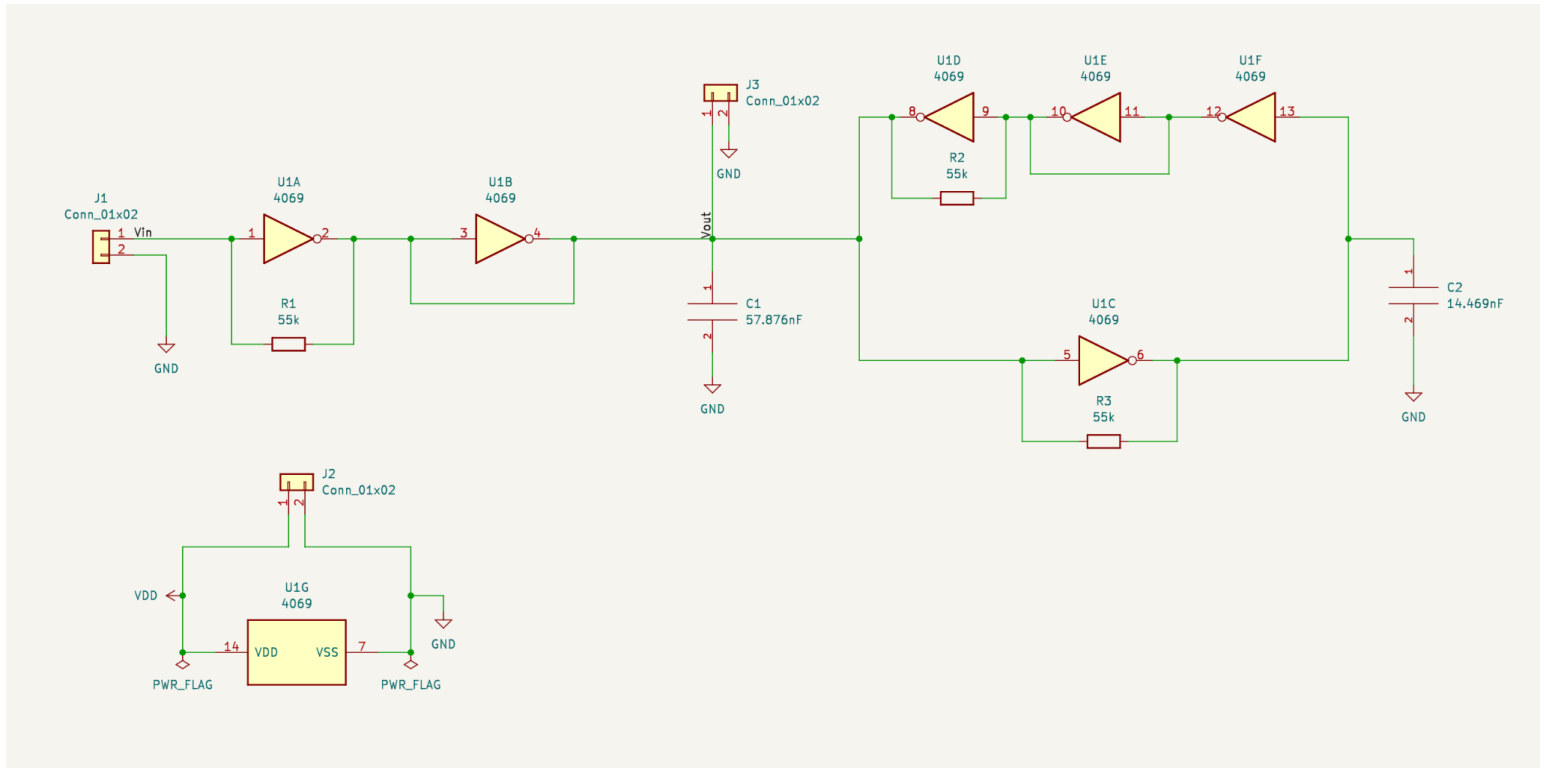


Experiment 3: PCB Design

Name- Pushkal Mishra
Roll- EE20BTECH11042

1. Schematic used



2. Layout

2.1 Specifics

Two layered PCB and uses copper as conductor in both layers.

2.2 Components and Footprints Used

- One CD4069 IC - Package_DIP:DIP-14_W7.62mm
- Three Resistors - 55k Ω each

Footprint - Resistor_THT:R_Axial_DIN0411_L9.9mm_D3.6mm_P5.08mm_Vertical

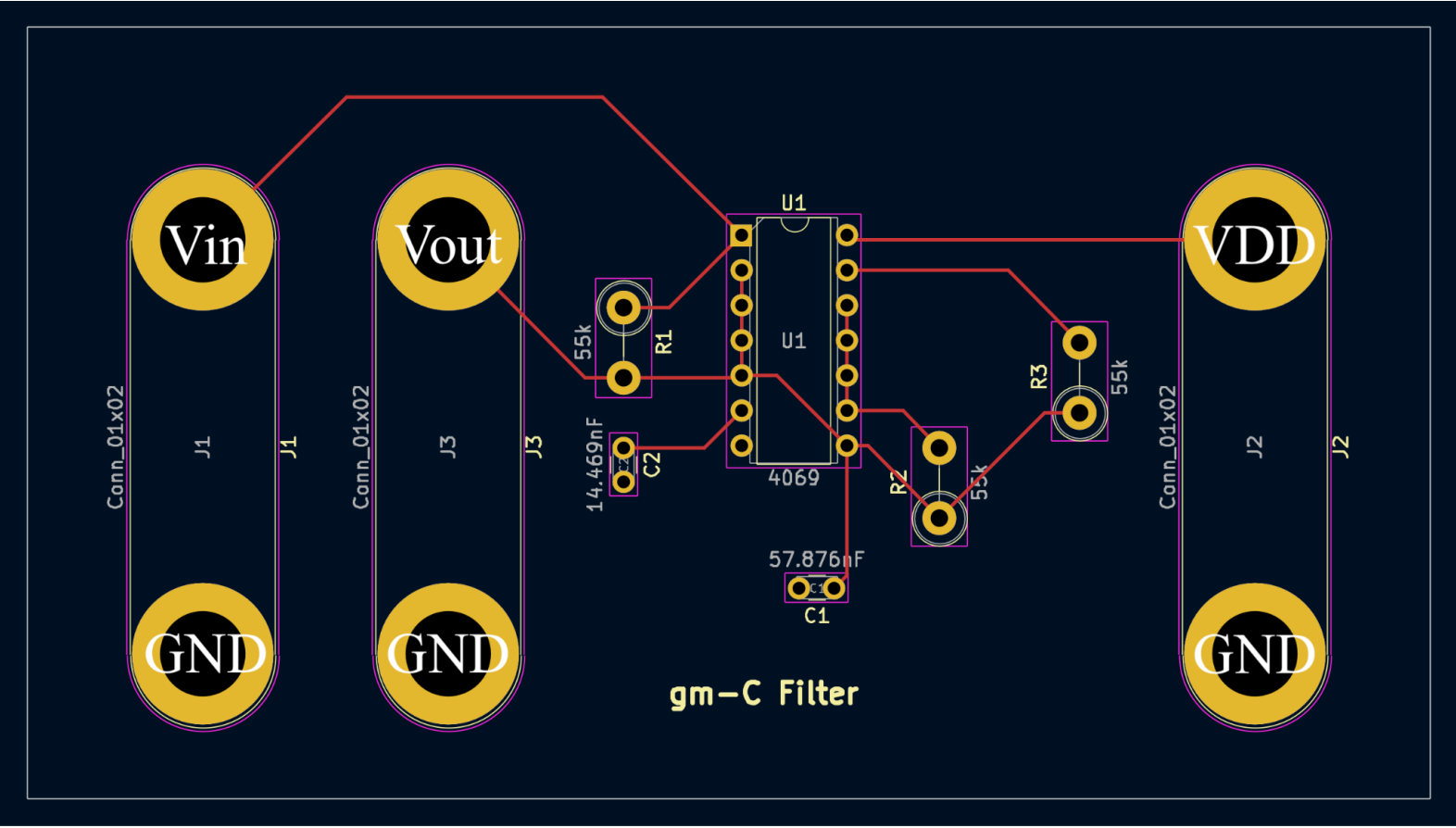
- Three 01x02 connectors - Connector:Banana_Jack_2Pin
- Two capacitors - 57.876 nF and 14.469 nF

Footprint - Capacitor_THT:C_Disc_D3.0mm_W1.6mm_P2.50mm

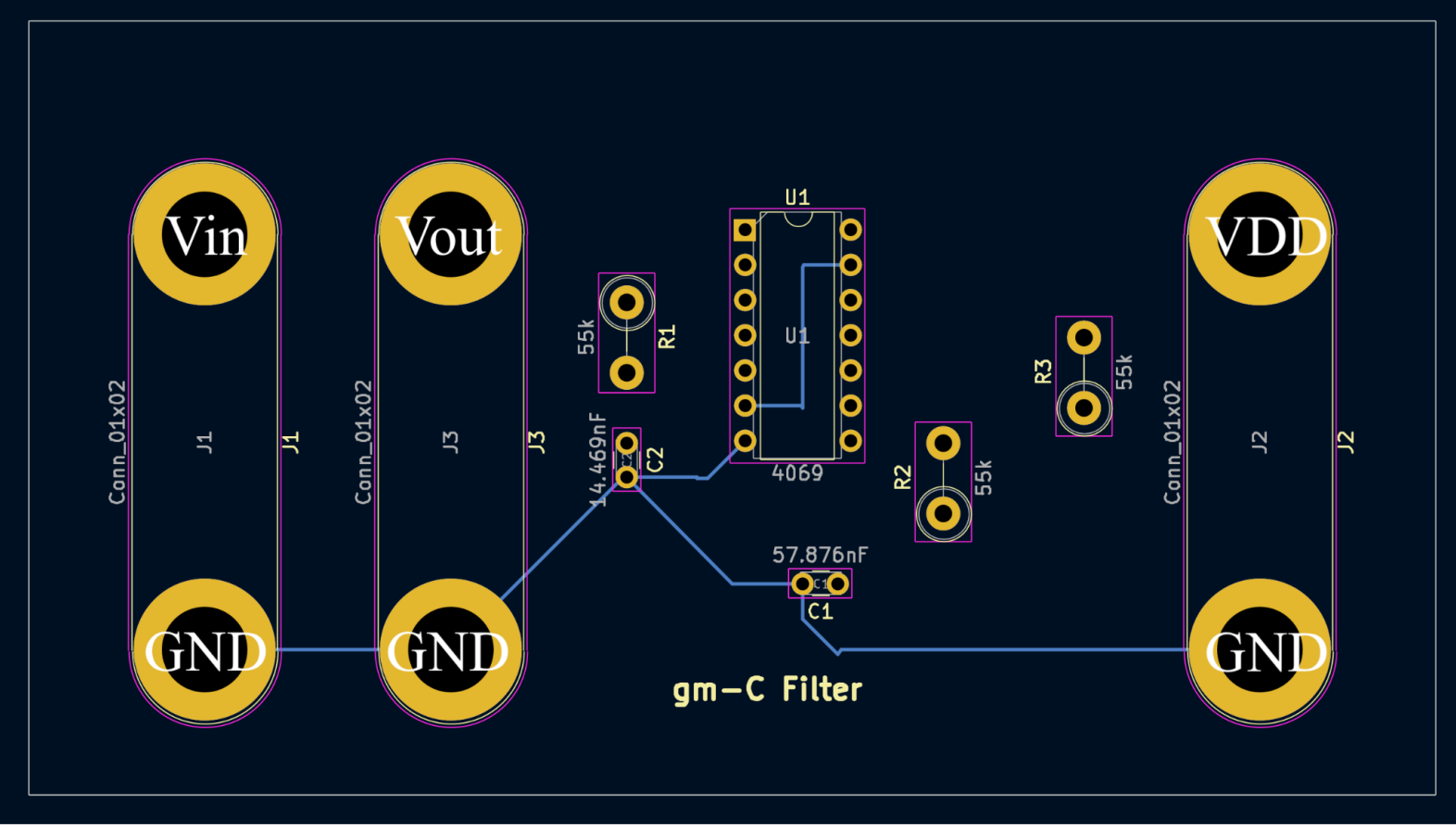
Ceramic capacitors are used here because they can have low capacitances.

3. PCB Editor Views

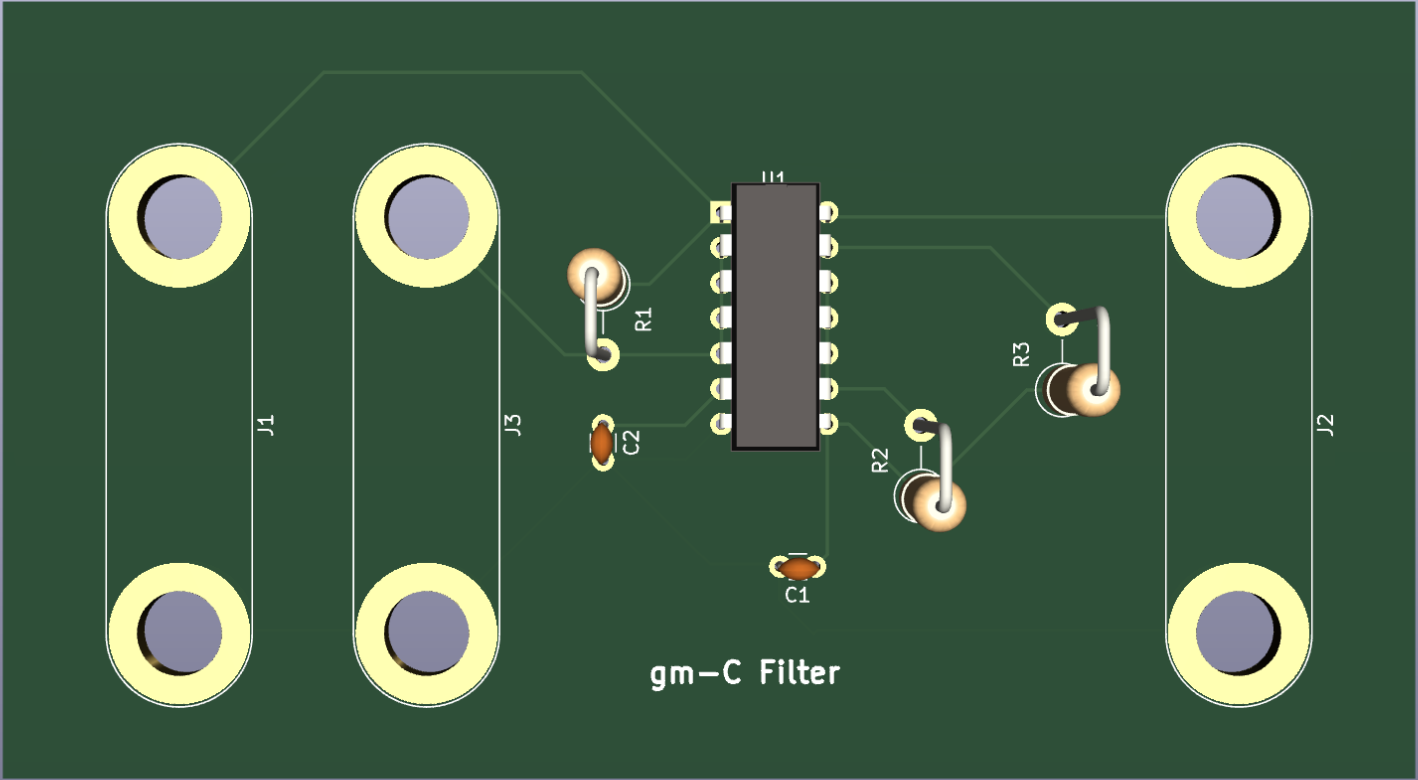
3.1 Front Layer (used red color for wires)



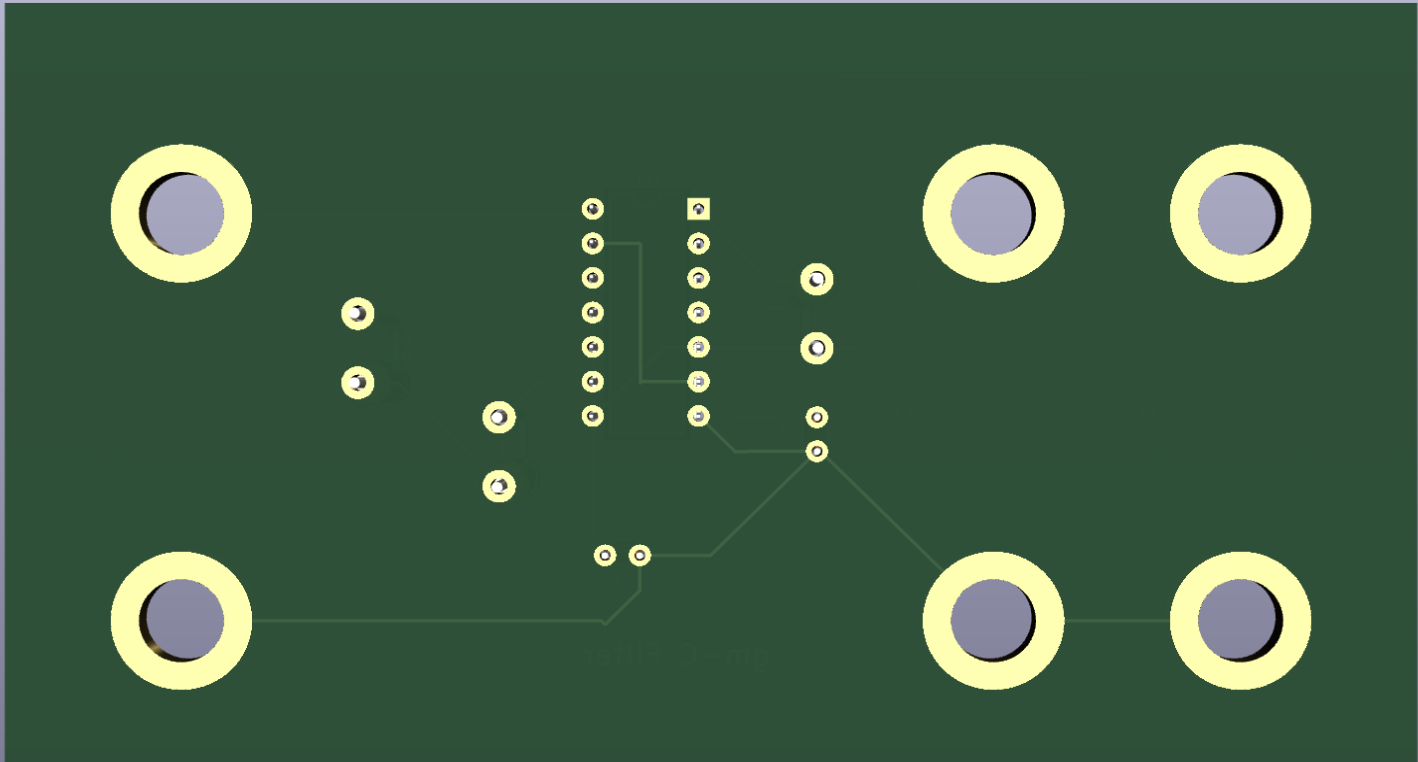
3.2 Back layer (used blue color for wires)



3.3 Front View in 3D



3.4 Back View in 3D



3.5 Other Views in 3D

