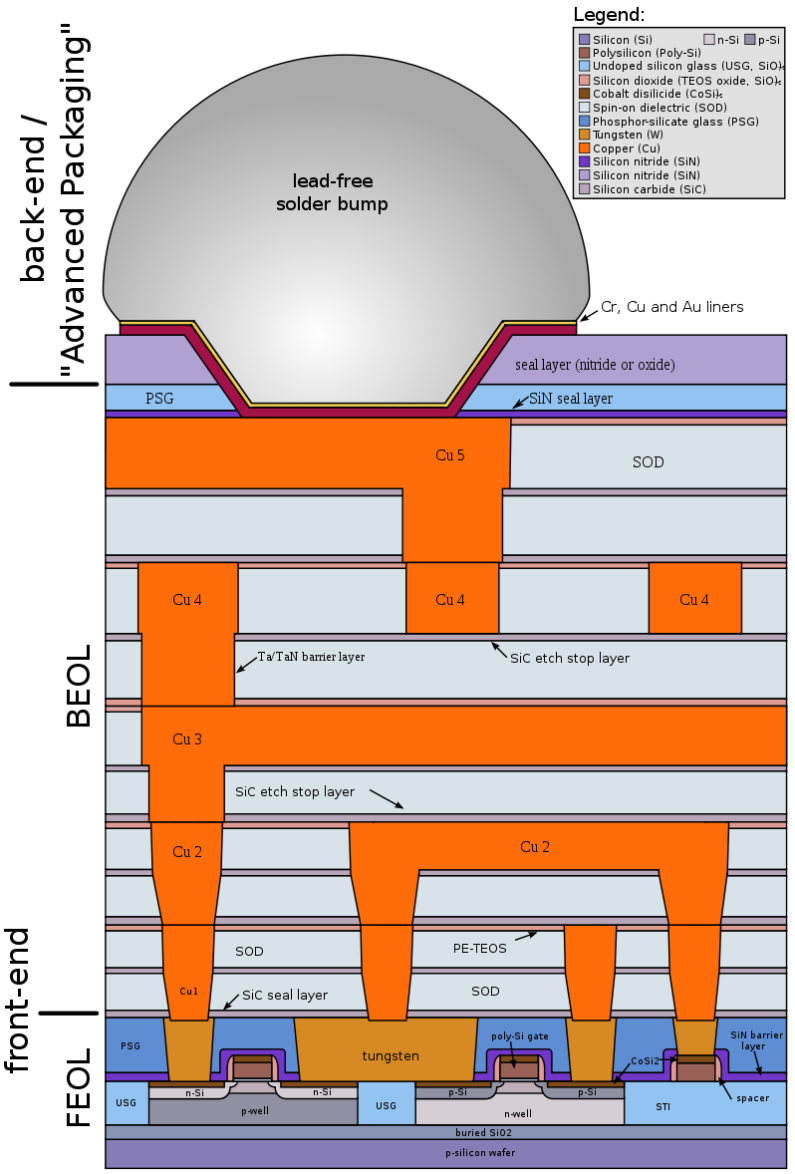
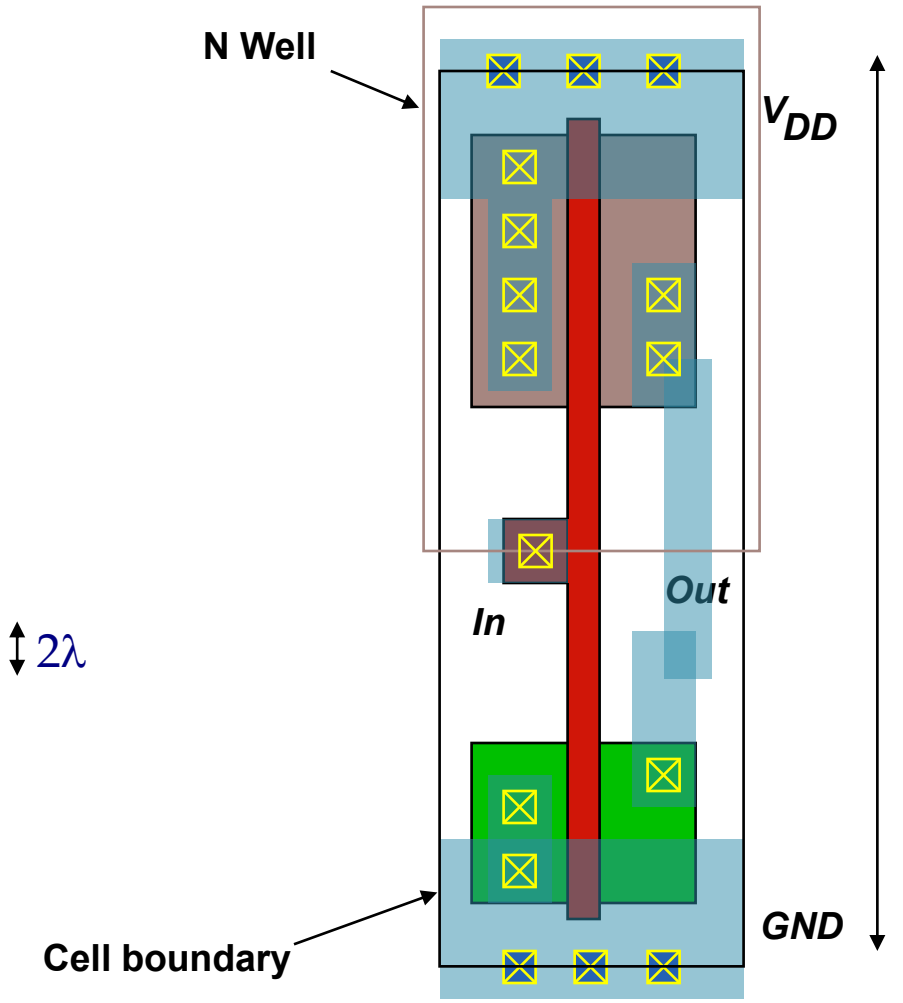
CAD Design to Chips ..



CAD Design to Chips ..

- Standard Cells
  - General Purpose Logic
  - Used to synthesize RTL
  - Same height, varying width
  - Most common
- Datapath Cells
  - For structured designs (adders, multiplexers, etc)
  - Same width and varying height

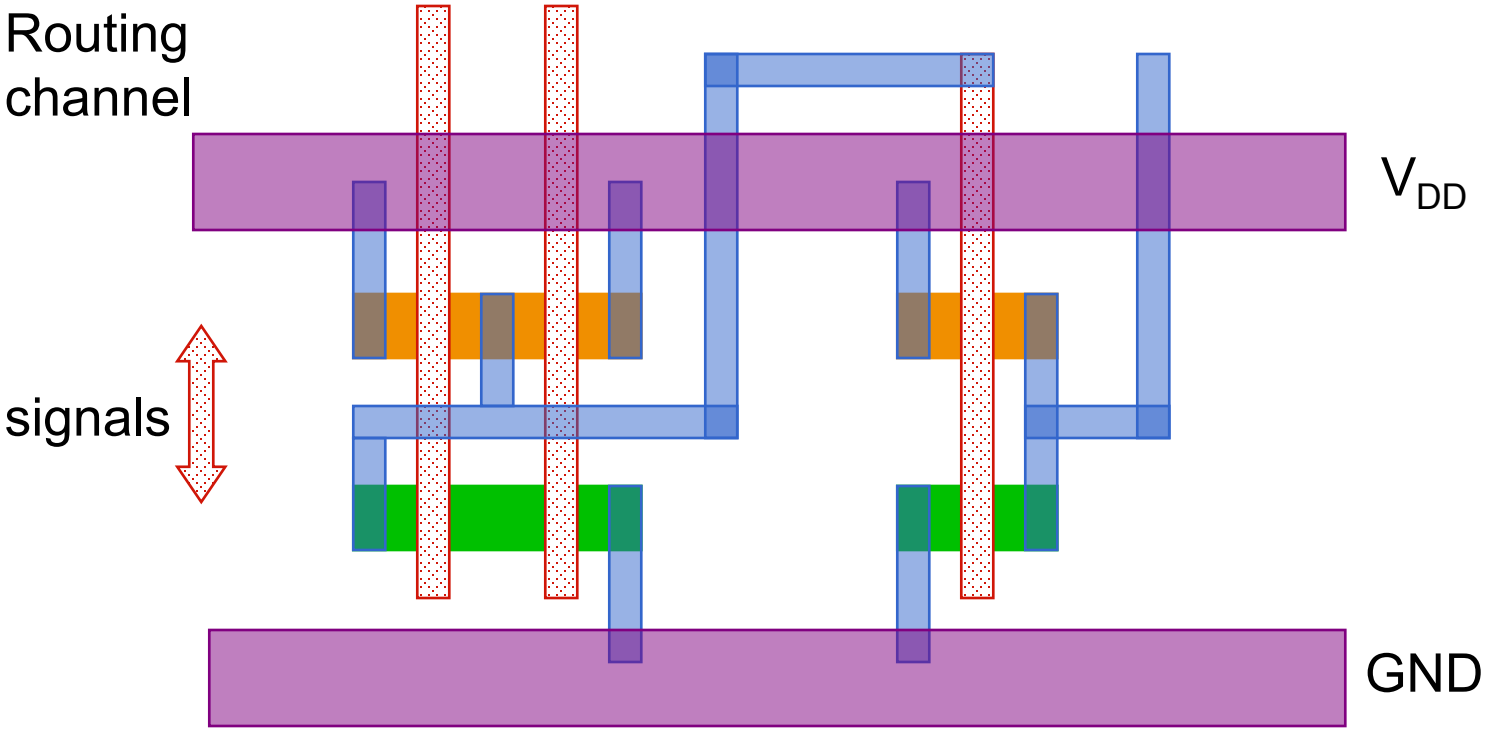
Standard Cell Approach



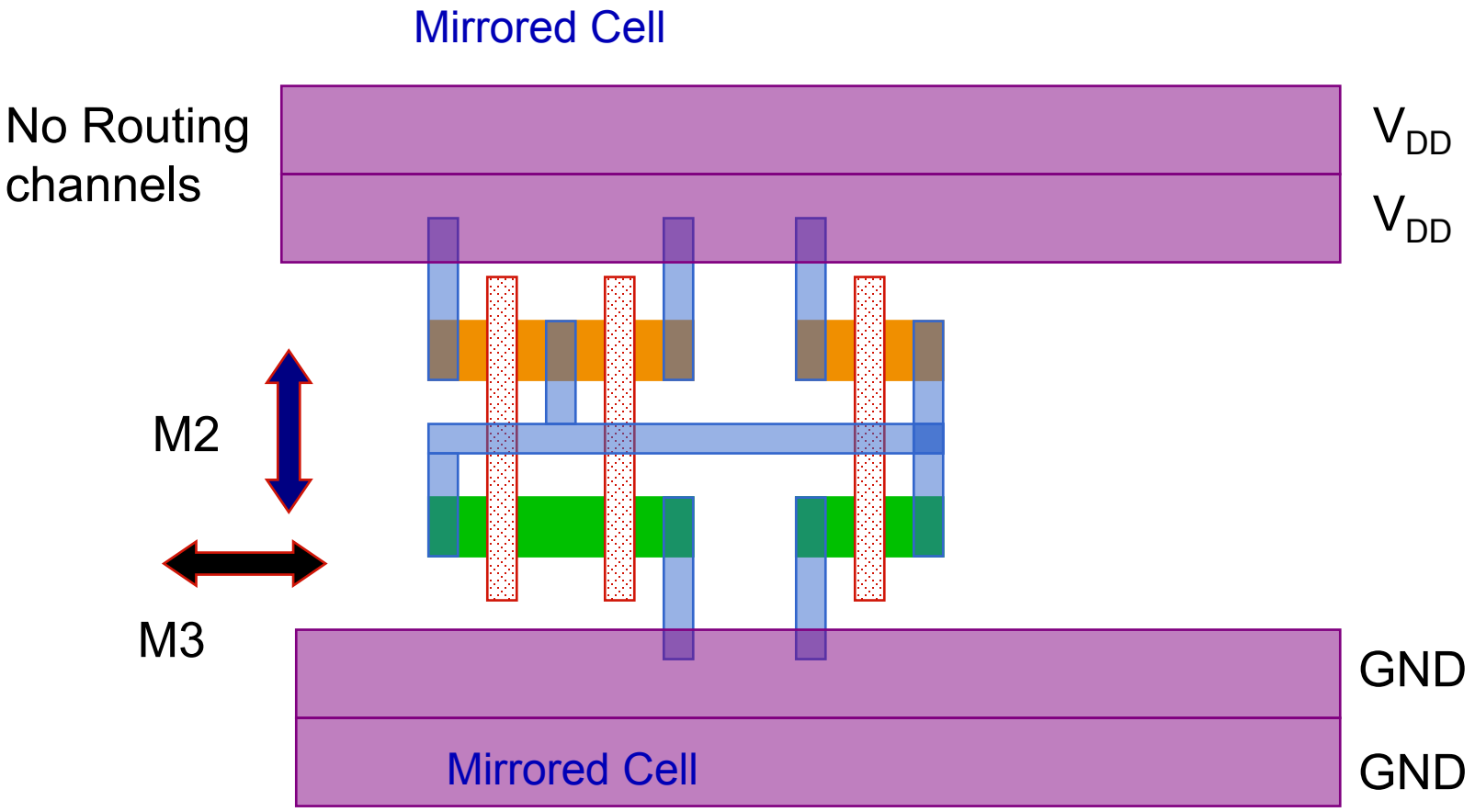
Cell height 12 metal tracks
Metal track is approx. 3λ + 3λ
Pitch = repetitive distance between objects

Rails ~10λ

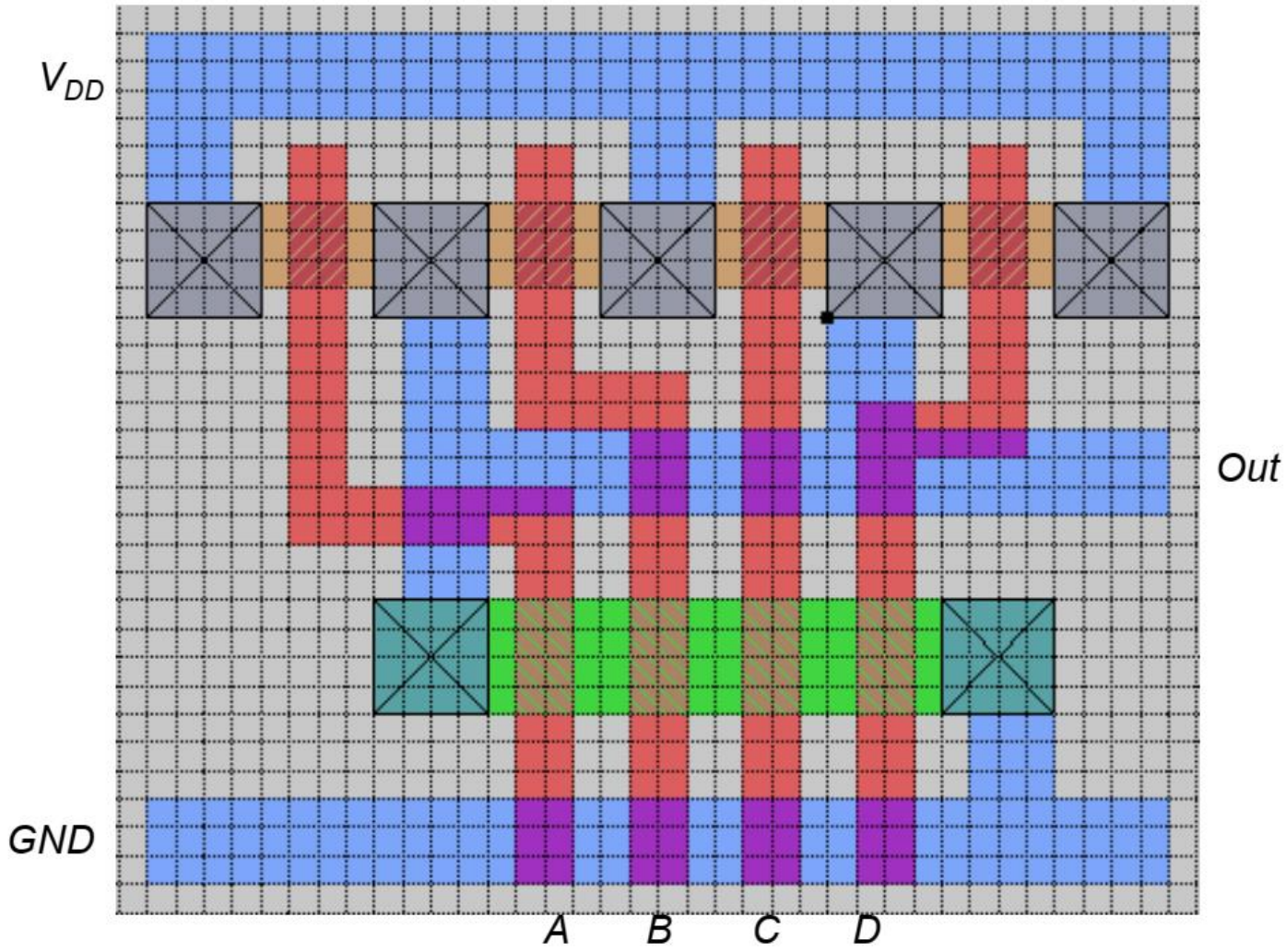
Standard Cell Layout Methodology – 1980s



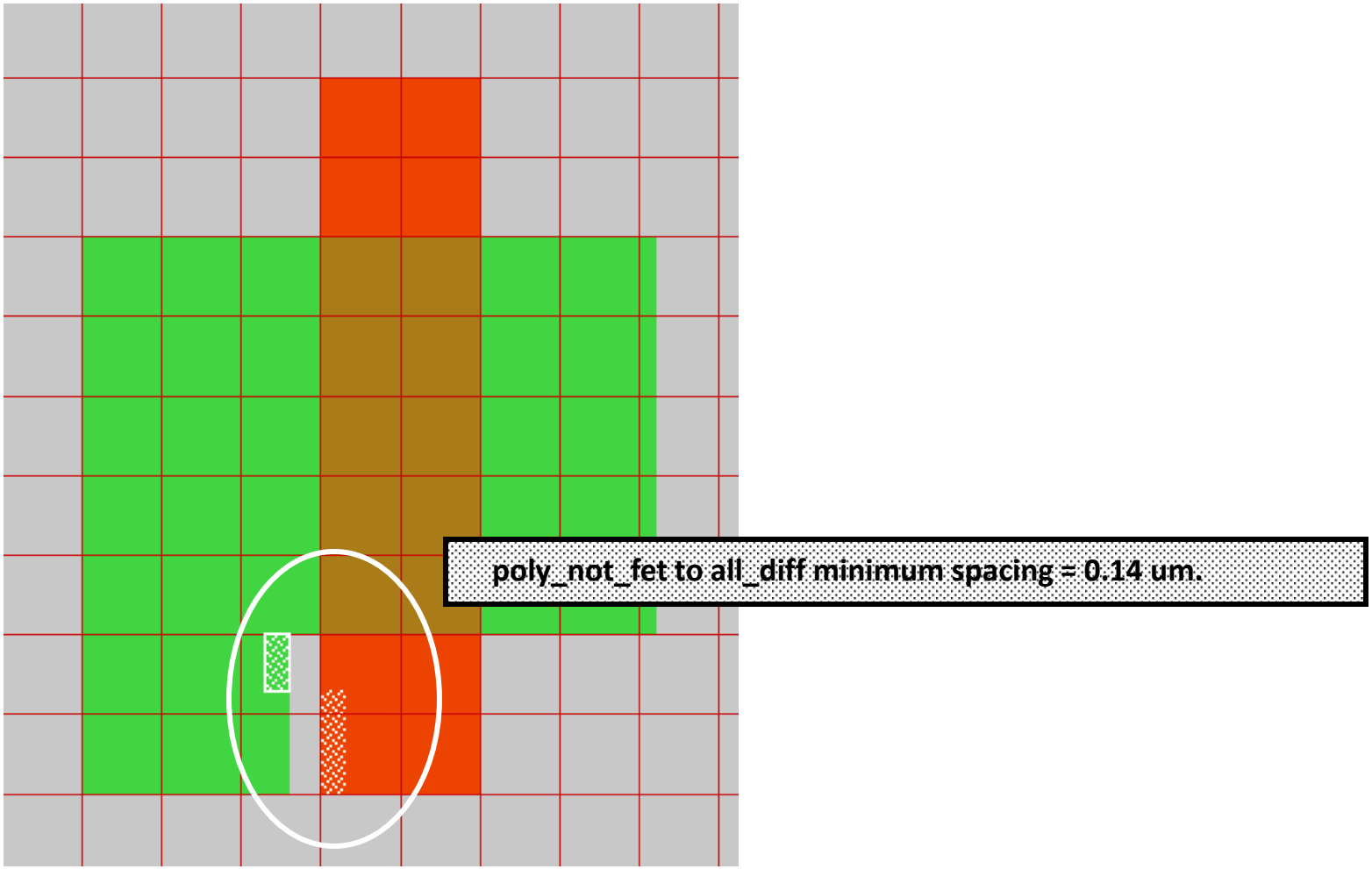
Standard Cell Layout Methodology – 1990s



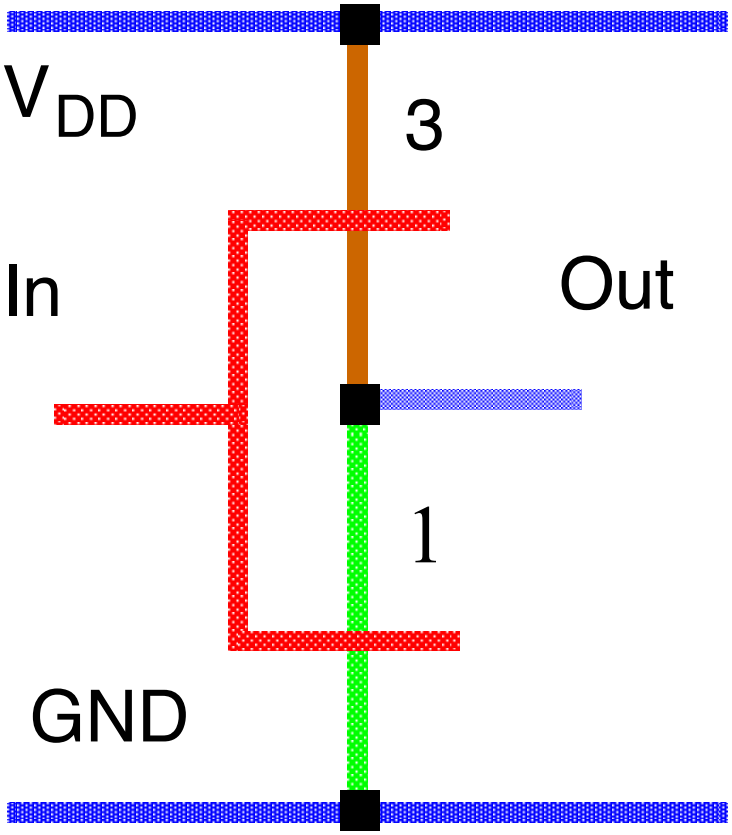
Nand Gate – Standard cell approach



Design Rule Checking (DRC)



Stick Diagram

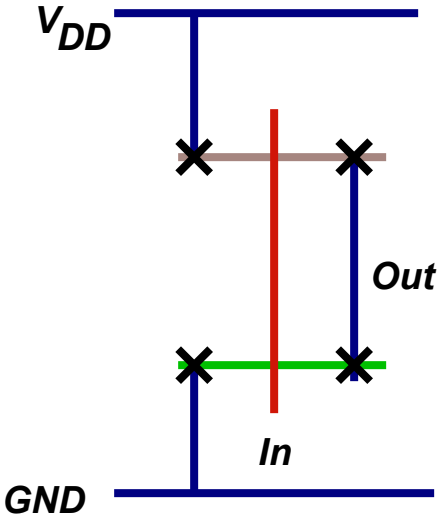


Stick diagram of inverter

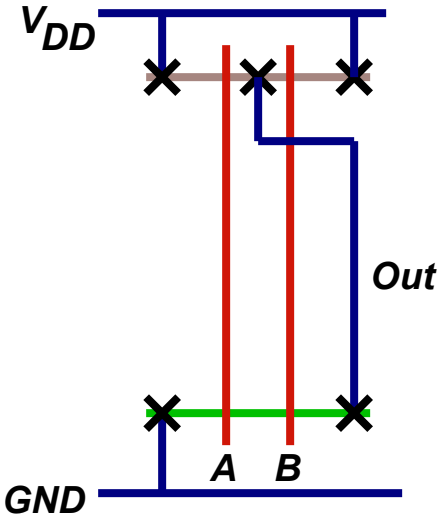
- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program

The Stick Diagrams

Inverter

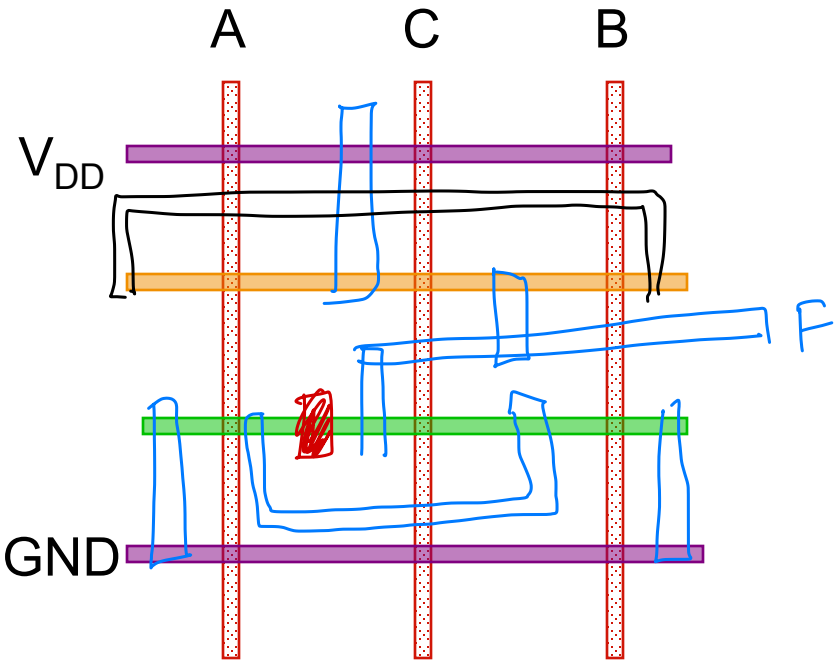


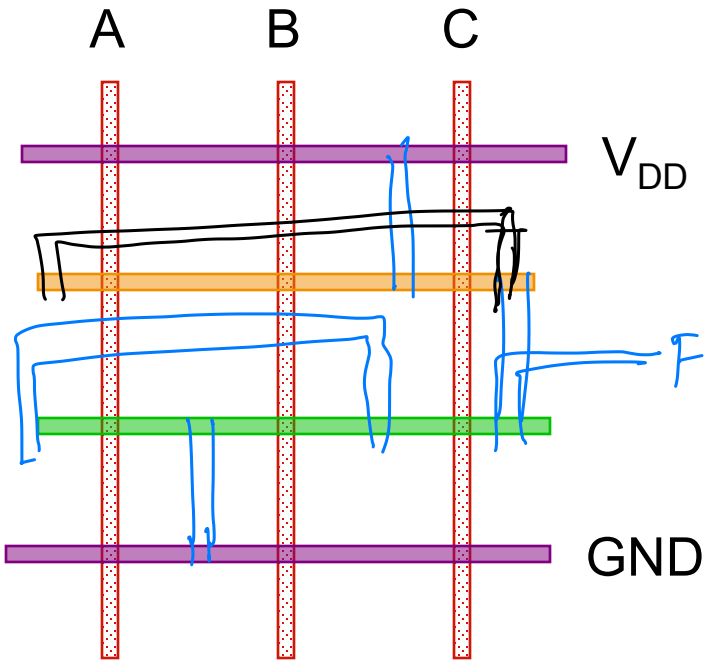
NAND2

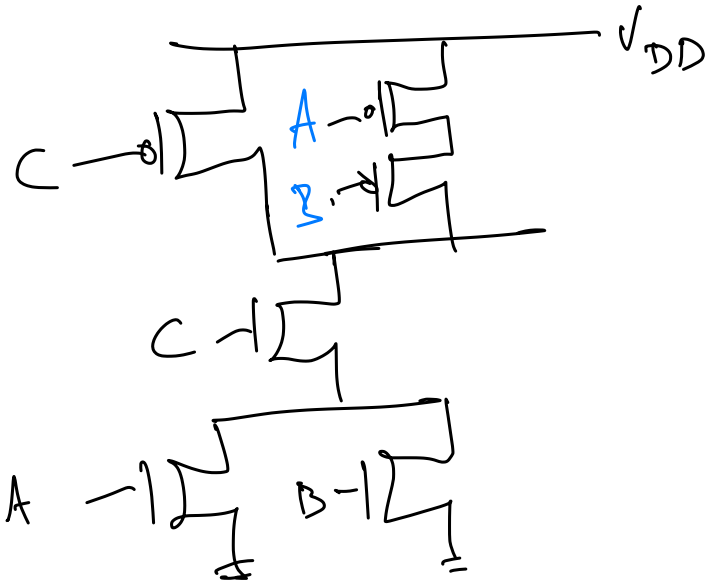


Contains no dimensions
Represents relative positions of transistors
Only topology is important
Final layout generated by “compaction” program

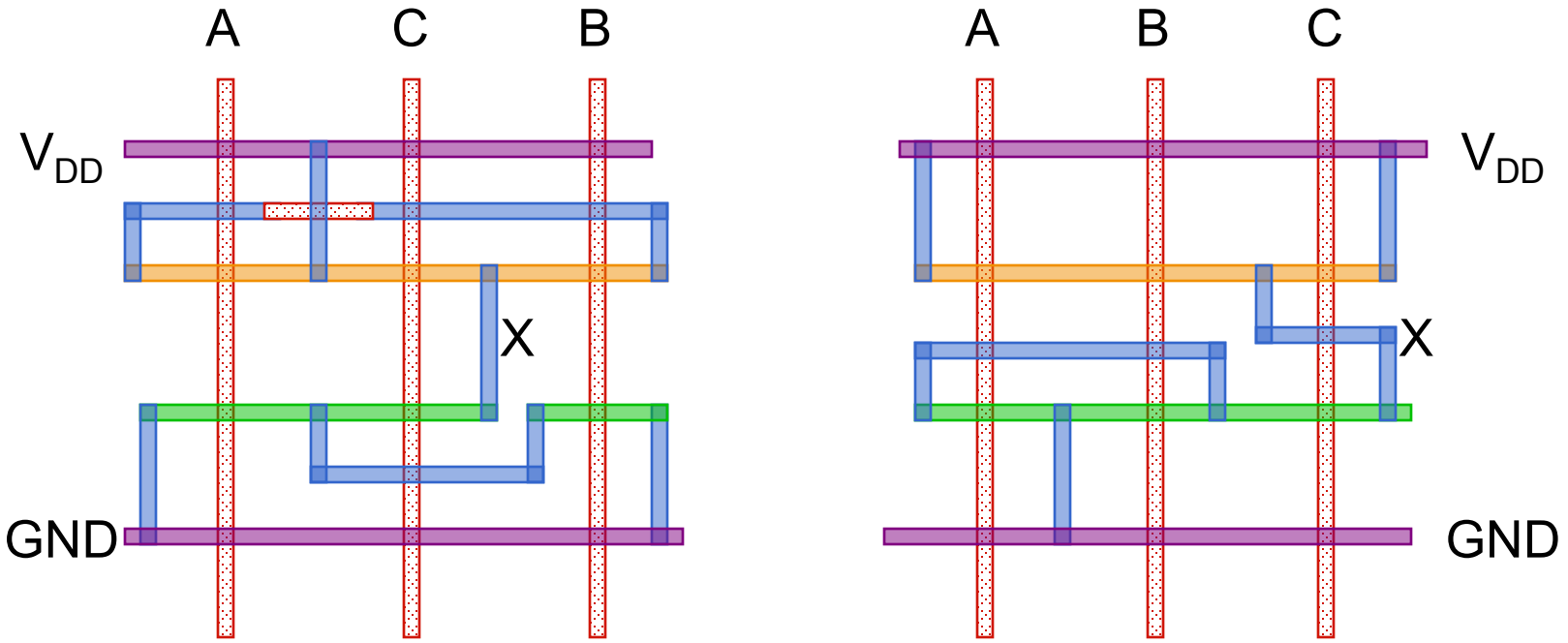
Two versions of $\overline{C.(A+B)}$







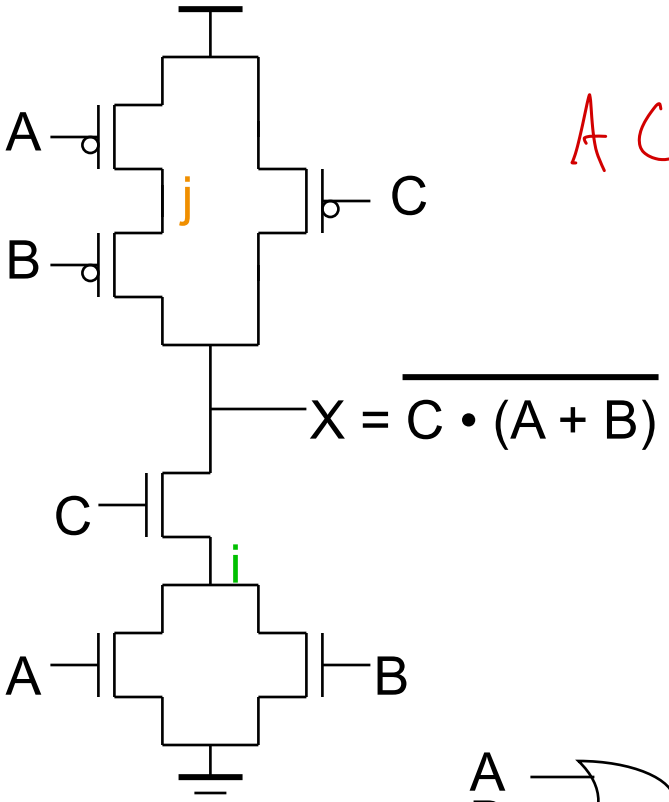
Two versions of C.(A+B)



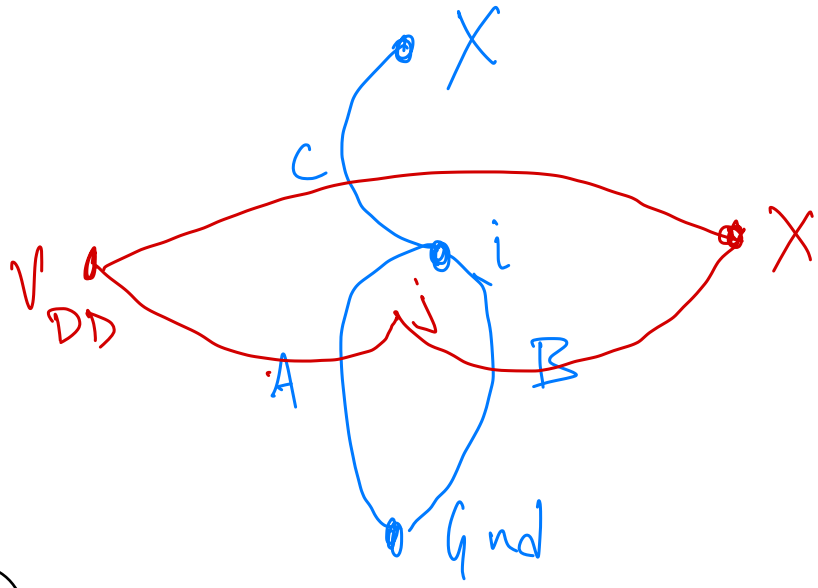
- Suggestions for efficient layout planning
  - Gate signals vertical, Supply rails and diffusion areas horizontal
  - M1 and M2 are perpendicular to each other, and so on (violated above)
  - Plan the ordering of inputs using logic graphs and identify Euler path

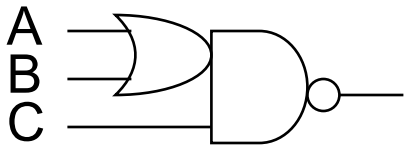
The Logic Graphs

Use edges and nodes to symbolically represent the circuit



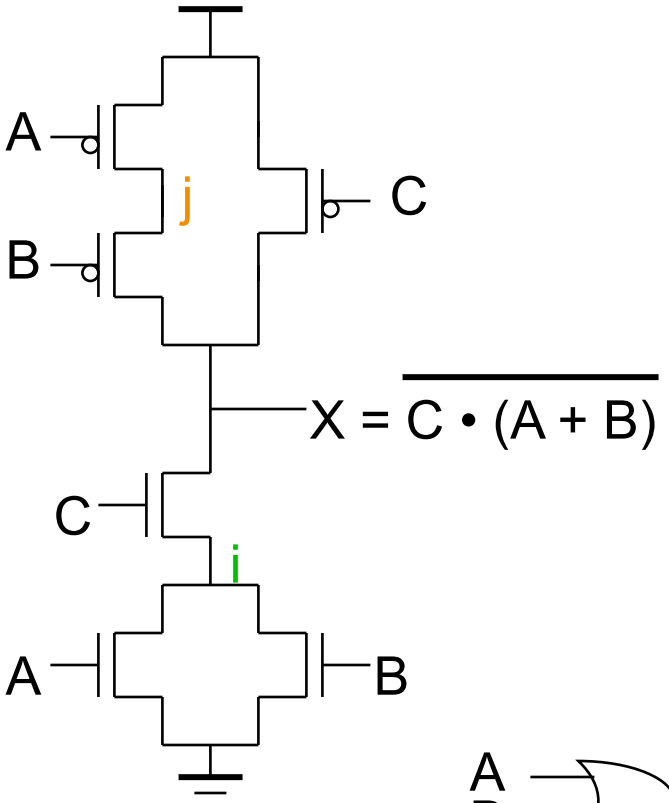
A C B A B C

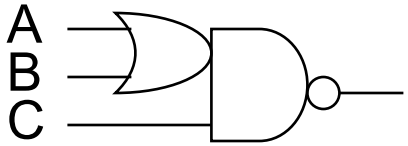


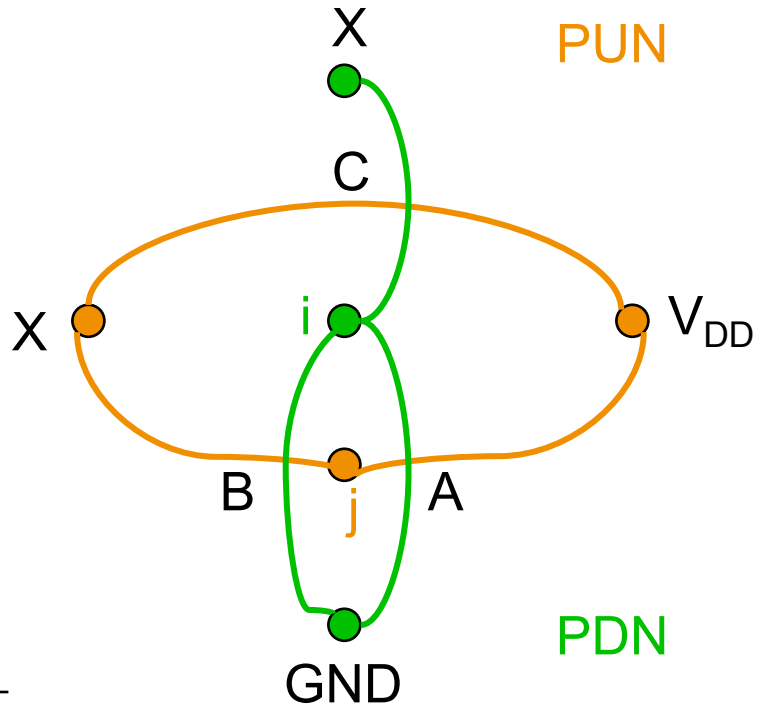


The Logic Graphs

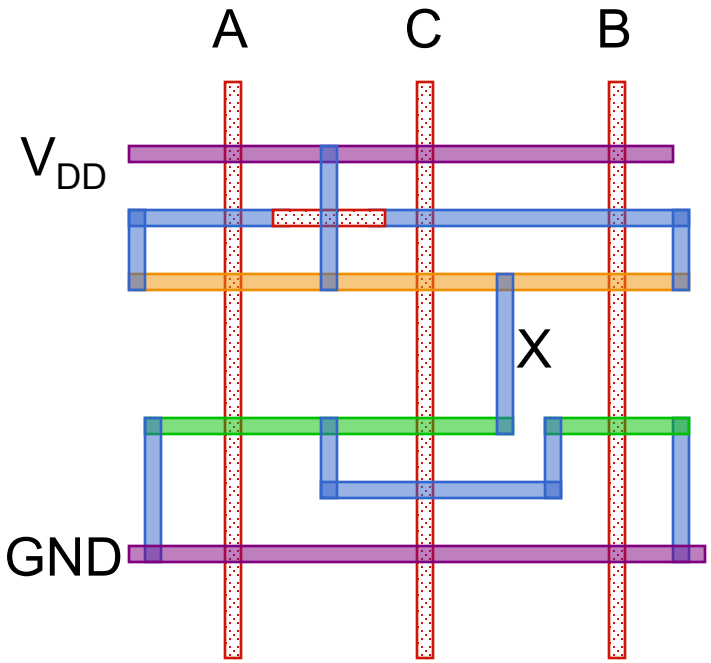
Use edges and nodes to symbolically represent the circuit

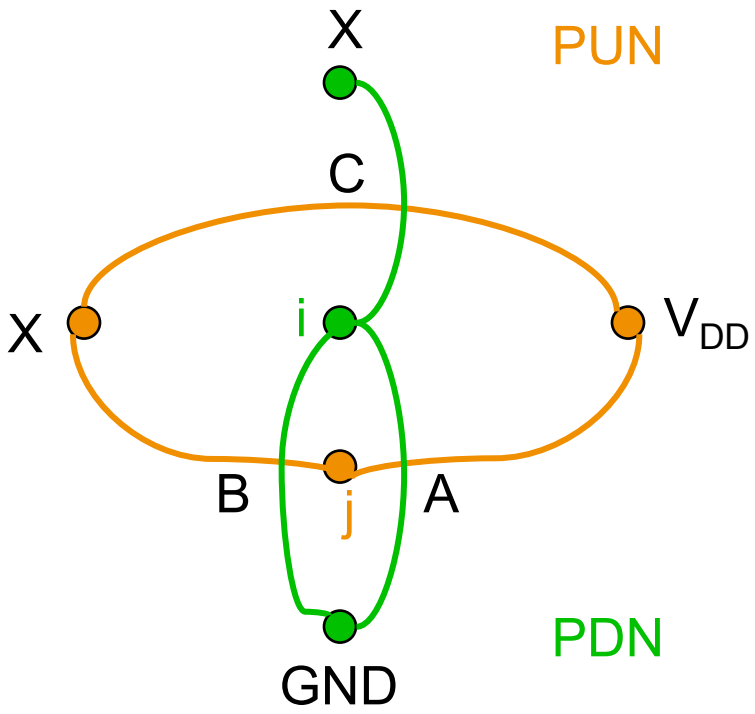




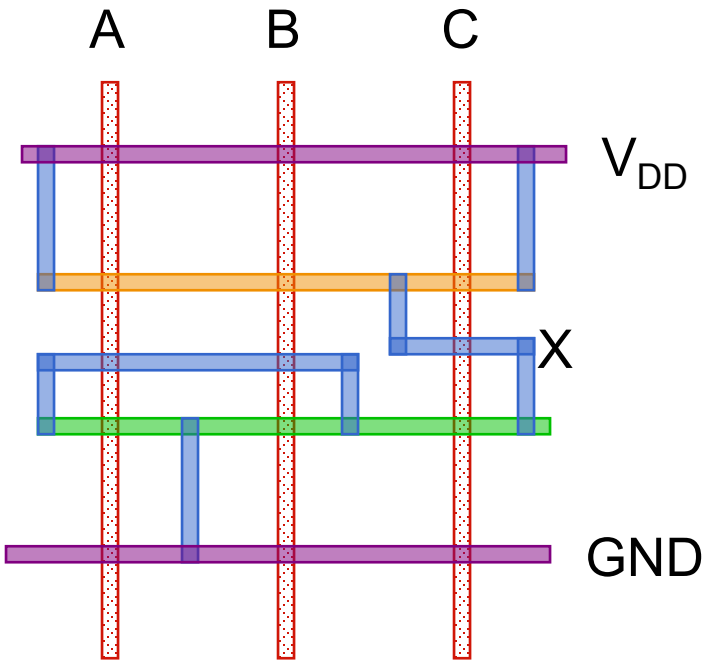


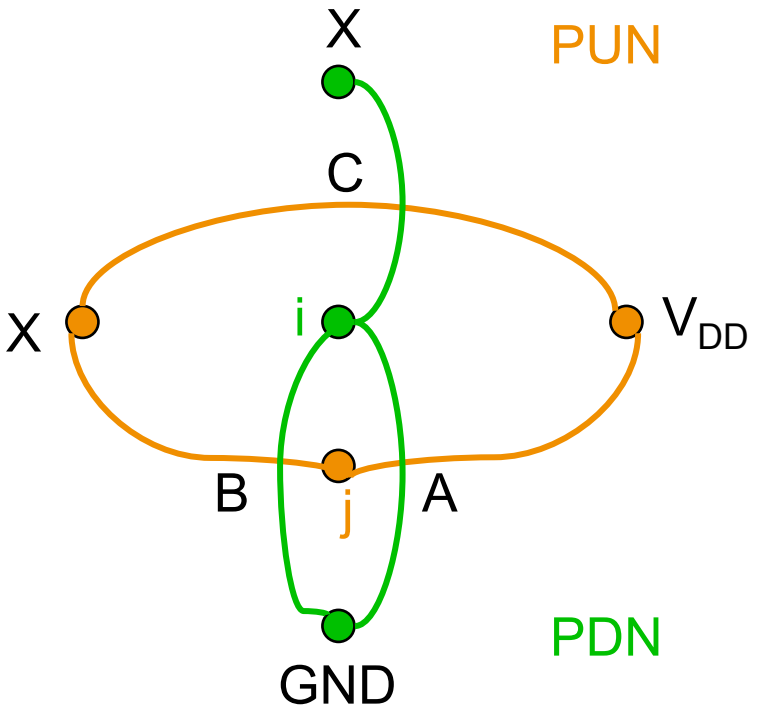
Two versions of $\overline{C.(A+B)}$



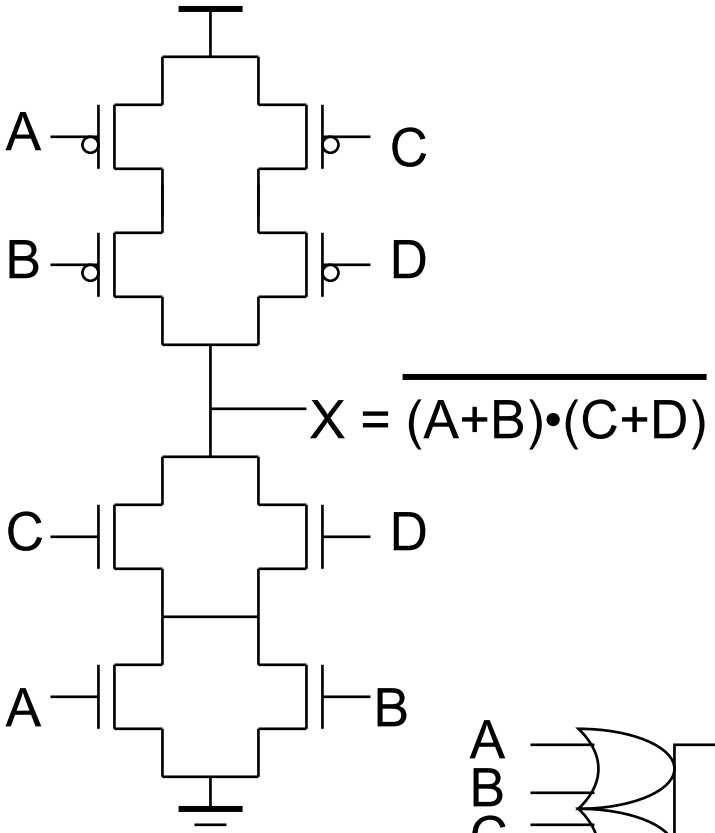


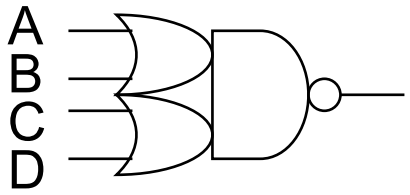
Two versions of C.(A+B)

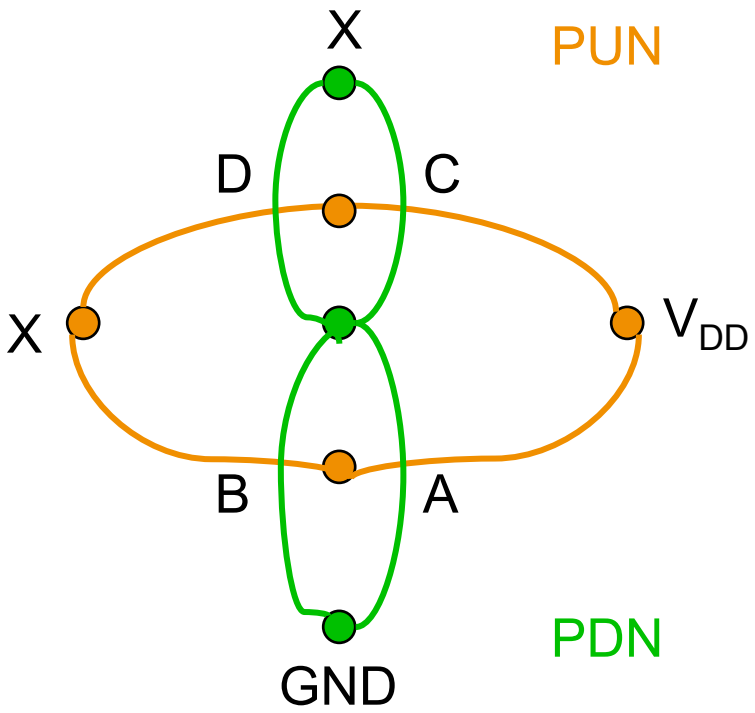




OAI22 Logic Graph

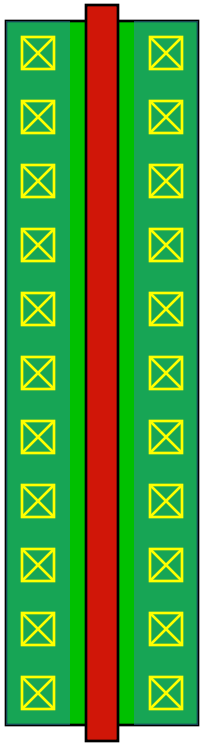




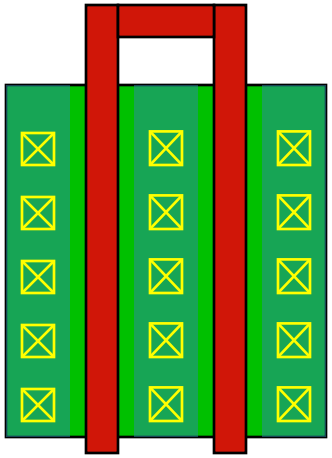


Multifingered Transistors

One finger



Two fingers (folded)



Less diffusion capacitance