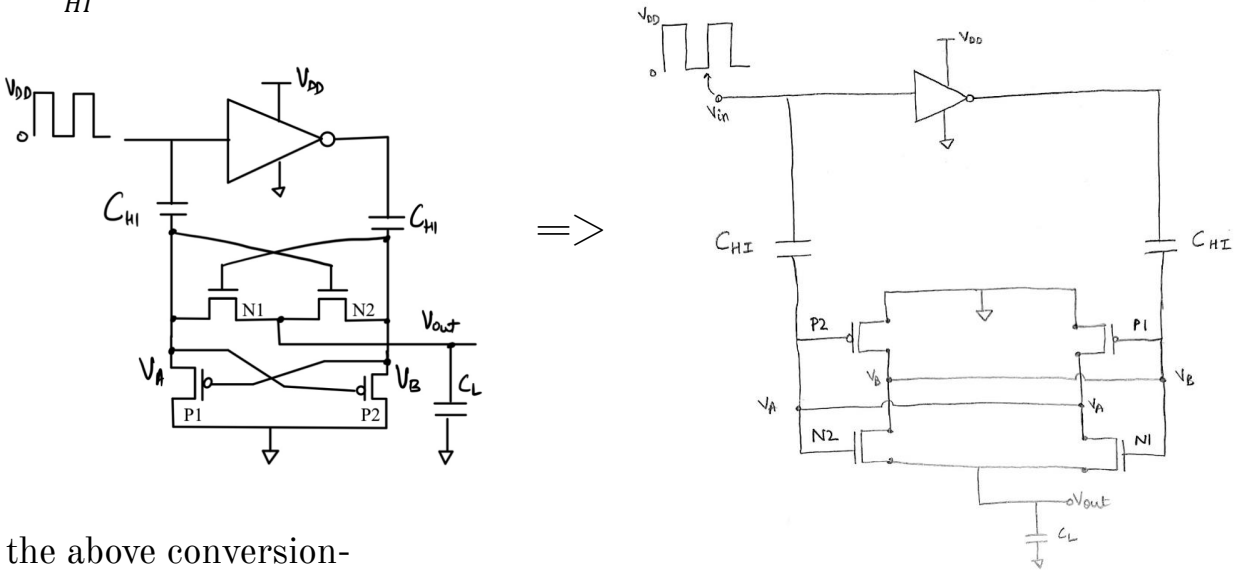
2. To construct given circuit with

Clock Frequency: $f_o = 10kHz$

Supply Voltage: $V_{DD} = 5V$

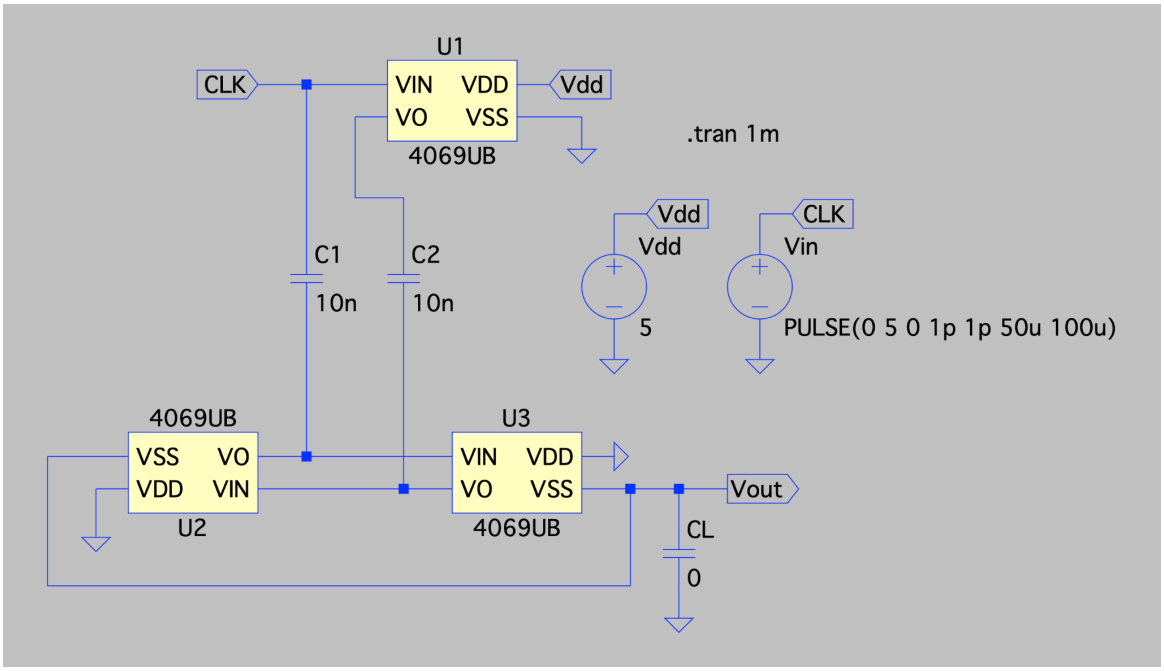
Capacitors: $C_{HI} = 10nF$



Steps for the above conversion-

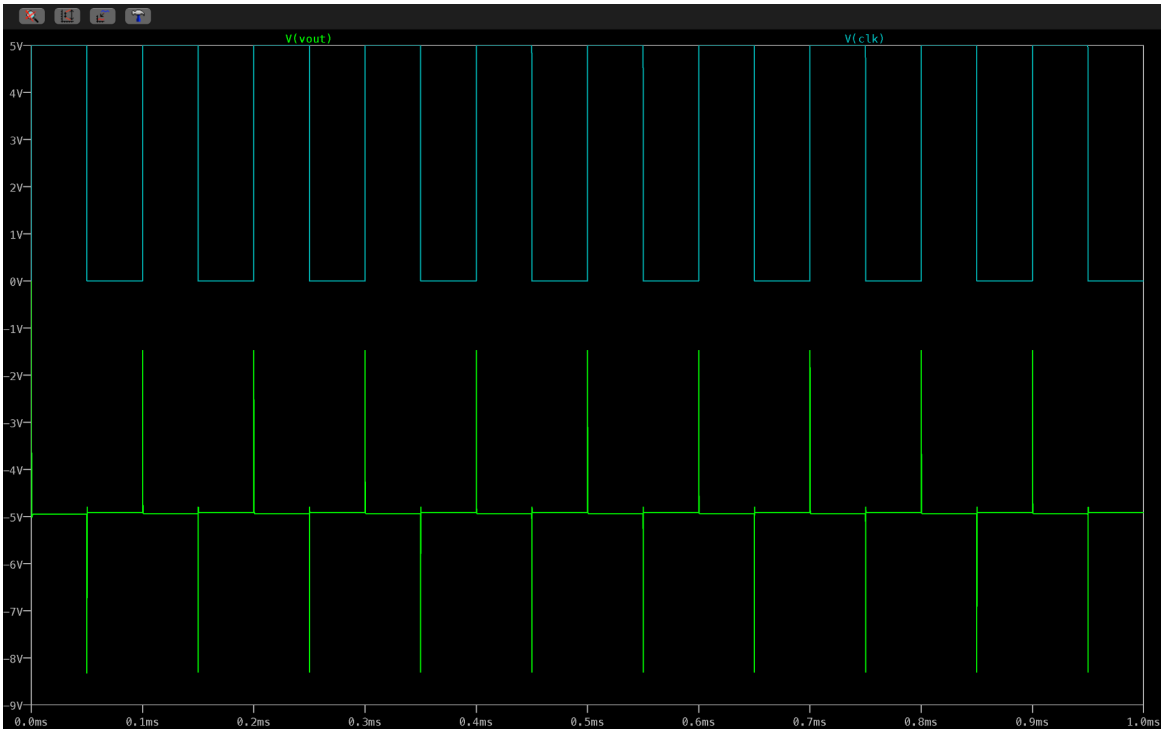
1) Observe that P1 and N1 have the same
   a) Gate voltages V_B
   b) One common terminal connected with V_A
2) Observe that P2 and N2 have the same
   a) Gate voltages V_A
   b) One common terminal connected with V_B
3) P1 and P2 both have one terminal grounded
4) N1 and N2 both have one terminal as V_{out}
5) Now construct the circuit as shown with the help of above observations

Implementation in LTSpice for $C_L = 0F$



Since C_L = 0F, from the formula q = CV we get that q is always 0 irrespective of V which means that no current can flow through C_L and it acts as an open circuit.

Output Plot

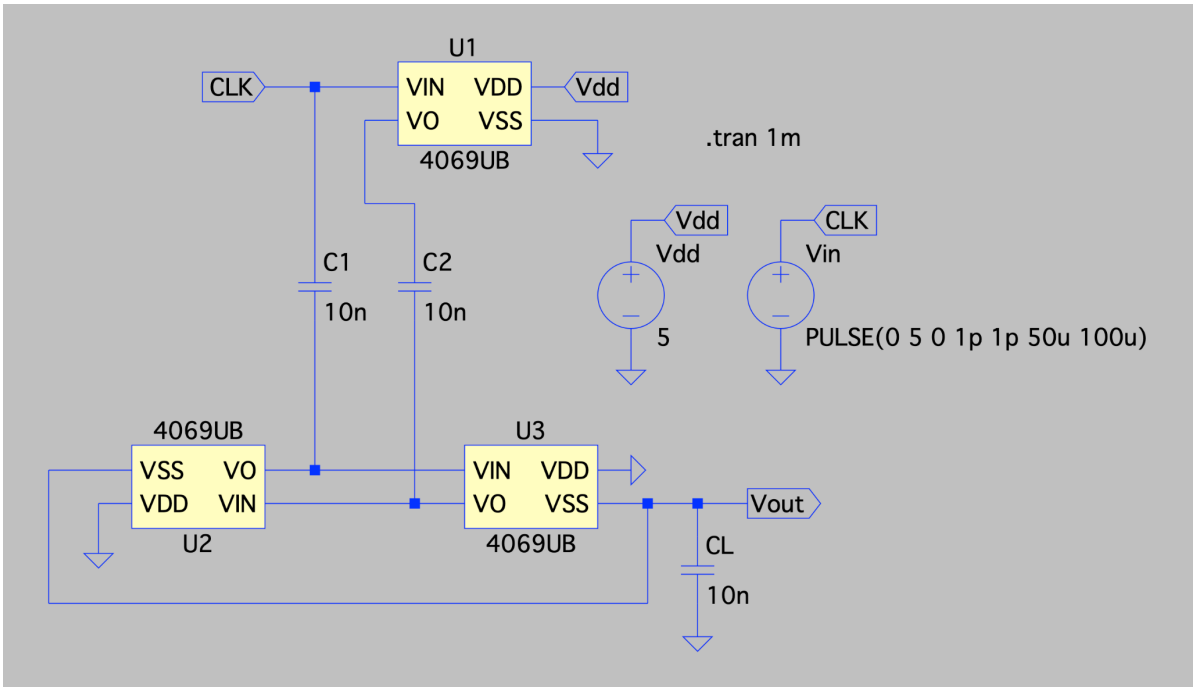


Both CMOS inverters act as switches connecting V_{out} to either V_A or V_B depending on CLK, essentially it either enables or disables the inverters. Also at steady state, both capacitors are charged to 5V.

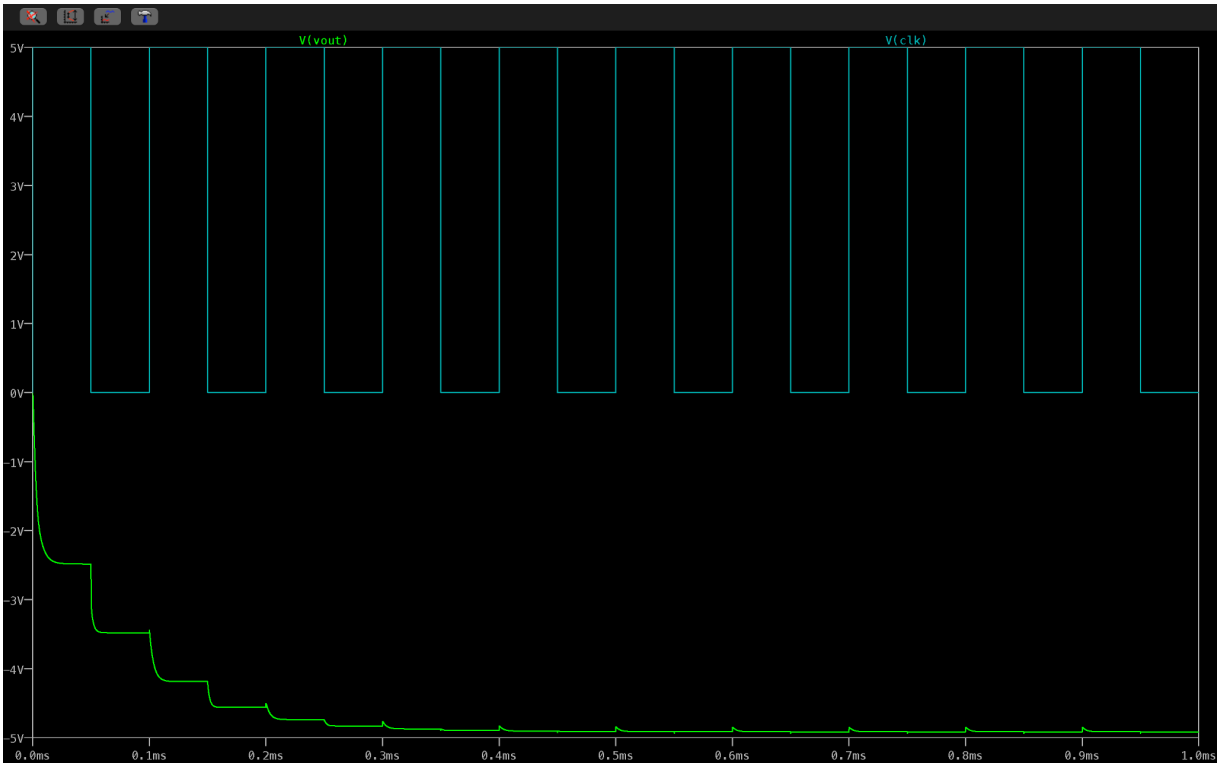
The average voltage is not exactly -5V due to the non-idealities in the MOSFETs.

There are spikes in the output waveform when clock changes it's value and that is due to the fact that the MOSFETs require finite time to change their region of operation.

Implementation in LTSpice for C_L = 10nF

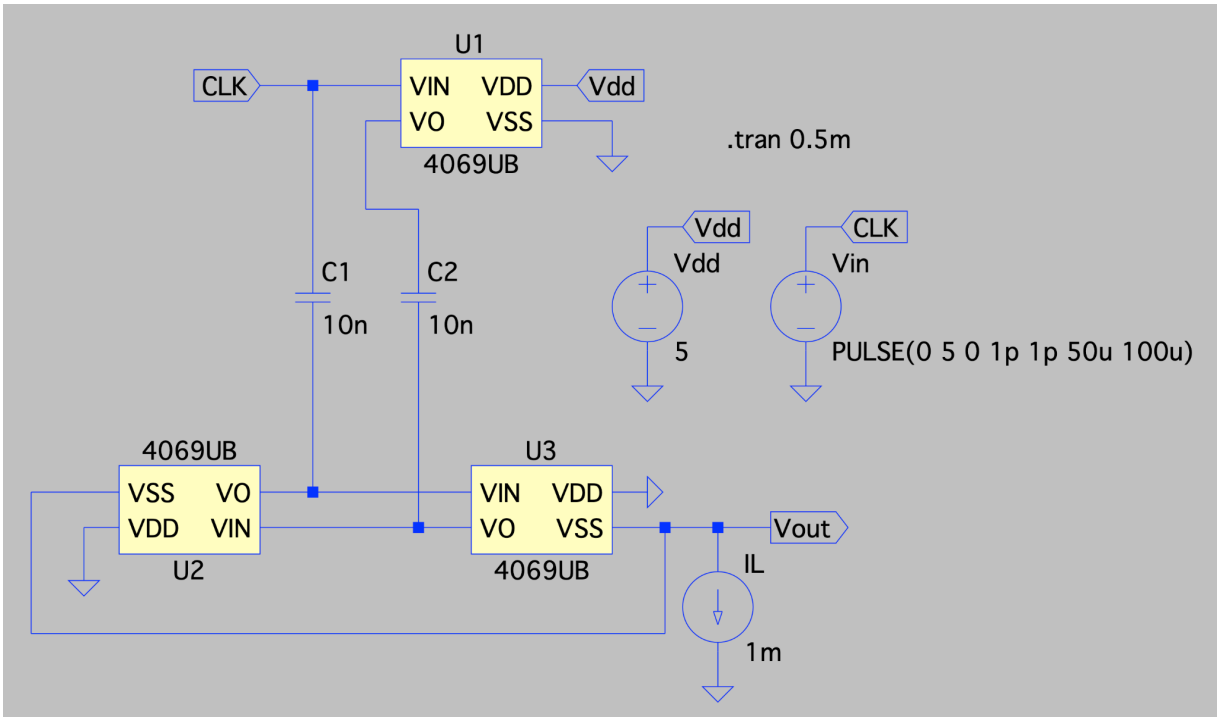


Output Plot

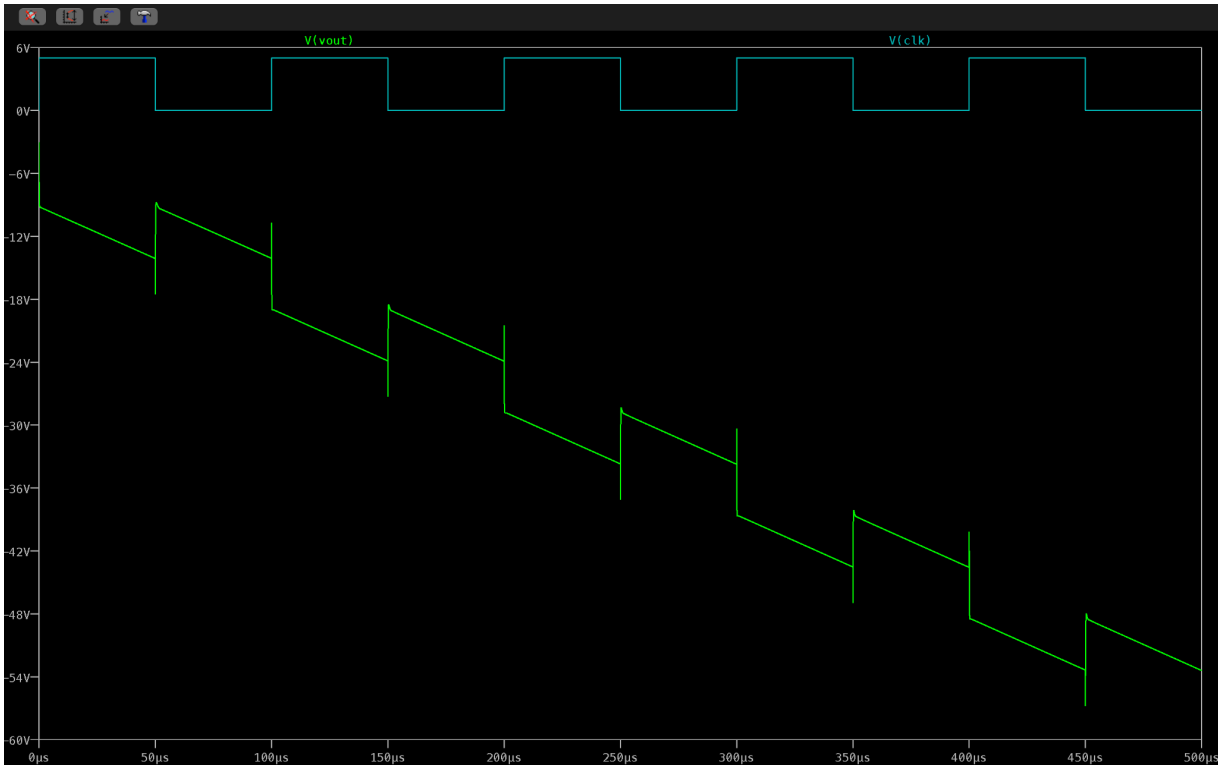


Here as C_L is non-zero, current actually flows through the capacitor which is shown by the steady reduction in voltage from 0V to -5V. If we see closely due to the resistance offered by the MOSFETs, the graph has inverse exponentials every half cycles as it is an RC circuit. Also after introducing a capacitor the spikes disappeared since it maintains a constant voltage.

Implementation in LTSpice for current source of 1mA



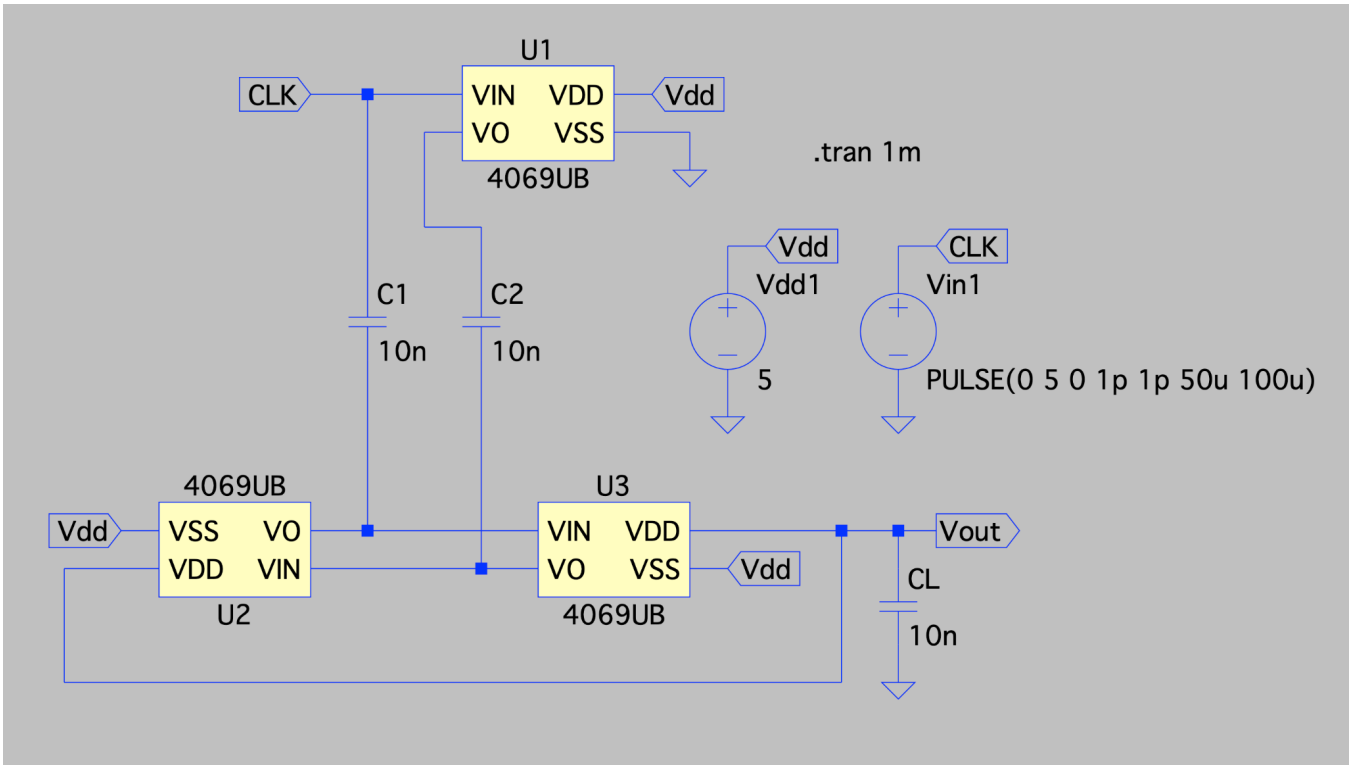
Output Plot



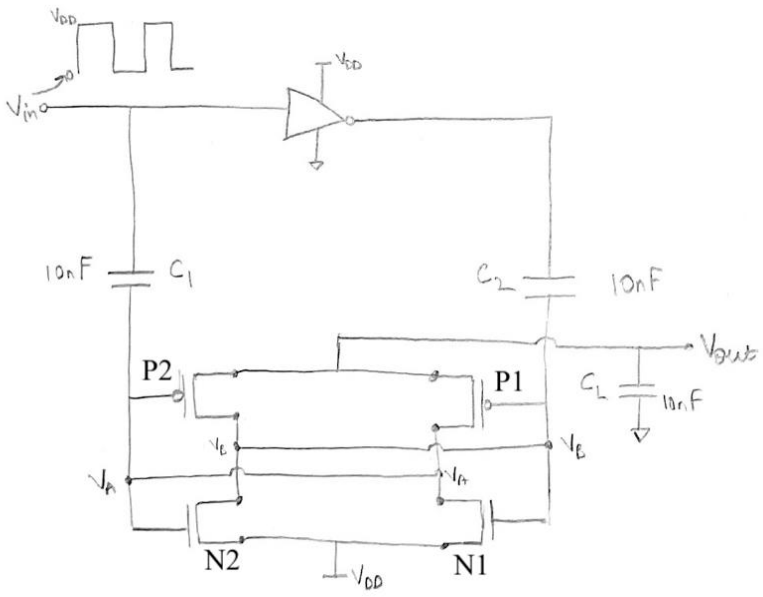
In this case, we are always drawing 1mA current from the circuit so based on CLK either C1 or C2 are being charged which causes this step format. This mode is unstable as V_{out} is infinity at steady state.

3. To design a circuit that gives a positive output with close to twice the supply voltage

Implementation in LTSpice



We can use the same setup from Q2 with a slight modification as shown.



Also note that V_{GS} for-

- N1 is V_B - V_A
- N2 is V_A - V_B
- P1 is V_B - V_{out}
- P2 is V_A - V_{out}

Analysis of the circuit-

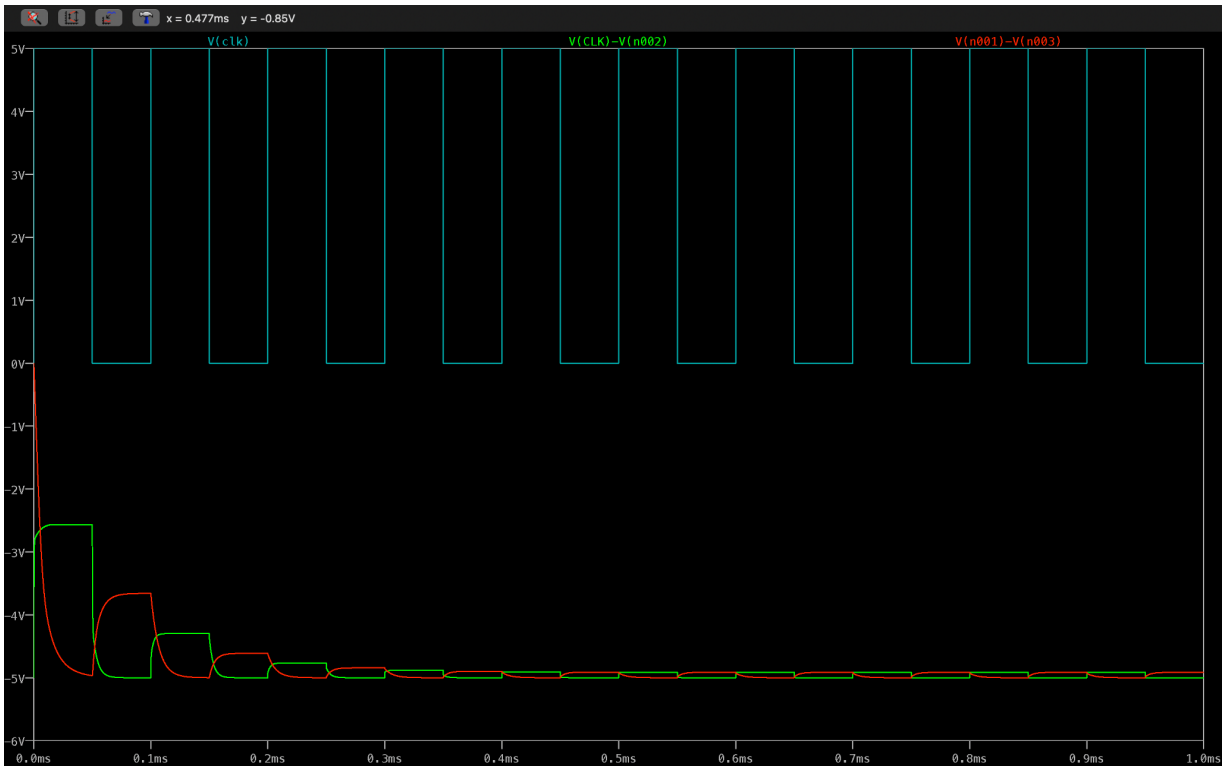
- When $V_{in} = 5V$ -
  $V_A = 5V$ and $V_B = 0V$ as both C1 and C2 are not charged.
  So V_{GS} for N1 is $-V_{DD}$ and for N2 is V_{DD} . Hence N1 acts as an open switch and N2 acts as a closed switch. As N2 opens up it allows V_{DD} to flow through which makes $V_B = 5V$ and hence the capacitor C2 charges to -5V (at the end of half cycle) . Looking at P1 and P2, their V_{GS} are 5 - V_{out} and since the drain voltages are 5V each we get

$$V_{GS} = 5 - V_{out} <- 5 \implies V_{out} > 10V$$

  But V_{out} does not become 10V instantaneously as there is a capacitor C_L connected (same reason in Q2) and C_2 takes time to charge.

- When $V_{in} = 0V$ -
  A similar charging process happens as above.

Graph for charging (Green for C1 and Red for C2)



At steady state, both capacitors charge to -5V.

- When CLK is 5V, V_A is 10V and V_B is 5V which makes P1 as closed switch that passes the drain voltage $V_A = 10V$ to V_{out} and P2 as open switch.
- When CLK is 0V, V_A is 5V and V_B is 10V which makes P2 as closed switch that passes the drain voltage $V_B = 10V$ to V_{out} and P1 as open switch.

Note that C_L was included to avoid the ripples in voltage as seen in Q2.

Output Plot