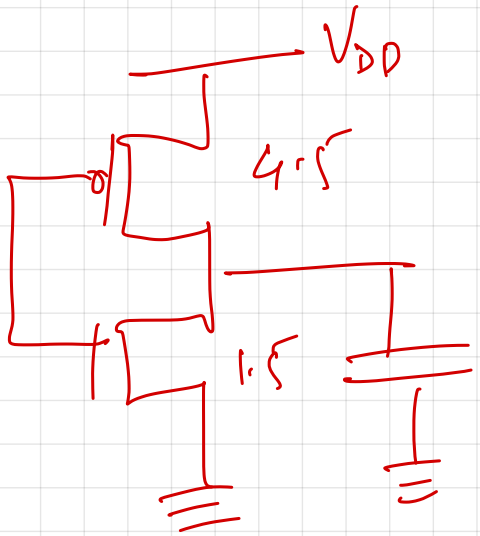
VLSI Design - Lecture 7

19th Aug 2022

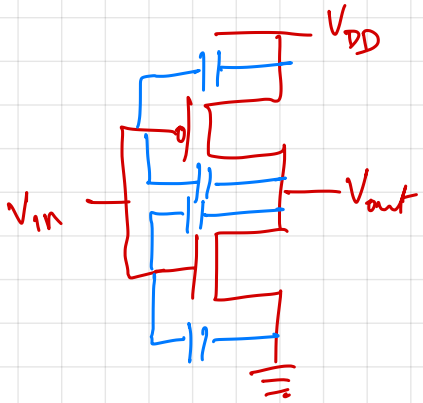


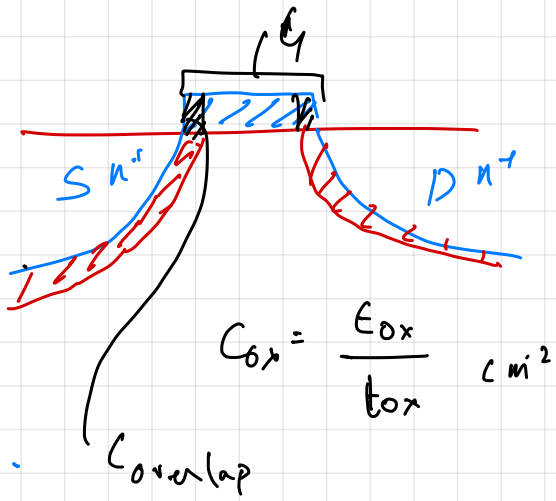
$$t_{pHL} = 0.69 \times \frac{13k\Omega}{1.5} \times 6fF$$

$$= 36\,ps$$

$$t_{pLH} = 0.69 \times \frac{31k\Omega}{4.5} \times 6fF$$

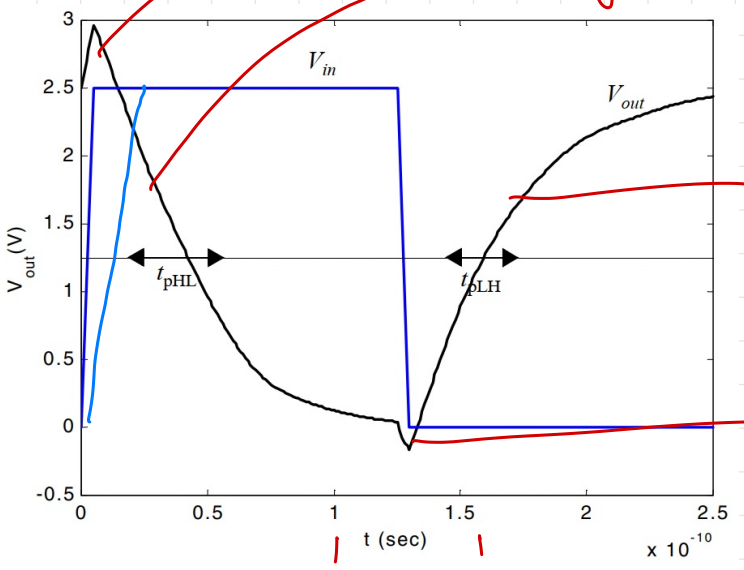
$$= 28\,ps$$





Spike due to C_{gdo}

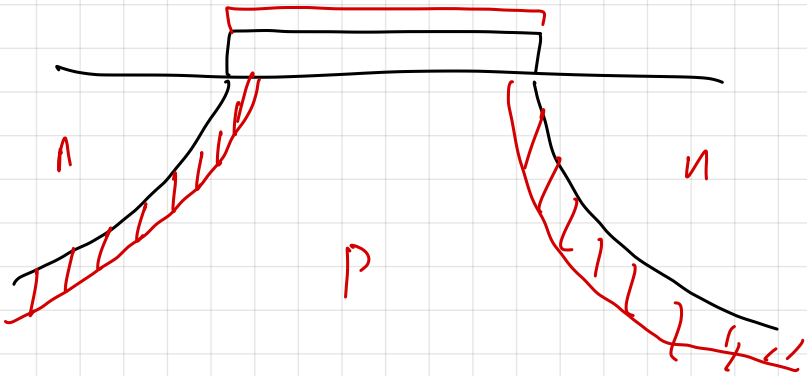
Discharge due to NMOS



Pull up due to PMOS

Undershoot due to C_{gdo}

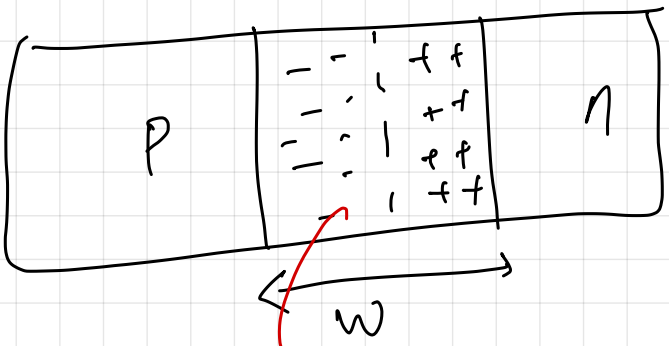
100 ps 150 ps



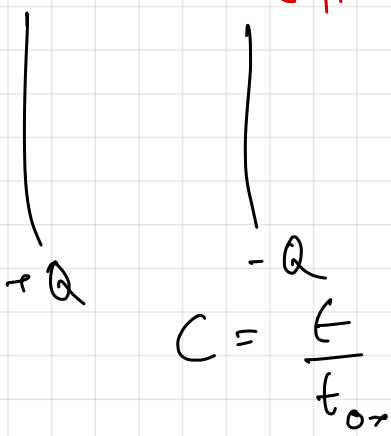
① Gate C_{ox}

② C_{gdo}, C_{gso}

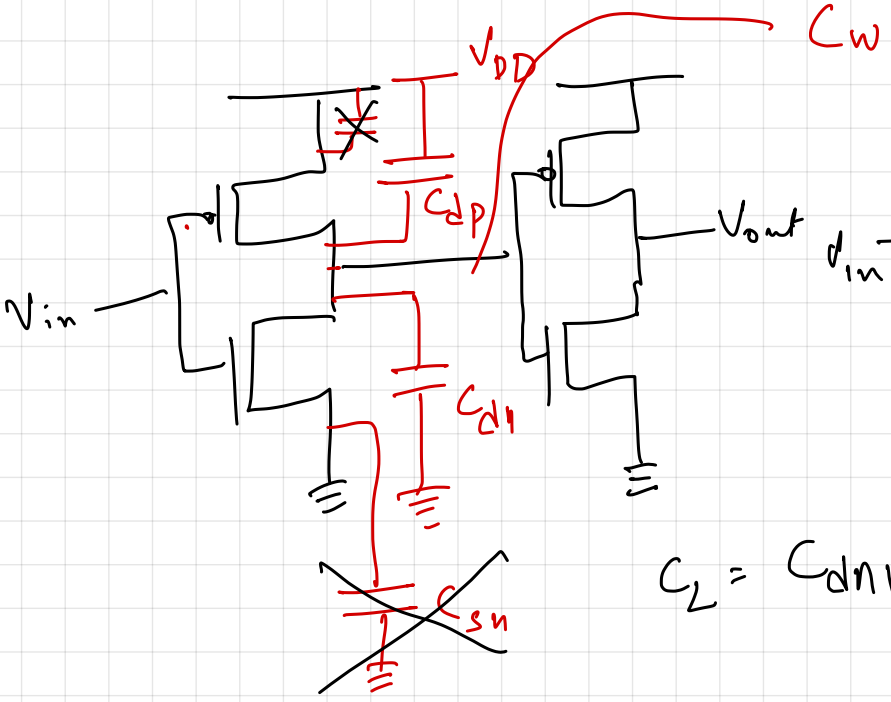
③ Diffusion capacitance / source & drain diffusion

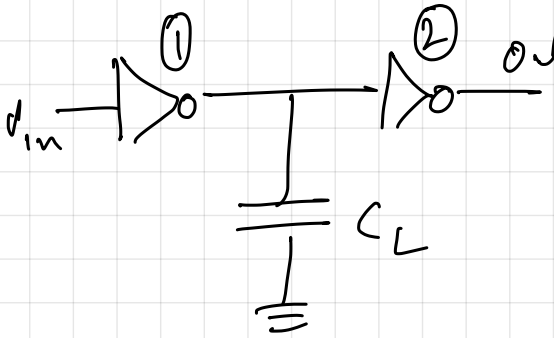


$$C_{dep} = \frac{\epsilon_{si}}{W_{dep}}$$



$$C = \frac{\epsilon}{t_{ox}}$$



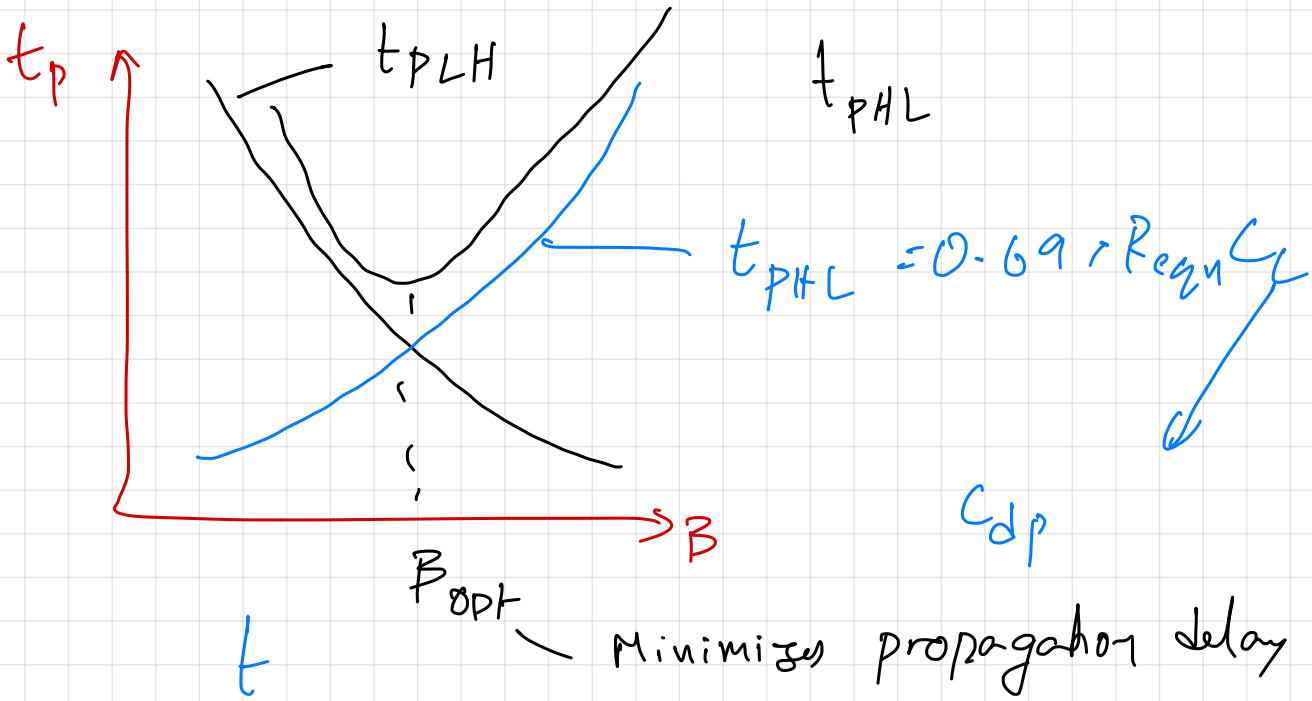


$$C_L = C_{dn1} + C_{dp1} + C_w + C_{gn2} + C_{gp2}$$

$$\beta = \frac{(W/L)_p}{(W/L)_n} \qquad t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

$$R \xrightarrow{\alpha} R/\alpha$$

$$C \rightarrow \alpha C$$



t — Minimizes propagation delay

$$t_p = \frac{0.69}{2}\left(R_{eqn} + \frac{R_{eqp}}{\beta}\right)\left(C_{dn1} + \beta C_{dn1} + C_w + C_{gn2} + \beta C_{gn2}\right)$$

$$\frac{dt_p}{d\beta} = 0$$

$$\beta^2 = \alpha\left(1 + \frac{C_w}{C_{dn1} + C_{gn2}}\right)$$

$$\alpha = \frac{R_{eqp}}{R_{eqn}}$$

$$= \frac{31\,k\Omega}{13\,k\Omega} = 2.48$$

$\beta_{opt} = \sqrt{2.48}$ assuming C_w is negligible