Analog Lab

Experiment 10: Buck Converter with Regulator

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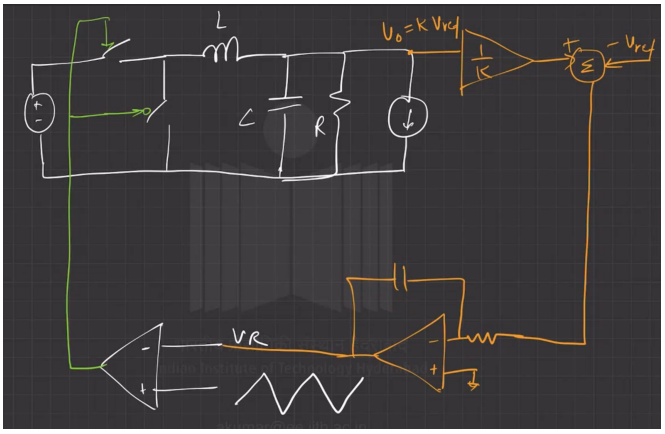
1. To close the loop of Buck converter from Experiment 9 using an integrator



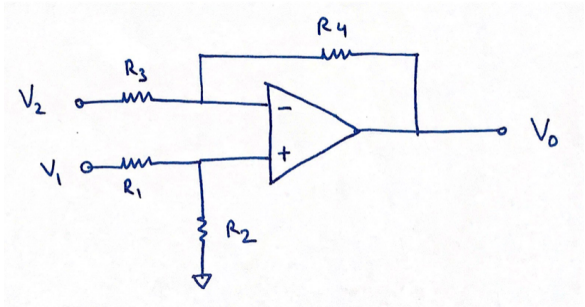
As seen in the adjacent circuit diagram (taken from a lab lecture) we need to implement 3 blocks, i.e. voltage divider, voltage subtractor and integrator and then decide the R and C values for the integrator.

1.1. Voltage Divider block

We can use a simple resistance divider network with resistances as (k-1)R and R respectively. Note that we have to pick a relatively large value of R so as to not load the resistance present in the buck converter. If we use a large value of R, the effective resistance does not vary much as resistance from the buck converter and the divider are in parallel.

1.2. Subtracting V_{ref} block

Here we can use a differential amplifier in negative feedback implemented in the following way-



KCL @V_+

$$\frac{V_+ - V_1}{R_1} + \frac{V_+ - 0}{R_2} = 0 \quad \Rightarrow \quad V_+ = \frac{V_1 R_2}{R_1 + R_2}$$

KCL @V_-

$$\frac{V_- - V_2}{R_3} + \frac{V_- - V_o}{R_4} = 0 \quad \Rightarrow \quad V_- = \frac{V_2 R_4}{R_3 + R_4} + \frac{V_o R_3}{R_3 + R_4}$$

As the Op-amp is in negative feedback, we can apply the virtual short property, i.e. $V_+ = V_-$. So we get-

$$V_o = \left(\frac{R_3 + R_4}{R_1 + R_2}\right)\frac{V_1 R_2}{R_3} - \frac{V_2 R_4}{R_3}$$

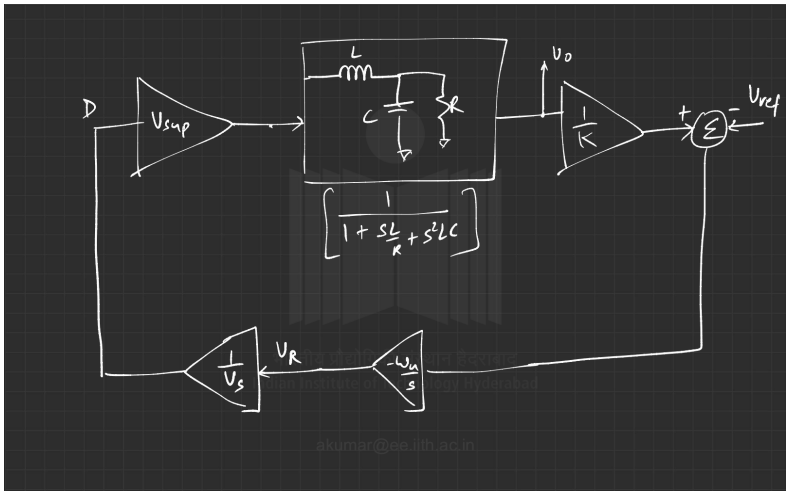
Now if we set $R_1 = R_2 = R_3 = R_4$, we will get-

$$V_o = V_1 - V_2$$

Which is clearly what we want. So if we feed V_{ref} to V_2 and output of the voltage divider to V_1 , we get V_o as the difference between (V_o / k) and V_{ref}.

1.3. Integrator block

From the adjacent image taken from lecture 26, the overall loop gain of the system is-



$$LG(s) = \frac{\omega_u}{s}\frac{1}{kV_s}V_{sup}\frac{R}{s^2LCR + sL + R}$$

And so for stable operation-

$$\frac{\omega_o}{\omega_n}Q < 1$$

where $\omega_o = \frac{\omega_u V_{sup}}{kV_s}$, $Q = R_L\sqrt{\frac{C_1}{L_1}}$, $\omega_n = \frac{1}{\sqrt{LC}}$ and $\omega_u = \frac{1}{RC}$.

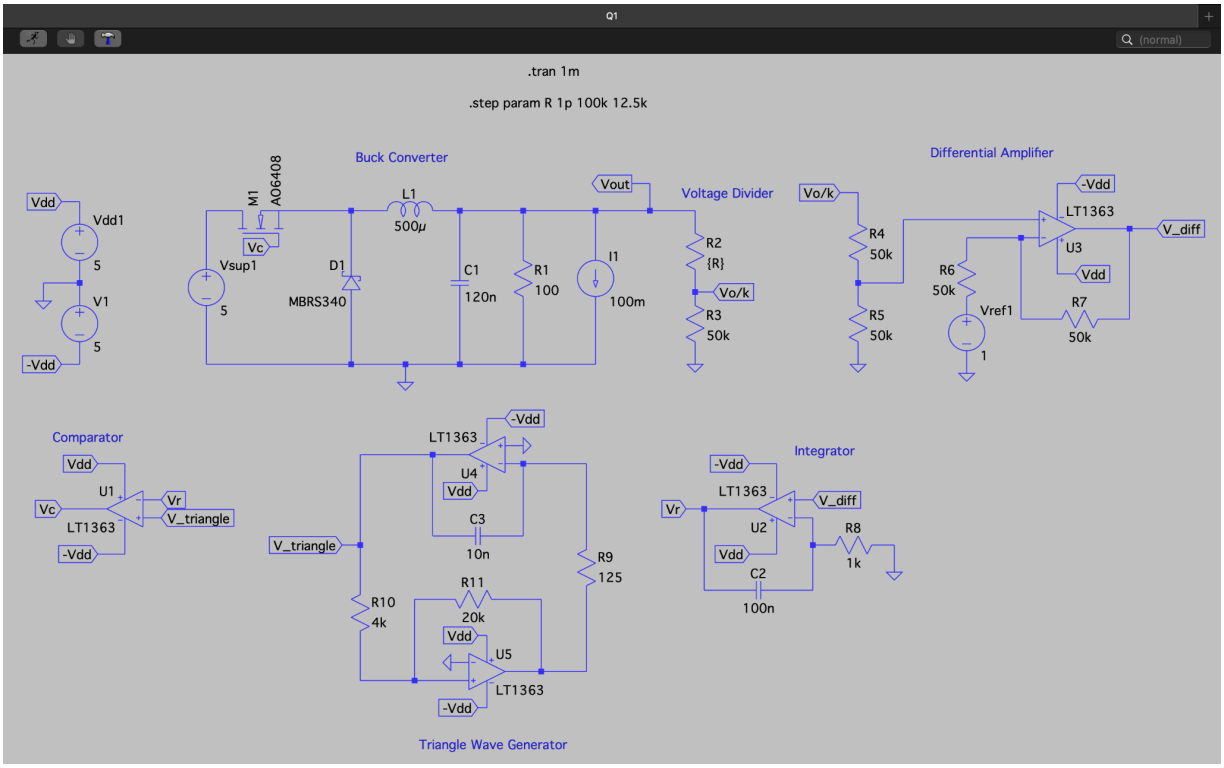
Substituting in for the values of L_1(500μH), C_1 (120nF), R_L(100Ω), V_{sup} (5V), V_s (1V) and k = 1 we get-

$$RC \geq 60\mu s$$

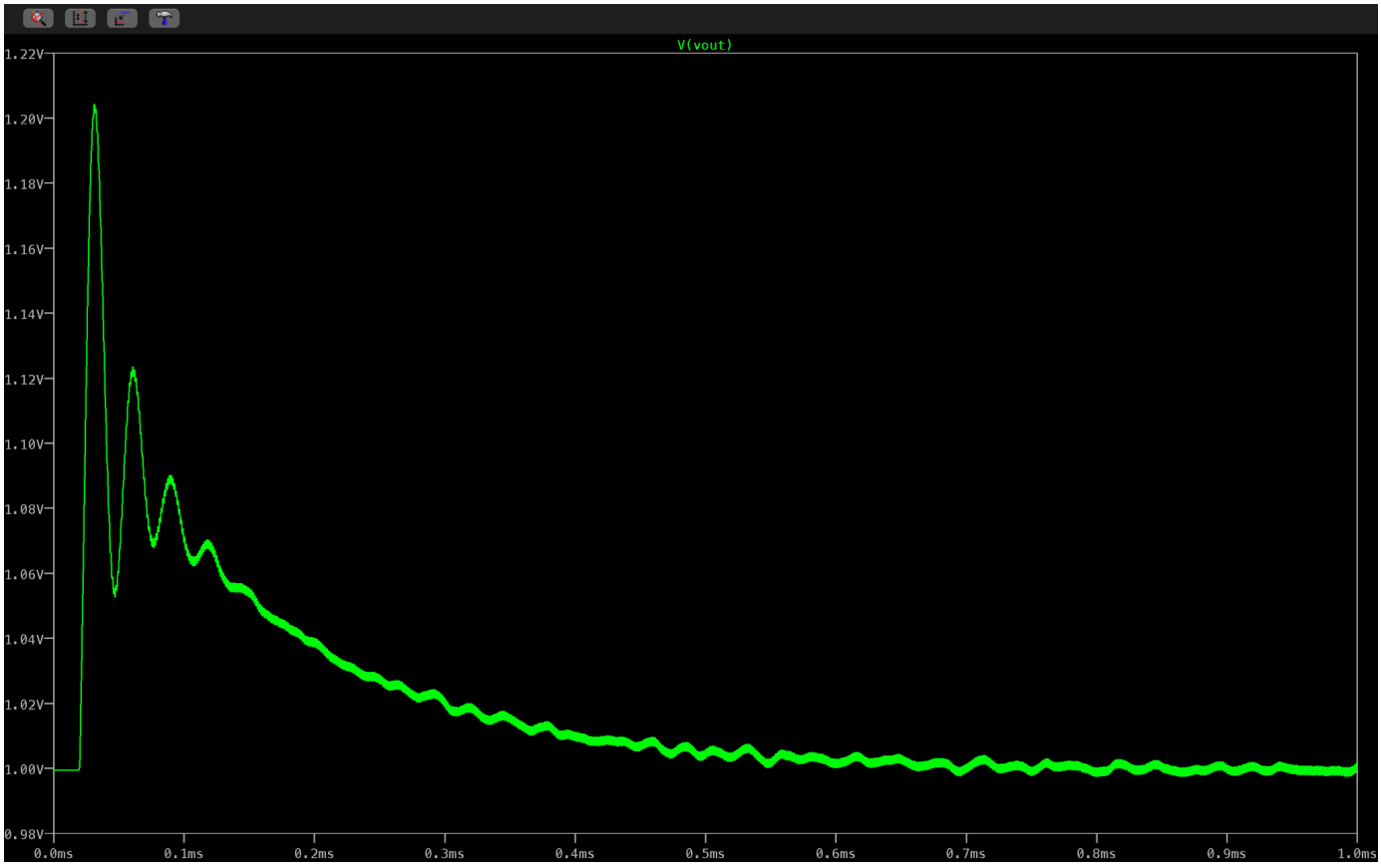
So for this experiment, I have taken R as 1kΩ and C as 100nF. (all of these formulas are taken from analog electronics course lecture 26)

The above equation comes from the bode and the nyquist plot where the magnitude of loop gain must be less than 1 at cutoff frequency ω_n (since the phase at ω_n is −180 degrees and so it lies on the real axis) so that the nyquist plot does not touch the point (-1, 0).

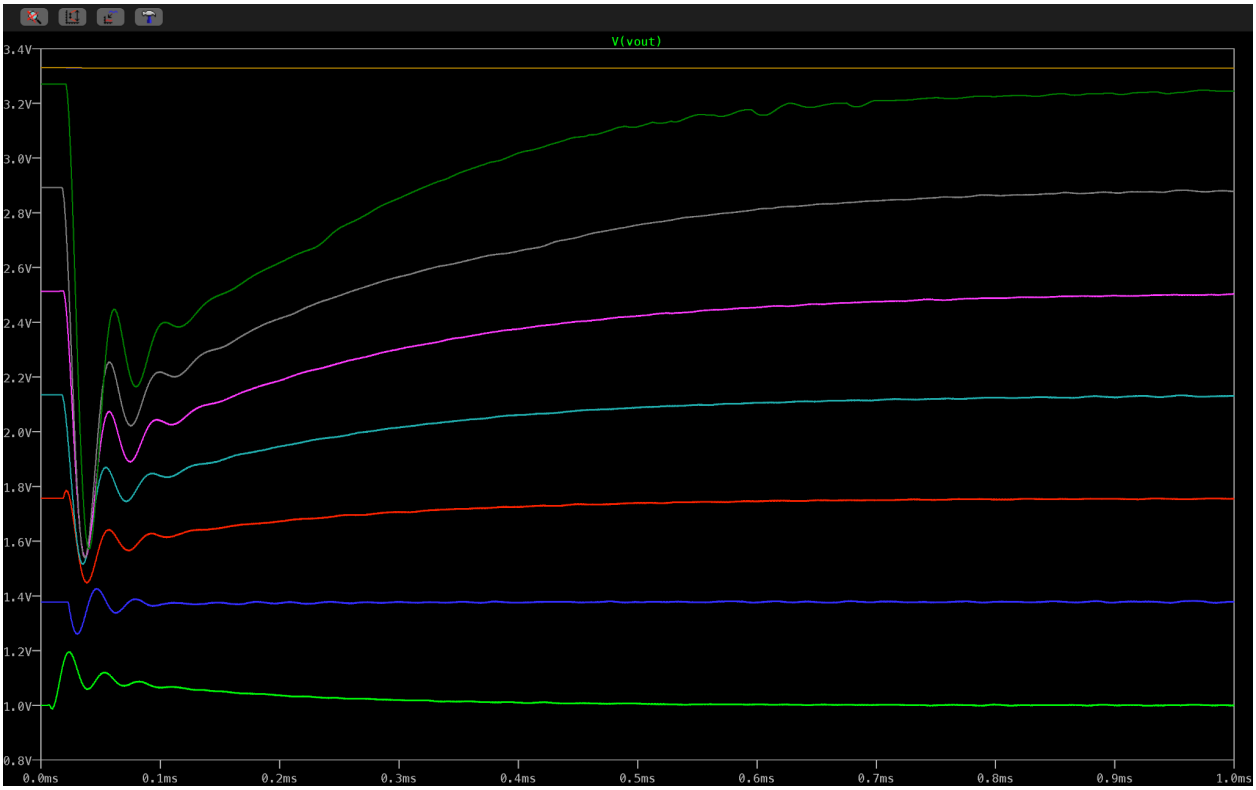
Implementation in LTSpice

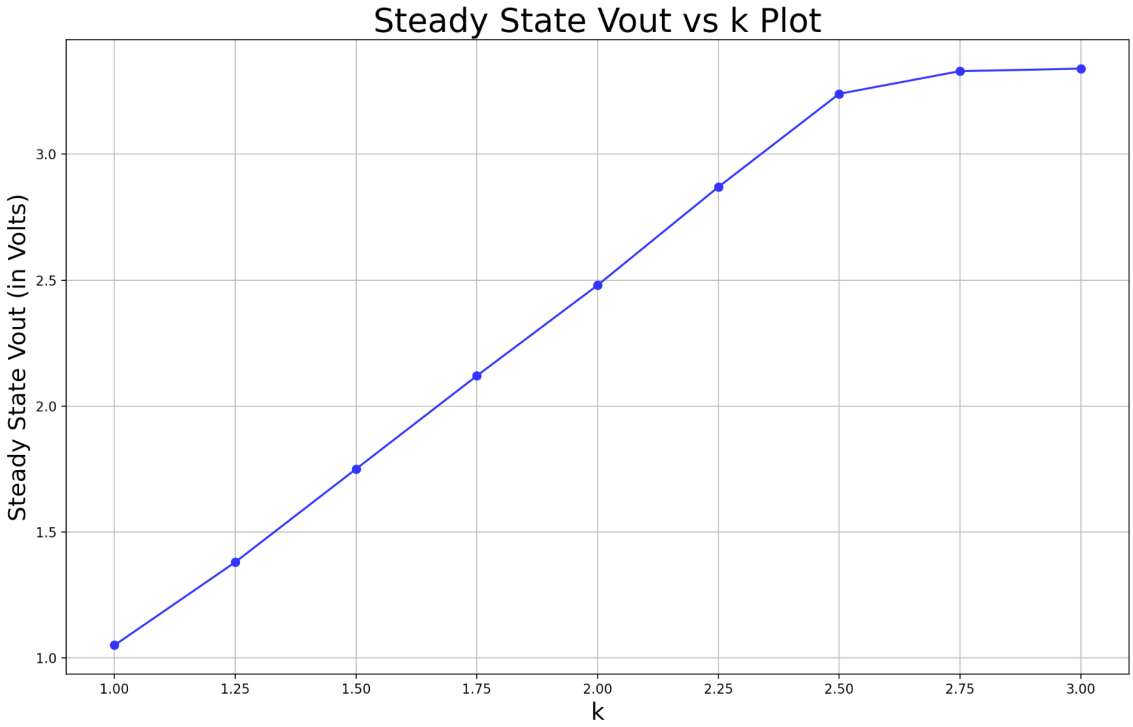


Output Voltage for k = 1



V_{out} vs Time for various k





The resistance in the divider network was varied from 0Ω to 100kΩ using the .step function which effectively varies k from 1 to 3 (taking R = 50kΩ for resistance of the first resistor as (k-1)R).

The lower bound of k is 1 due to the resistance divider network. In that network, the first resistance value is (k-1)R and so since there is no negative resistance the lower bound on k is 1.

This lower bound can be reduced by dropping the voltage divider network and connecting the output voltage of the buck converter directly to the differential amplifier. From the formula on page 2, we can set $R_3 = R_4$ and we get the following result-

$$V_e = \frac{2R_2}{R_1 + R_2} V_o - V_{ref}$$

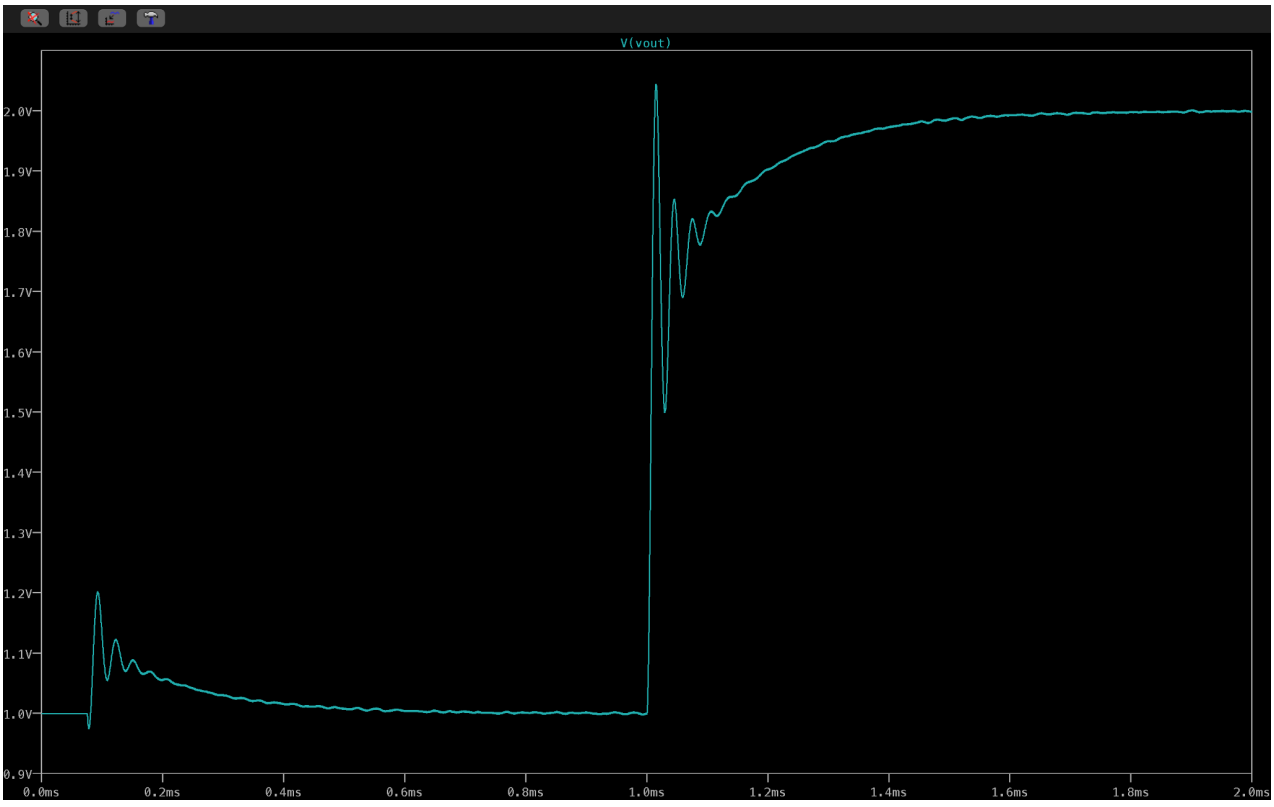
$$\Downarrow$$

$$k = \frac{1}{2} + \frac{R_1}{2R_2} \text{ (as coefficient of } V_o \text{ must be } 1/k)$$

The upper bound on k is 3.3 as seen in the transient plot that the voltage saturates to 3.3V. This can be credited to the saturation voltage of the op-amp. So we can increase the upper bound of k if we have higher supply voltage.

Therefore the working range of k is 1 to 3.

1.4. To plot for k = 1 when V_{ref} goes from 1V to 2V



The above plot was implemented using pulse function for the V_{ref} voltage source which jumped from 1V to 2V at 1ms. The output plot is as expected where the V_{out} saturates to kV_{ref} , i.e. 1V for $V_{ref} = 1$ and 2V for $V_{ref} = 2$.

1.5. Observations

1) The settling time of the output voltage is around 0.5ms.
2) The buck converter works as expected for k ranging from 1 to 3.
3) Lower bound of k is due to the resistance divider network and can be avoided by the above method.
4) Almost linear characteristic for $V_{out,\ sat}$ vs k for k between 1 and 3 which satisfies the equation $V_{out,\ sat} = kV_{ref}$.
5) The upper bound of k is due to the saturation voltage of the op-amp and the bound can be increased by changing the supply voltages.
6) As we have designed the system for $k = 1$, it is stable for $k \geq 1$.