

Analog Lab

Experiment 5: Voltage Controlled Oscillator

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1. To design schmitt trigger based oscillator with

Oscillation Frequency: 10kHz

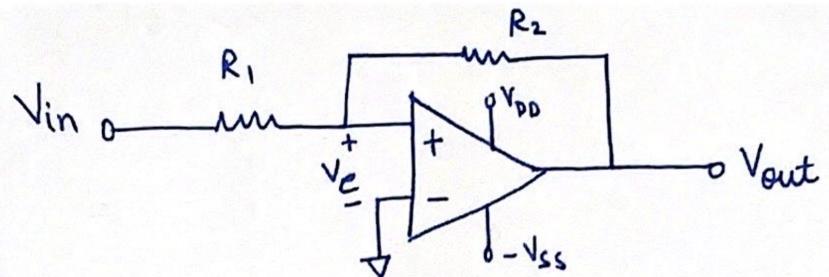
Hysteresis width for schmitt trigger: 20% of op amp peak-to-peak output swing
 LF347 op amp with +5V/-5V dual supply

Schmitt trigger used-

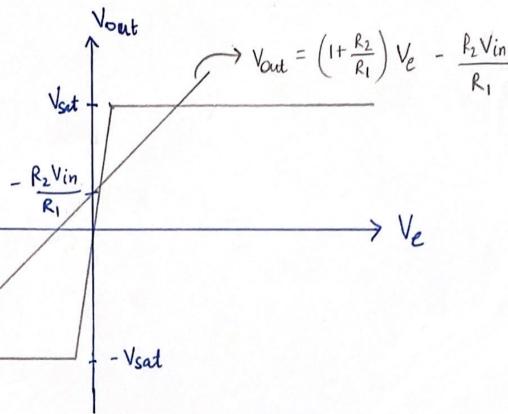
Writing KCL at V_+ we get-

$$\frac{V_{in} - V_e}{R_1} = \frac{V_e - V_{out}}{R_2}$$

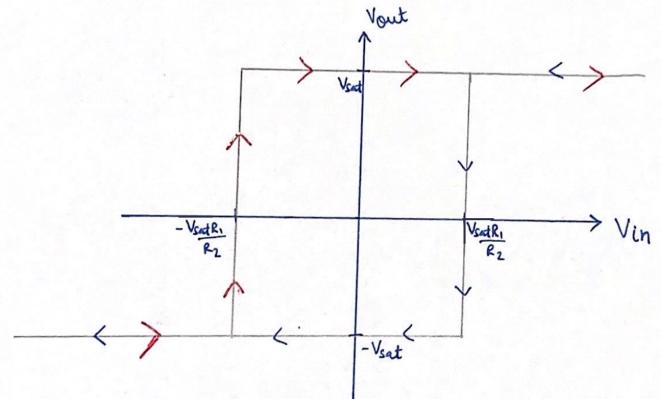
$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) V_e - \frac{R_2}{R_1} V_{in}$$



Here, $V_{DD} = V_{SS} = 5V$



Graph for V_{out} vs V_e



Hysteresis Loop from graph

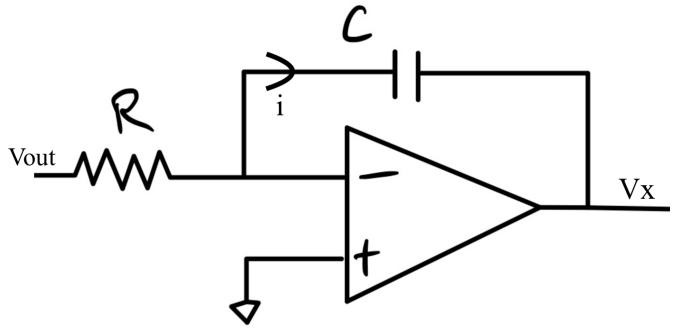
From the given specifications- $2V_{sat} \frac{R_1}{R_2} = 20\% \text{ of } 2V_{sat} = \frac{2}{5}V_{sat}$

So we get- $R_2 = 5R_1$

In this experiment, I took R_1 to be $4k\Omega$ and R_2 to be $20k\Omega$.

Integrator used-

Current in the capacitor, i is V_{out} / R . Considering V_X is $V_{sat} / 5$, for the schmitt trigger to change V_{out} from V_{sat} to $-V_{sat}$, V_X must be charged to $-V_{sat} / 5$ and this process must take $T/2$ time (where T is the time period). So writing the integral equation-

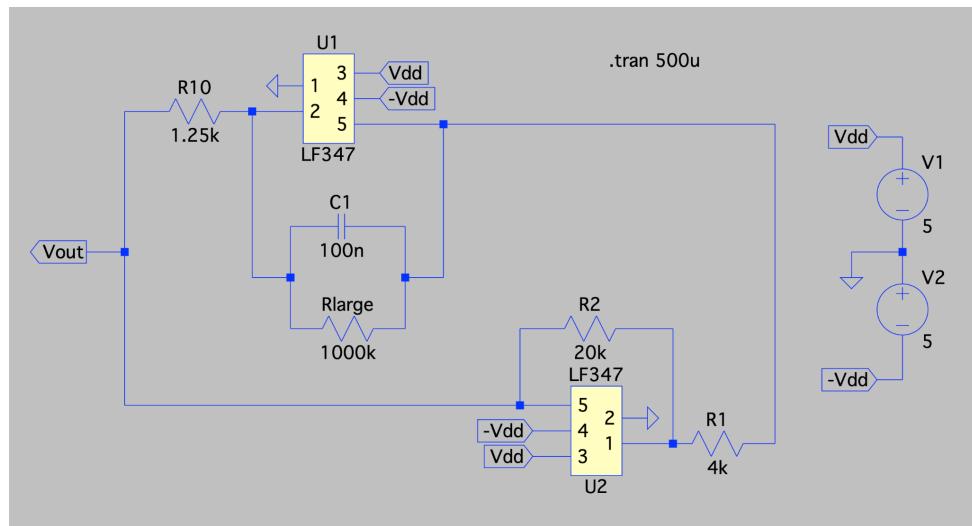


$$\int_x^{x+T/2} \frac{V_{sat}}{R} dt = \frac{V_{sat} \cdot T}{2R} = C \left\{ \frac{V_{sat}}{5} - \left(-\frac{V_{sat}}{5} \right) \right\} = \frac{2CV_{sat}}{5}$$

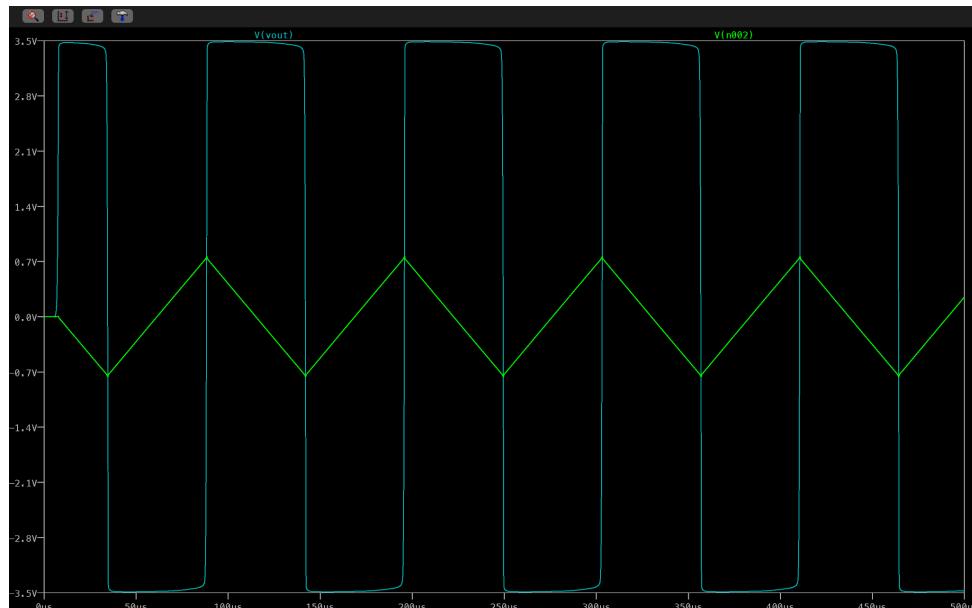
$$\text{Therefore: } RC = \frac{5T}{4} \Rightarrow RC = 125\mu\text{s}$$

In this experiment, I took C as 100nF and R as $1.25\text{k}\Omega$.

Implementation in LTSpice



Output Plot



2. To build a modified oscillator with control voltage V_c

Specifications-

Output Frequency: 10-15kHz

V_c ranging from 4-6V

In the given circuit, diode D_1 is used to protect the transistor from breakdown during negative swing and the NMOS transistor is used to introduce an inversion in the voltage.

$$\text{In Op-Amp 1, } V_+ = V_- = \frac{V_c}{2}$$

When $V_{out} = V_{sat}$, the transistor acts as a closed switch and so connects the output to ground. So current through capacitor is: $i_C = \frac{V_c}{2R} - \frac{V_c}{R} = -\frac{V_c}{2R}$

When $V_{out} = -V_{sat}$, the transistor acts as an open switch and does not allow current to flow through the $R/2$ resistor.

$$\text{In this case, current through capacitor is: } i_C = \frac{V_c}{2R}$$

Writing KCL at V_+ of Op-Amp 2:

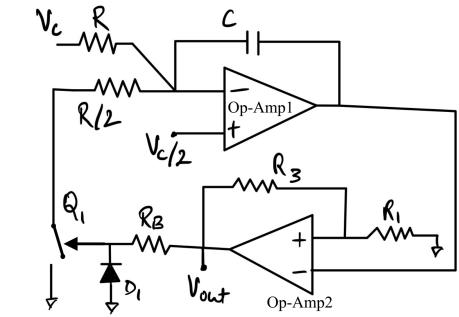
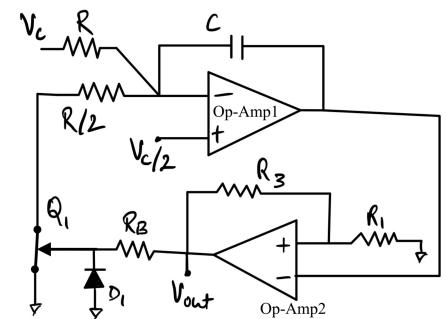
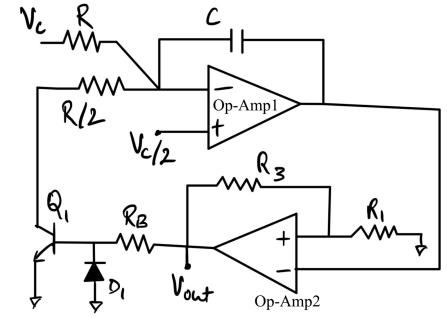
$$\frac{V_+ - 0}{R_1} + \frac{V_+ - V_{out}}{R_3} = 0 \Rightarrow V_{out} = \frac{(R_1 + R_3)V_+}{R_3} \Rightarrow V_{out} = \frac{(R_1 + R_3) \times (V_e + V_-)}{R_1}$$

Now for V_{out} to switch polarity, V_e must become ~ 0 and V_- will be $V_{sat}/5$ (from the previous part). Substituting this into the above equation, we get: $R_3 = 4R_1$

In this experiment, I took R_1 as $10k\Omega$ and R_3 as $40k\Omega$.

For the transistor, I_B is $5mA$ and V_{BE} is $0.7V$ (from datasheet), so writing KVL across R_B we get:

$$R_B = \frac{V_{out} - V_{BE}}{I_B} = \frac{3.5V - 0.7V}{5mA} = 560\Omega$$



Writing integral equation across capacitor when $V_{out} = V_{sat}$, current through capacitor will be $-V_C/2R$:

$$\int_x^{x+T/2} i_C dt = \int_x^{x+T/2} -\frac{V_c}{2R} dt = -\frac{V_c T}{4R} = C \left(\left(\frac{V_c}{2} - \frac{V_{sat}}{5} \right) - \left(\frac{V_c}{2} + \frac{V_{sat}}{5} \right) \right)$$

↓

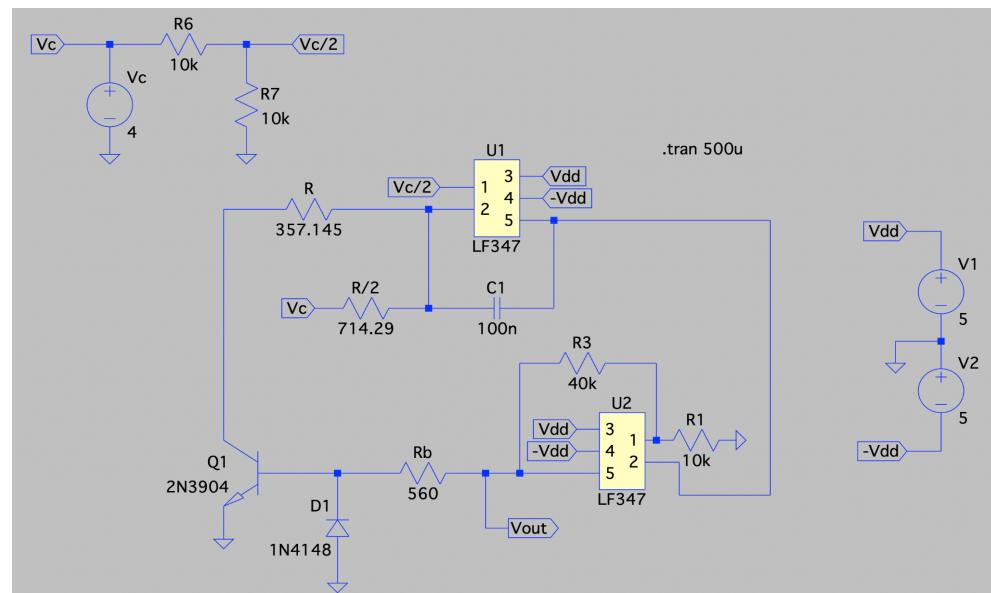
$$RC = \frac{5V_c T}{8V_{sat}} = \frac{5V_c}{8V_{sat} f}$$

For calculation, we take the least limit, so $f = 10\text{kHz}$, $V_c = 4\text{V}$ and $V_{sat} = 3.5\text{V}$.

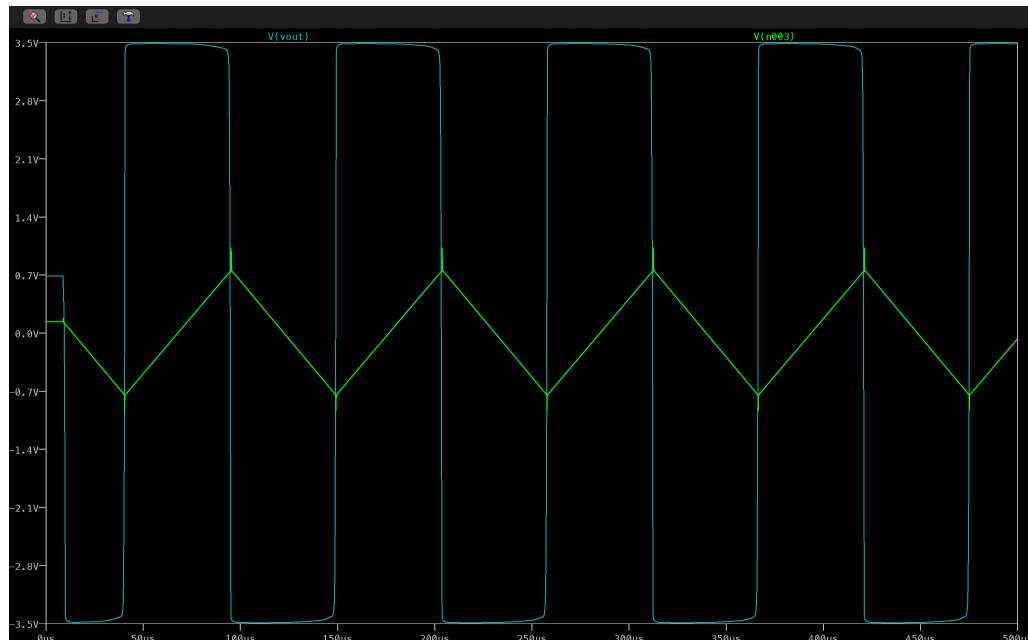
So, $RC = 71.4285\mu\text{s}$

In this experiment, I took C as 100nF and 714.29Ω .

Implementation in LTSpice

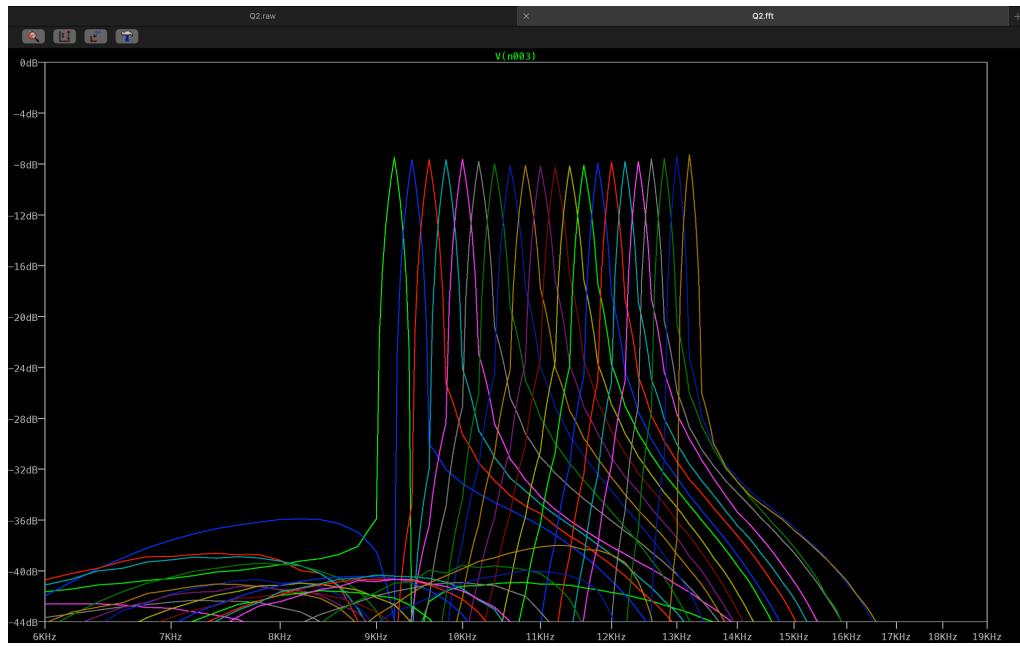


Output Plot

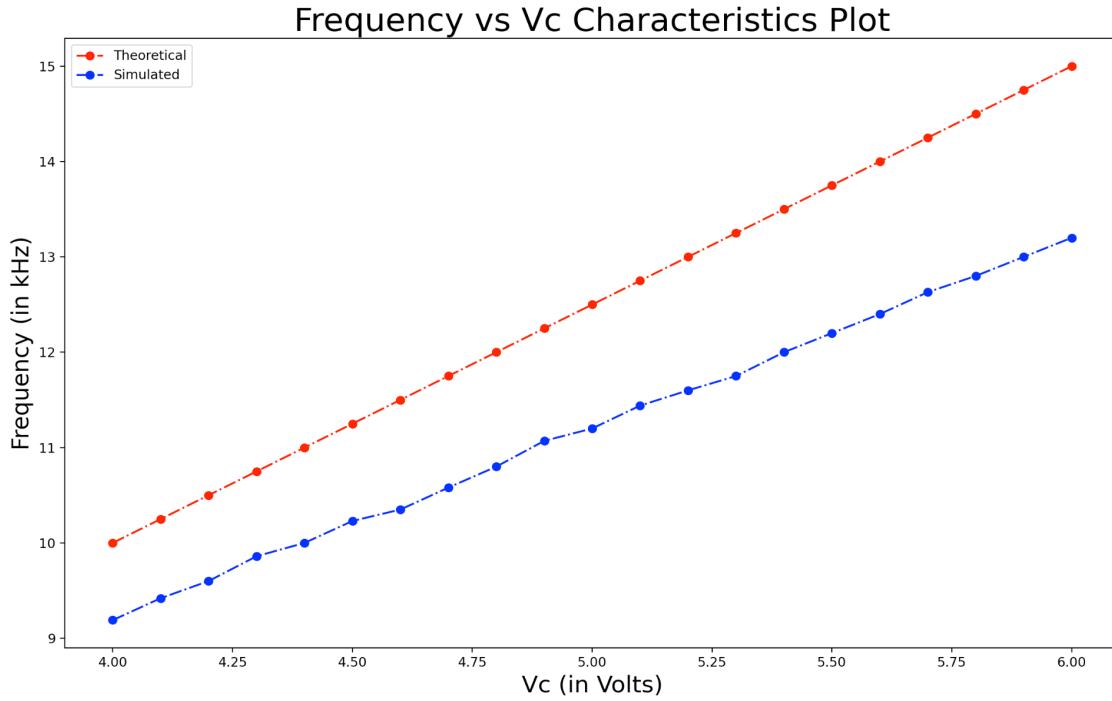


For plotting Frequency vs V_C characteristics, I used “.step” to vary V_C , then used FFT to find the peak at every V_C and used python to plot.

FFT plot for various V_C 's



(Note that this is just the peak of each V_C)



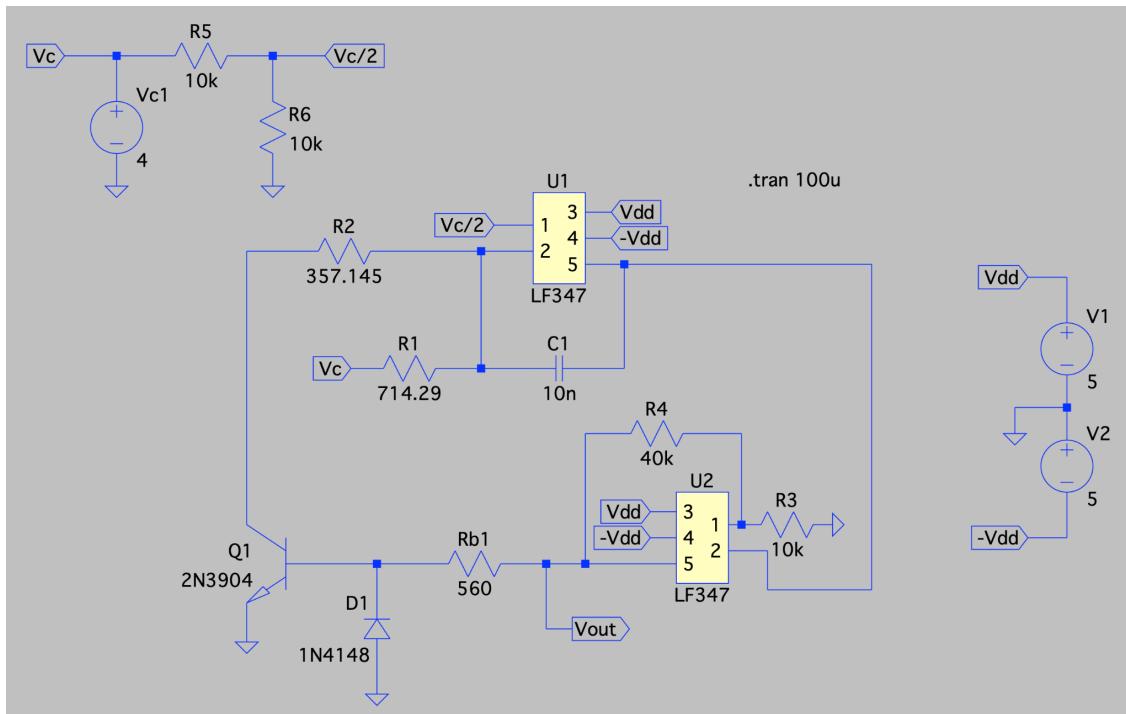
The simulated plot is almost a straight line but the frequency range it covers does not match with the theoretical plot because we did not take into account the saturation voltage across CE junction and also due to the non-ideality of op-amps ($V_{sat} = 3.5V$).

3. To obtain a new frequency range of 100-150 kHz for same V_c range

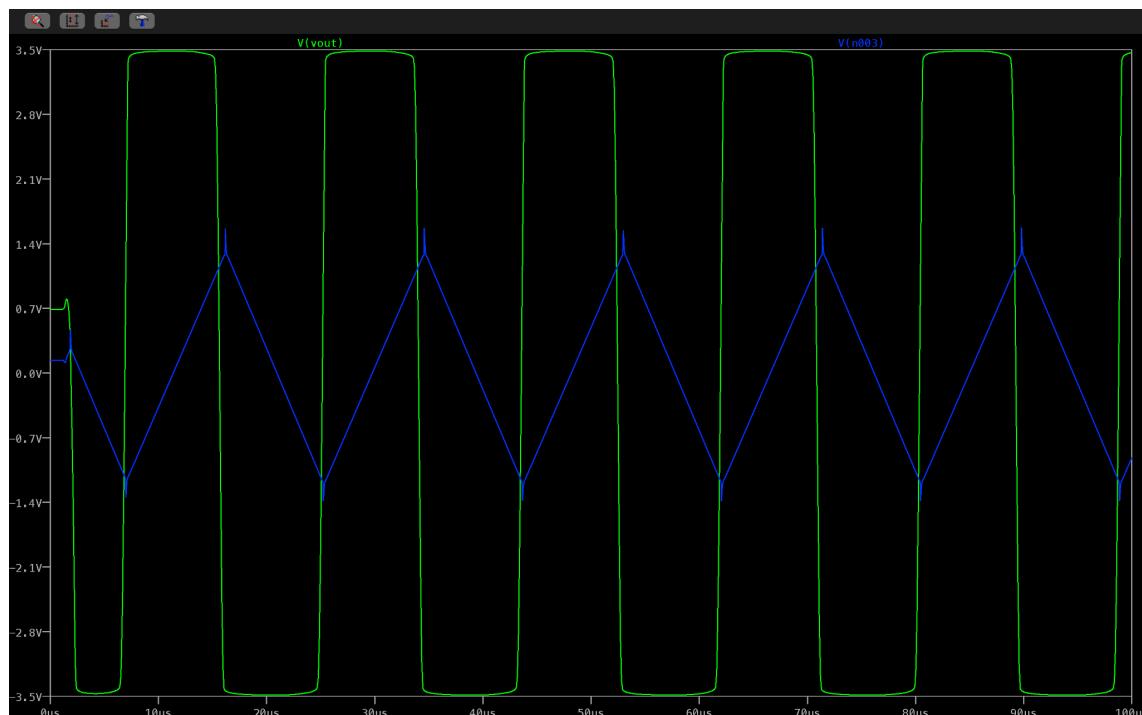
Since the frequency range is 10 times the frequency range from part 2, we can use the same formula from part 2 that is: $RC = \frac{5V_c}{8V_{sat}f}$.

So plugging in $f = 100\text{kHz}$, $V_c = 4\text{V}$ and $V_{sat} = 3.5\text{V}$, we get that $RC = 7.14285\mu\text{s}$. In this experiment, I took C as 10nF and 714.29Ω .

Implementation in LTSpice

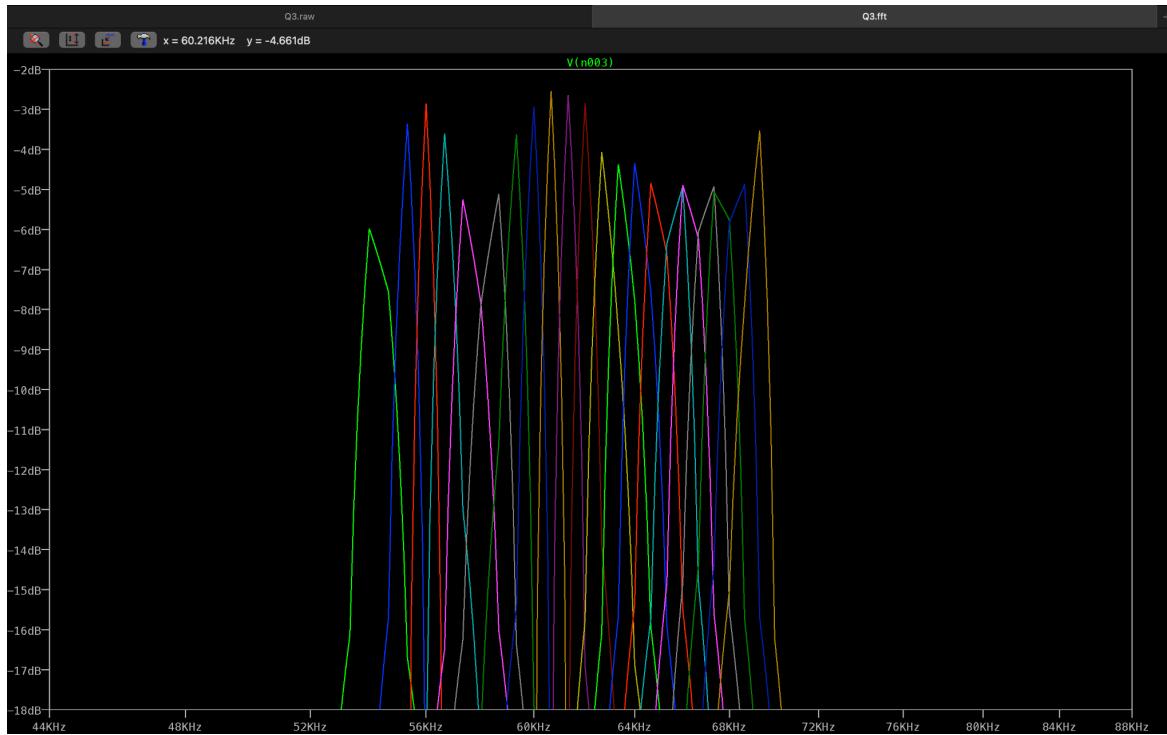


Output Plot

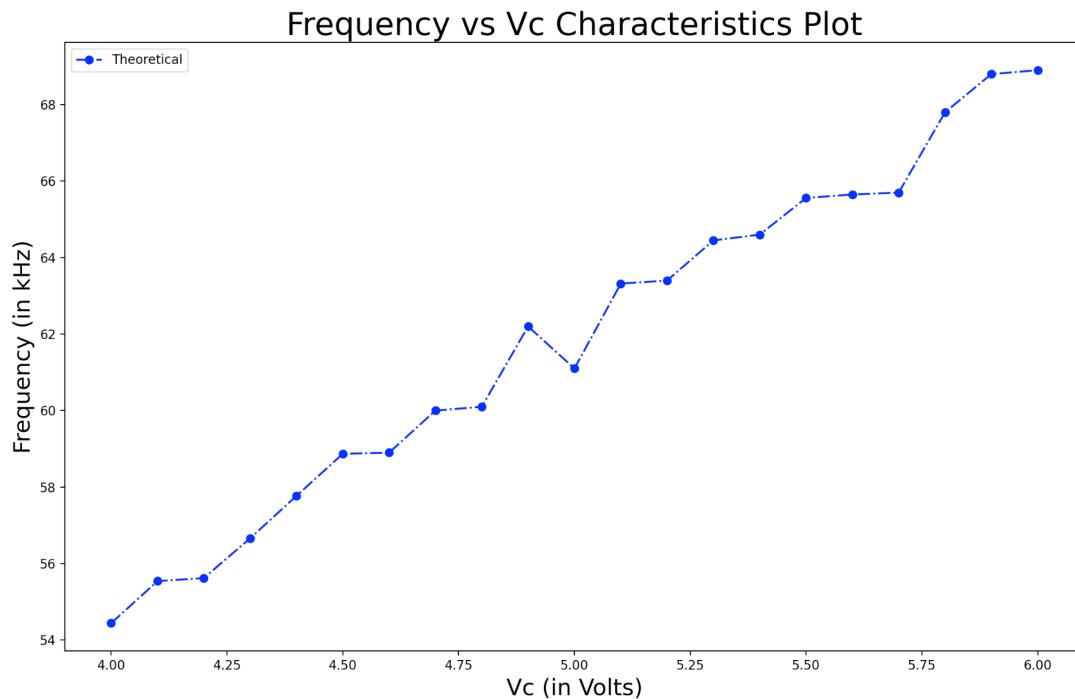


For plotting Frequency vs V_C characteristics, I used the same method described in part 2.

FFT plot for various V_C 's



(Note that this is just the peak of each V_C)



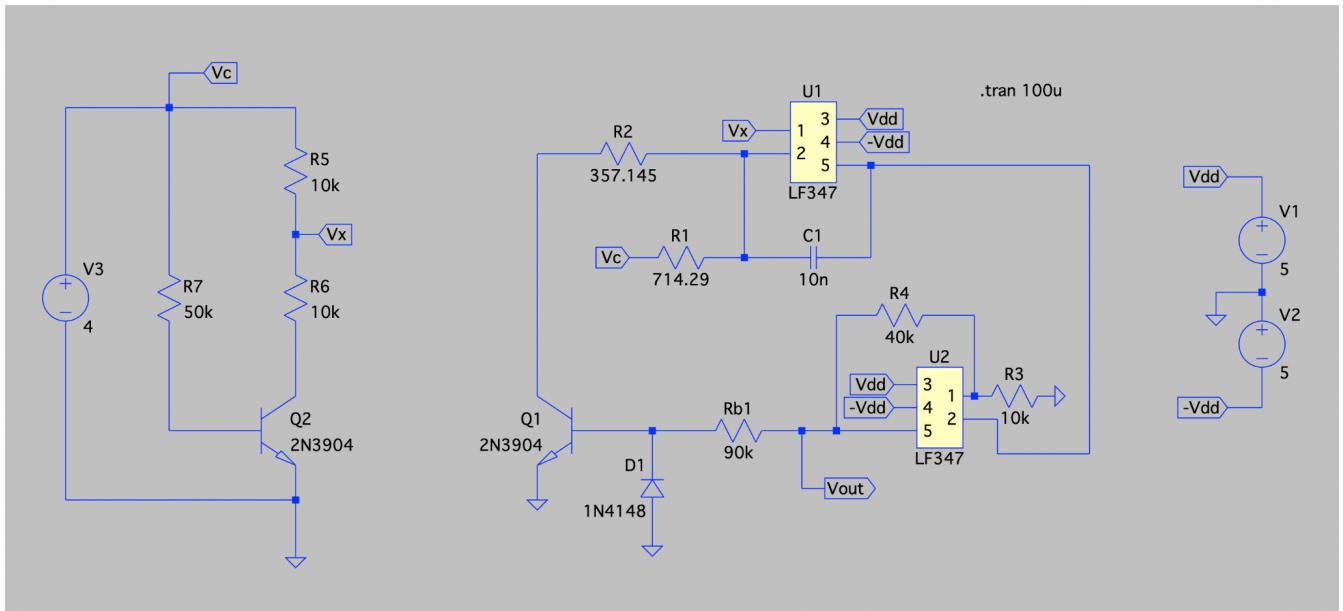
Clearly the plot is not linear and frequency range is far from expected values due to the previously explained reasons. Also the slew rate of the opamp is far greater than the time period of oscillations. It takes about $1-2\mu s$ to switch from $+3.5V$ to $-3.5V$ which allows the capacitor to charge for additional time and hence increases the trigger voltage.

Observe that here the trigger voltage is almost doubled which makes the frequency range almost half than the theoretical expectation.

Correction-

The duty cycle also depends on the CE junction (of transistor) saturation voltage. In the above circuit the duty cycle is less than 50%. So to eliminate this effect we can modify the voltage divider network to add $V_{CE,\text{saturation}}$ to V_- terminal.

Modified Implementation in LTSpice



Output Plot

