Introduction to VLSI Design
Assignment 1: Study of CMOS Inverter

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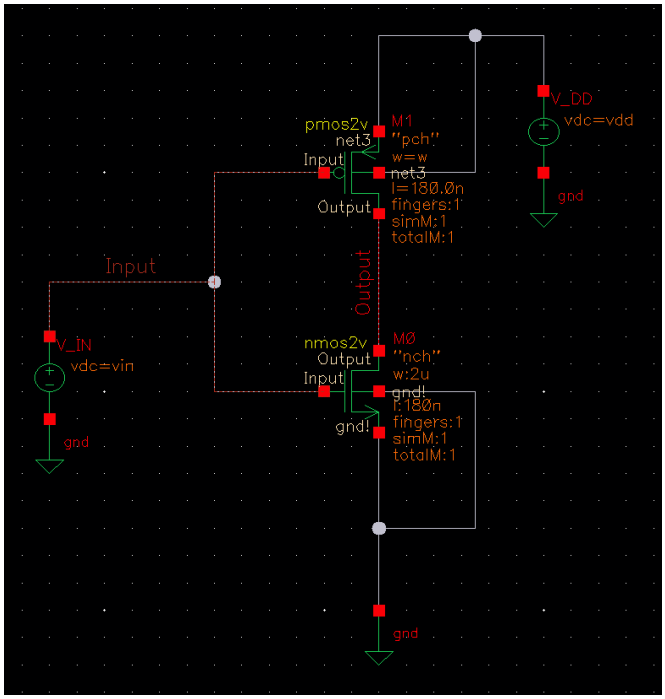
Specs of the devices used –

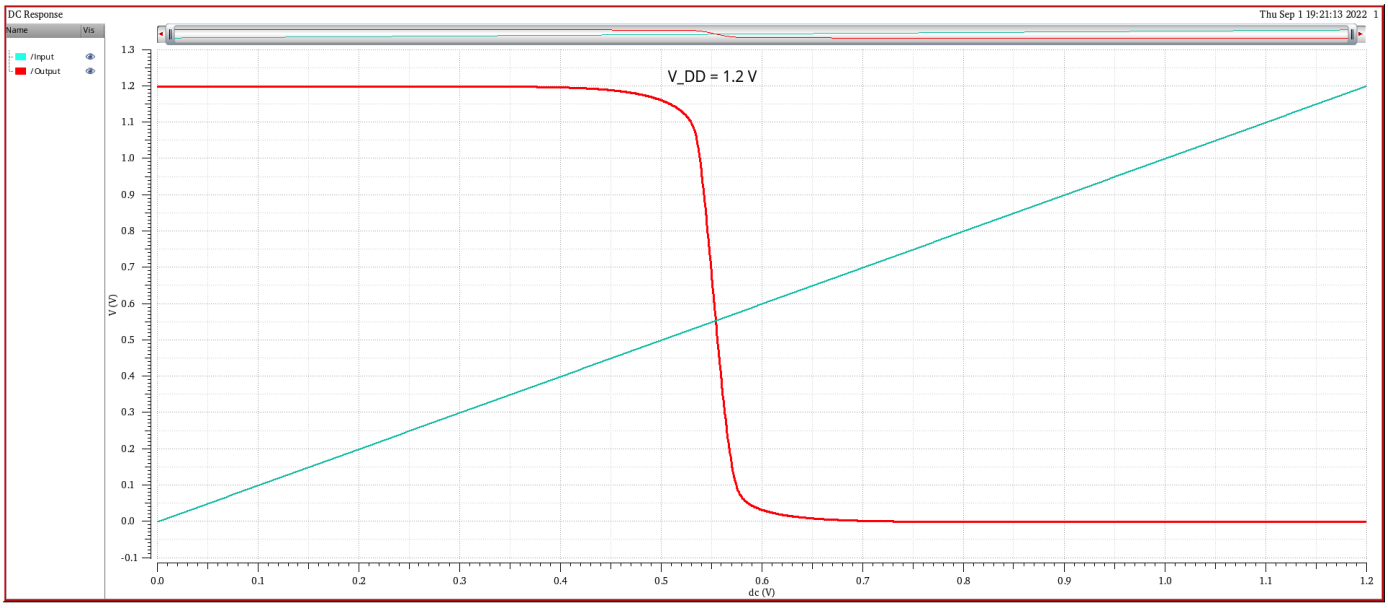
Both PMOS and NMOS are from the TSMC 180 nm technology library which has Length as 180 nm and Width as 2 µm.

Implementation of CMOS

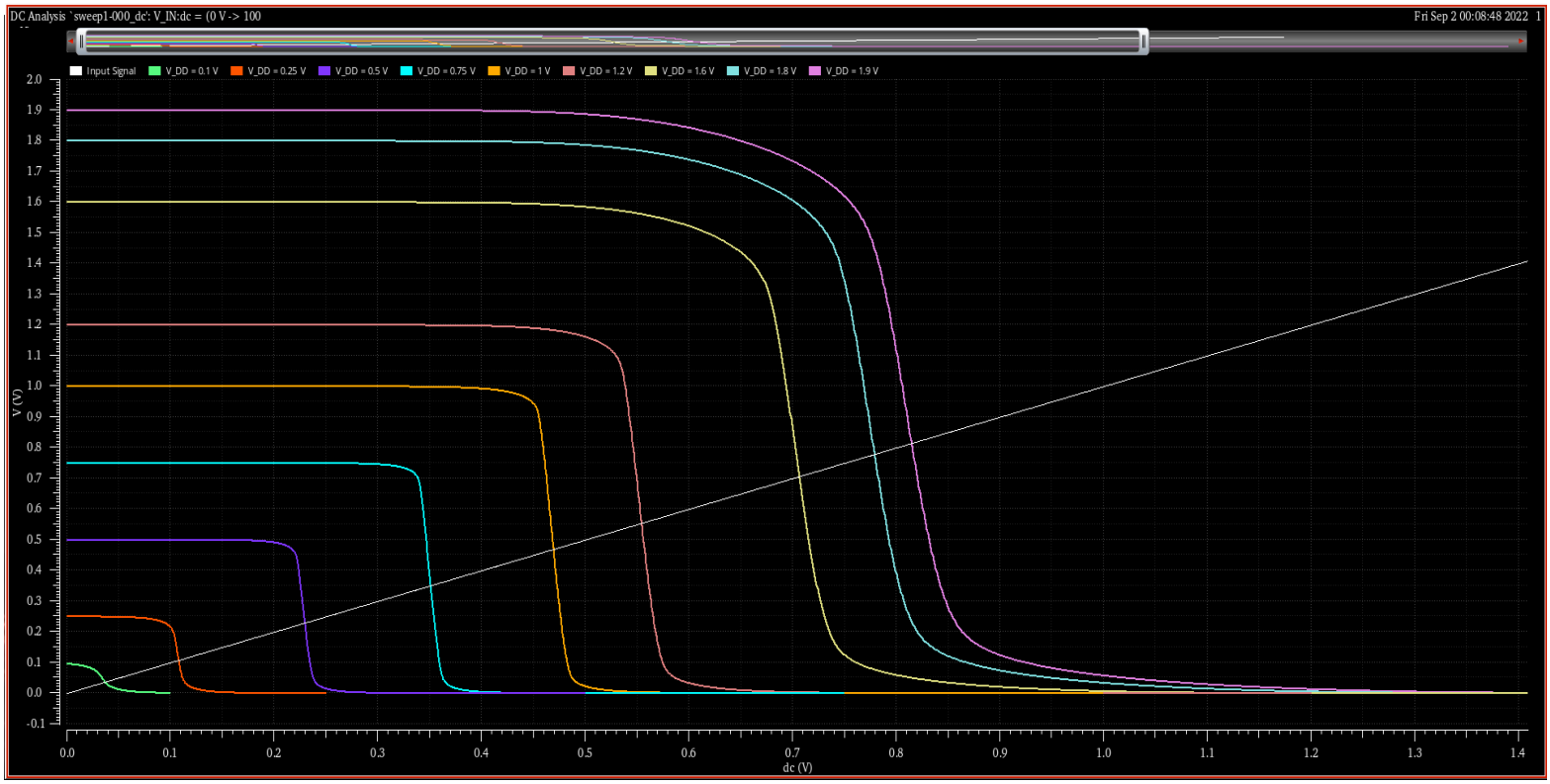


DC Simulations –

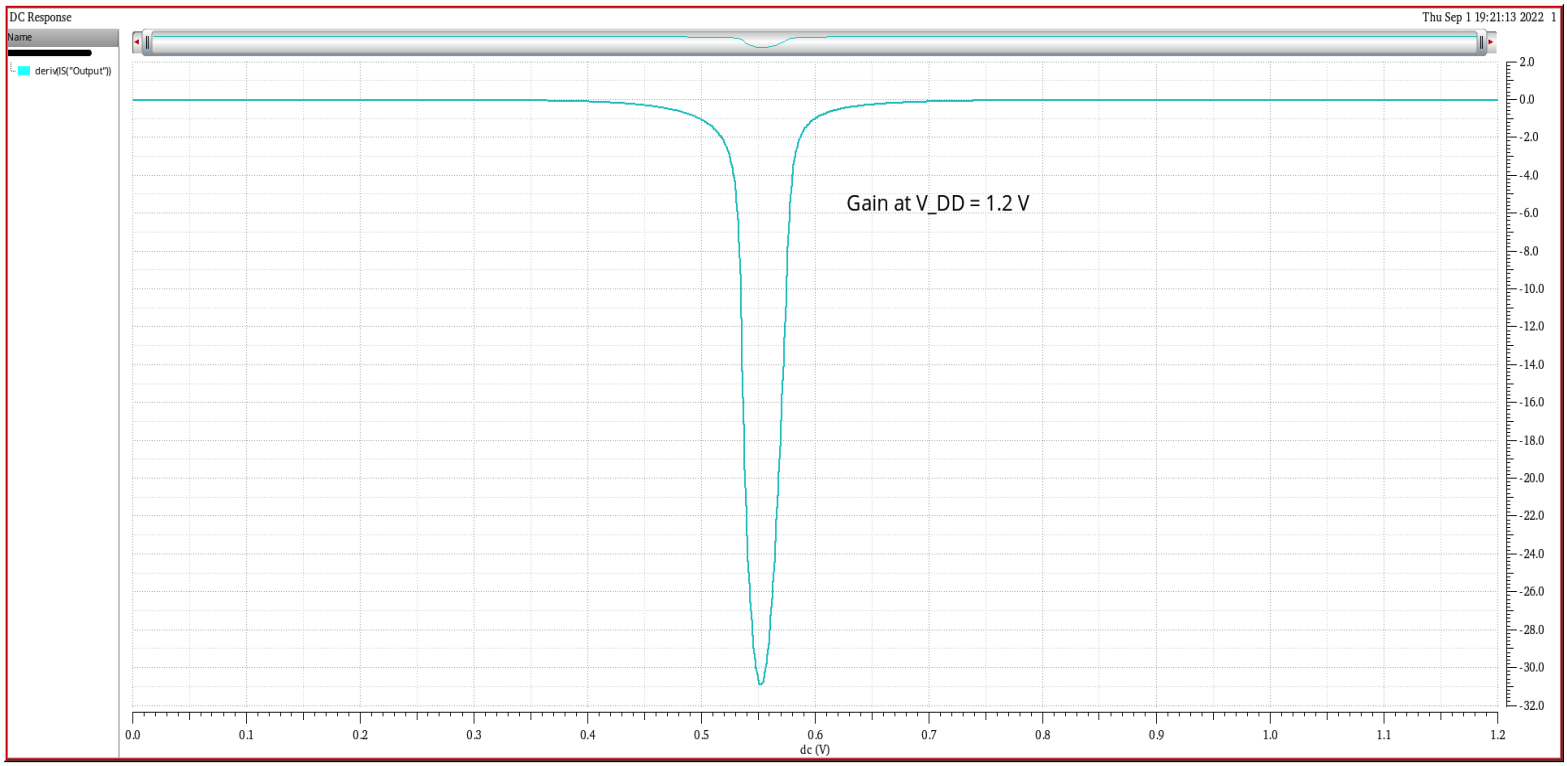
Voltage Transfer Characteristics



V_{DD} = 1.2V and input voltage sweep is upto 1.2V

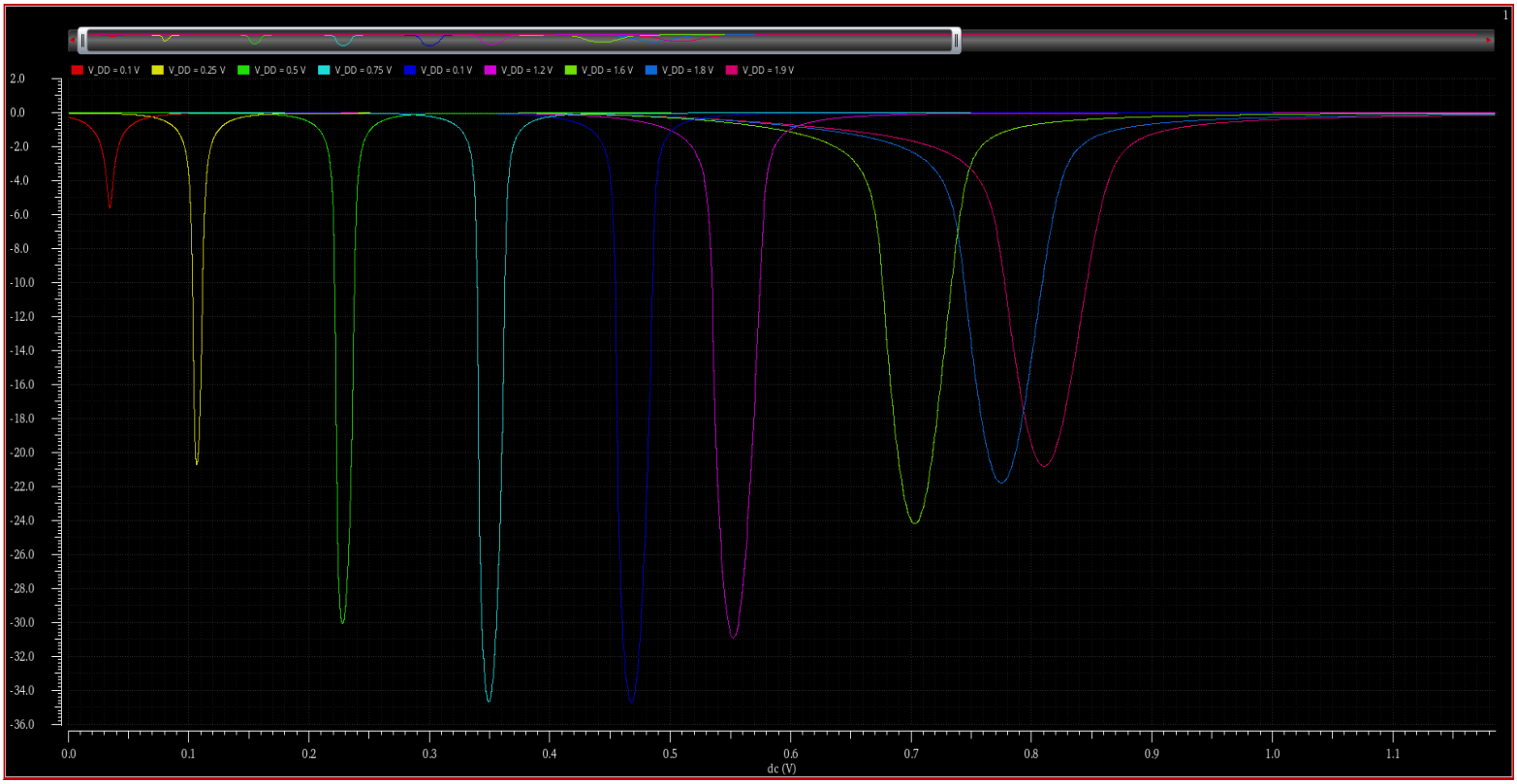


VTC by varying V_{DD} from 0.1V to 1.9V



Gain for $V_{DD} = 1.2V$

Noise margins (both NM_H and NM_L) can be calculated using the gain plots to find out the frequency crossings at which gain is -1 and then subtracting V_{OL} and V_{OH} to find NM_L and NM_H respectively.



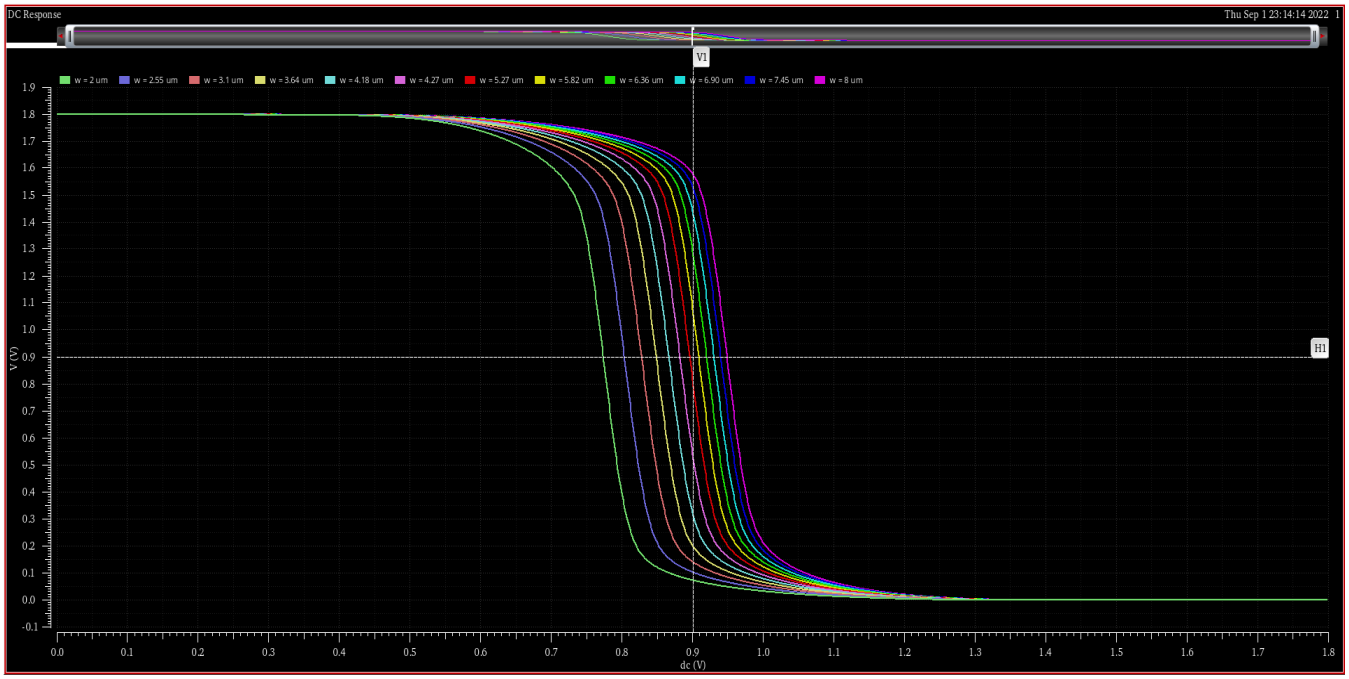
Gains for varying V_{DD}

Table for calculated Noise Margins and Peak gains

V_{DD}	Noise Margin Low	Noise Margin High	Peak Gain
0.1V	19.97 mV	52.28 mV	-5.515
0.25V	89.66 mV	125.69 mV	-20.705
0.5V	208.15 mV	249.75 mV	-30.008
0.75V	325.85 mV	374.40 mV	-34.686
1V	434 mV	498.57 mV	-34.651
1.2V	499.27 mV	601.27 mV	-30.849
1.6V	591.9 mV	818.65 mV	-24.122
1.8V	628.36 mV	930.83 mV	-21.652
1.9V	644.91 mV	987.79 mV	-20.705

From the above graph and table, the peak gain first increases when V_{DD} is swept from 0.1V to 0.75V and then decreases.

VTC Plot by changing relative sizes



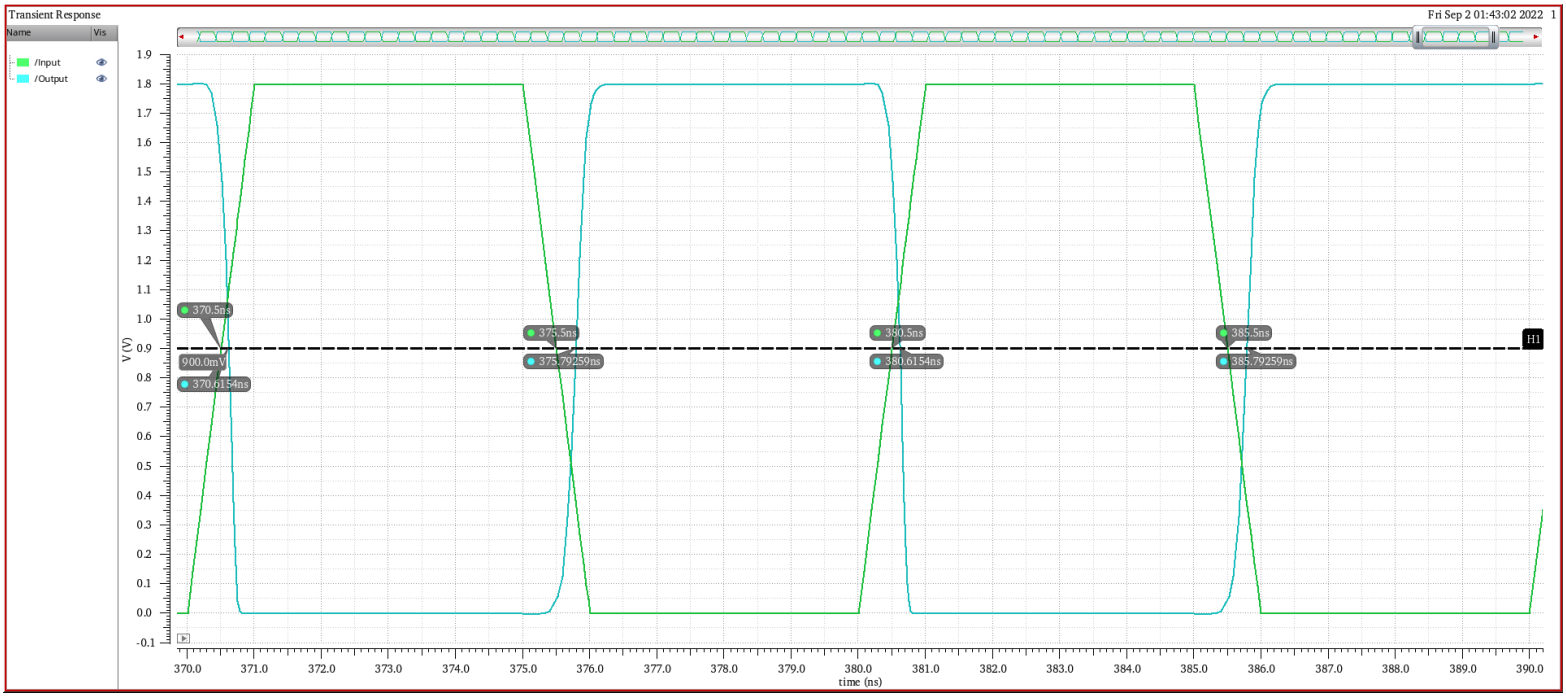
V_{DD} = 1.8V and width of PMOS is varied

Clearly from the plot, the ideal CMOS inverter has PMOS width around 5.4 µm for NMOS width at 2 µm.

Transient Simulations –

Here we provide a pulse at the input with a time period of 10 ns and rise time and fall time of 1 ns with duty cycle of 50% to observe the propagation delay.

Transient Plot



Load Capacitance of 50 fF

Propagation delay can be written as: $t_p = \frac{t_{pHL} + t_{pLH}}{2}$

From the above plot, $t_{pHL} = 115.4\,ps$ and $t_{pLH} = 292.59\,ps$

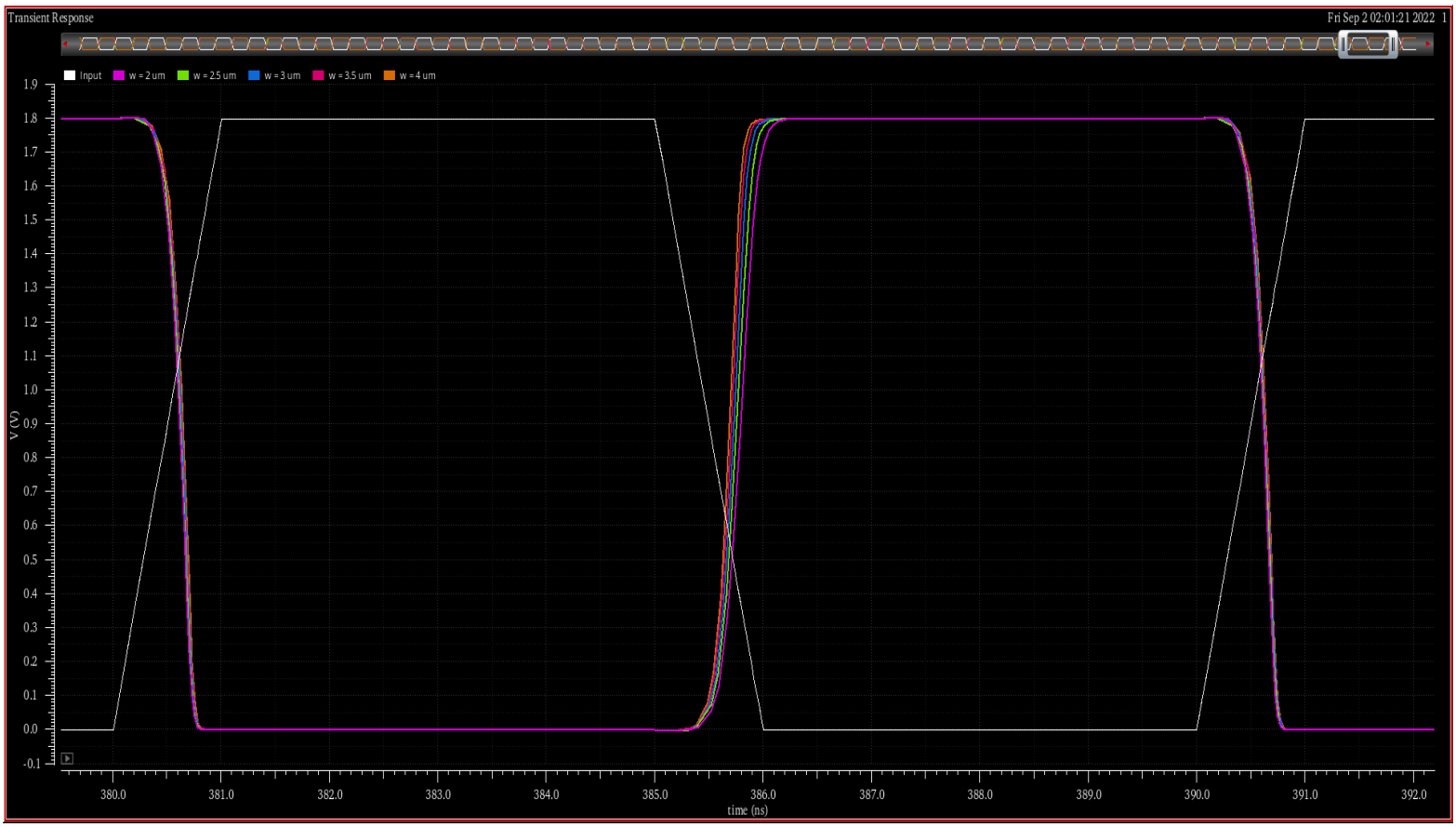
So propagation delay, $t_p = 203.995\,ps$

Now we can also calculate the resistance of mosfets by the formula-

$$R_{PMOS} = \frac{t_{pLH}}{0.693 * C_L} = 8.44\,k\Omega$$

$$R_{NMOS} = \frac{t_{pHL}}{0.693 * C_L} = 3.33\,k\Omega$$

Transient plot by varying width of PMOS



$V_{DD} = 1.8V$ and width is varied between 2 µm and 4 µm

Observe that t_{pHL} increases (almost insignificant) as width increases and t_{pLH} reduces as width increases.

Conclusions from DC simulation plots –

- VTC is not exactly symmetrical about V_{DD} / 2 but slightly shifted left for regular parameters.
- From the gain plots, we can say that as we increase V_{DD} , at first the peak gain increases till $V_{DD} = 0.75V$ and then peak gain reduces upon further increasing V_{DD} .
- The noise margin increases upon increasing V_{DD} but observe that NM_H and NM_L are not equal. This is due to VTC not being centered at V_{DD} / 2.
- For an ideal CMOS, the output voltage at applied input voltage of V_{DD} / 2 must be V_{DD} / 2 , for which the width of PMOS must be around 5.4 μm (width of NMOS is 2 μm).

Conclusions from Transient plots –

- The propagation delay in CMOS with load capacitance of 50 fF is 203.995 ps.
- Resistance of NMOS and PMOS are 3.33 kΩ and 8.44 kΩ respectively.
- Due to the lower mobility of holes, the current provided by PMOS is lower than that of NMOS which is indicated by higher value of t_{pLH} with respect to t_{pHL} .
- To overcome this we can increase the width of PMOS which reduces t_{pLH} which is evident from the last graph. There is also a slight increase in t_{pHL} but this is insignificant when compared to the change in t_{pLH} and so in effect the overall delay (t_p) of the system reduces.