Introduction to VLSI Design

SRAM and DRAM Cells

Material primarily form textbook and lecture slides for Rabaey et. al. Digital Integrated Circuits, 2nd Edition (2002) and other online resources

Read-Write Memories (RAM)

- STATIC (SRAM)

  Data stored as long as supply is applied

  Large (6 transistors/cell)

  Fast

  Differential

- DYNAMIC (DRAM)

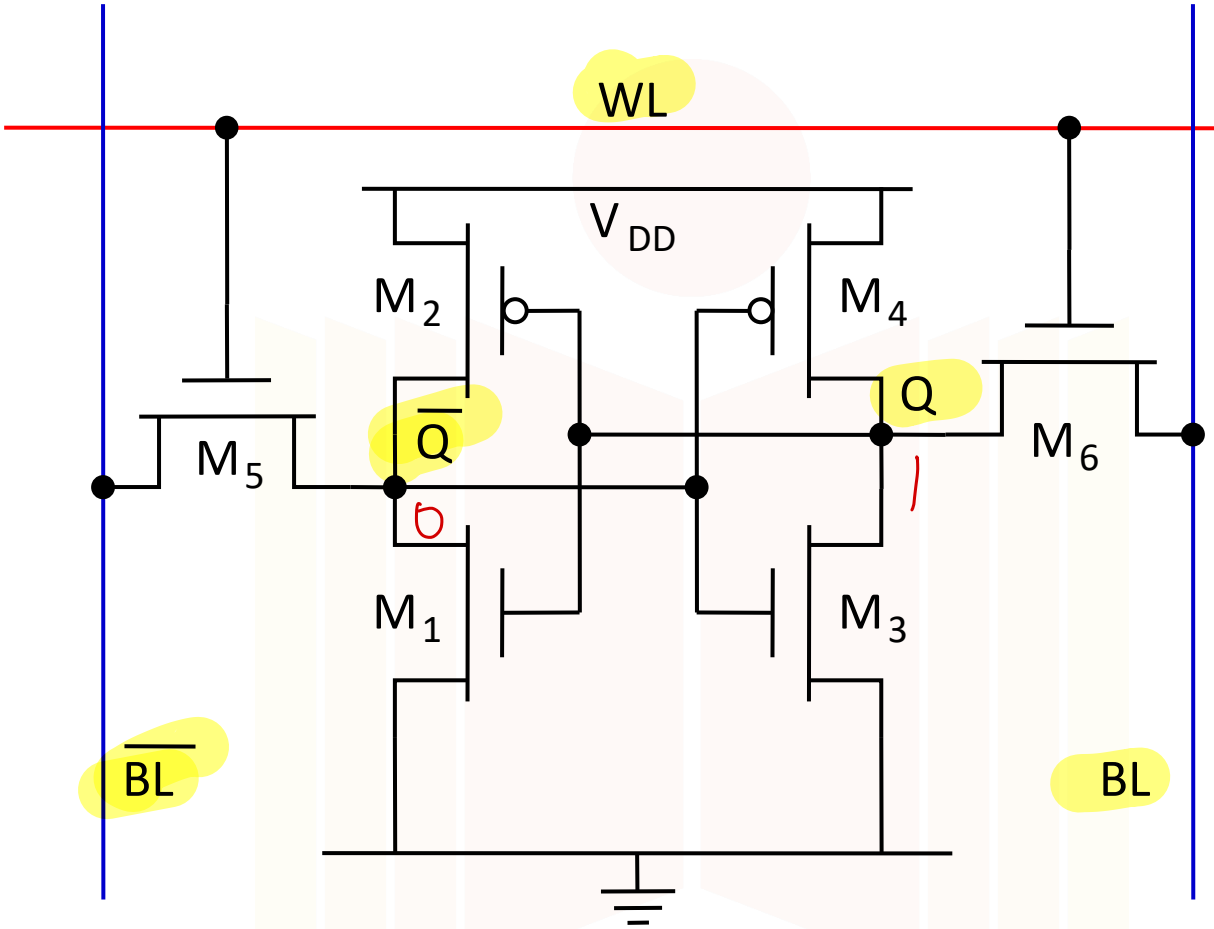
  Periodic refresh required

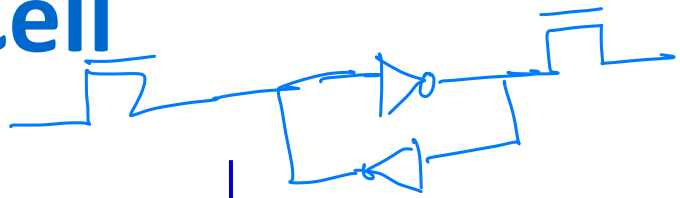
  Small (1-3 transistors/cell)

  Slower

  Single Ended

6-transistor CMOS SRAM Cell





WL = 0

SRAM - Hold

WL = High

Read Write

SRAM Evolution with technology nodes

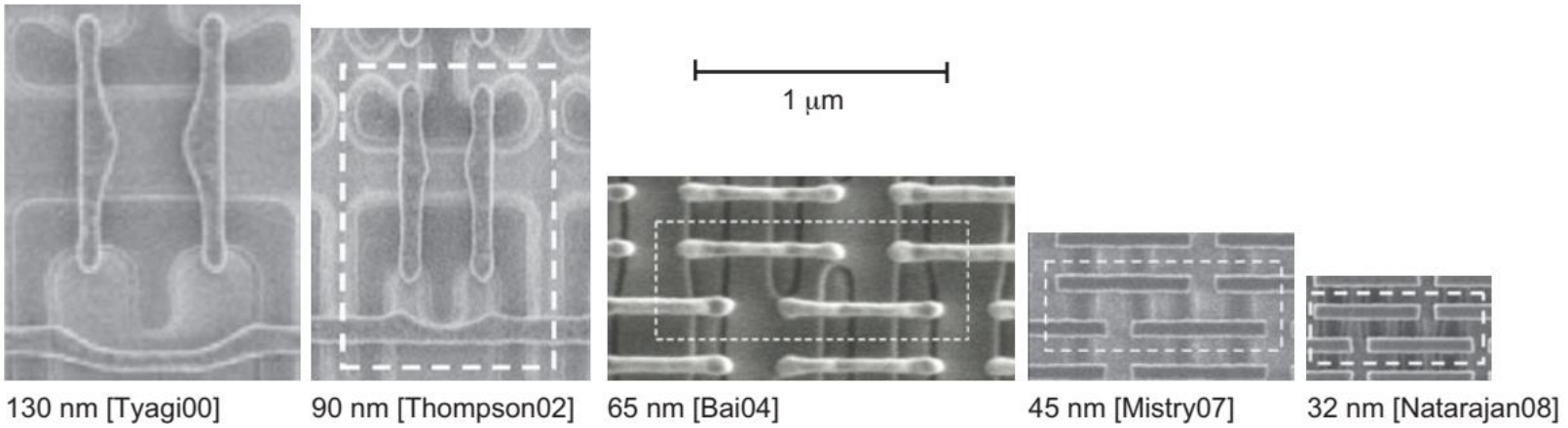


FIGURE 12.16 SRAM scaling (© 2000–2008 IEEE.)

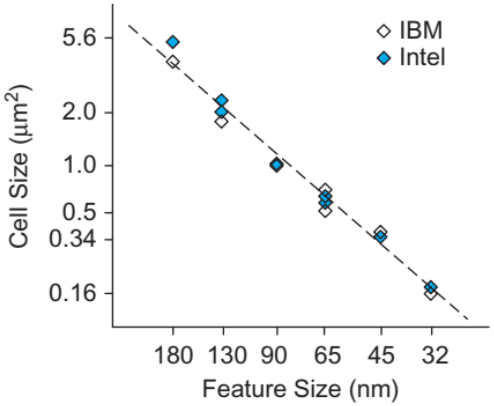
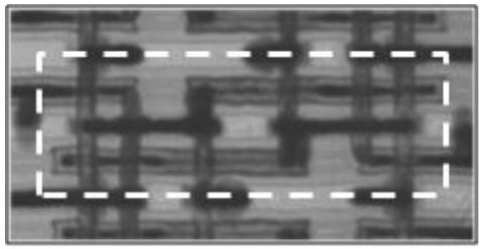


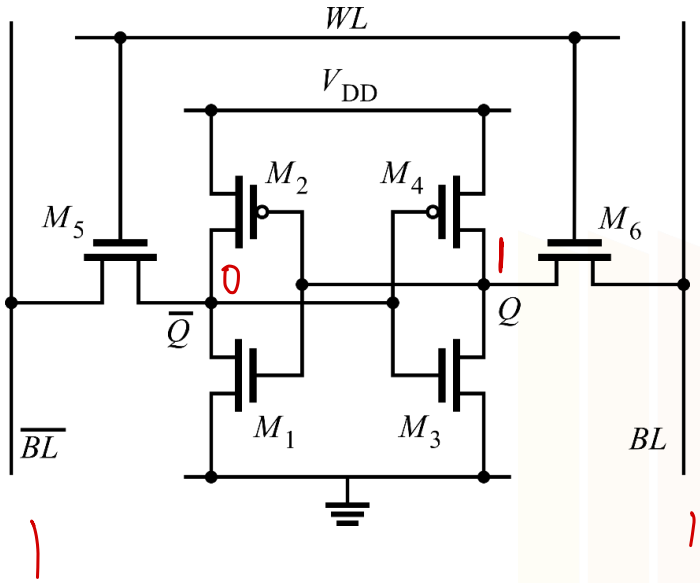
FIGURE 12.17 SRAM cell size vs. feature size

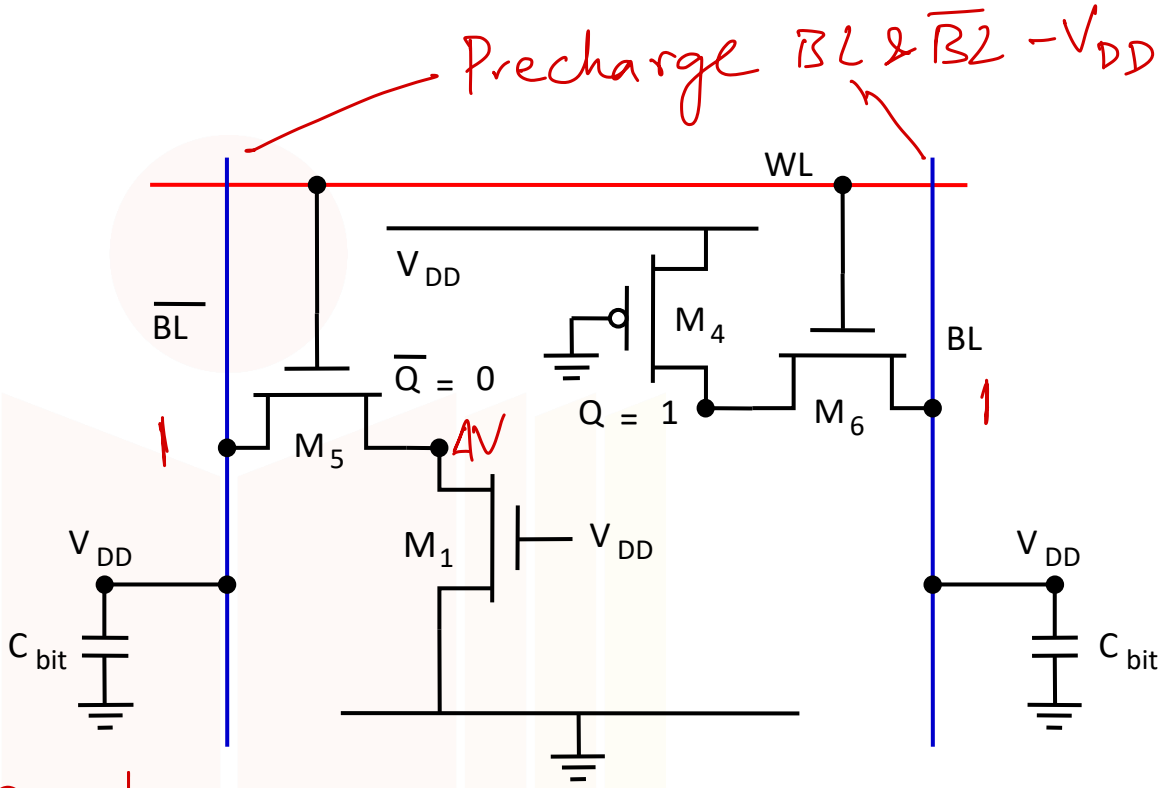
14 nm Process



.0588 um²

CMOS SRAM Analysis (Read - 1)





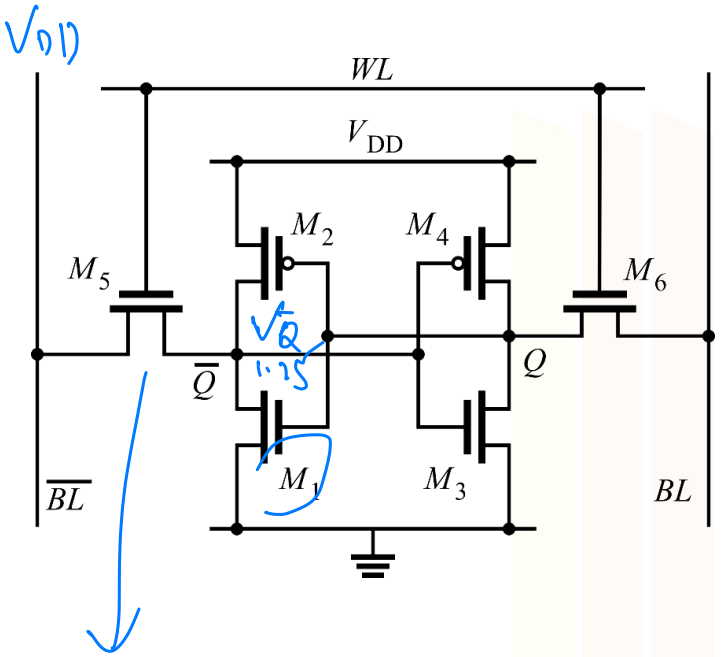
$\overline{BL}$ discharges $\Rightarrow Q = 1$

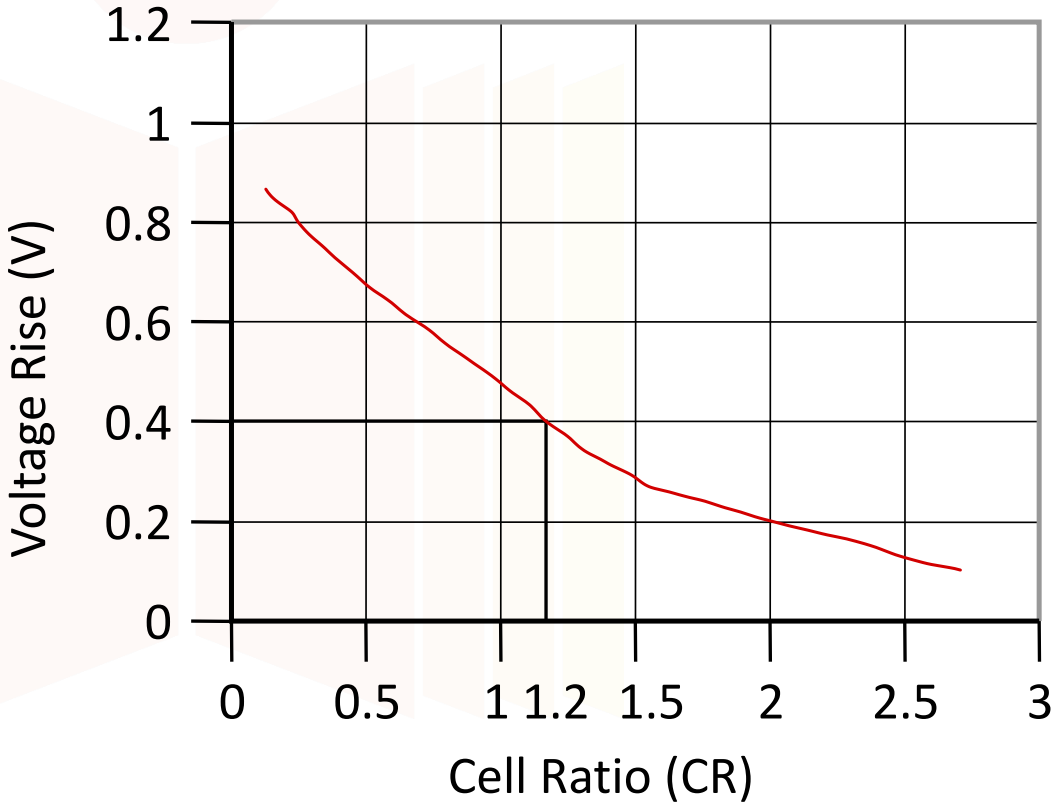
BL discharges $\Rightarrow Q = 0$

CMOS SRAM Analysis (Read)

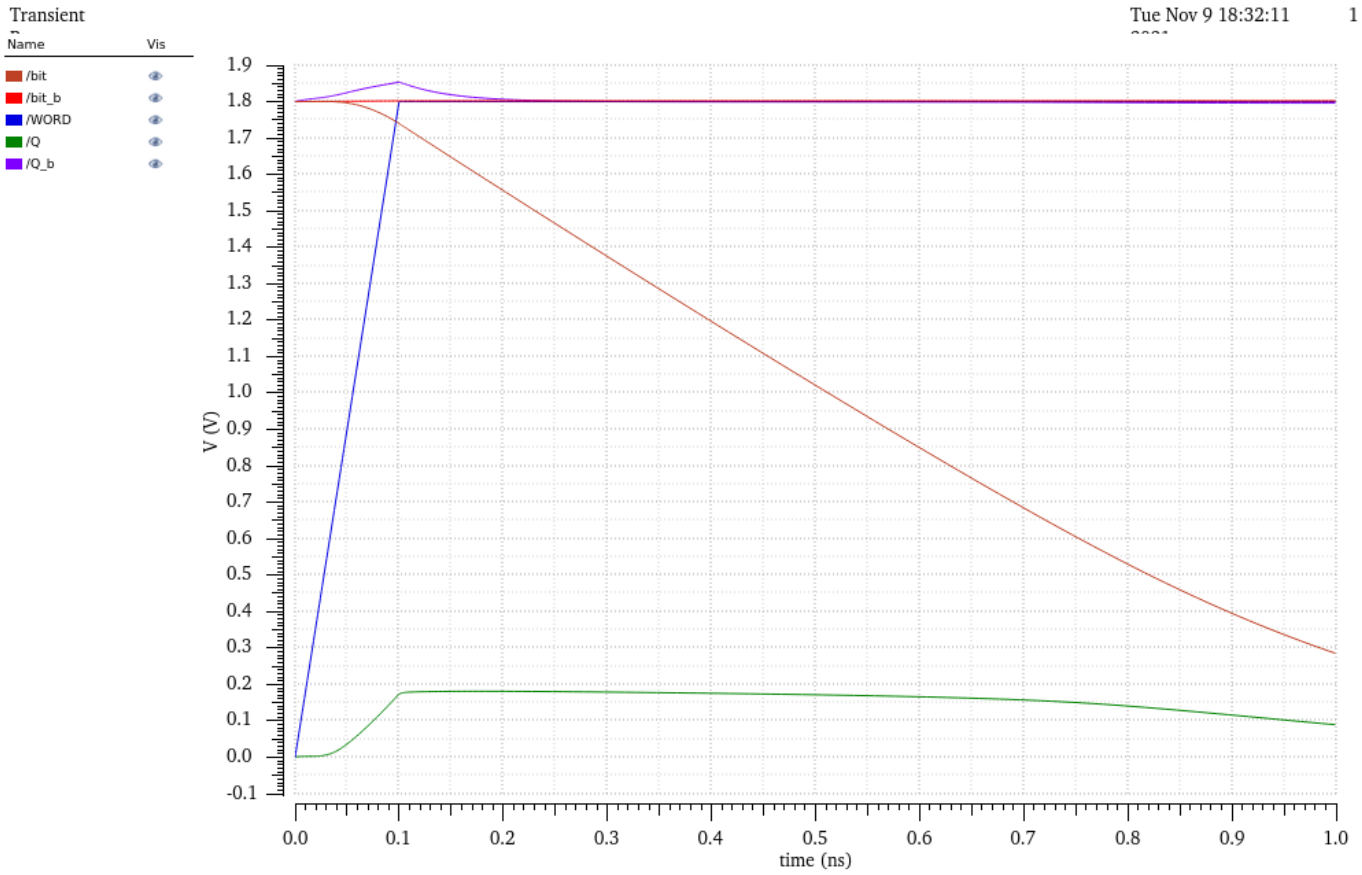
$$CR = \frac{W_1/L_1}{W_5/L_5}$$ > 1.2

to avoid read upset



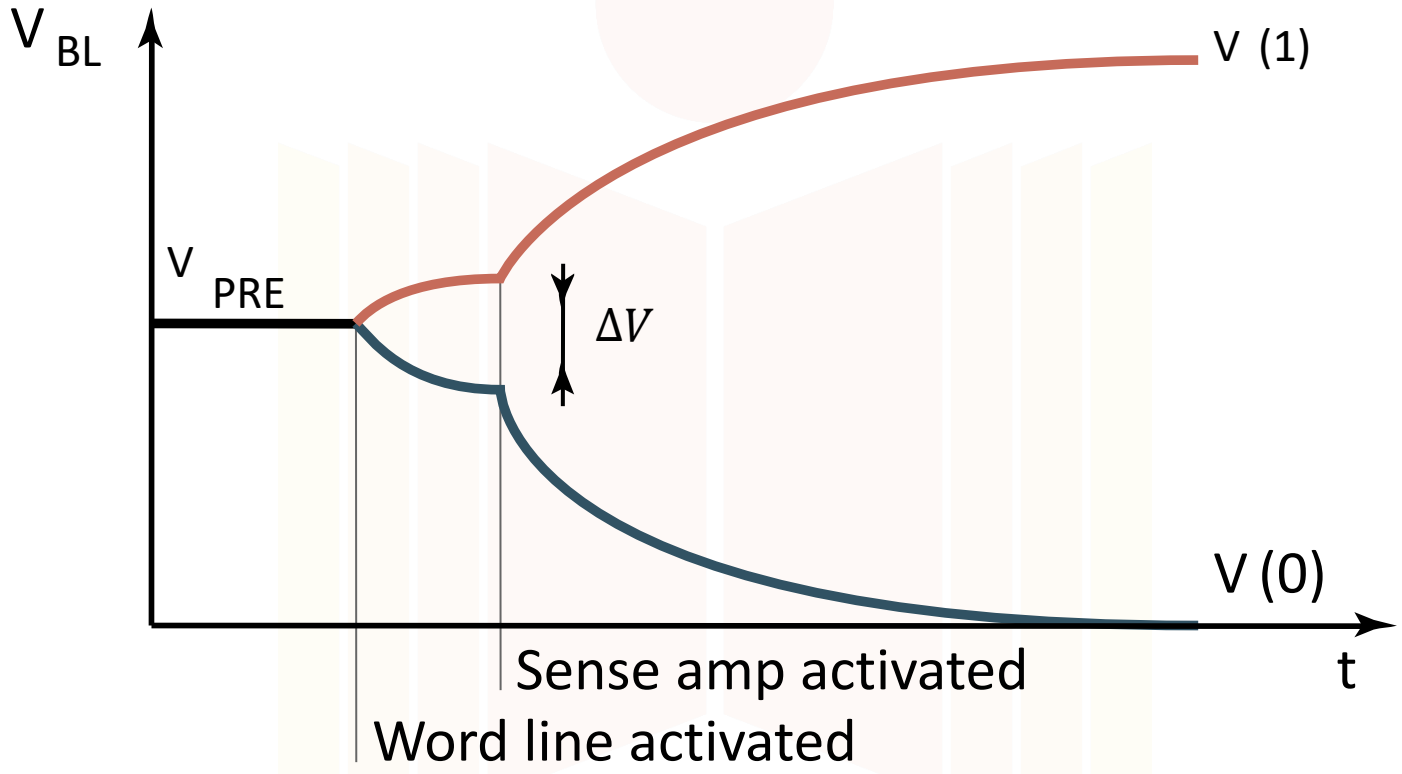


SRAM Read Operation

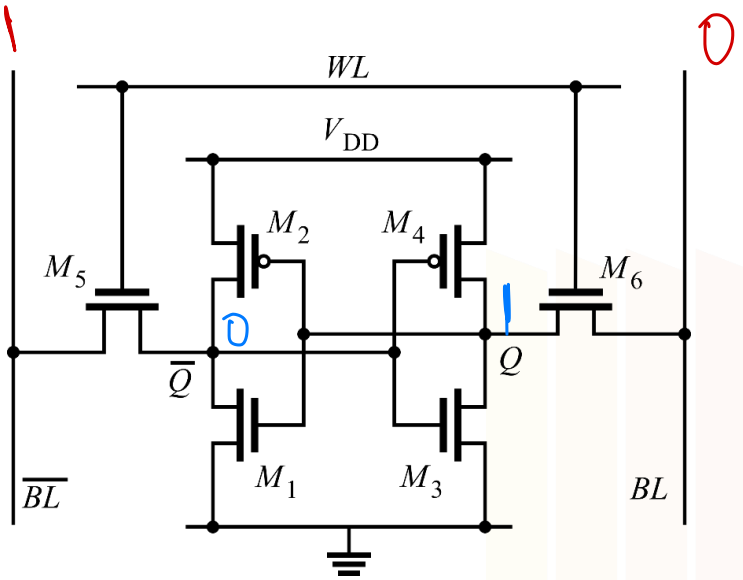


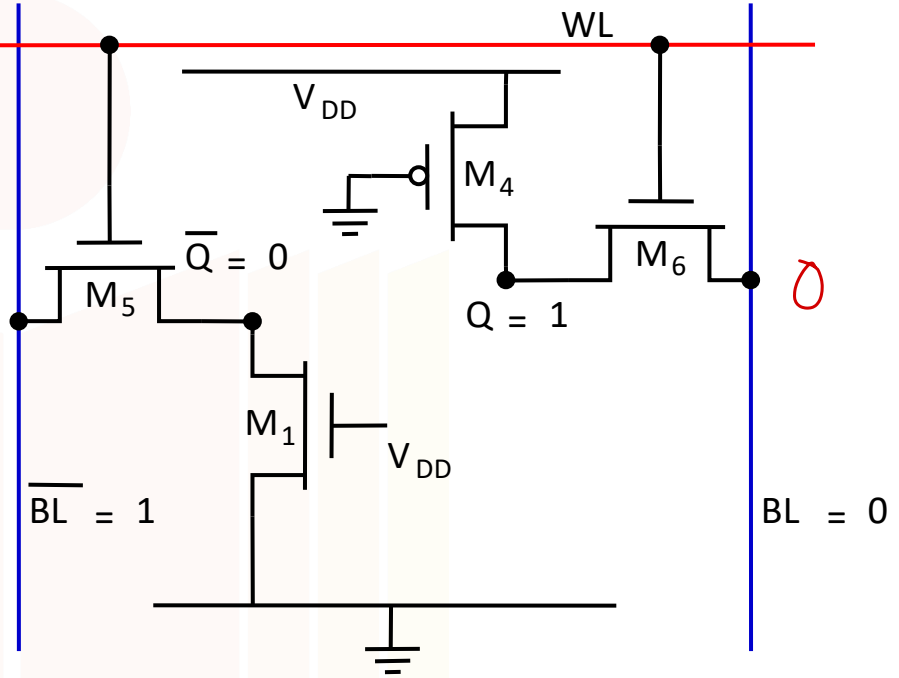
(Memory has Q = 0&Q_b = 1) this should be reflected in bit and bit_b respectively which are pre-charged initially

Sense Amp Operation



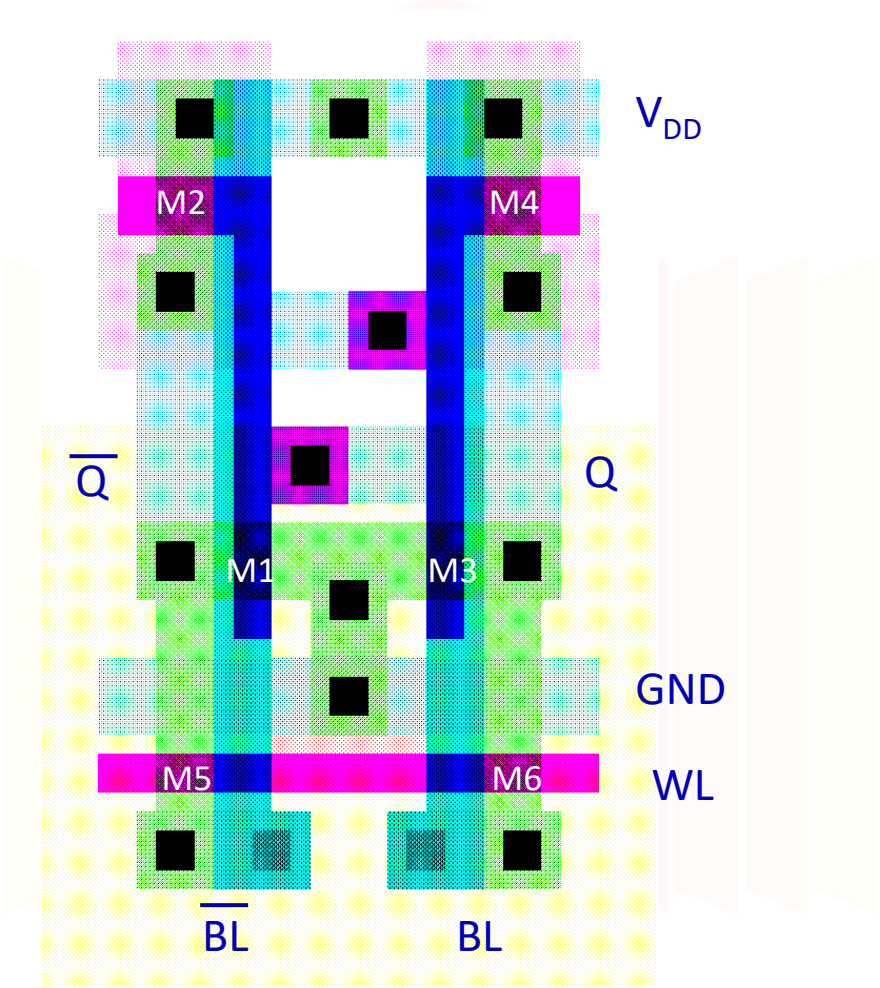
CMOS SRAM Analysis (Write-0)



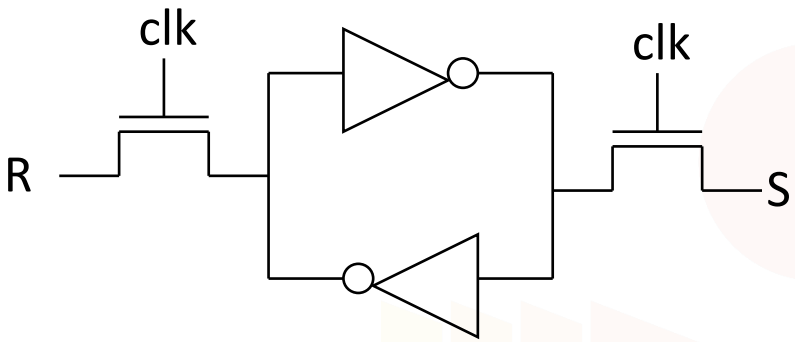


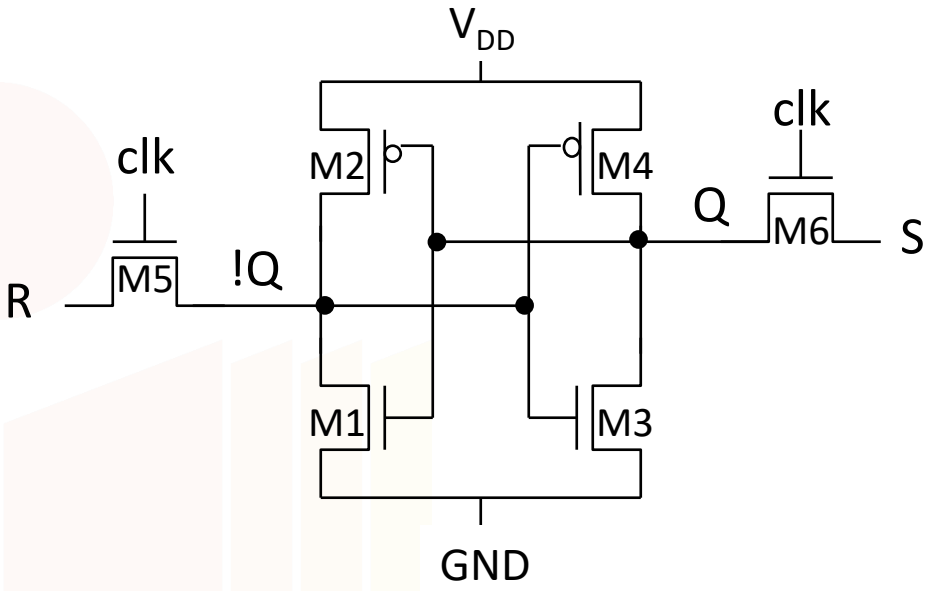
PU ratio = $\frac{W_4/L_4}{W_6/L_6}$

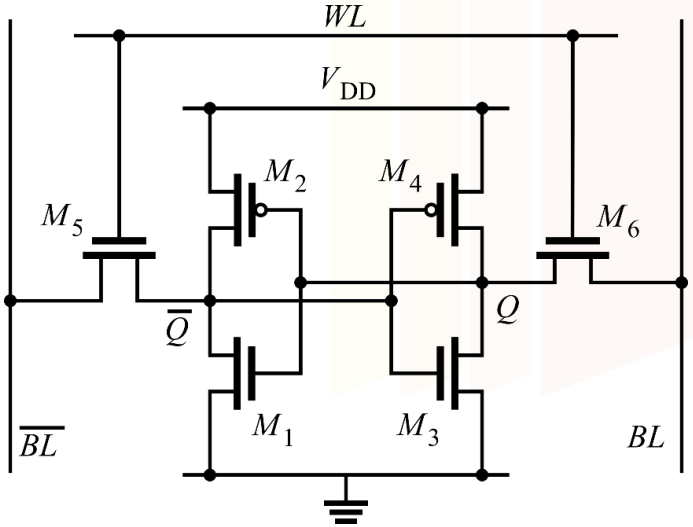
6T-SRAM — Layout



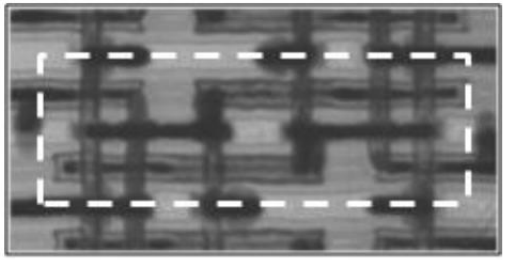
6T SR Latch





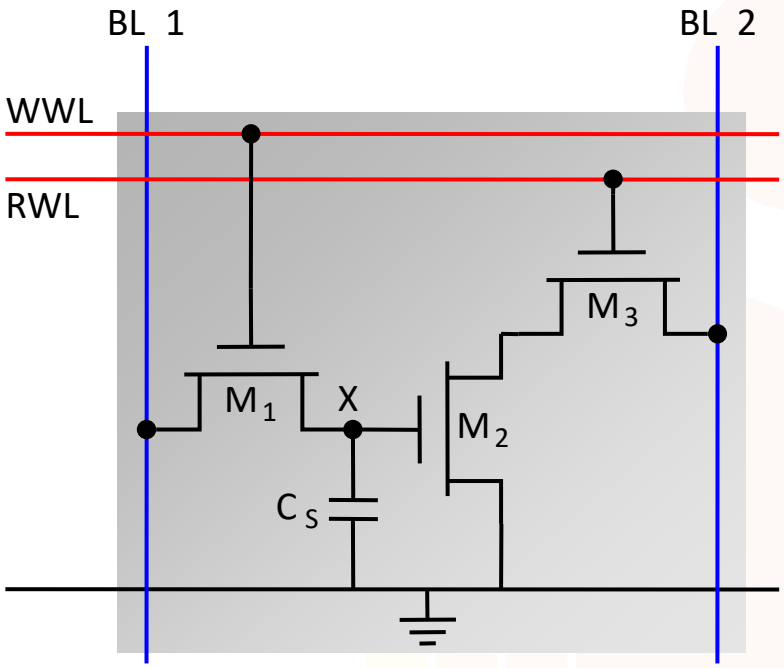


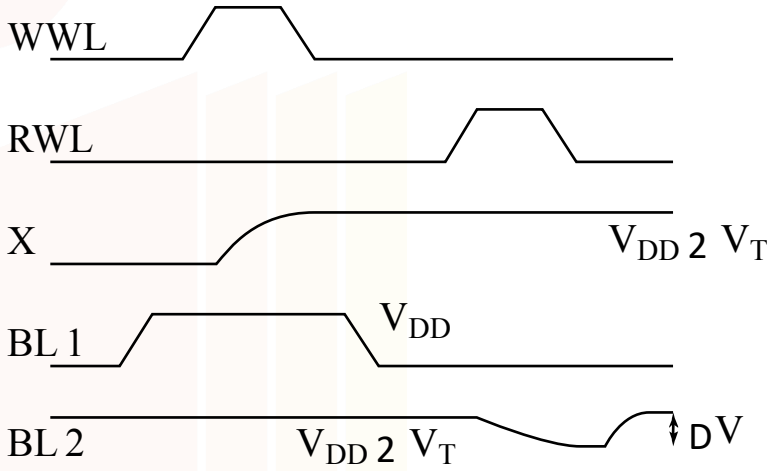
14 nm Process



.0588 um^2

3-Transistor DRAM Cell





No constraints on device ratios

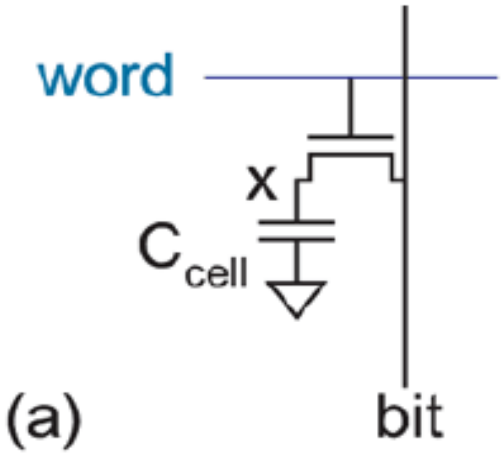
Reads are non-destructive

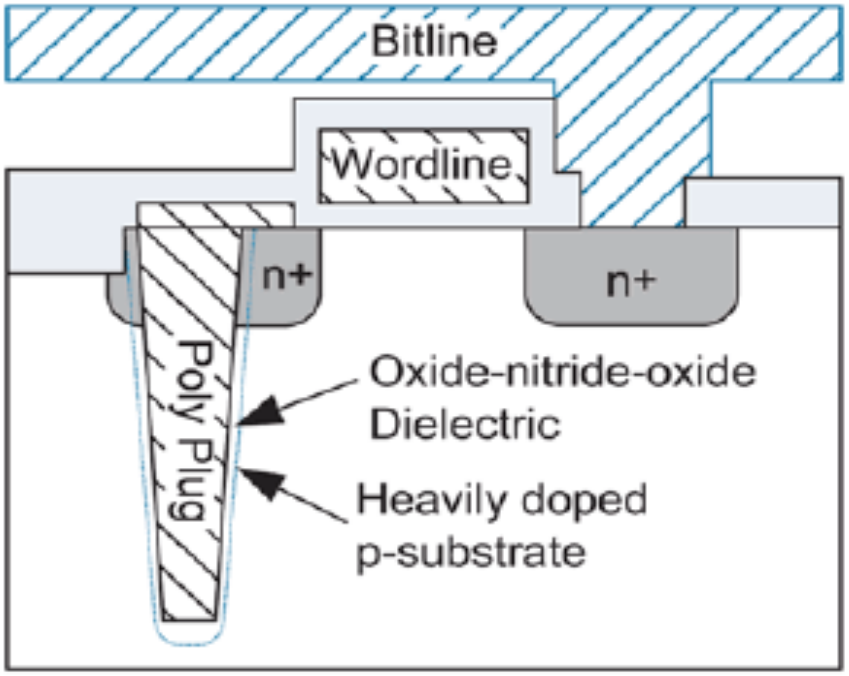
Value stored at node X when writing a “1” = V

WWL -V_{Tn}

DRAM: Dynamic RAM

- Store their contents as charge on a capacitor rather than in a feedback loop.
- 1T dynamic RAM cell has a transistor and a capacitor





1-Transistor DRAM Cell