VLSI Design - Lecture 9

26th Aug 2022

$t_p = t_{p0}\left(1 + \frac{C_{ext}}{S\,C_{int}}\right)$

C_{ext} → Gate cap of next stage $j+1$

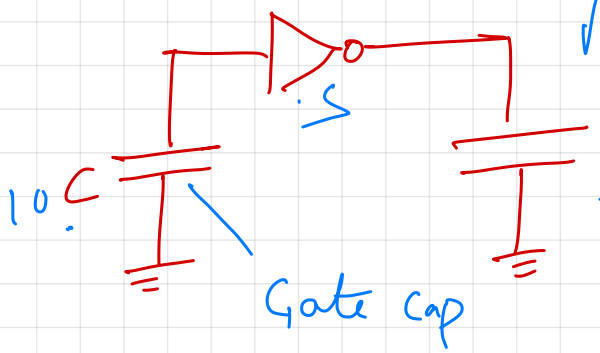
C_{int} → Drain cap of current stage j^{th} stage

$C_{diff} = \gamma\, C_{gate}$

↳ Technology dependent parameter

$= t_{p0}\left(1 + \frac{C_{g,j+1}}{\gamma\, C_{g,j}}\right)$ $\quad f = \frac{C_{g,j+1}}{C_{g,j}}$

$= t_{p0}\left(1 + \frac{f}{\gamma}\right)$



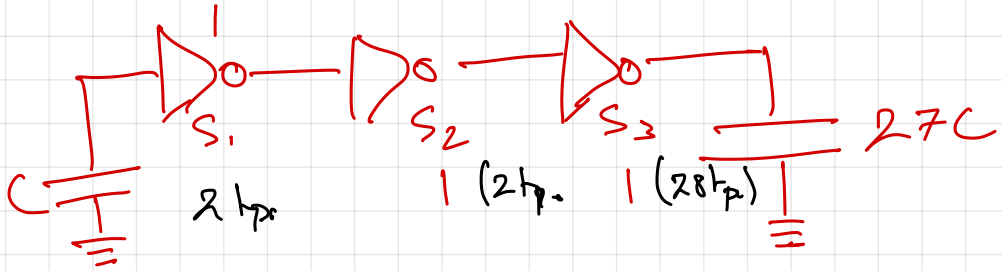
Gate cap

↳ Load capacitance

$\gamma = 1$ $\quad t_p = t_{p0}(1 + 27)$

$= 28\, t_{p0}$

$S = 10$ $\quad t_p = t_{p0}(1 + 2.7) = 3.7 t_{p0}$



$1\,(2t_{p0})$ $\quad 1\,(11t_{p0})$ $\quad 10\,(3.7t_{p0})$

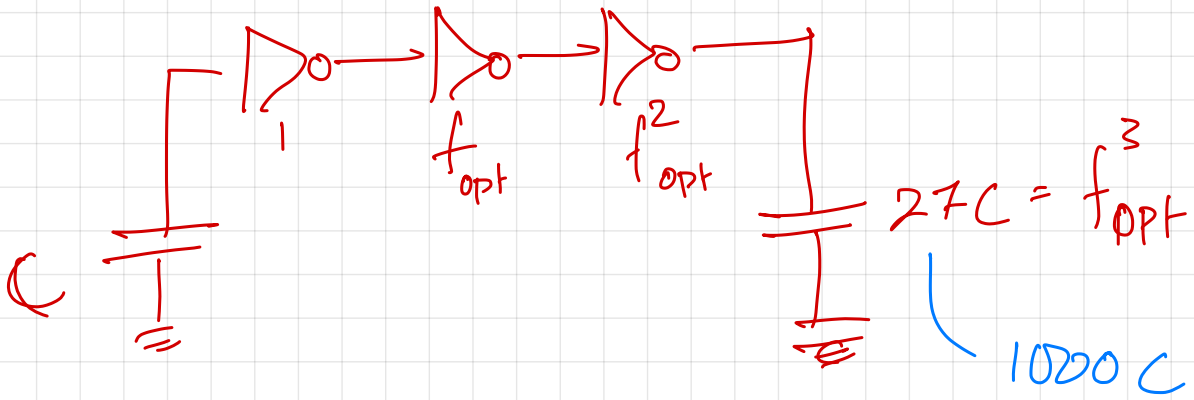
① $32\, t_{p0}$

② $16.7\, t_{p0}$

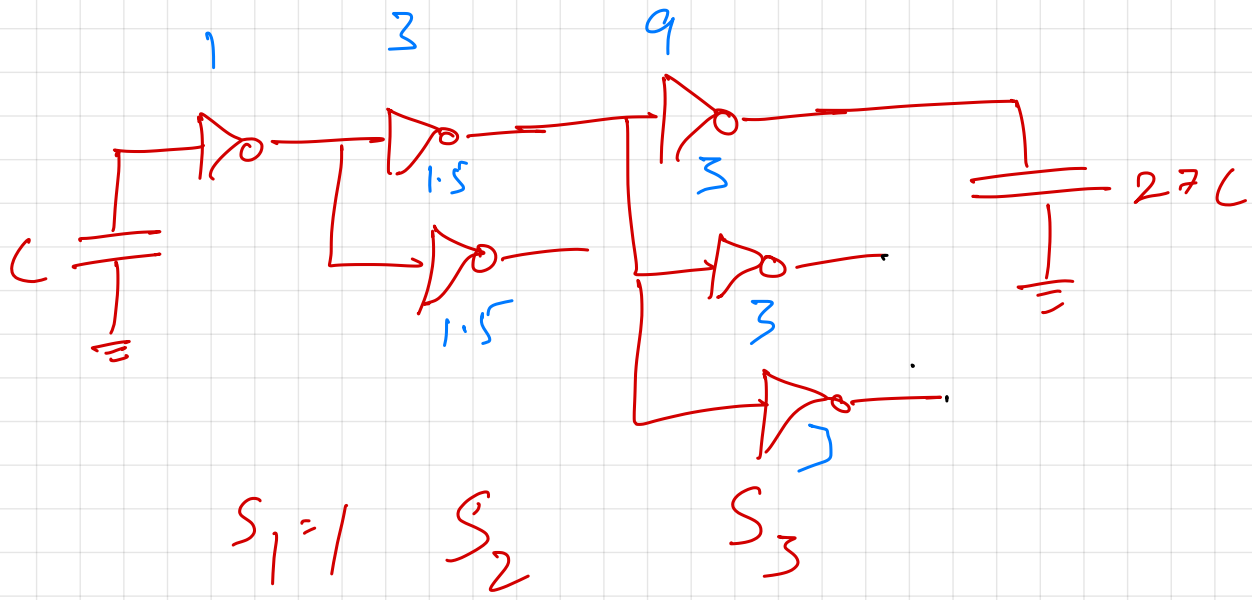
$$t_p = \sum_j t_{p,j} = \sum_j t_{p0}\left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}}\right)$$

$$\frac{dt_p}{dC_{g,j}} \qquad \frac{t_{p0}}{\gamma}\left(1 + \cdots \frac{C_{g,j}}{C_{g,j-1}} + \frac{C_{g,j+1}}{C_{g,j}} + \cdots\right)$$

$$\Rightarrow \quad \frac{1}{C_{g,j-1}} - \frac{C_{g,j+1}}{C_{g,j}^2} = 0 \qquad C_{g,j} = \sqrt{C_{g,j-1}\,C_{g,j+1}}$$



F	No. of stages	Delay per stage	Total delay
27	1	$28\,t_{p0}$	$28\,t_{p0}$
1000	1	$1001\,t_{p0}$	$1001\,t_{p0}$
10000	1	$10000\,t_{p0}$	$10001\,t_{p0}$
10000	2	$101\,t_{p0}$	$202\,t_{p0}$
10000	3	$22.5\,t_{p0}$	$45\,t_{p0}$
10000	4	$11\,t_{p0}$	$44\,t_{p0}$



$S_1 = 1 \quad S_2 \quad S_3$