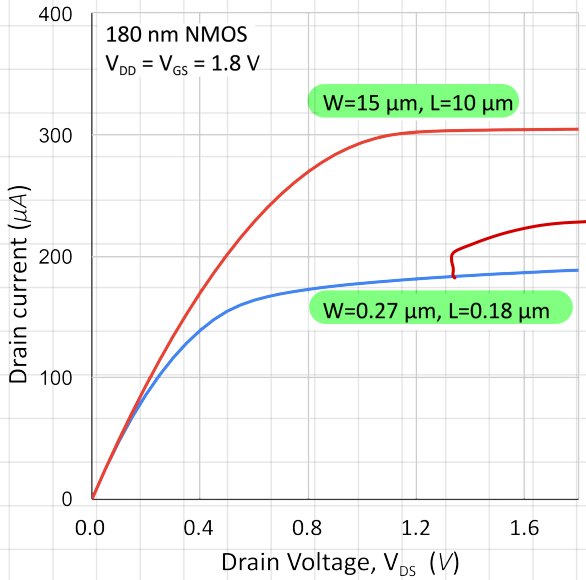
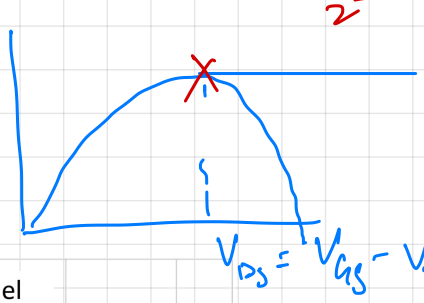
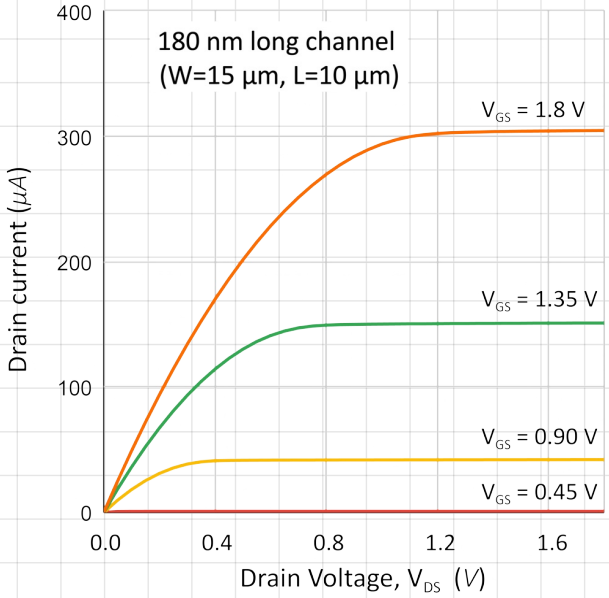
VLSI Design - Lecture 4
8th Aug 2022

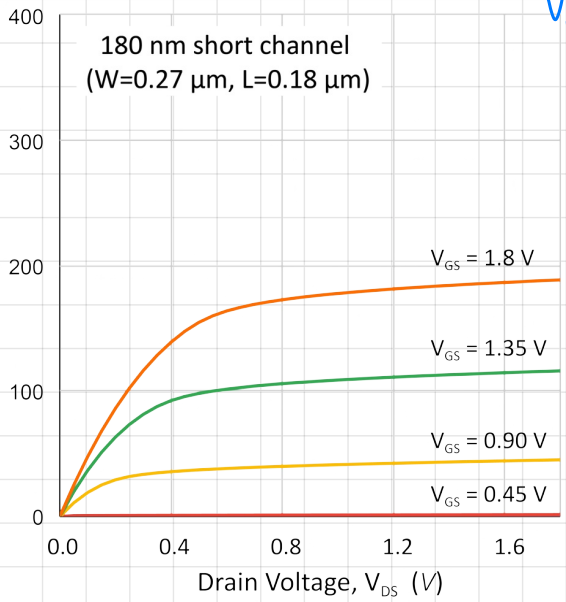


$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_T)V_{DSATn} - \frac{V_{DSATn}^2}{2}\right]$$

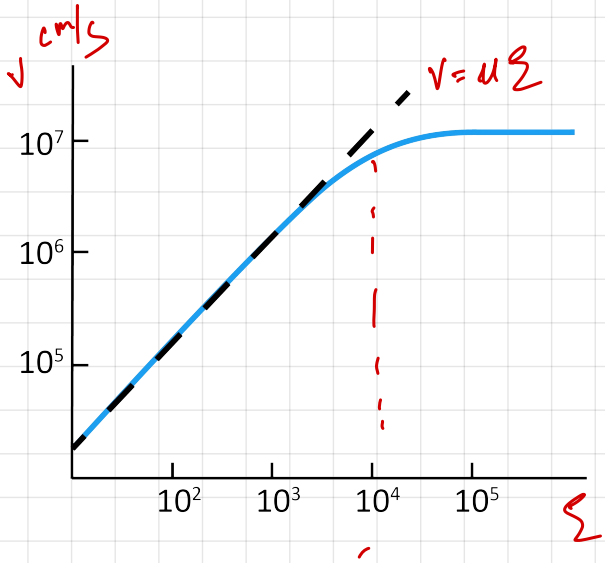
$$I_D = \left(k_n' \frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

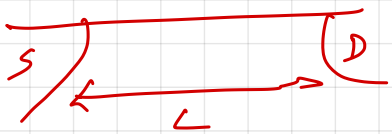




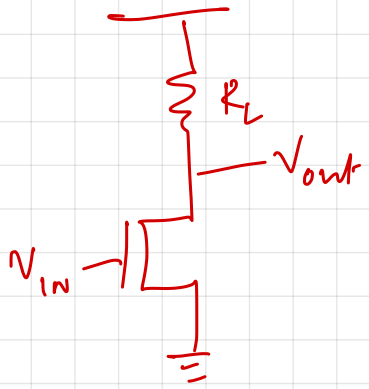


$$I_D = \frac{1}{2} k_n' \frac{W}{L}(V_{GS} - V_T)^2$$





$$\mathcal{E} = \frac{V_{DS}}{L}$$

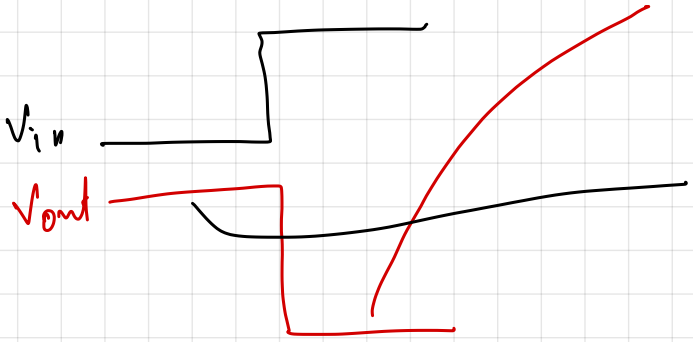


① $V_{OL} \neq 0$

② R_L is not area efficient

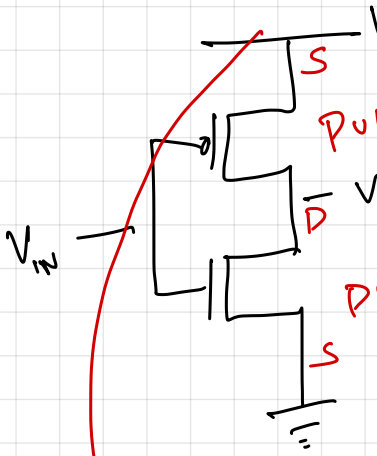
③ Power dissipation is significant

$$P_{drawn} = V_{DD} \times \left(\frac{V_{DD} - V_{out}}{R_L} \right) = mW$$



$P_{drawn} = V_{DD} \times I_{off} = pW$

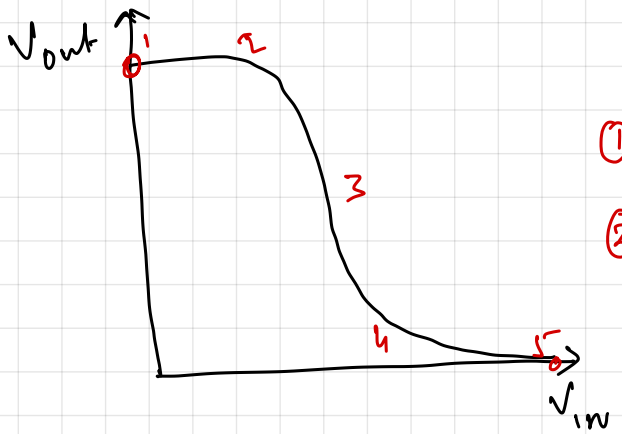
$P_{avg} = mW$



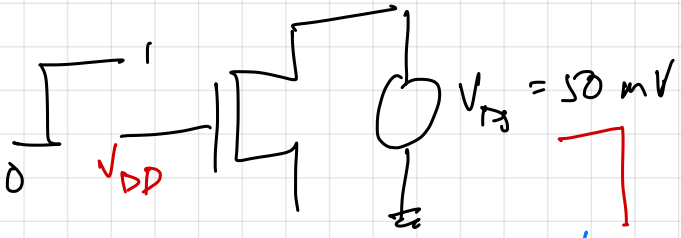
	NMOS	PMOS
$V_{IN} = 1$	$V_{GS} = V_{IN}$ $V_{DS} = 0$	$V_{GS} = 0$ $V_{DS} = -V_{DD}$
$V_{IN} = 0$	$V_{GS} = 0 < V_T$ NMOS is off	$V_{GS} = -V_{DD} > V_T$ PMOS is on V_{DS}

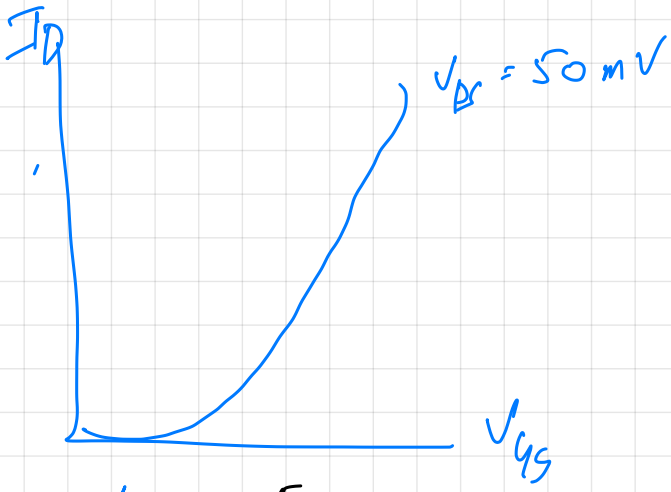
Direct path from V_{DD} to Gnd doesnot exist in static phase

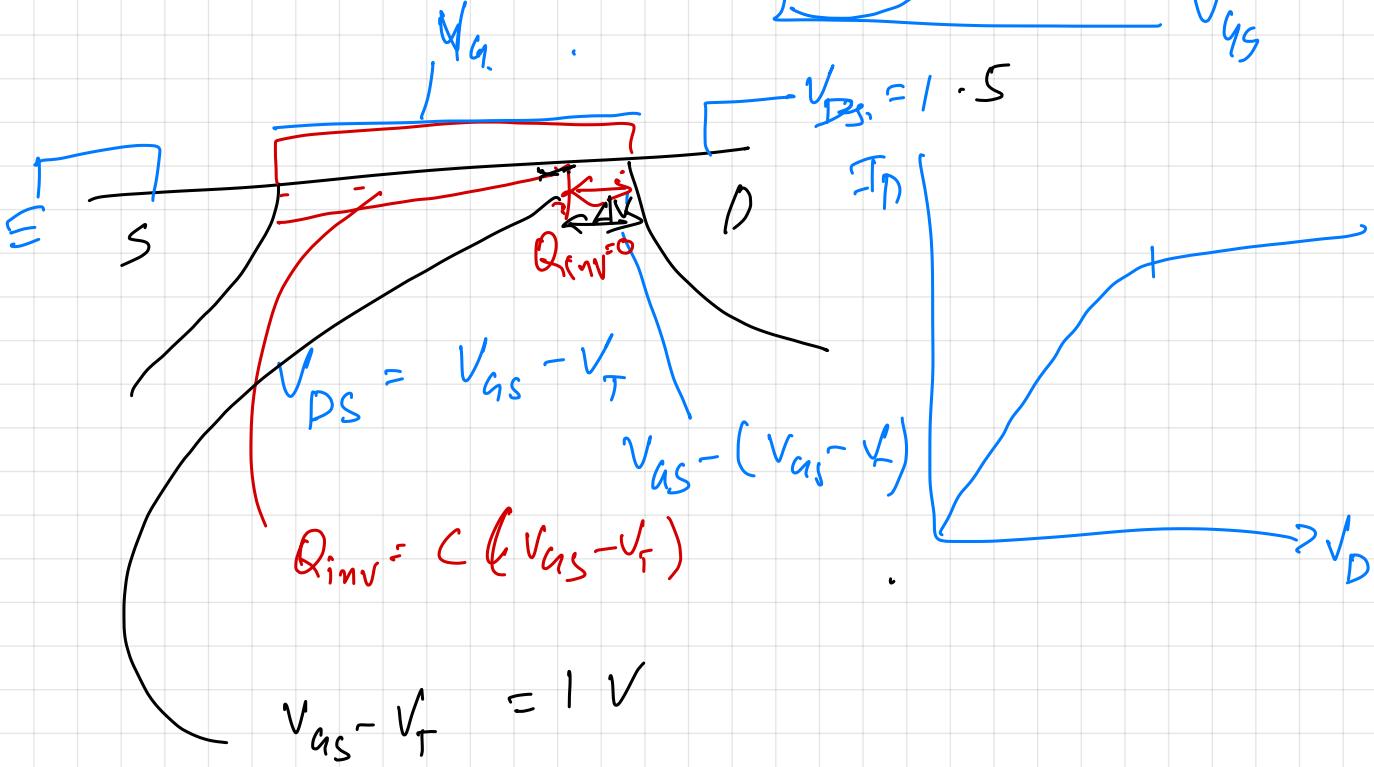
$P_{avg} \sim pW$



	NMOS	PMOS
①	OFF	ON, linear
②	saturation	

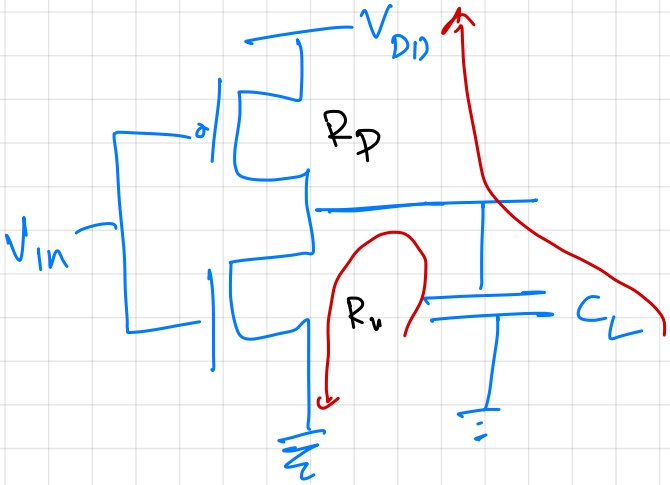


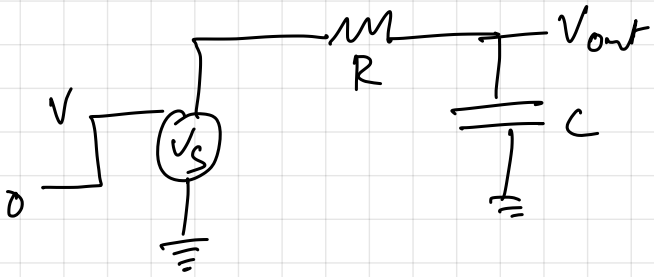




	NMOS	PMOS
①	OFF	ON, linear
②	saturation	linear
③	saturation	saturation
④	linear	saturation
⑤	linear	off

$P_{dynamic}$ is significant

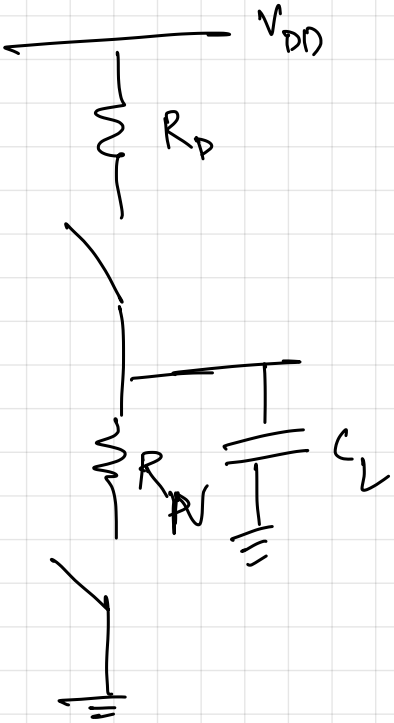




$$E_{drawn} = \int_0^{\infty} V_s \cdot i(t)\, dt$$

$$= V \int_0^{V} C \frac{dV_{out}}{dt} \cdot dt = CV^2$$

$$E_{Cap} = \frac{1}{2} C V^2 \qquad E_{diss} = \frac{1}{2} C V^2$$



$$P_{diss} = CV^2 f$$

$$t_{pLH} = 0.69 \times R_P \cdot C_L$$

$$t_{pHL} = 0.69 \times R_N \times C_L$$

$$t_p = 0.69 \times \frac{R_p + R_N}{2} C_L$$