Electronic Devices and Circuits Lab
Experiment 7- Group 2

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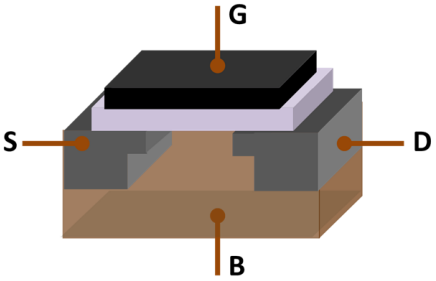
Aim-

The nominal values of the p-MOSFET are Threshold Voltage VTH0 = -0.5V, Length of the channel L=500 nm or 1 μm and Thickness of oxide layer t_{OX} = 5 nm. To plot the following curves- (Here $V_G = V_{SG}$)

1) I_D - V_D Output characteristics graph for V_G = 1.25V and V_G = 2.5V and to mark the important regions of operations.
2) I_D - V_G Transfer characteristics for V_D = 1.25
3) Transfer characteristics for V_D = 0.1V and 2.5V with L = 500 nm and 1 μm. Calculate the Drain Induced Barrier Lowering in both cases.
4) Output Characteristics for with L=500 nm and 1 μm with V_G = 1.25V

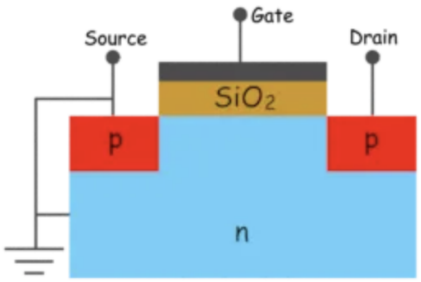
Theory-

A MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a semiconductor device which is the basic building block of any modern day electronic devices. They are generally used as switching devices, power converters, etc. It has 4 terminals- Source, Gate, Substrate and Drain. We can vary the voltage applied at the gate which directly affects the conductivity of the substrate and hence conductivity of the device. In this experiment we will be simulating a p-MOSFET in enhancement mode.



Working of p-MOSFET-

In a p-MOSFET, the substrate is lightly doped n-type semiconductor whereas the source and drain are heavily doped with p-type and there is a thin layer of metal oxide that acts like a di-electric medium with a metal plate attached to it as a gate. Together the metal, metal oxide and the substrate act as a capacitor on the device. We connect the source and substrate of the device to ground to facilitate the supply/withdrawal of electrons as per the operating conditions.

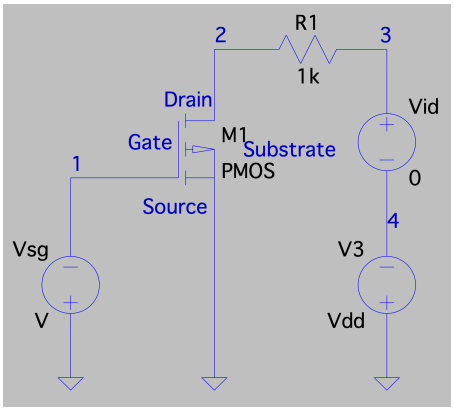


If we apply a negative voltage at the gate, since the gate-metal oxide-substrate acts as a capacitor there is negative charge deposition on the gate and correspondingly positive charges get accumulated just below the di-electric layer. Upon further increasing the gate voltage (negative), after a certain voltage called threshold voltage the covalent bonds in the substrate near the junction breaks down into electrons and holes. The electrons are repelled away from the oxide-substrate junction due to the negative charges on the metal and leaving behind holes.

In this way by increasing the gate voltage, the concentration of holes increases at the junction and creates a channel of holes linking source and drain. We say that an Inversion has occurred when the hole density near the junction becomes equal to the doping density of n-type substrate. This newly formed channel allows for holes to flow from source to drain through the channel. Due to the high concentration of holes in drain and

source the channel is also populated with holes which in-turn enables more current to flow from source to drain. The current is essentially carried by holes in a p-MOSFET type.

Circuit Used



Understanding-

Everywhere I have reversed the polarity of V_{DD} (by connecting it in reverse) and $V_G = V_{SG}$ - so that we don't have to deal with negative voltages.

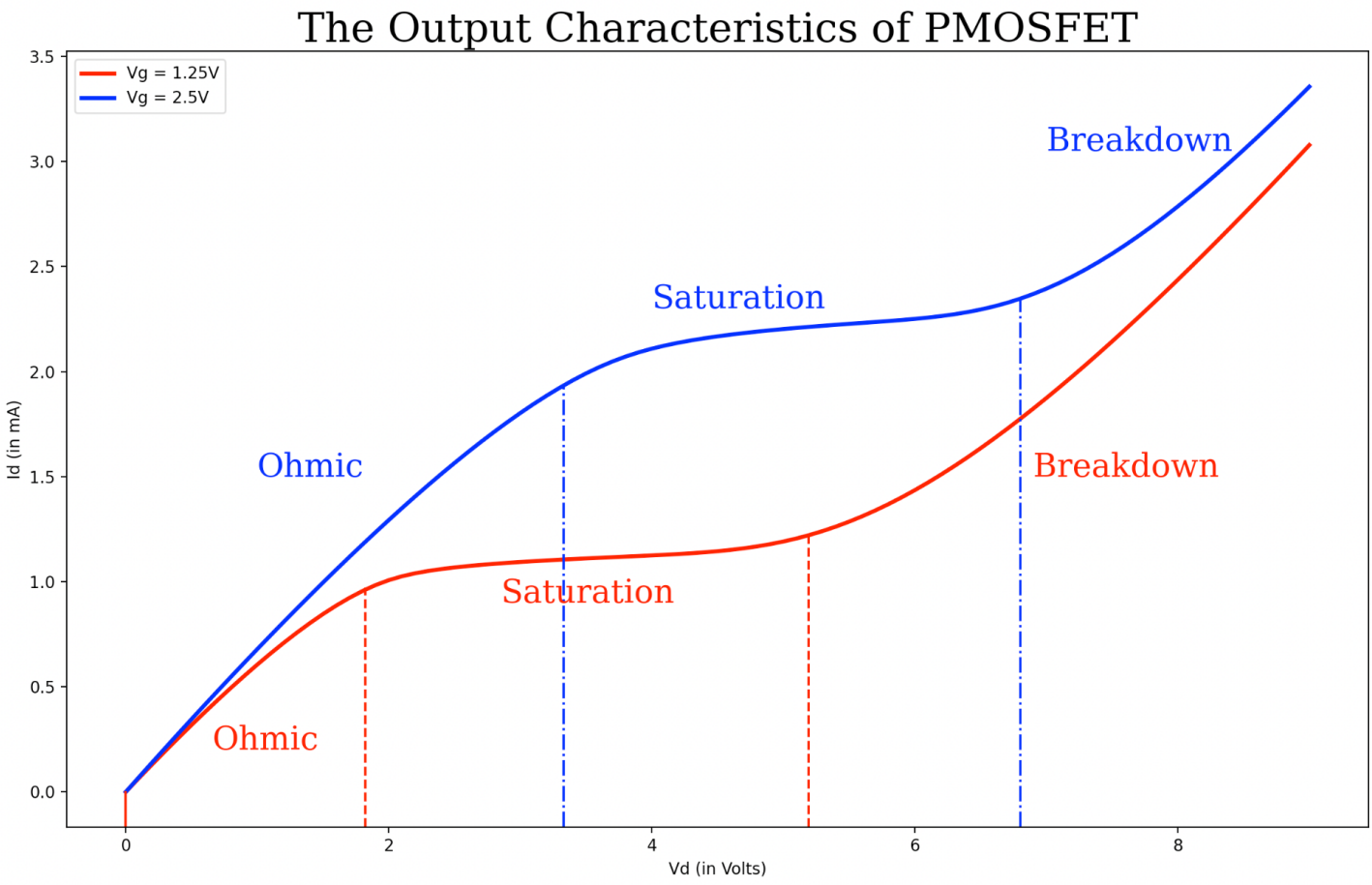
Experiment 1-

The output characteristics is a plot of I_D vs V_D by varying the gate-source voltage. When $|V_{GS}| < |V_{Th}|$ the current is zero as there is not enough voltage for a channel to form for the charge carriers to flow. This is called the cutoff region.

When $|V_{GS}| > |V_{Th}|$ the holes are attracted to the substrate-metal oxide junction which allows for a channel to be formed that enables flow of current. In this region, the I_D increases linearly with V_{DD} and hence this region of operation is called the ohmic region.

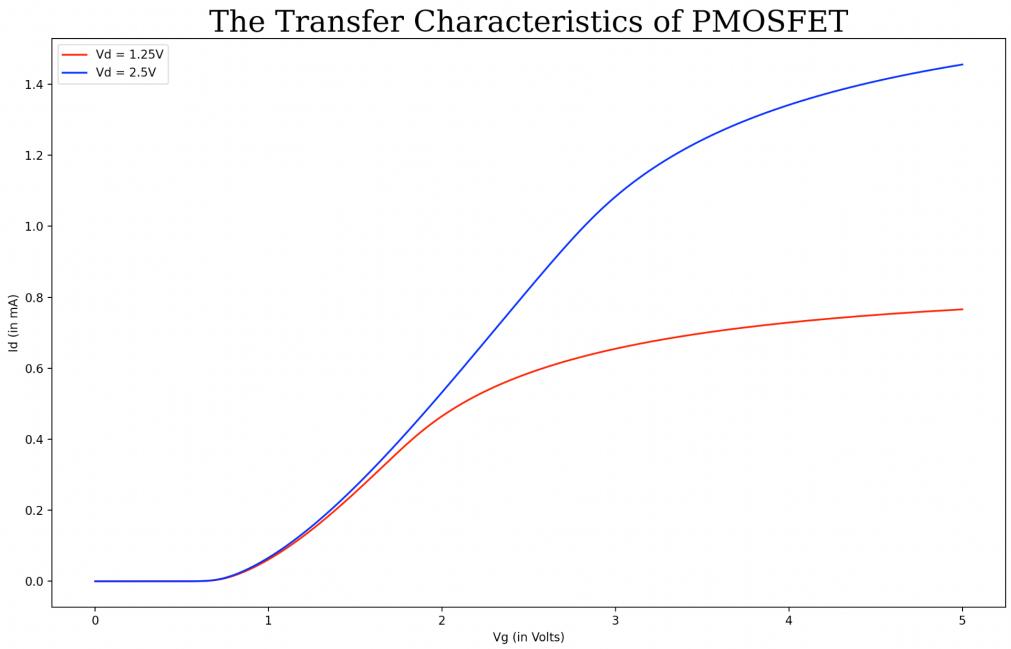
The p-n junction between Drain and Substrate acts like a diode in reverse bias and as we increase the value of V_{DD} the depletion region of drain-substrate increases in width. This causes the channel length to reduce. There comes a point when the length of the depletion region is almost equal to the width of the channel and at this point, the corresponding V_{DD} is known as pinch off voltage. After this point onwards the current I_D remains constant and this region of operation is called the saturation region.

Upon further increasing V_{DD} , the high energy electrons collide with the ions in the depletion region which causes more electrons to come out and hence increasing I_D sharply. This region of operation is called Breakdown region. Here $V_G = V_{SG}$



Experiment 2-

The transfer characteristics is a plot of Drain Current vs Gate Voltage(I_D vs V_{GS}) at a constant drain voltage V_D. As explained before the current flows only when there is a channel connecting the drain and source. So the current remains 0 until $|V_{GS}|$ reaches a threshold value $|V_{Th}|$. After this voltage the current increases with increase in V_{GS} due to increase in concentration of holes in the channel. For any particular value of $|V_{GS}|$ as V_{DD} increases, the current increases as the holes are attracted towards the drain. Here $V_G = V_{SG}$



Experiment 3-

In this experiment we plot the transfer characteristics for $V_D = 0.1V$ and $2.5V$ for two different channel lengths $L = 500$ nm and $1\mu m$ to calculate the Drain induced Barrier Lowering (DIBL). We plot $\log(I_D)$ vs V_G . DIBL is another short channel effect wherein the threshold voltage is lowered due to the applied drain bias. From previous experiments we have seen that the gate voltage must be greater than the threshold value for a channel to form in the substrate. But if the channel length is small then a large V_{DD} almost achieves the same effect as applying voltage at the gate which in turn reduces the threshold voltage required to form a channel.

DIBL can be calculated as follows-

$$DIBL = \frac{\Delta Vth}{\Delta Vdd}$$

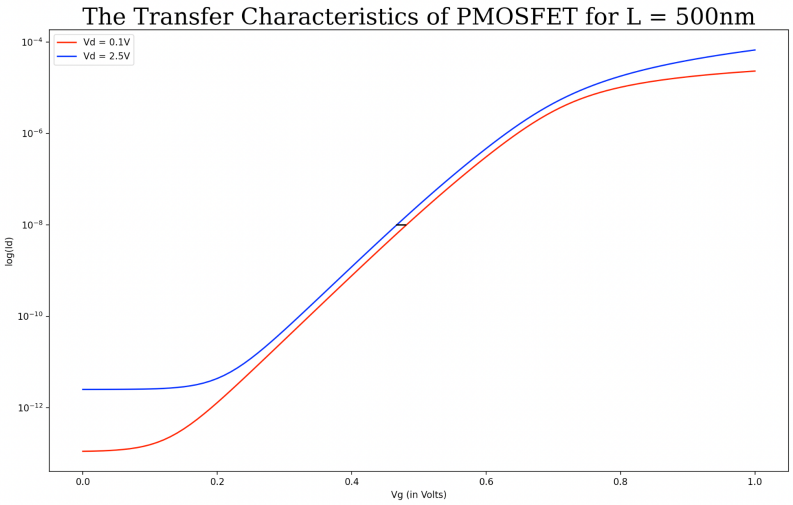
In our experiment, $\Delta V_{DD} = 2.5V - 0.1V = 2.4V$. We draw a horizontal line on the graph that intersects both the plots in it's ohmic region. Then ΔV_{Th} will be the difference in the x-coordinates of the intersection of the horizontal line with the curve.

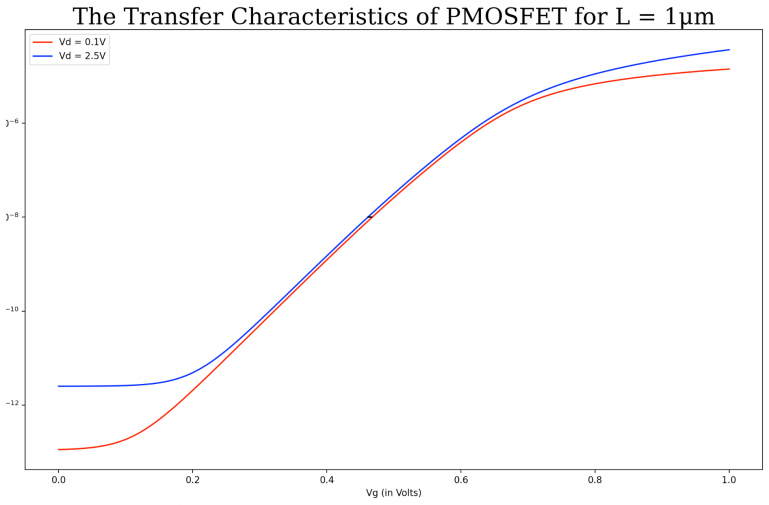
For $L = 500$ nm, $DIBL = \frac{482.8 - 467.5}{2.4} = 6.375\, mV/V$

For $L = 1$ µm, $DIBL = \frac{469.4 - 462.5}{2.4} = 2.875\, mV/V$

Also observe that the DIBL value is greater for smaller gate length which follows from our explanation.

Here $V_G = V_{SG}$





For $L = 500$ nm

For $L = 1$ µm

Experiment 4-

The graph for this experiment is obtained in a similar way as the graph for Experiment 2. Here we plot the graphs to understand the effects of channel length modulation.

As the channel length increases, the resistance offered by the channel increases and hence the current at a certain value of V_D current reduces.

Also notice that the current still increases even after the saturation point has been reached. This is due to an effect called Channel length modulation. The CLM is the decrease in the inverted channel length with increase in V_{DD} (for large values). In the saturation region as the length of the channel reduces (from expt. 2) the resistance decreases which causes a slight increase in current.

The slope of I_D - V_D in the breakdown region can be calculated by taking two points on the curve. Here I have taken the points at 3V and 4V. The slope for $L = 500$ nm comes out as 31.307 µA/V and slope for $L = 1$ µm comes out as 9.765 µA/V.