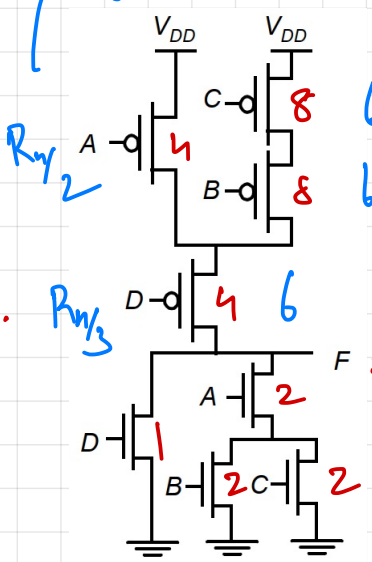
Introduction to VLSI Design

Lecture 13 - 5th Sep 2022



$R_n/6$

$R_n/2$

$R_n/3$

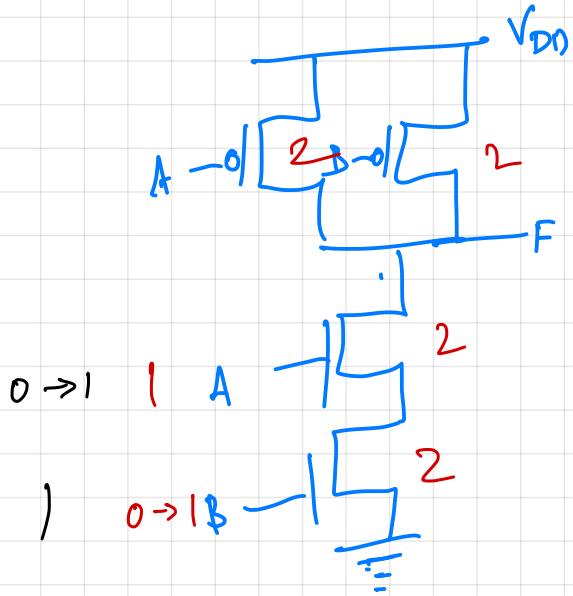
$F = \overline{A(B+C)+DE}$

6 - $R_n/3$ $R_n/4$

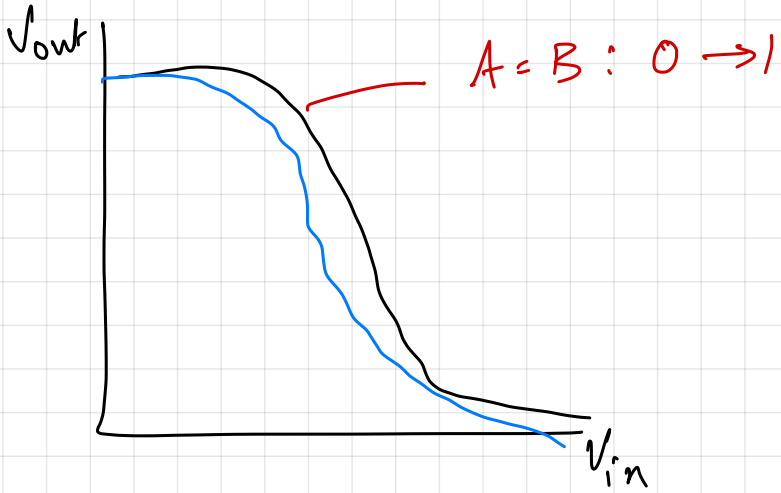
6 $R_n/3$ $R_n/4$

$R_n/3$ $R_n/2$

$F = \overline{A(B+C)+D}$



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



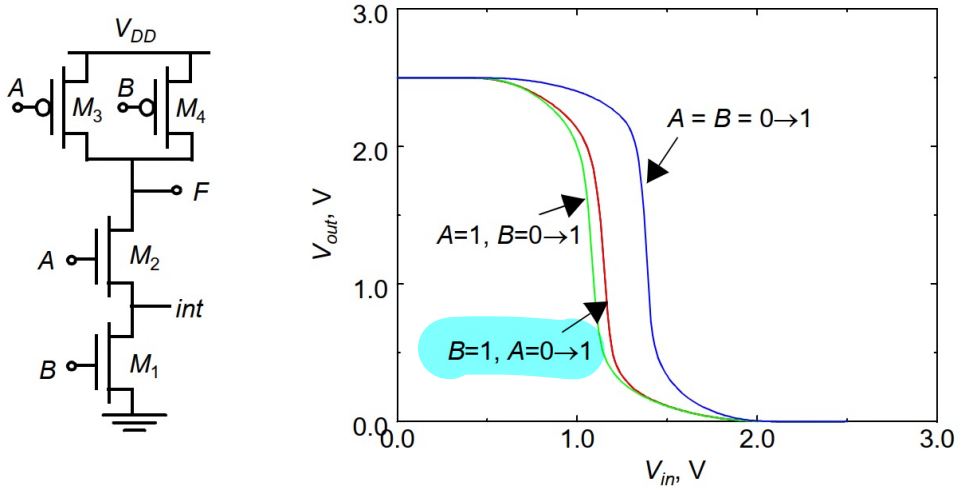
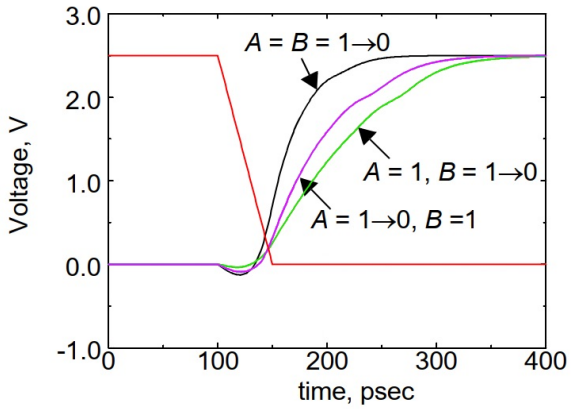


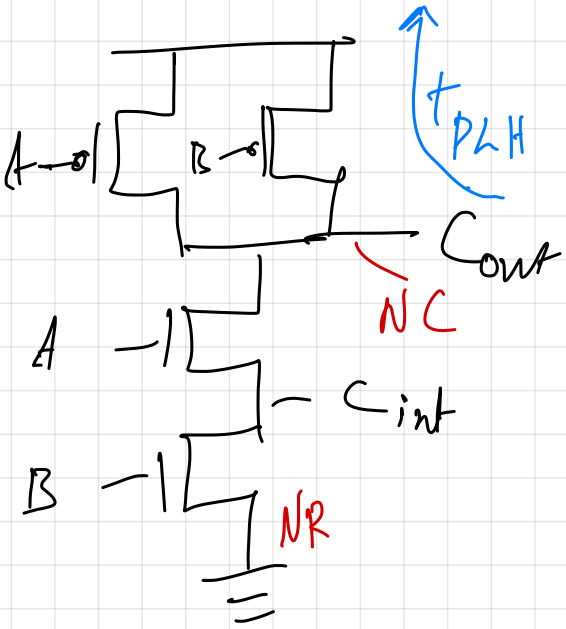
Figure 6.7 The VTC of a two-input NAND is data-dependent. NMOS devices are 0.5µm/0.25µm while the PMOS devices are sized at 0.75µm/0.25µm.

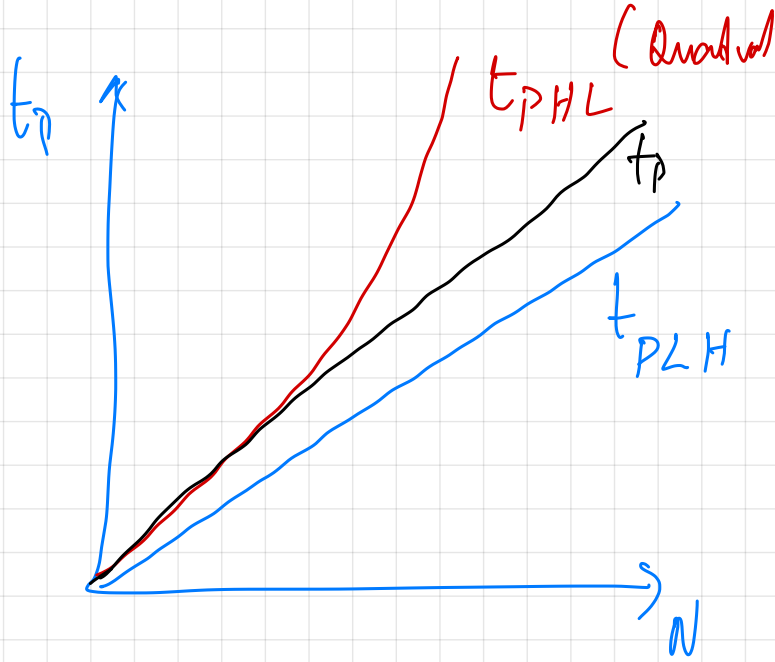
NMs are dynamic



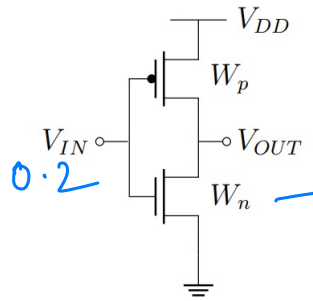
Input Data Pattern	Delay (psec)
***A* = *B*= 0→1**	69
***A* = 1, *B*= 0→1**	62
***A*= 0→1, *B* = 1**	50
***A*=*B*=1→0**	35
***A*=1, *B* = 1→0**	76
***A*= 1→0, *B* = 1**	57

Figure 6.9 Example showing the delay dependence on input patterns.



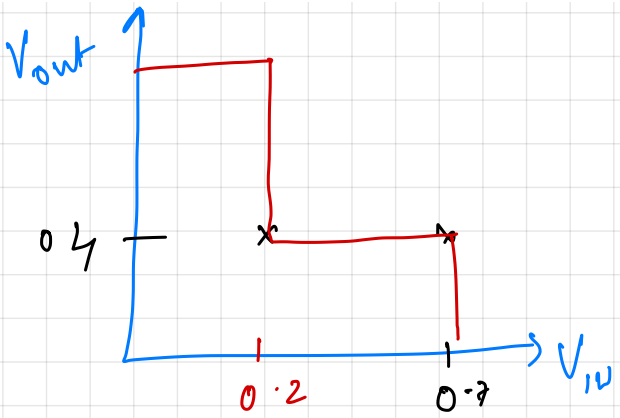


A particular technology has the following parameters: $V_{th,n} = 0.2\ V$ and $|V_{th,p}| = 0.3\ V$, $R_n = 2\ k\Omega * \mu m$, $R_p = 3\ k\Omega * \mu m$ at $V_{DD} = 1\ V$. Draw the VTC of the gate below with $W_p = W_n = 1\ \mu m$.



$V_{GS} = -0.8$

0.2 → On



$V_{Tn} = |V_{Tp}| = 0.2$

V_{DD} 1V

0.8

$V_{out} = 0V$

V_{IN}

0.8

0.6