Electronic Devices and Circuits Lab
Experiment 8- Group 2

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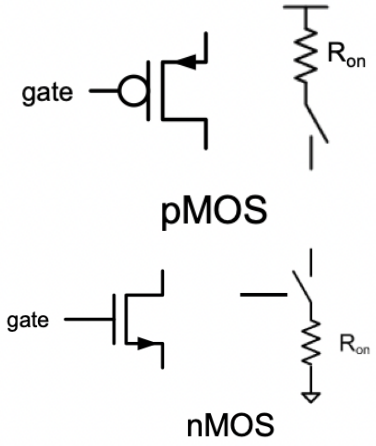
Aim-

1) Implement a NOT gate in NgSPICE and plot V_{out} vs V_{in} and explain the operation. Also highlight the region of operations of the MOS transistor.
2) Implement a 2 input NOR logic gate and verify the operation. The inputs are generated through a pulse generator.
3) Implement AND, OR and XOR gate using NOT and NOR gates as sub-circuits.

Theory-

Logic gates are devices that are fundamental building blocks of modern day digital circuits. They perform some basic logic functions that take in some input and give out logical outputs. We use Metal Oxide Semiconductor (MOS) transistors to build these logic gates. A few advantages of using a MOS transistor are - they can be used in both enhancement mode and depletion mode, offer high speed of operation, have high drain resistance due to lower resistance of the channel and the main MOSFET channel used for switching is purely resistive.

As concluded from previous experiments, MOSFET can be used as a switch without any moving parts by regulating the voltage at the gate to control the flow of current from source to drain. So if gate voltage is above a certain threshold voltage, then there is a flow of current thus in on state (1) and if not then there is no current flowing thus in off state (0). In a PMOS we connected the source and substrate to a higher voltage than the drain (as the gate must be at lower voltage than source to conduct) and in NMOS we connected the source and substrate to a lower voltage than the drain (as the gate must be at higher voltage than source to conduct). Following the same convention we connect V_{DD} to PMOS and ground to NMOS.



In this experiment we build 5 different logic gates- NOT (1 i/p), NOR, AND, OR and XOR. Suppose A and B are inputs and Y is output, then the logic relations are-

- NOT $\Rightarrow$ $Y = A'$
- NOR $\Rightarrow$ $Y = (A + B)' = A' \cdot B'$
- AND $\Rightarrow$ $Y = A \cdot B$
- OR $\Rightarrow$ $Y = A + B$
- XOR $\Rightarrow$ $Y = A' \cdot B + A \cdot B'$

All the above logic gates are built using Complementary Metal-Oxide Semiconductor (CMOS) design. It consists of two parts and each part is complementary and symmetrical to each other. Both pMOS and nMOS transistors are used, pMOS part to connect the output to V_{DD} and nMOS part to connect output to GND.

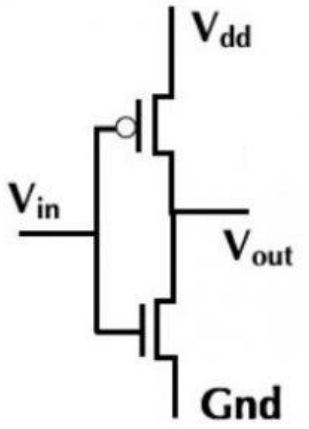
They are used in such an arrangement to reduce static power dissipation drastically and increase noise immunity.

In CMOS circuits, the same signal which turns on (1) one type of transistor turns off (0) another type of transistor and hence the name complement. This type of design allows the devices to use only simple switches without the need of a pull up resistor.

Procedure-

Experiment 1-

Using CMOS, we can implement a NOT gate as follows-



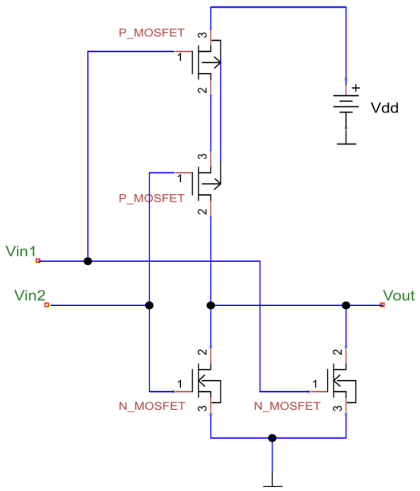
In this circuit, the source of pMOS is connected to V_{DD} and source of nMOS is connected to GND, gates of both MOS are connected to V_{in} and drain terminals of both MOS are connected to the output terminal.

When V_{in} is 0V (Low), V_{GS} at nMOS is 0V - 0V = 0V $<$ V_{Th} and so there is no channel formed for current to flow. V_{GS} at pMOS is 0 - V_{DD} = -5V $<$ V_{Th} and so current flows from source to drain, i.e. $V_{out} = V_{DD}$. In this case pMOS acts as a closed switch and nMOS acts as an open switch.

When V_{in} is 5V (High), V_{GS} at pMOS is 5V - 5V = 0V $>$ V_{Th} and so there is no channel formed for current to flow. V_{GS} at nMOS is 5V - 0 = 5V $>$ V_{Th} and so current flows from source to drain, i.e. $V_{out} = 0V$. In this case nMOS acts as a closed switch and pMOS acts as an open switch.

Experiment 2-

Using CMOS, we can implement a NOR gate as follows-



Again in this circuit, we use a CMOS design where the pMOS part is the conjugate of the nMOS part.

In this circuit when both V_{in1} and V_{in2} are low then both the pMOS act like closed switches which connects V_{DD} to V_{out} and both nMOS act as open switch so GND is not connected to V_{out} .

When either of V_{in1} and V_{in2} (or both) are high, one of the nMOS (or both) act as closed switch thus connecting GND to V_{out} and one of the pMOS (or both) act as open switch which causes the connection of V_{DD} to V_{out} to always remain incomplete.

Therefore we get a NOR gate wherein output is high only when both V_{in1} and V_{in2} are low and output is low when either of V_{in1} and V_{in2} are high.

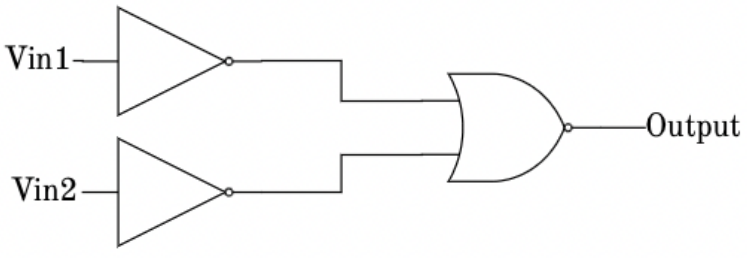
Experiment 3-

For AND Gate-

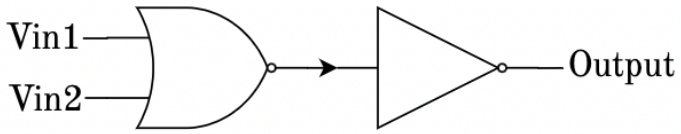
NOR Gate logic is A' . B'

So if we feed A' and B' as input to NOR gate we get AND gate

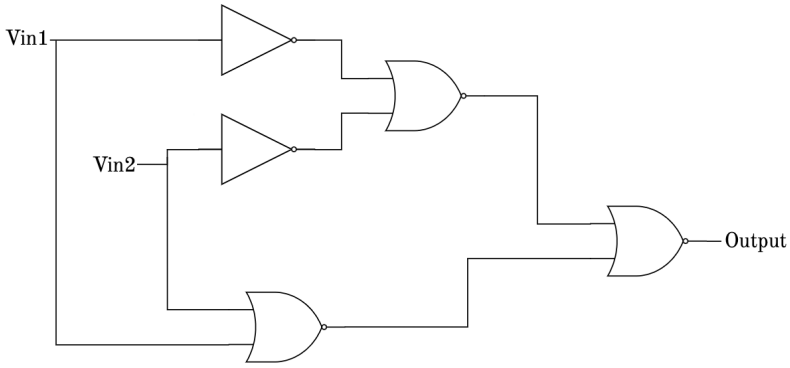
(A')' . (B')' = A . B



For OR gate-
NOR gate logic is $(A + B)'$
So if we invert the output of NOR we get OR
$((A + B)')' = A + B$

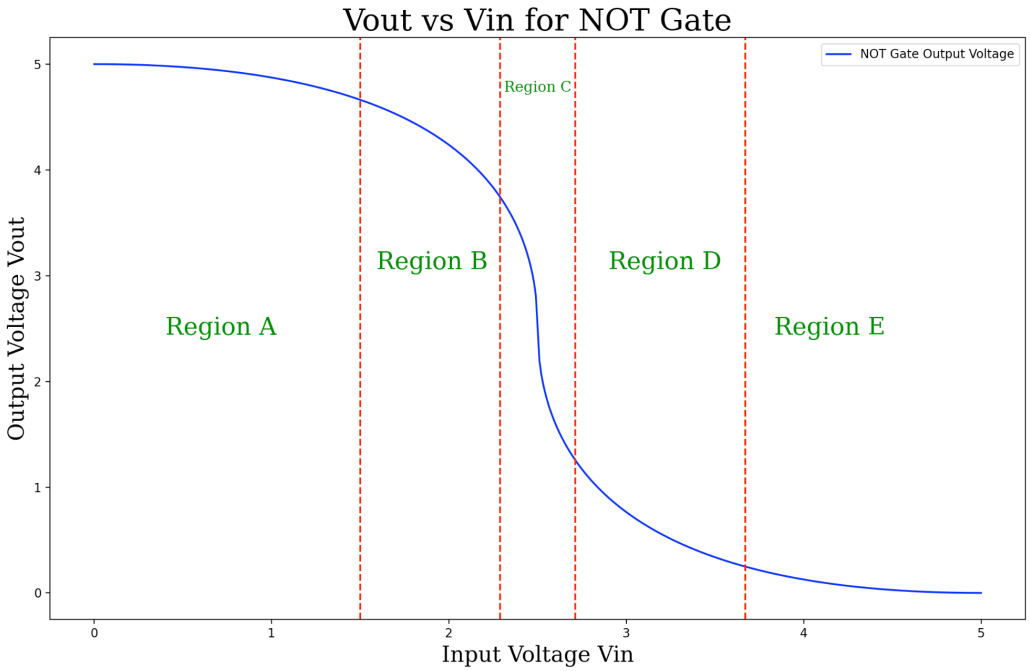


For XOR gate-
XOR Operation is $A'B + AB'$
We can use the following trick to simplify the expression-
$A'B + AB' = AA' + A'B + AB' + BB'$
$= (A + B)A' + (A + B)B'$
$= (A + B).(A' + B')$
= (A NOR B) NOR ((NOT A) NOR (NOT B))
This is the best way to write as it uses the least amount of transistors (with NOR and NOT gates) which is 16.



Plots and Understandings-

For NOT Gate-



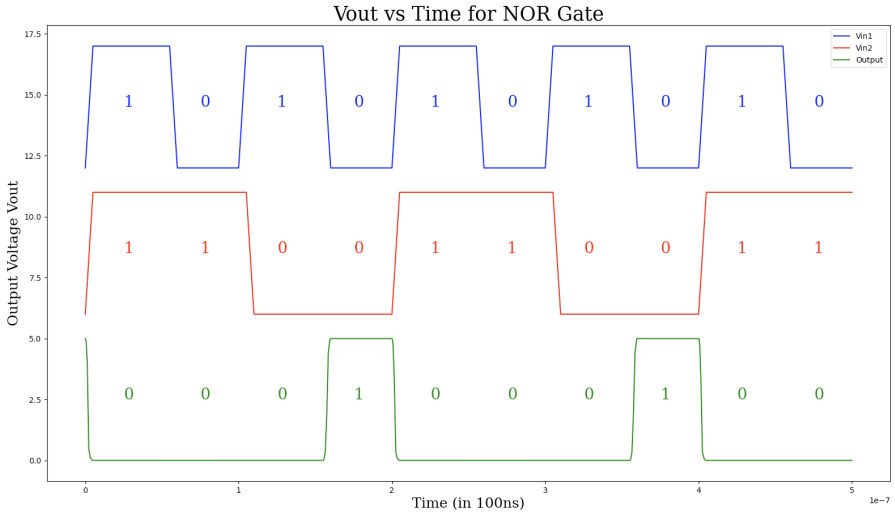
From the above graph, we can divide the transfer characteristics of a CMOS inverter into 5 regions-

- Region A-
  In this region, nMOS is in Off state as $V_{GS} < V_{Th}$ and it is in the cutoff region. For pMOS $|V_{DS}|<|V_{Th}|$, so it is in On state and in linear region of operation as voltage is less than pinchoff voltage.

- Region B-
  Here V_{GS} is just greater than the threshold voltage for nMOS and it is also greater than pinchoff voltage and so this is the saturation region for nMOS. pMOS will still be in the linear region. So both the transistors are on in this region.
- Region C-
  As V_{in} increases in this region, $|V_{DS}| > |V_P|$ for both nMOS and pMOS and hence they are in the saturation region. Here both the transistors are still in On state.
- Region D-
  V_{GS} for nMOS is greater than its threshold voltage, and $V_{DS} < V_P$ so this is the linear region of operation for nMOS. For pMOS, $|V_{DS}| > |V_P|$ so it is in the saturation region. Notice here that both the transistors are in On state.
- Region E-
  For nMOS is in its On state as $V_{DS} > V_{Th}$ and $V_{DS} < V_P$ so nMOS operates in linear region of operation. For pMOS, V_{GS} is almost zero so it is in the cutoff region.

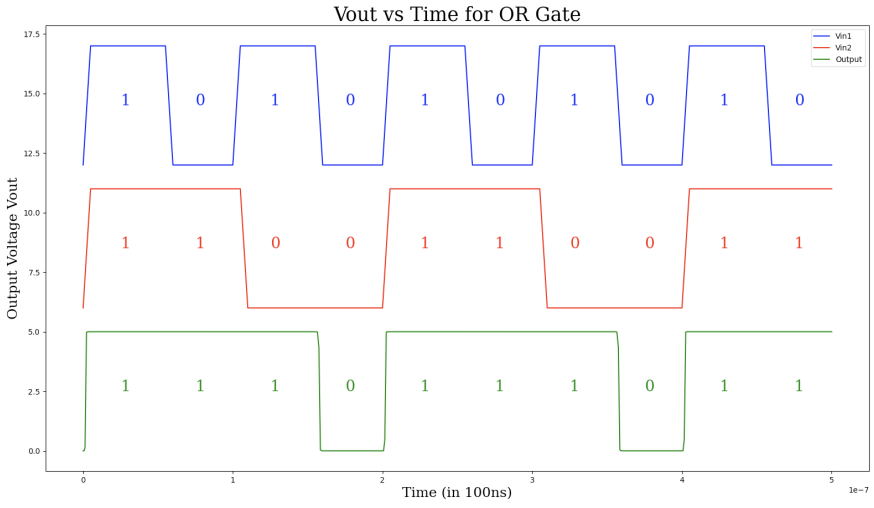
For NOR Gate-

The above plot is as expected with output 1 if both inputs are 0 and output is 0 otherwise.



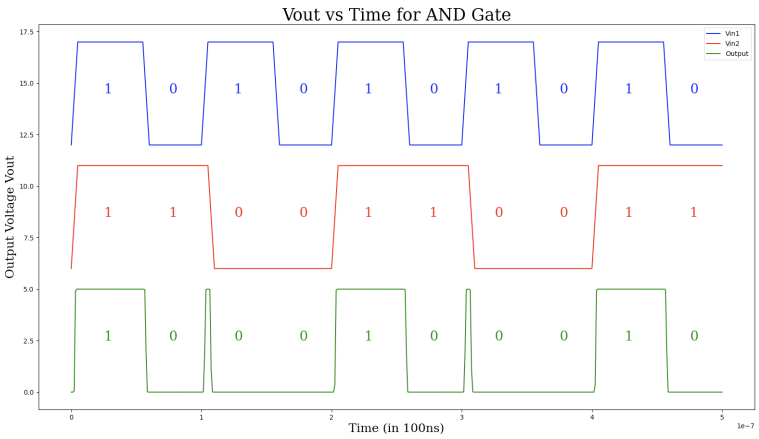
For OR Gate-

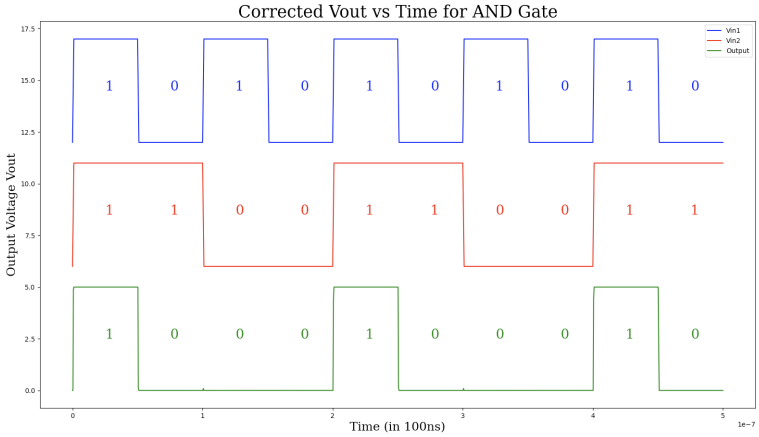
The above plot is as expected with output 1 if both inputs are 1 and output is 0 otherwise.



For AND Gate-

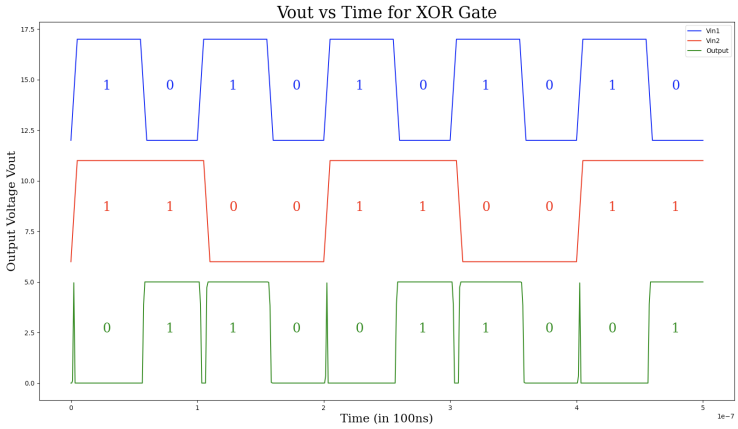
The output plot is not exactly as expected due to the rise and fall times of the input waveform. Consider at t=100ns, V_{in1} increases from 0 to 1 in the next 5ns but V_{in2} still stays at 1 in the 5ns duration. So due to the apparent combination of V_{in1} and V_{in2} , V_{out} also increases with V_{in1} . Now consider at t = 105ns where V_{in2} changes from 1 to 0 in the next 5ns and V_{in1} stays at 1. Again due to the apparent combination V_{out} also reduces for the next 5ns. This discrepancy in the output waveform can be removed by reducing the rise and fall time of the input waveforms.

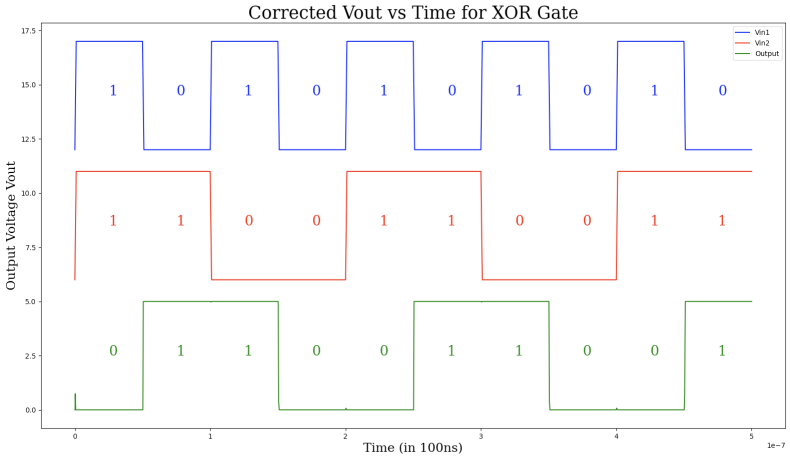




For XOR Gate-

We find the same discrepancy as stated above and correction is also the same.





Conclusions-

- We use a CMOS inverter as it uses very less power in static mode, that is clear from the output plot. Both the transistors in the inverter are On only in regions B, C and D when the inverter is switching its state and hence does not consume any power in static mode.
- Due to the non-ideality of the CMOS inverter, it takes time for switching between the states and this time delay is called propagation delay.
- Even for gate voltages below threshold voltage, there is still some leakage current from source to drain even if the transistors are in Off state. This is the reason why electronic devices dissipate power even when they are not being used.