EE3113/3301/5184: Introduction to VLSI Design

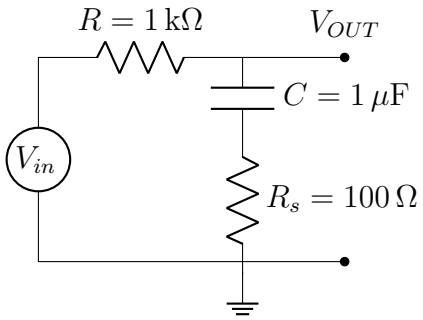
Homework Assignment 1 **Deadline: Fri, 27th Oct 2020**

1. **SPICE Analyses**

   (a) Calculate the operating point of the circuit in Figure 1 using '*.op*' command given $V_{IN} = 2.5\ V$.

   (b) Perform a transient simulation to calculate the phase lag introduced by the circuit if $V_{IN} = \sin \omega t$ with $\omega = 100\ Hz$ and $1\ MHz$. Estimate the phase lag using analytical expression and compare.

   (c) Plot the amplitude and phase transfer characteristics of the filter using $V_{IN} = \sin \omega t$. Determine the $3\ dB$ point and the corresponding phase lag. Compare with analytic expressions.

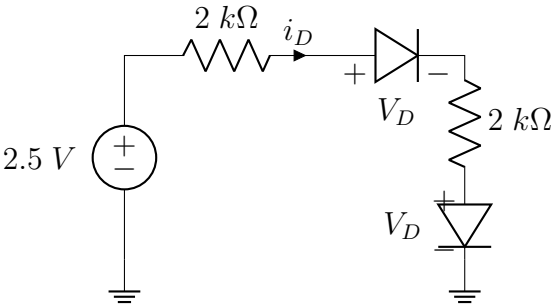


2. **Analytic calculations *vs* SPICE simulations**

   (a) Consider the adjacent circuit. Using a simple model, with $V_{Don} = 0.7$ V, solve for I_D.

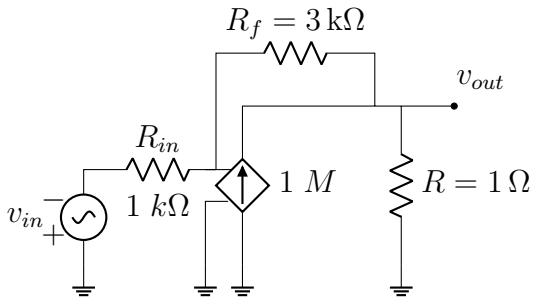
   (b) Find I_D and V_D using the ideal diode equation. Use $I_s = 10^{-14}\ A$ and $T = 300\ K$.

   (c) Run a SPICE simulation to validate your results in (a) and (b).



3. **Controlled sources**

   A voltage controlled current source is driven by ac source, $v_{in} = 1\ V_{p-p},\ 1\ kHz$. Simulate the output response and calculate the gain in the circuit.



4. **MOSFET Characteristics**

   Consider long and short channel MOSFETs with $L = 10\ \mu m$ and $L = 0.18\ \mu m$ respectively. Both devices have identical W/L of 1.5

   (a) Simulate the IV characteristics of PMOS and NMOS devices using 180 nm Predictive Technology Model (PTM). Your results will be similar to Fig. 3.19 and

3.21 of reference [1]. Remember the maximum supply voltage for regular devices is only 1.8 V in this technology.

(b) Identify the transition between linear and saturation regions of operation of these MOSFETs. Annotate the regions of operation on the graphs obtained in part (a). Indicate the differences between short and long channel MOSFETs in your graphs.

(c) Calculate the small signal output resistance of NMOS and PMOS devices.

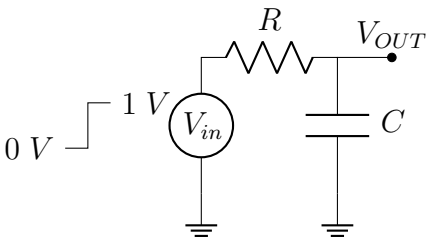
(d) Simulate the $I_d - V_g$ characteristics of the NMOS and PMOS devices with $|V_{ds}| = 1.8\ V$. Plot on a log-lin scale and calculate the sub-threshold slope of NMOS and PMOS devices. The subthreshold slope of MOSFET is given by $S = n(kT/q)ln(10)$ where n is a geometry and technology dependent parameter. Calculate n from your simulations of 180 nm technology.

5. **Propagation Delay**
A first order RC circuit is frequently used to estimate the propagation delay in logic gates. In the class we have seen that the propagation delay for an ideal step input($t_{r,in} = 0$) is $t_p = 0.69RC$. Further, the output rise time $t_r = 2.2RC$.

(a) Verify the expressions given above using SPICE simulations. Choose appropriate values for R and C components.

(b) Now consider a *non-ideal* step input with $10\ ps < t_{r,in} < 10\ ns$. Simulate the propagation delay, and plot t_p as a function of $t_{r,in}$.

(c) Arrive at an analytical (or empirical!) expression for propagation delay in presence of *non-ideal* step input.



Submission

Please prepare a pdf of all your solutions, graphs and SPICE netlist (whereever necessary) and submit on Google Classroom.

Simulation setup in NGSPICE

We will use predictive technology models (PTM) for simulations of MOS devices. The instructions to setup the library are as follows:

- Download and install NGSPICE. Use this Installation and Tutorial Guide: https://drive.google.com/file/d/1H6shLV3BGI5wkpwhNbN-r0XI536x1_lC/view?usp=sharing.
- **Download Technology File**: Download the TSMC 180nm predictive technology file TSMC180.lib from this link: https://drive.google.com/file/d/1cTsloYSmTUf__21MMn0_jOgCI4T0TS8O/view?usp=sharing.
- To link the technology file to your SPICE netlist use command .include "path to file".

- The .model statements in the technology library file contain model name and type *(e.g. .model nch_tt nmos)*. Make sure you use the correct model names in the SPICE netlist.

References

[1] Rabaey, Jan M and Chandrakasan, Anantha P and Nikolic, Borivoje. *Digital Integrated Circuits*, Prentice Hall, 2002

[2] Holger Vogt, Marcel Hendrix Paolo Nenzi, *Ngspice User's Manual: Version 32*, 2020

EE3113/3301/5184: Introduction to VLSI Design

Homework Assignment 2 **Deadline: Fri, 13th Nov 2020**

1. **MOSFET Resistance**

   The MOSFET output small signal resistance is defined by the slope of the $I_D - V_D$ characteristics. However, in digital circuits we are often interested in *equivalent resistance* presented by the MOSFET during charging/discharging of a capacitor (see example 3.8 of your textbook). In this exercise you will run simulations to determine the equivalent resistance of the regular NMOS and PMOS transistors in 0.18 μm process as a function of V_{DS}.

   (a) Perform a transient simulation of the circuit in Figure 1 using $W/L = 240/180$ or $W/L = 400/180$ and $V_{DD} = 1.8\,V$. Set the initial voltage across the capacitor to be $1.8\,V$. You should submit plots of R_{eq} as a function of V_{DS} for NMOS and PMOS devices (*c. f. Figure 3.27 of course textbook*). *Note: For PMOS devices you need to modify the circuit*

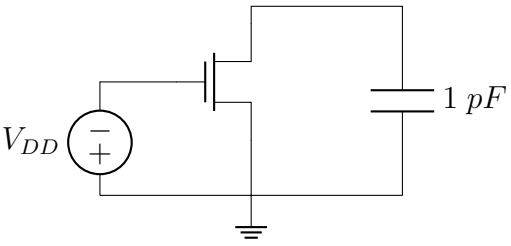


Figure 1

   (b) Compare your answers with Table 3.3 of textbook and explain the differences.

2. **MOSFET Capacitance**

   The gate capacitance of a MOSFET can be calculated by applying a gate voltage $V_{applied} = V_{CM} + V_0 \sin(\omega t)$ in the circuit in Figure 2. Since $I = CV_0\omega\cos(\omega t)$ we can obtain the CV characteristics by sweeping V_{CM} (in ac analysis) and setting AC magnitude to $1/(2\pi f)$, where f is the frequency of choice. The capacitance will then be given by the current in gate terminal.

   Consider long and short channel MOSFETs with $L = 10\ \mu m$ and $L = 0.18\ \mu m$ respectively. Both devices have identical W/L of 1.5/2.5

   (a) Simulate the CV characteristics of NMOS devices using 180 nm technology. Generate plots of $C(V_{CM})$ for short and long channel devices, and explain the trends you observe in your simulations. (*c. f. Example 3.9 of textbook*)

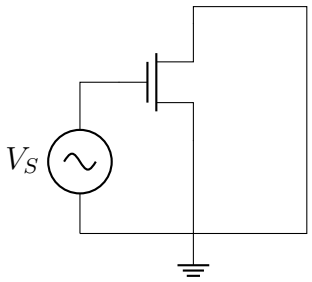


Figure 2

   (b) Will the CV characteristics change when you set the frequency to 10 MHz and 10 GHz? Explain your results.

3. **Inverter Implementations**

   The circuits in Figure 3 show different implementations of a digital inverter ($V_{DD} = 1.2\,V$), whose output is connected to a capacitor. Assume $V_{TN} = |V_{TP}| = 0.3\,V$, and the output capacitor, C_L, is initially discharged. Ignore sub-threshold conduction and body effect. Without running simulations answer the following:

   (a) Which one(s) of the circuits consume(s) static power when the input is high ($V_{IN} = 1.2\,V$)?

(b) Which one(s) of the circuits consume(s) static power when the input is low($V_{IN} = 0\ V$)?

(c) V_{OH} of which circuit(s) is 1.2 V (if possible)?

(d) V_{OL} of which circuit(s) is 0 V (if possible)?

(e) The proper functionality of which circuit(s) depends on the size of the devices? (Note that they are designed for a digital inverter)

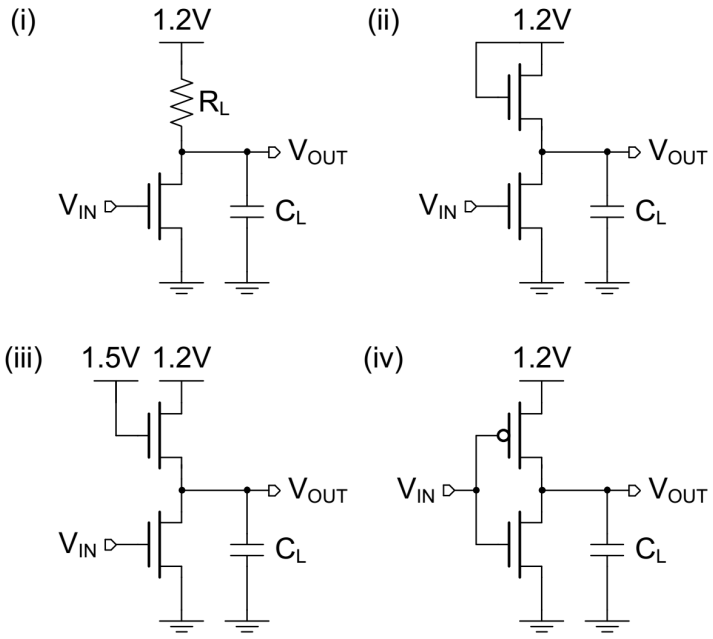


Figure 3

4. **NMOS Inverter - manual analysis**
Consider a NMOS inverter shown in Figure 4.

(a) Calculate V_{OH}, V_{OL} and V_M.

(b) Derive expressions for V_{IL}, V_{IH} and hence determine the noise margin. You may ignore channel length modulation in your analysis.

(c) Derive an expression for the peak gain and estimate the same.

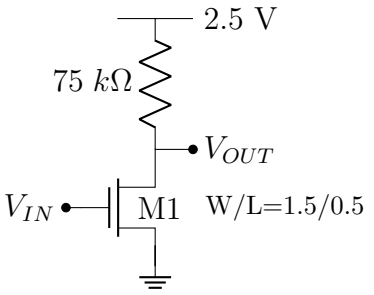


Figure 4

5. **NMOS Inverter- SPICE simulations**
Compare the results of question 4 by performing simulations in SPICE with 180 models.

(a) Simulate the VTC and plot the gain of the inverter by calculating dV_{out}/dV_{in}.

(b) How does the load resistance impact the threshold and peak gain of the inverter? Verify by simulating for a wide range of resistances.

(c) Simulate the frequency response using transient analysis at $f = 250\ kHz$, 50% duty cycle and $C_L = 3\ pF$. Calculate t_r, t_f and t_p for the inverter. Are the rise and fall times equal? Why or why not? What are the geometric parameters that influence the maximum operating frequency of the inverter? What is the dynamic power dissipation assuming that the inverter is clocked at highest possible frequency?

EE3113/3301/5184: Introduction to VLSI Design

Homework Assignment 3 **Deadline: Wed, 16th Dec 2020**

1. **Impact of Sizing on Performance**

   Design and implement an inverter such that $V_M = V_{DD}/2$ using TSMC 180 nm technology.

   (a) Investigate the impact of scaling factor $S > 1$ on the performance of inverter in (i) no external load, and (ii) $C_L = 20pF$ conditions. Tabulate your results.

   (b) What is the impact of increasing W_p or W_n on t_{pHL} and t_{pLH}? Substantiate your answer by performing simulations and tabulating results.

2. **Ring Oscillator**

   Simulate the transient response of a 7 stage ring oscillator circuit by cascading unit inverters.

   (a) Plot the time response over 10 periods and calculate the frequency of oscillation

   (b) Estimate the propagation delay of the circuit and compare with result in 1(a).

   (c) What is the frequency of oscillation when the inverters are sized up by a factor 'S'? How does the sizing impact the power consumption?

   (d) Suggest a modification to ring oscillator circuit so that a control signal can be used to turn the oscillator *on/off*.

3. **Sizing of Inverters**

   In order to drive a large capacitance ($C_L = 20pF$) from a minimum size gate (with input capacitance $C_i = 10fF$), you decide to introduce a two-staged buffer as shown in Figure 1. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size.

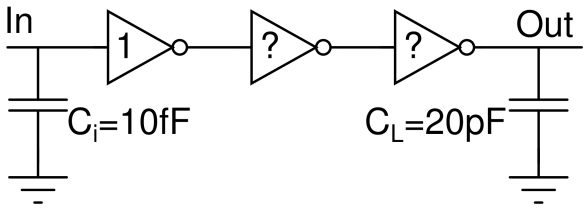


Figure 1

   (a) Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

   (b) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

   (c) Describe the advantages and disadvantages of the methods shown in (a) and (b).

   (d) Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V?

4. **CMOS Logic**

   Design a complex CMOS logic gate that implements the function

$$f(A;B;C;D) = \overline{A.(B.(C+D)+C.D)}$$

How do you size the gate to improve it's performance?

5. A particular technology has the following parameters: $V_{th,n} = 0.2\ V$ and $|V_{th,p}| = 0.3\ V$, $R_n = 2\ k\Omega * \mu m$, $R_p = 3\ k\Omega * \mu m$ at $V_{DD} = 1\ V$. Draw the VTC of the gate below with $W_p = W_n = 1\ \mu m$.

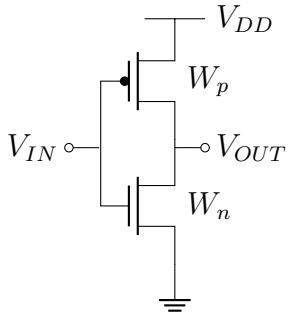


Figure 2

Optional Questions

You do not need to submit the following questions, but it is highly recommended that you analyze and answer them.

6. **Clock Distribution**
Consider the H-tree clock distribution network in Fig. 3. The inverter 1 is a minimum sized inverter with input capacitance of 10 fF. Your goal is to minimize the delay between IN and Clk_1 in the given schematic by choosing appropriate sizes of the inverters. You donot need to worry about the delay in Clk_2, Clk_3 and Clk_4 branches while answering this question. You may assume $\gamma = 1$.

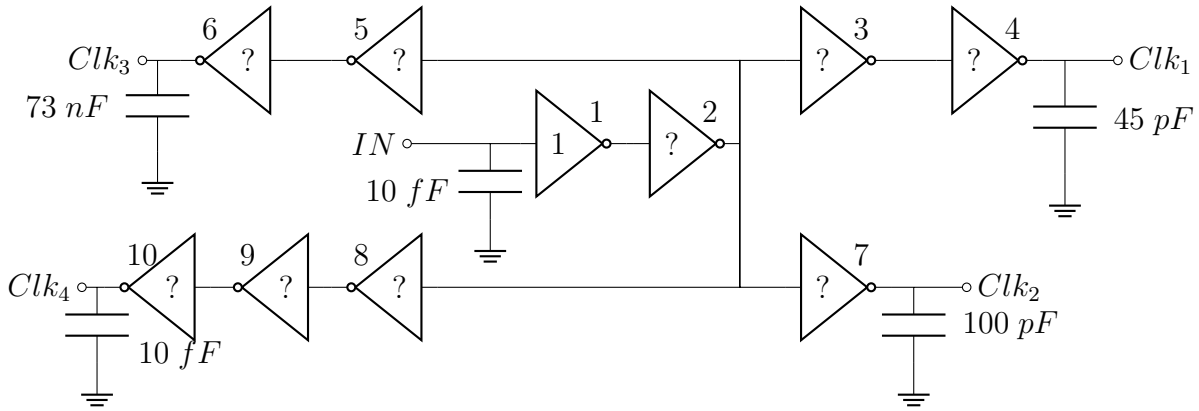


Figure 3

(a) Some inverter sizes may not influence the delay between IN and Clk_1. Clearly mark those with a symbol 'X' in the picture above.

(b) Let the size of remaining inverters be S_i for i^{th} inverter. Write down the expression for time delay between IN and Clk_1.

(c) Determine the sizes of remaining inverters so that the above delay is minimized subject to the constraints specified.

7. **Logical Effort and Gate Sizing**

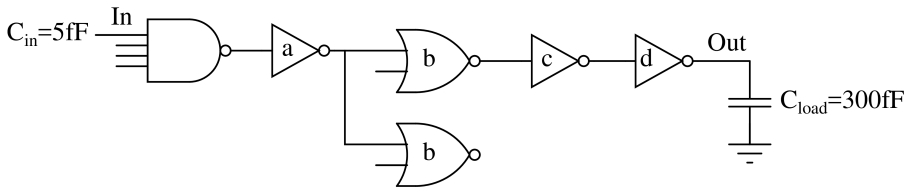


Figure 4

(a) What is the path effort from In to Out?

(b) What effective fanout/stage(EF) minimizes the delay of this chain of gates?

(c) Size the gates to minimize the delay from In to Out.

8. **Scaling trends in VLSI circuits**

(a) Sketch the variation of t_{pHL}, t_{pLH}, and t_p as a function of PMOS/NMOS transistor size ratio β for the generic 0.25 μm technology.

(b) Sketch the functional dependence of $t_p(normalized)$ on effective fanout per stage in a inverter chain in Fig. 8(b). Clearly indicate the effective fanout at which optimal delay is achieved. You may consider $\gamma = 1$, and also account for parasitic overheads.