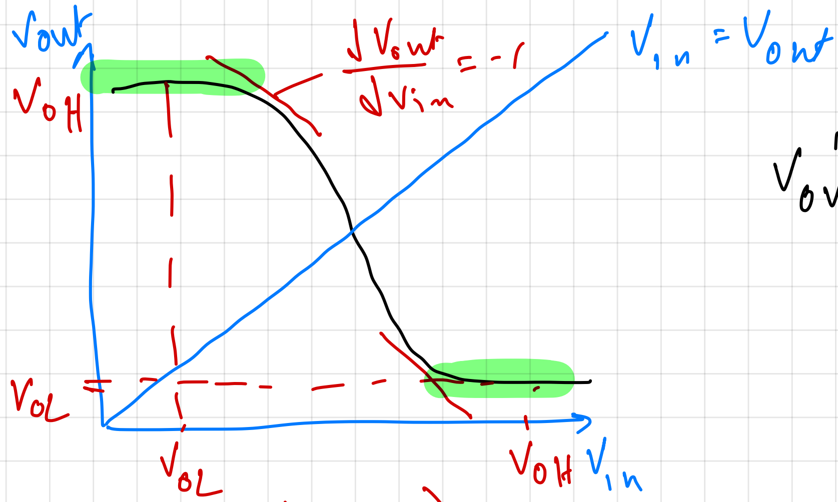
VLSI Design - Lecture 3
5^{th} Aug 2022

Use the generic 0.25 μm CMOS model below for all your work unless otherwise specified. Assume $|2\phi_F| = 0.6\ V$.

	$V_{T0}\ (V)$	$\gamma\ (V^{0.5})$	$V_{DSAT}\ (V)$	$k'\ (A/V^2)$	$\lambda\ (V^{-1})$	$R_{eq}\ (k\Omega)@V_{DD}$
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06	13
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1	31



$$V'_{out} = f(V_{in} + \Delta V)$$

$$= f(V_{in}) + \frac{df}{dV}\Delta V + \ldots$$

gain

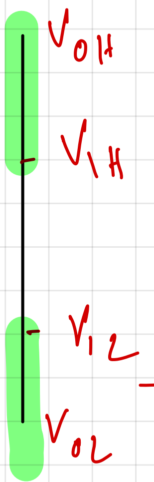
$$V_{out} = f(V_{in})$$

$$V_{OH} = f_{inv}(V_{OL})$$

$$V_{OL} = f_{inv}(V_{OH})$$

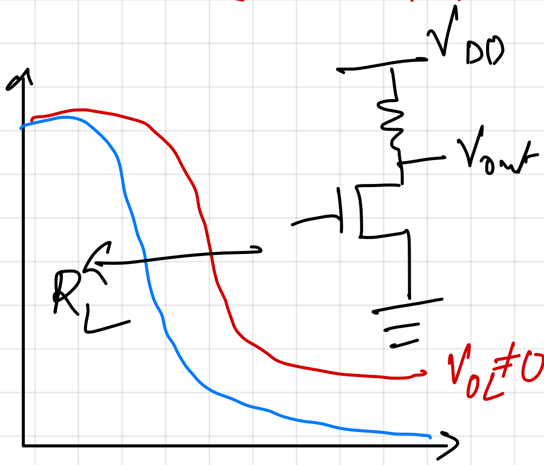
If gain < 1
Noise is supressed

gain > 1
Noise is amplified



$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$



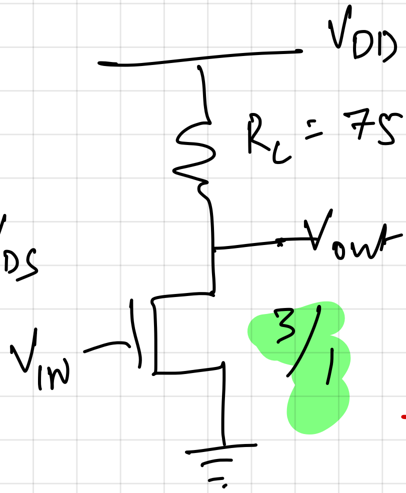
$$NM_L = V_{IL} - V_{OL}$$

$$V_{OL} = \frac{R_{ON}}{R_{ON} + R_L}$$

$I_R = I_D$ $\qquad \mu C_{ox}$

V_{OL} :

$$\frac{V_{DD}-V_{out}}{R_L} = k_n' \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \cancel{\frac{V_{DS}^2}{2}}\rightarrow 0\right]$$



$3/1$ $\qquad W = 3\,\mu m$, $L = 1\,\mu m$

$V_{GS} - V_T = 2.5 - 0.43$

$V_{DS} \sim < V_{GS} - V_T$

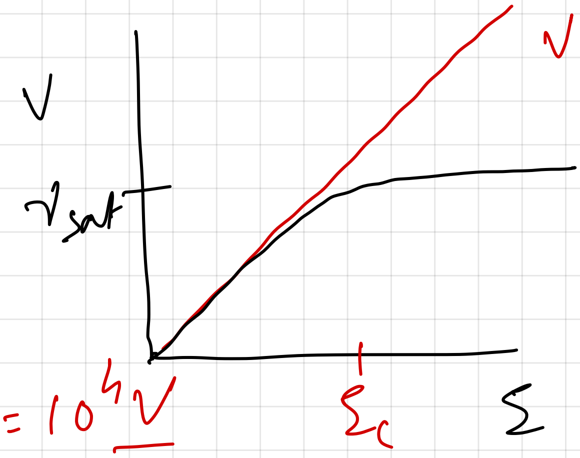
$$I_D = \frac{1}{2} k_n' \frac{W}{L}(V_{GS}-V_T)^2 (1+\lambda V_{DS})$$

$$\frac{0.75}{0.25}$$

$$\frac{2.5 - V_{OL}}{75\,k\Omega} = 115\times10^{-6} \times 3 \times \left((2.5-0.43)\,V_{OL}\right)$$

I_D for a short channel transistor

$v = \mu \xi$ – ξlectric field between S & D



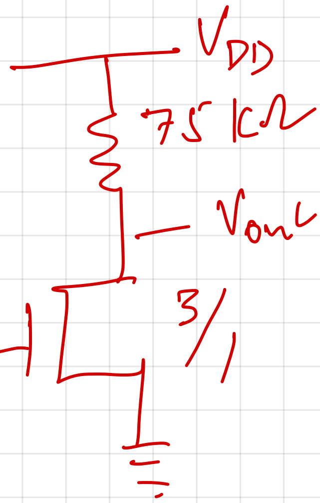
$\xi_c = 10^4 \frac{V}{cm}$

$$I_D = k' \frac{W}{L}\left[(V_{GS}-V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right](1+\lambda V_{DS})$$

$V_{OL} \sim 50$ mV (Please check)

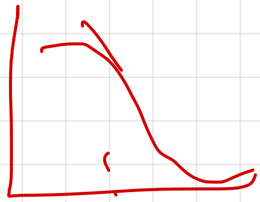
43.1 mV

V_M = $I_R = I_D$



$$\frac{V_{DD}-V_M}{R_L} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS}-V_T)^2$$

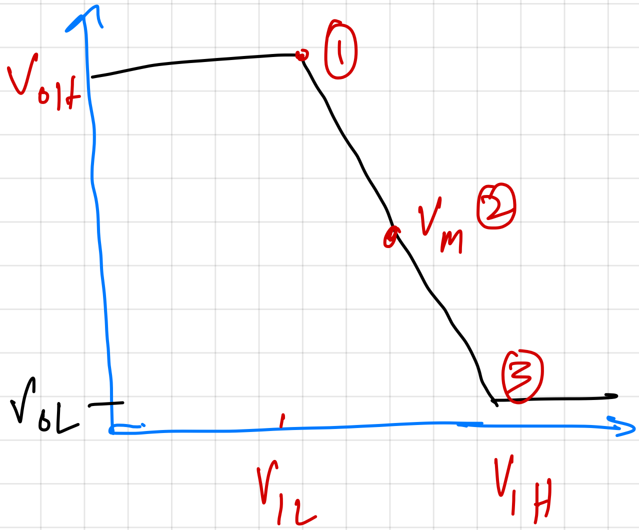
$$= \frac{2.5 - V_M}{75K} = \frac{1}{2} \times 115 \times 10^{-6} \times 3 \times (V_M - 0.43)^2$$



$= V_M \sim ?$

V_{IL}: $$\frac{V_{DD}-V_{out}}{R_L} = \frac{1}{2} K_n' \frac{W}{L} (V_{in}-V_T)^2$$

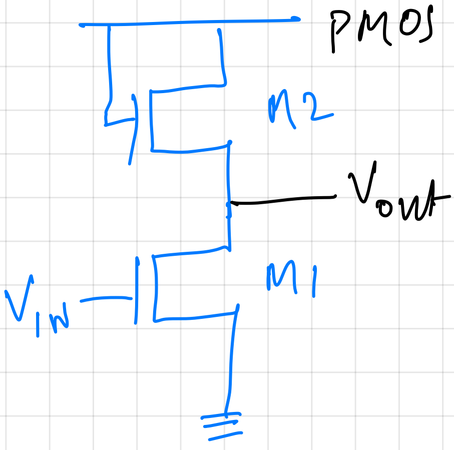
$$-\frac{1}{R_L}\frac{dV_{out}}{dV_{in}} = K_n' \frac{W}{L} (V_{IN}-V_T)$$



$$g = \frac{V_{OH}-V_M}{V_{IL}-V_M}$$

$$g = \frac{V_M - V_{OL}}{V_M - V_{IH}}$$

NMOS Bulk is at GND
PMOS " V_{DD}



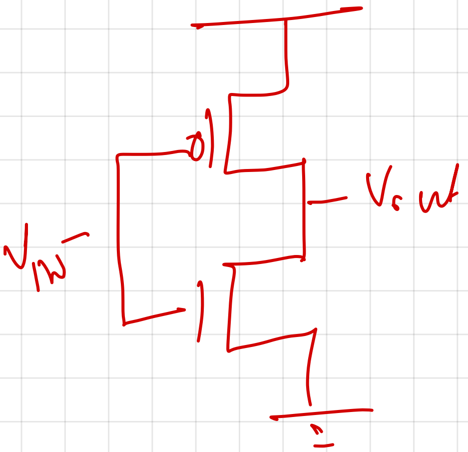
V_{OH} : ?

$V_{DD} - V_T$

$V_{GS} = V_{DD} - V_{out}$

If $V_{out} > V_{DD} - V_{out}$

then $V_{GS} < V_T$

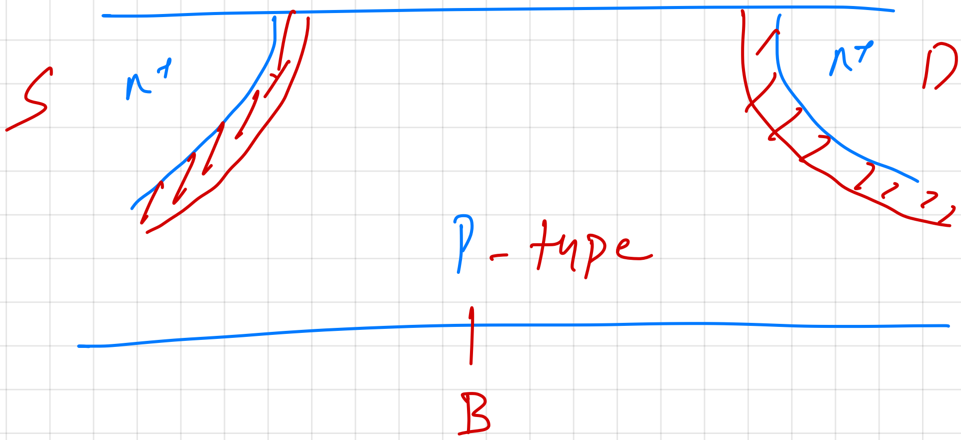


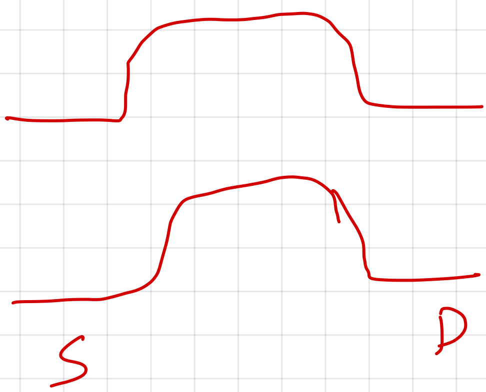
a) $V_T = 0.43V$

(b) $V_T = -0.4V$ X PMOS

(c) It depends

(d) I don't care X

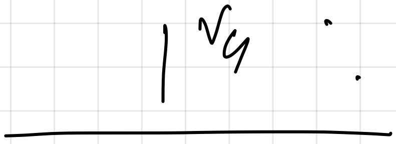




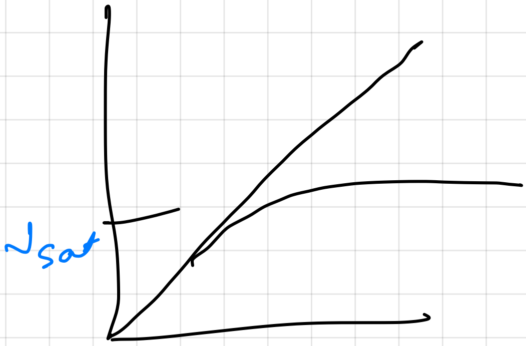
V_{SB} If V_{SB} is negative

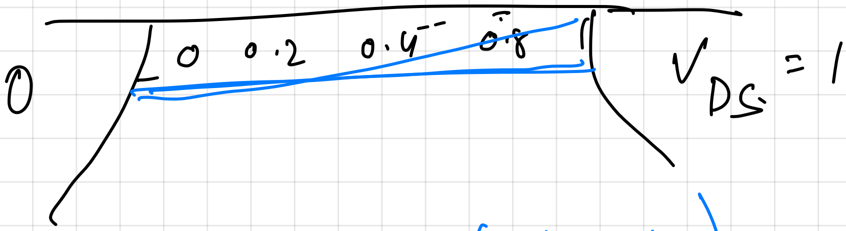
$$V_T = V_{T0} + \gamma\left(\sqrt{2\phi_F + |V_{SB}|} - \sqrt{2\phi_F}\right)$$

$$J_{drift} = ne\mu E$$



$$\frac{V}{L}$$





$~~V_G~~$

$$V_{DS} = 2.5 - 0.43$$

$$Q_{inv} = C(V_G - V_C)$$

0.63 V