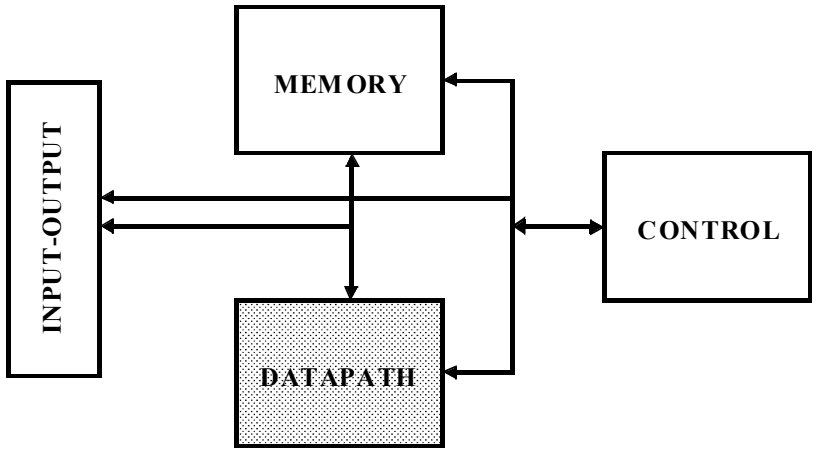
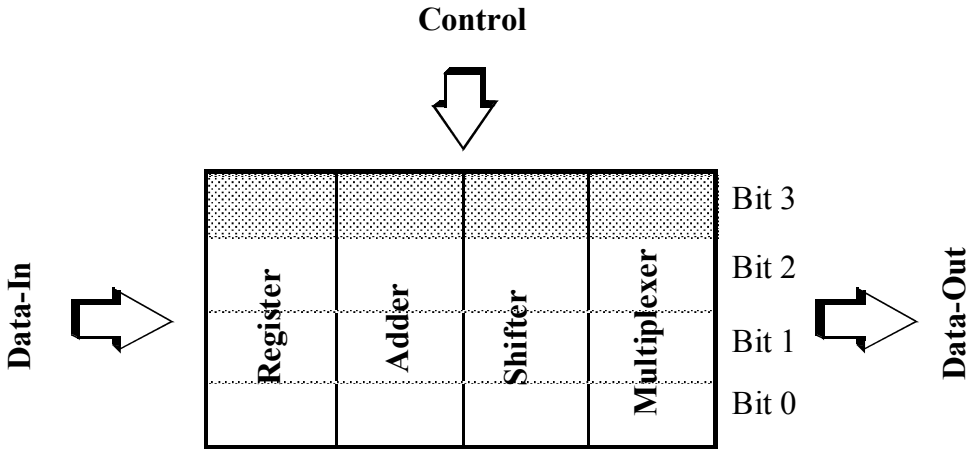
EE5153: Introduction to VLSI Design

Implementation of Arithmetic in VLSI

Acknowledgement: Material primarily form textbook and lecture slides for Rabaey et. al. Digital Integrated Circuits, 2nd Edition (2002).

A Generic Digital Processor





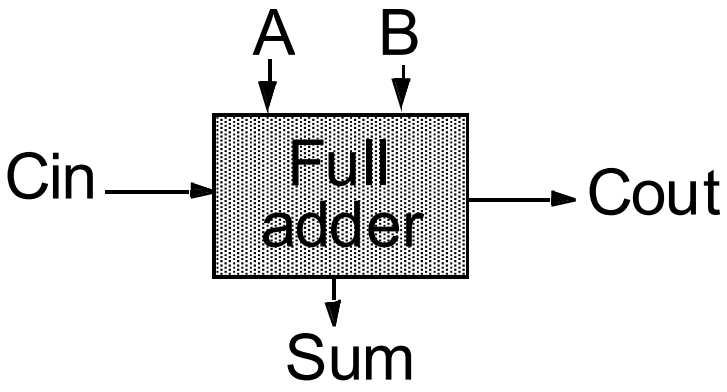
Bit sliced design for datapath

- Arithmetic Unit
  - Datapath (adder, multiplier, shifter, comparator, etc)
- Memory
  - RAM, ROM, Buffers, Shift Registers
- Control
  - Finite State Machine (PLA, random logic)
  - Counters
- Interconnect
  - Switches
  - Bus

Adders

- Half Adder
- Full Adder
- Ripple Carry Adder

Full Adder



$A \oplus B \oplus C$

$S = ?$ $ABC + A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C$

$C_{out} = ?$ $AB + BC + CA$

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

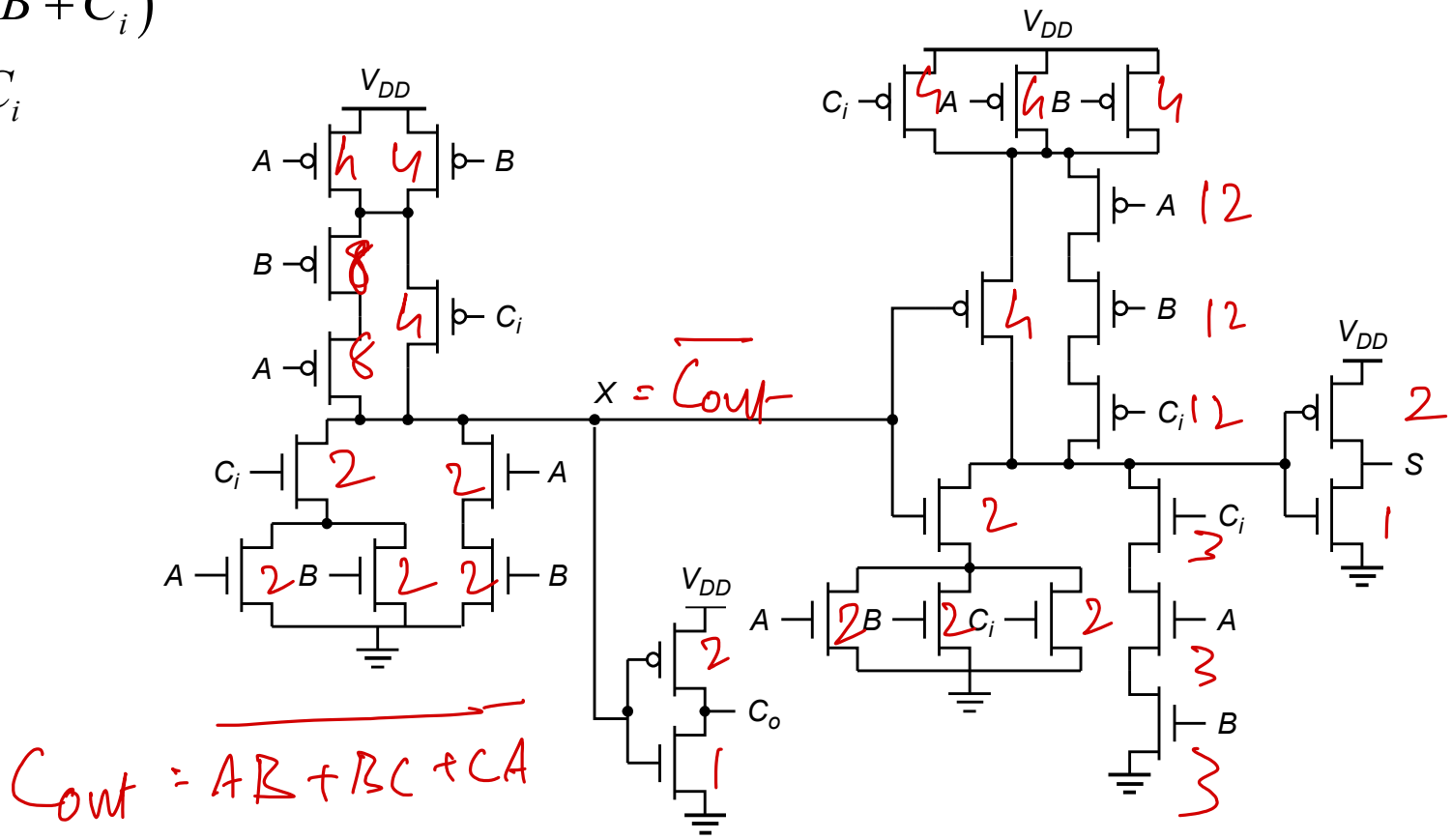
Direct CMOS Implementation of Full Adder

$$S = ABC_i + \overline{C_{out}}\left(A + B + C_i\right)$$

$$C_{out} = AB + BC_i + AC_i$$

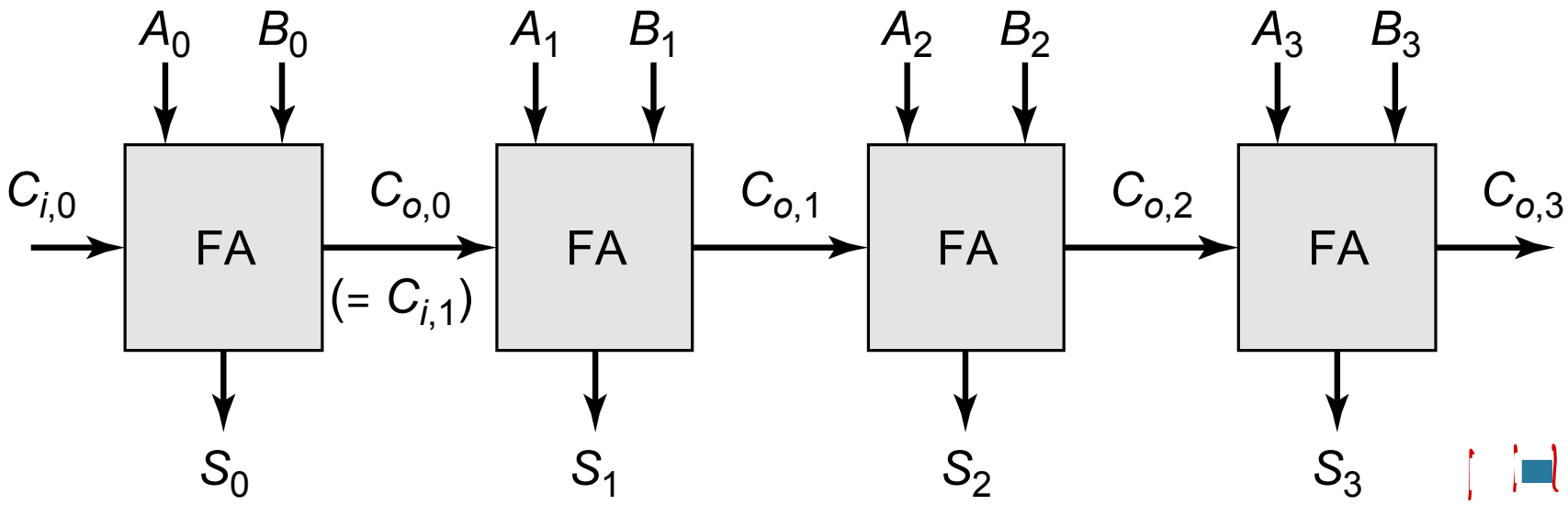
LE of C_i = ?

LE of A = ?



28 Transistors!!

Ripple Carry Adder (RCA)



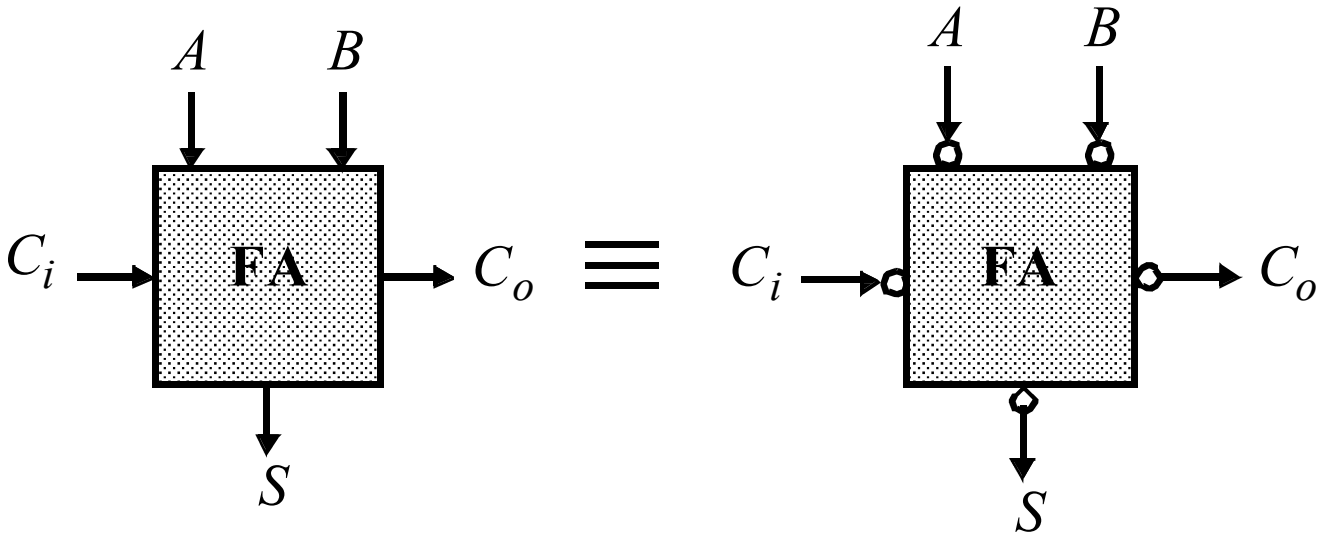
Worst case delay linear with the number of bits

$$t_d = O(N)$$

$$t_{adder} = (N-1)t_{carry} + t_{sum}$$

Goal: Make the fastest possible carry path circuit

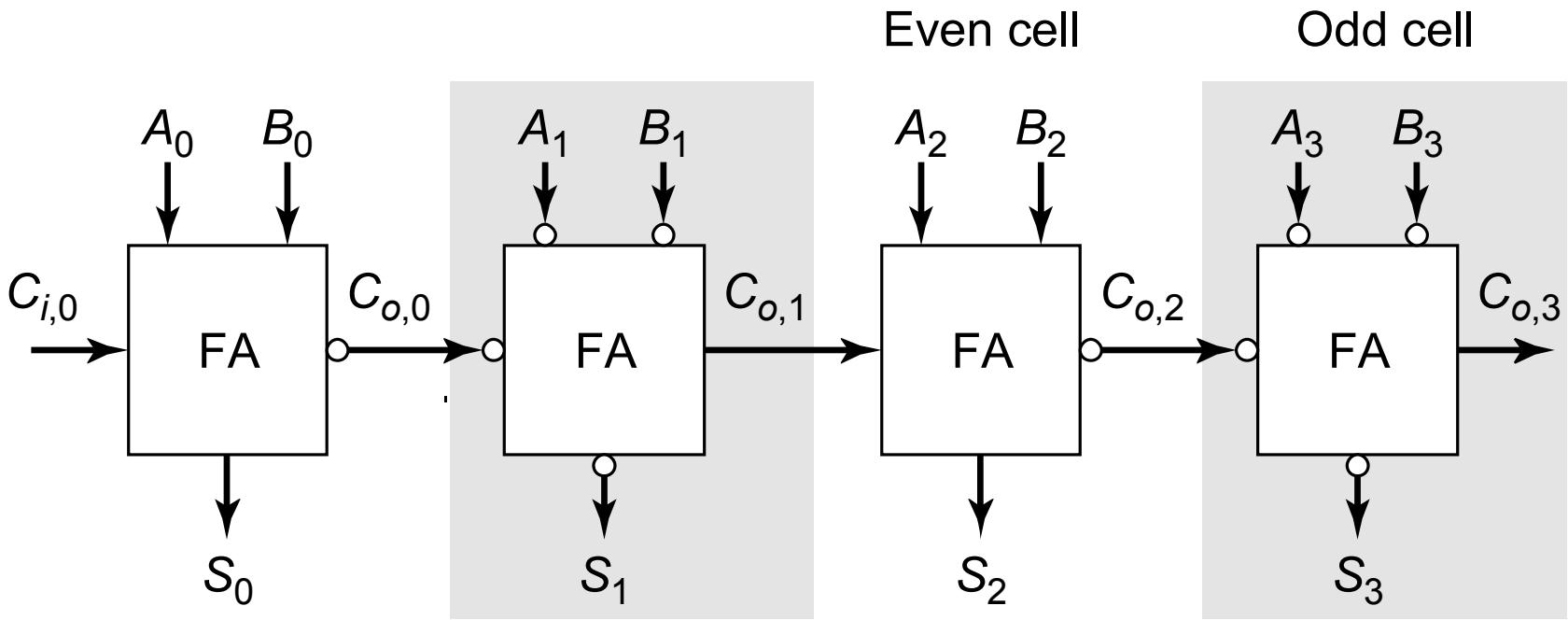
Inversion Property



$$\overline{S}(A,B,C_i) = S(\overline{A},\overline{B},\overline{C_i})$$

$$\overline{C}(A,B,C_i) = C(\overline{A},\overline{B},\overline{C_i})$$

Minimize Critical Path by Reducing Inverting Stages

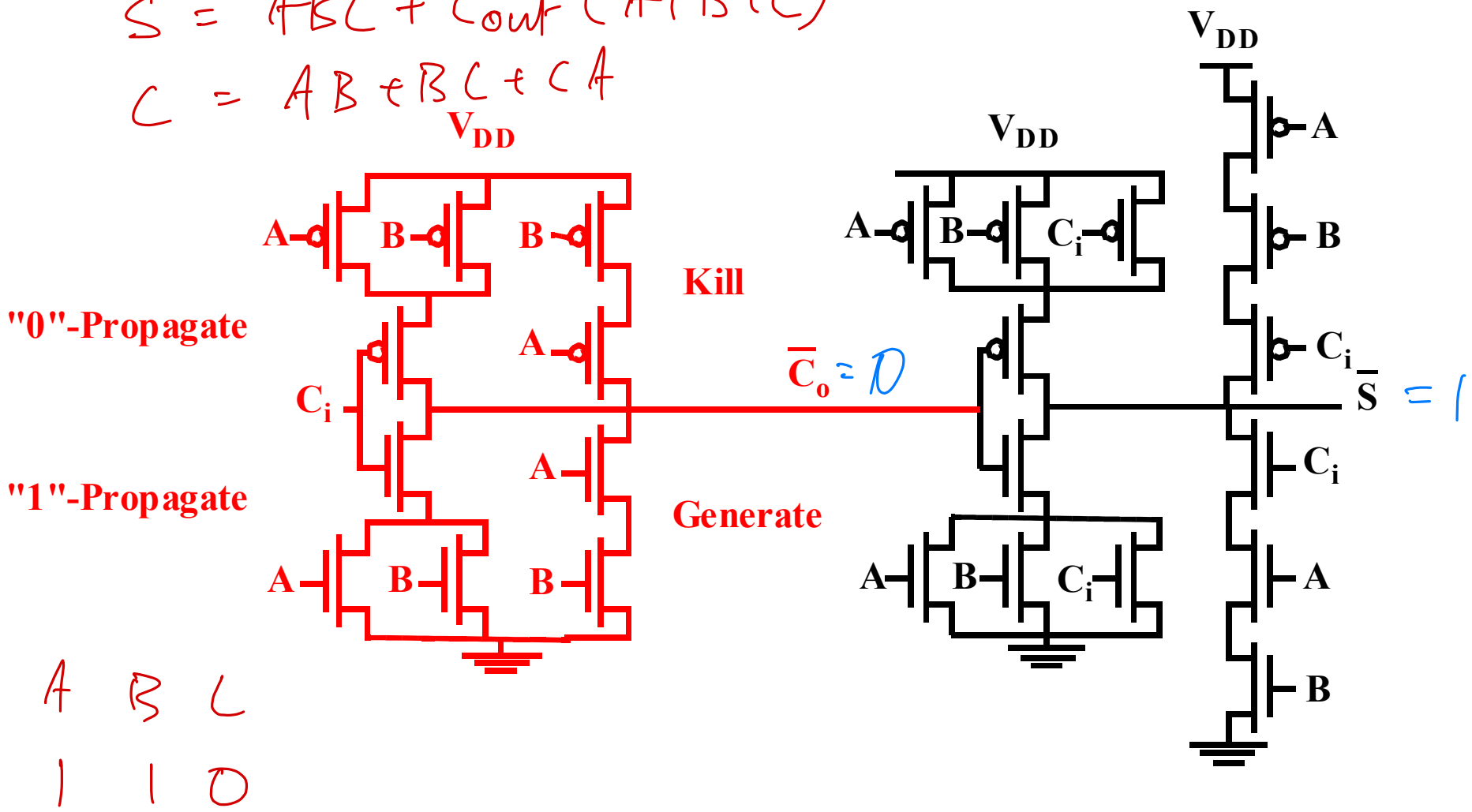


Here, FA stands for full adder without the inverter in carry path

The Mirror Adder

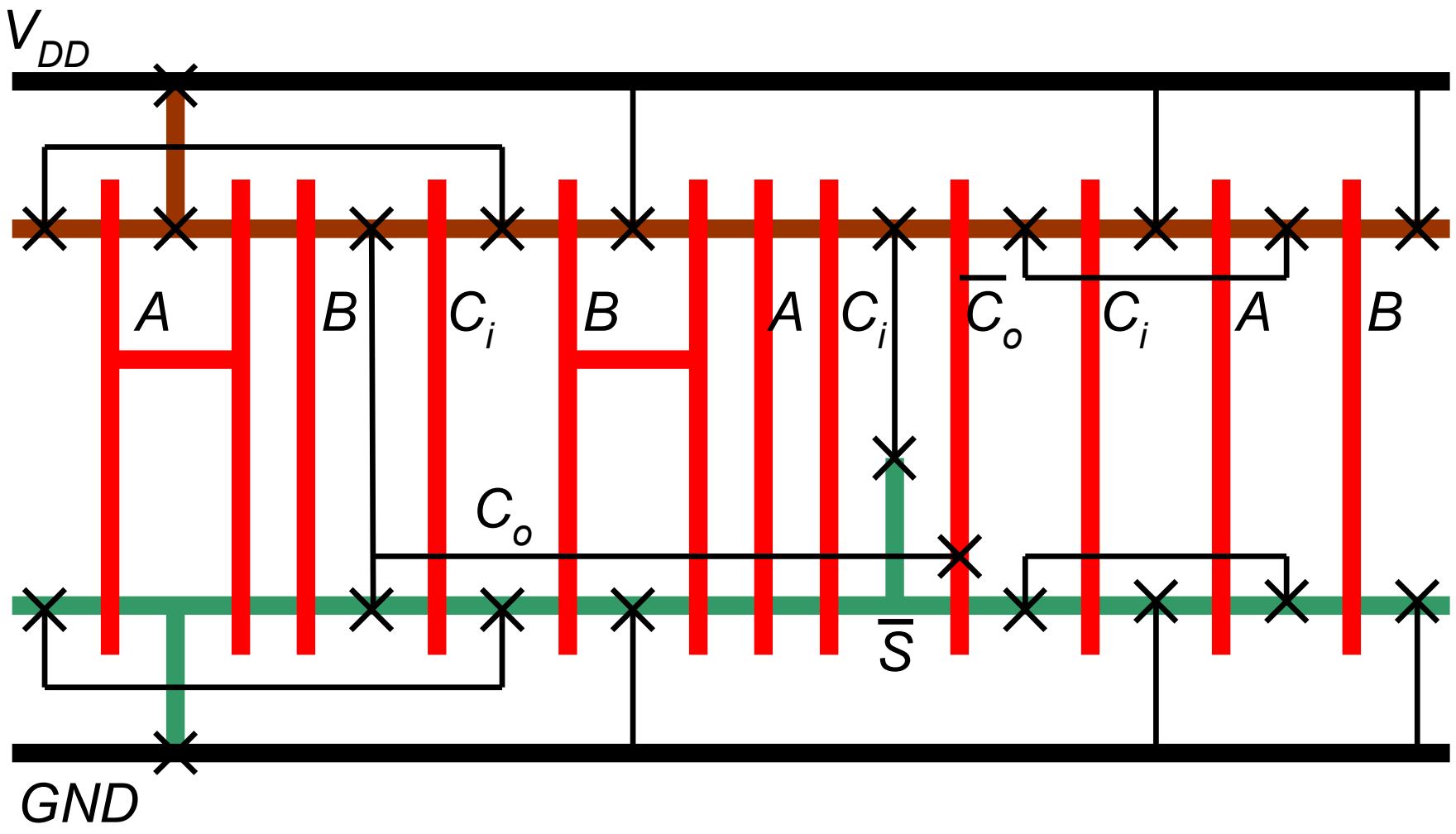
$S = ABC + \overline{C_{out}}(A+B+C)$

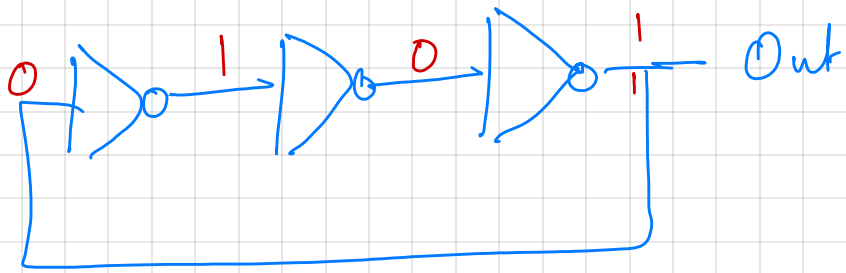
$C = AB + BC + CA$



How to size the adder to optimize the delay in the carry chain?

Mirror Adder – The stick diagram





N = 21, 101