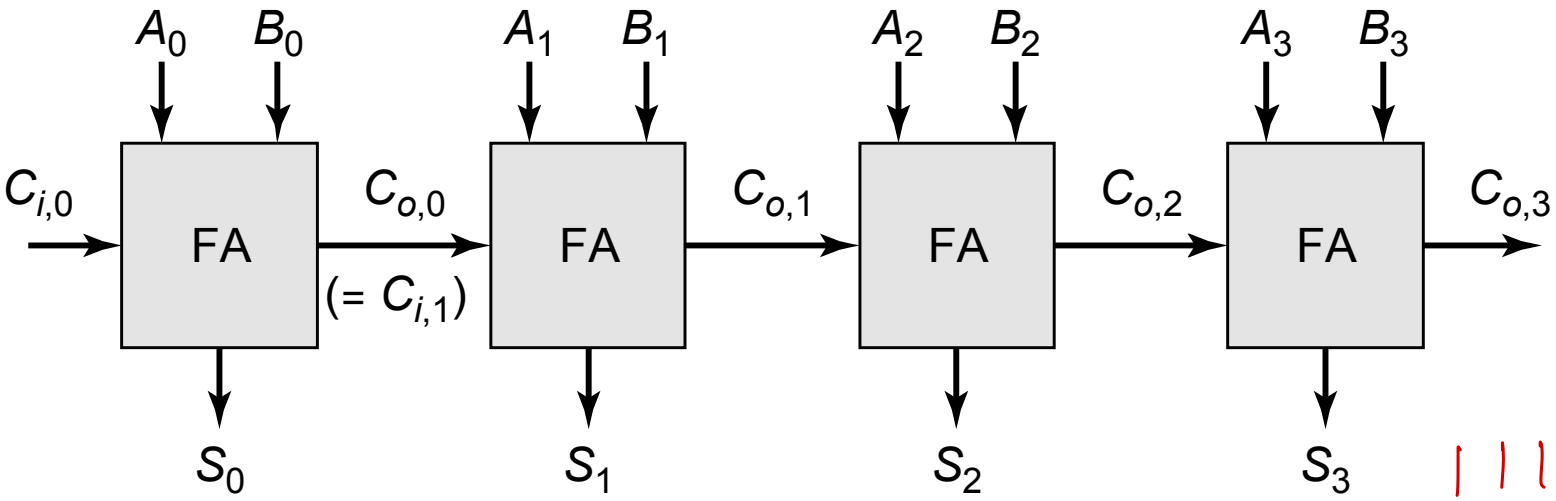
Ripple Carry Adder (RCA)



1111
0001
10000

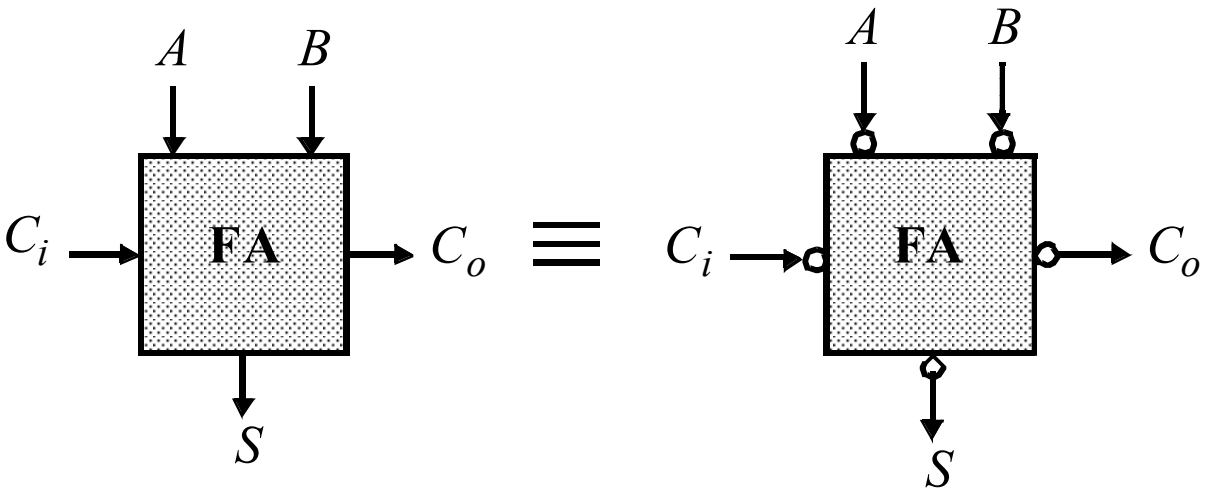
Worst case delay linear with the number of bits

$$t_d = O(N)$$

$$t_{adder} = (N-1)t_{carry} + t_{sum}$$

Goal: Make the fastest possible carry path circuit

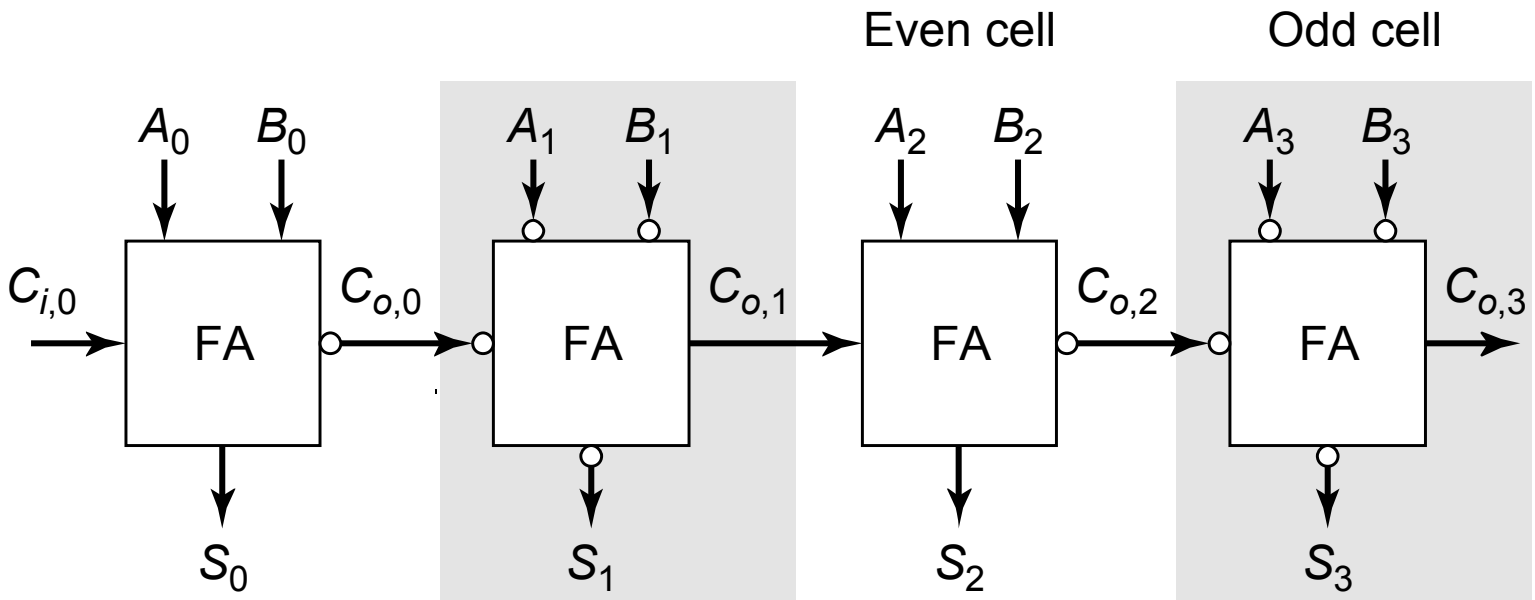
Inversion Property



$$\overline{S}(A,B,C_i) = S(\overline{A},\overline{B},\overline{C_i})$$

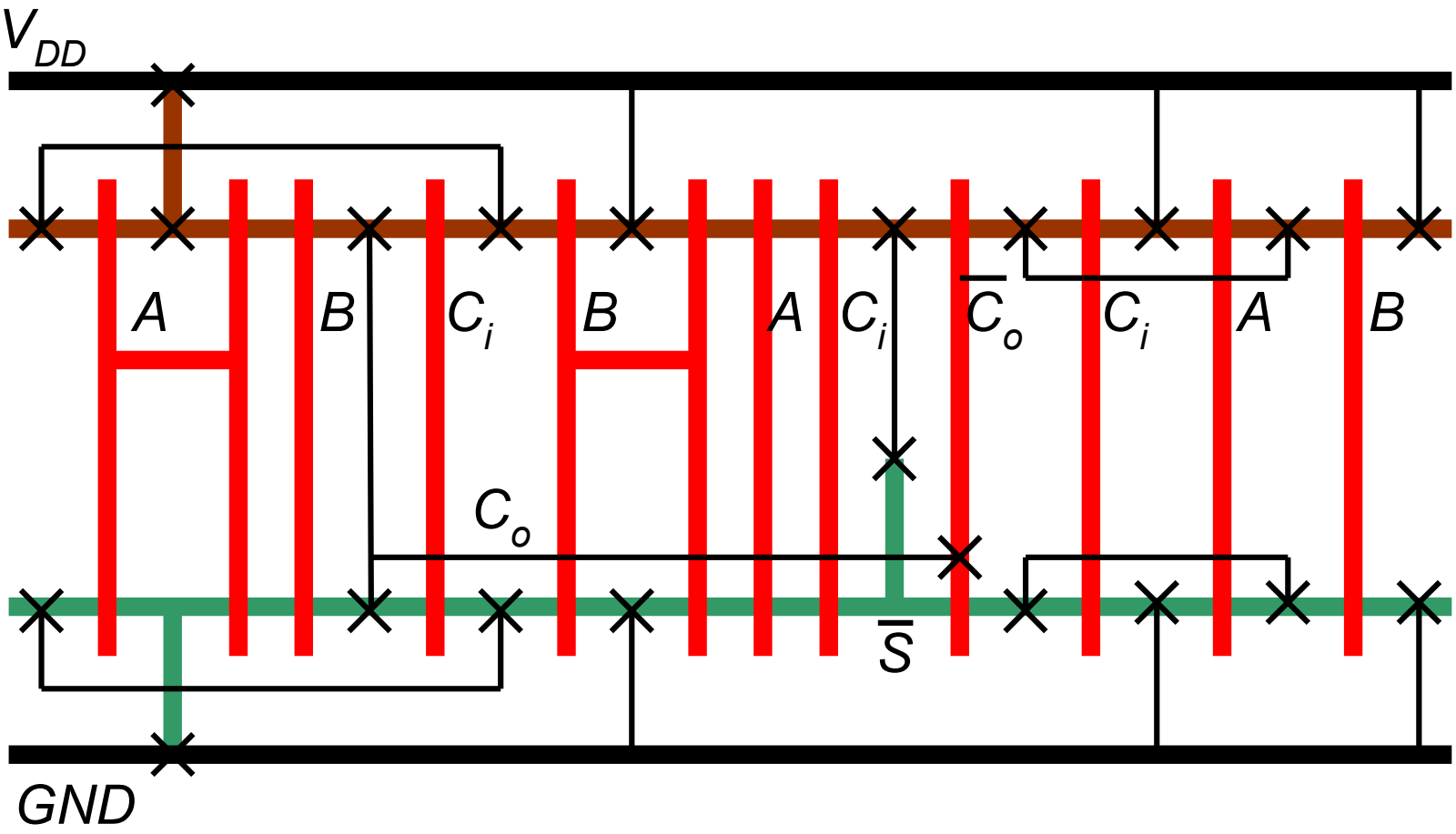
$$\overline{C}(A,B,C_i) = C(\overline{A},\overline{B},\overline{C_i})$$

Minimize Critical Path by Reducing Inverting Stages



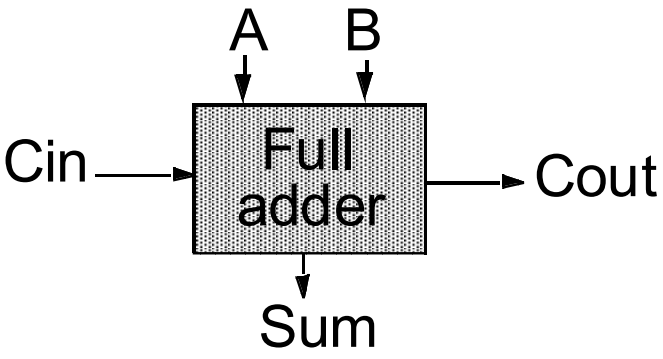
Here, FA stands for full adder without the inverter in carry path

Mirror Adder – The stick diagram



Kill, Propagate and Generate

Carry Look ahead



A	B	Cin	Sum	Cout	
0	0	0	0	0	Kill
0	0	1	1	0	
0	1	0	1	0	Propagate
0	1	1	0	1	
1	0	0	1	0	
1	0	1	0	1	
1	1	0	0	1	Generate
1	1	1	1	1	

No benefit w.r.t ripple carry adder in static implementation

$$G = AB \qquad S = A \oplus B \oplus C_i = ABC_i + \overline{C_o}\left(A + B + C_i\right)$$

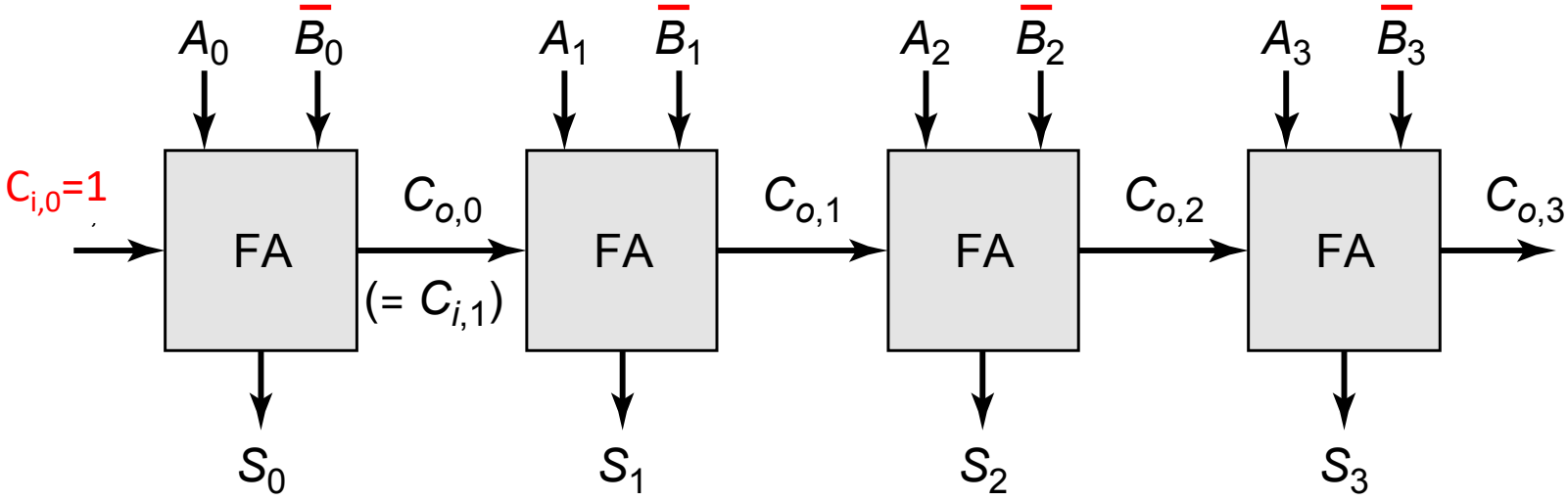
$$P = A \oplus B \qquad = P \oplus C_i$$

$$K = \overline{A}\,\overline{B} \qquad C_{out} = AB + BC_i + AC_i = G + PC_i$$

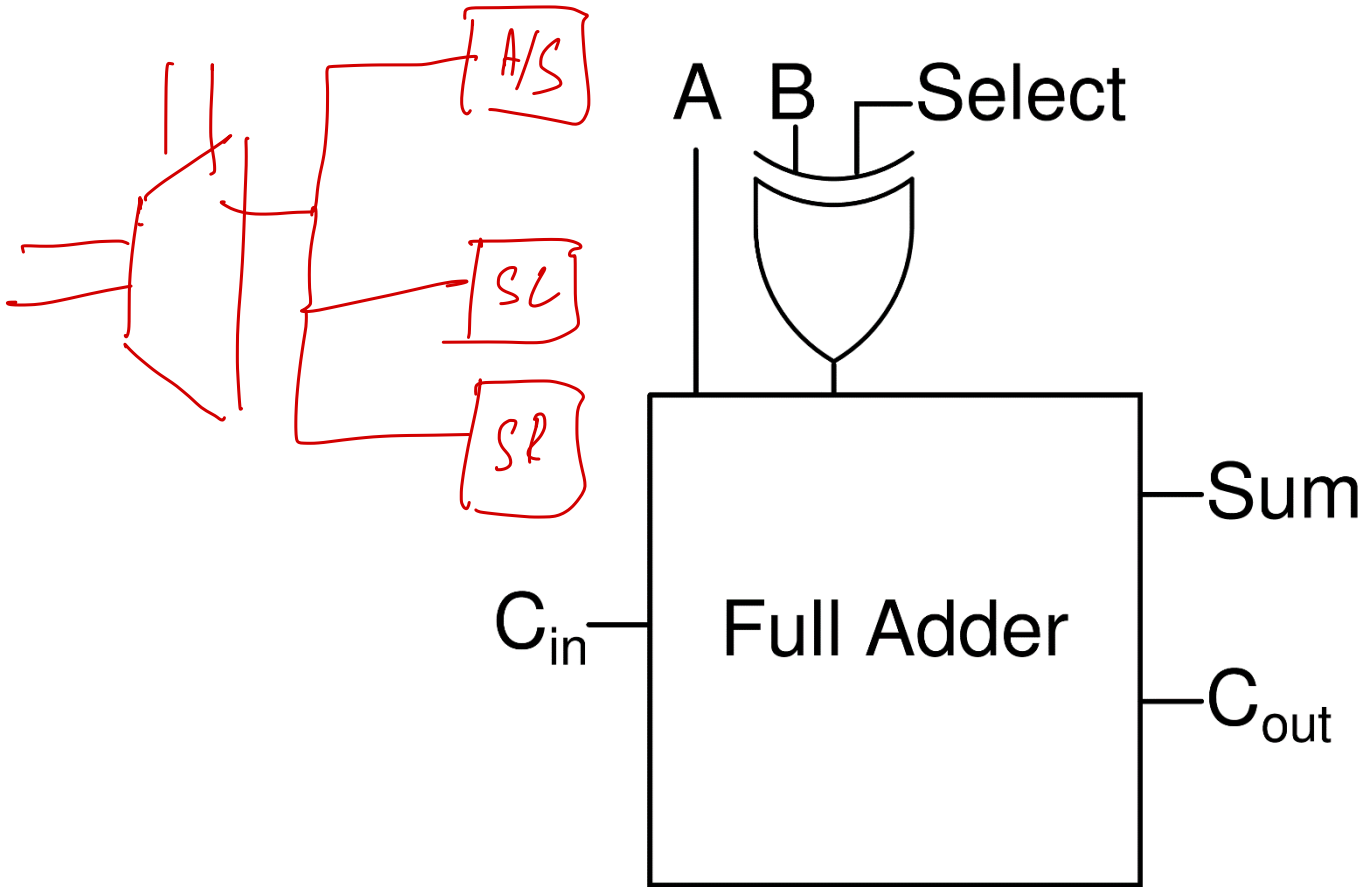
How to subtract?

- Subtraction can be implemented by using 2's complement notation

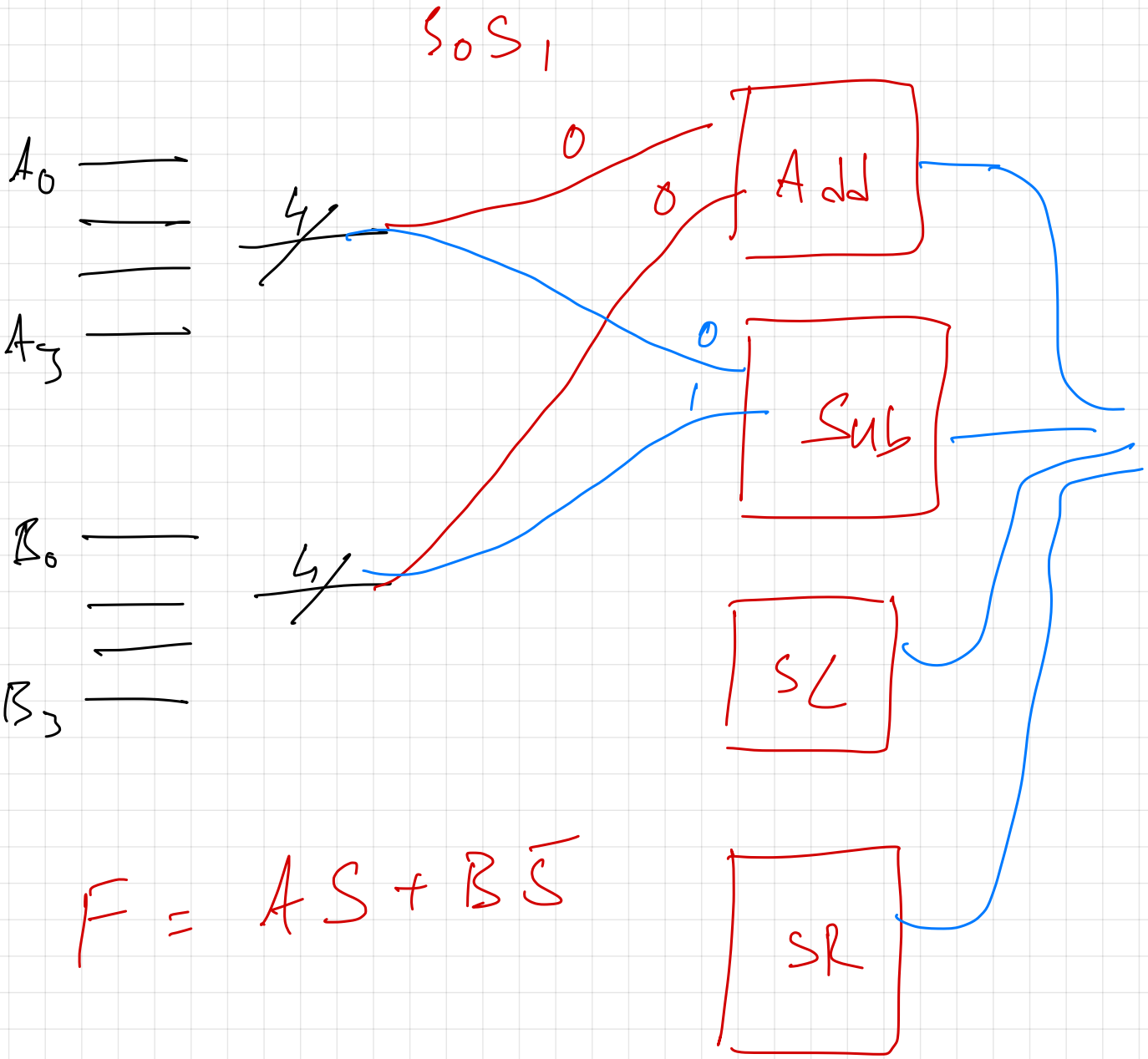
$$A - B = A + (-B) = A + \overline{B} + 1$$



Add and Subtract Unit

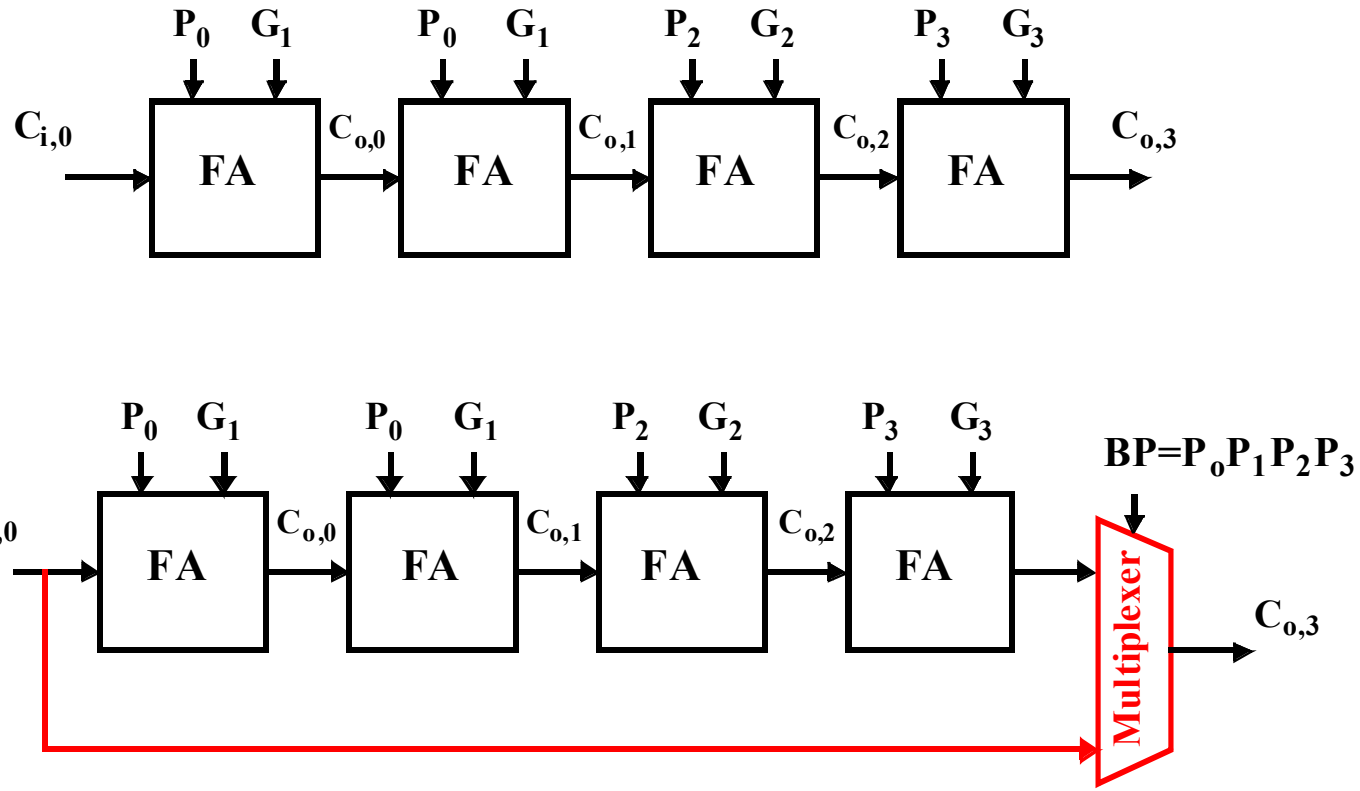


S1 S0
0 0 – add
0 1 – Subtract
1 0 – Shift L
1 1 – Shift R



$$F = AS + B\bar{S}$$

Carry Bypass/Carry-Skip Adder

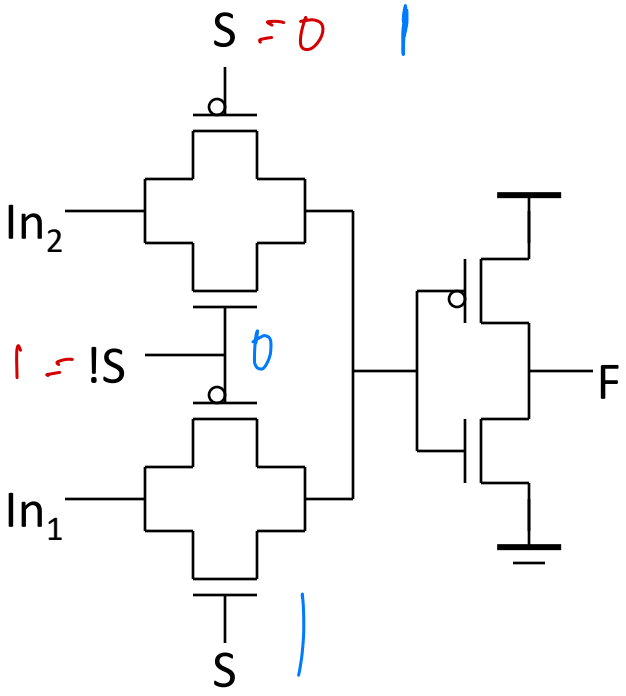


Idea: If (P0 and P1 and P2 and P3 = 1) then $C_{o3} = C_0$, else "kill" or "generate".

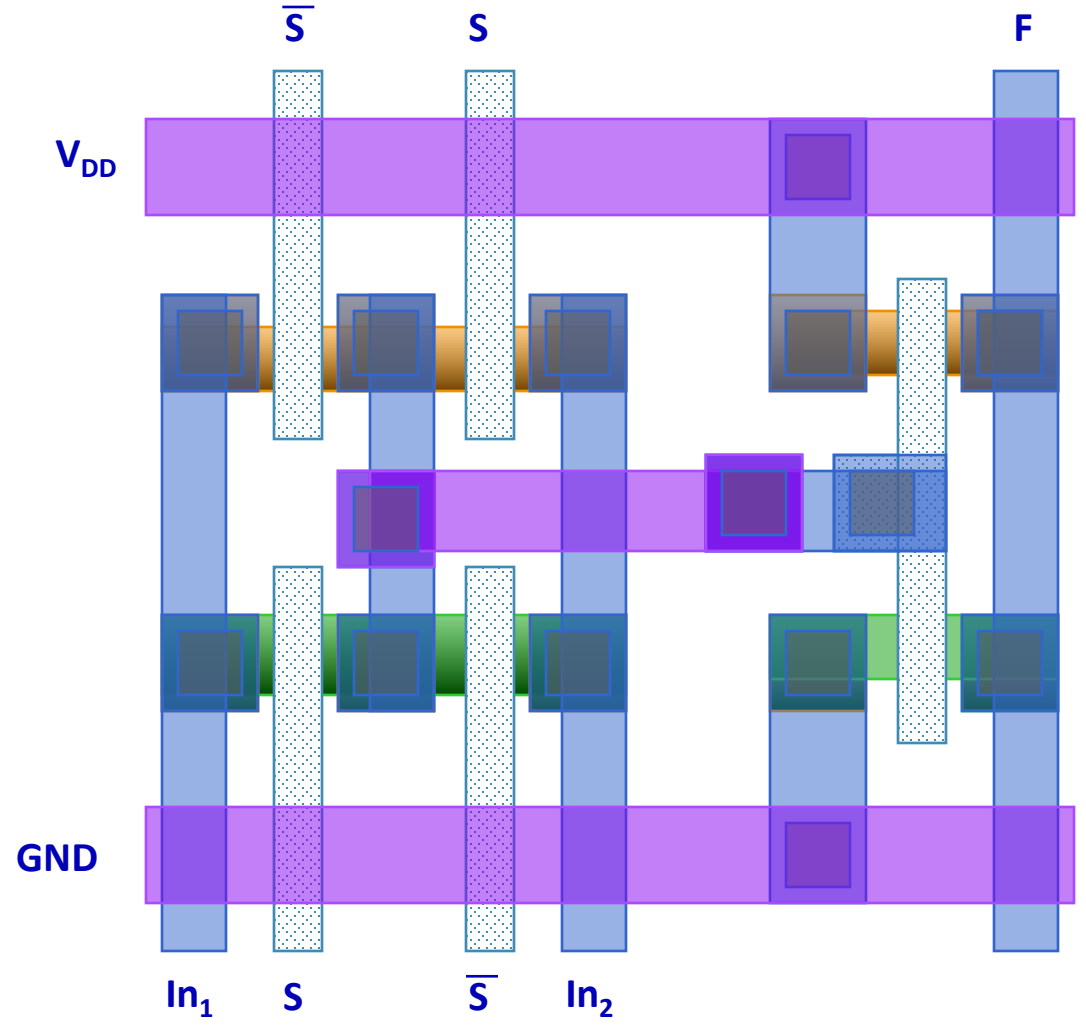
Summary - Adders

- The NMOS and PMOS chains are completely symmetrical.
  A maximum of two series transistors can be observed in the carry-generation circuitry.
- When laying out the cell, the most critical issue is the minimization of the capacitance at node Co. The reduction of the diffusion capacitances is particularly important.
- The capacitance at node Co is composed of four diffusion capacitances, two internal gate capacitances, and six gate capacitances in the connecting adder cell .
- The transistors connected to Ci are placed closest to the output.
- Only the transistors in the carry stage have to be optimized for optimal speed. All transistors in the sum stage can be minimal size.
- Many other types of adders are available such as Carry Select, Manchester Carry, etc

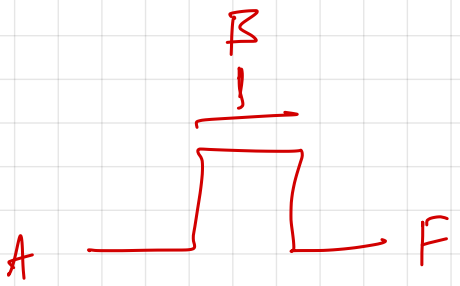
Transmission Gate Multiplexer



$$F = \overline{In_1 S + In_2 \overline{S}}$$

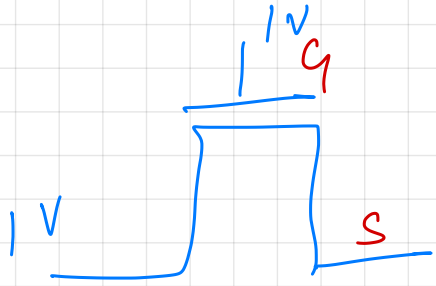


Pass gate:

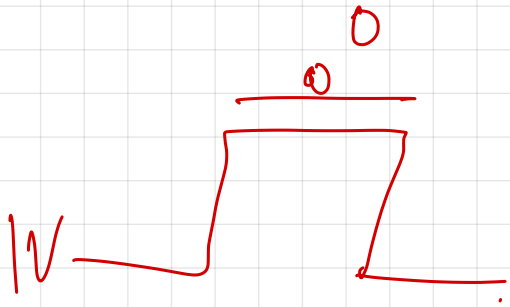


$F = A \cdot B$

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1



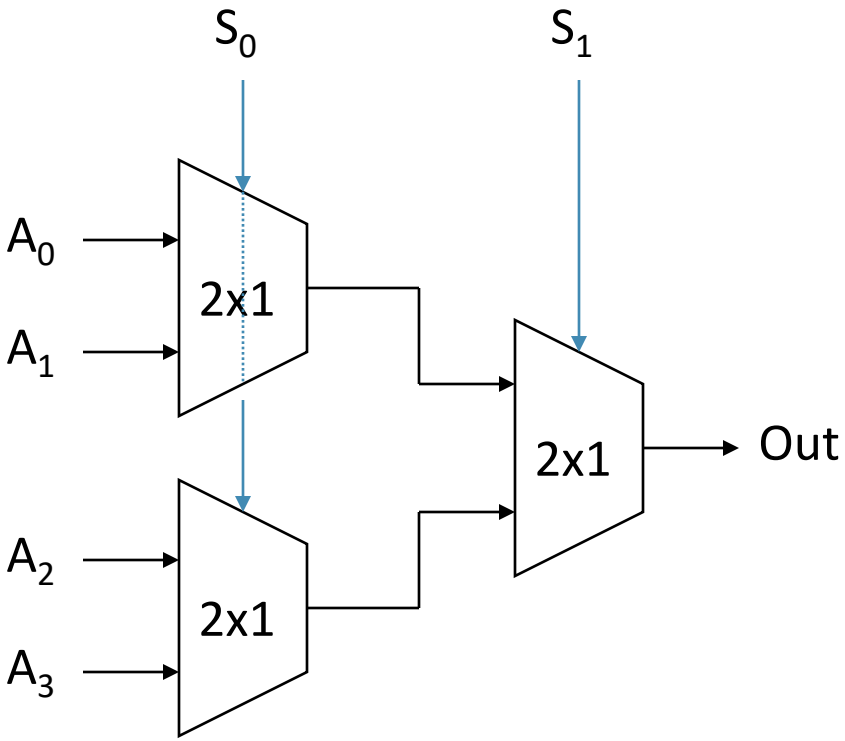
$F = ?$ $1 - V_{tn_0}$



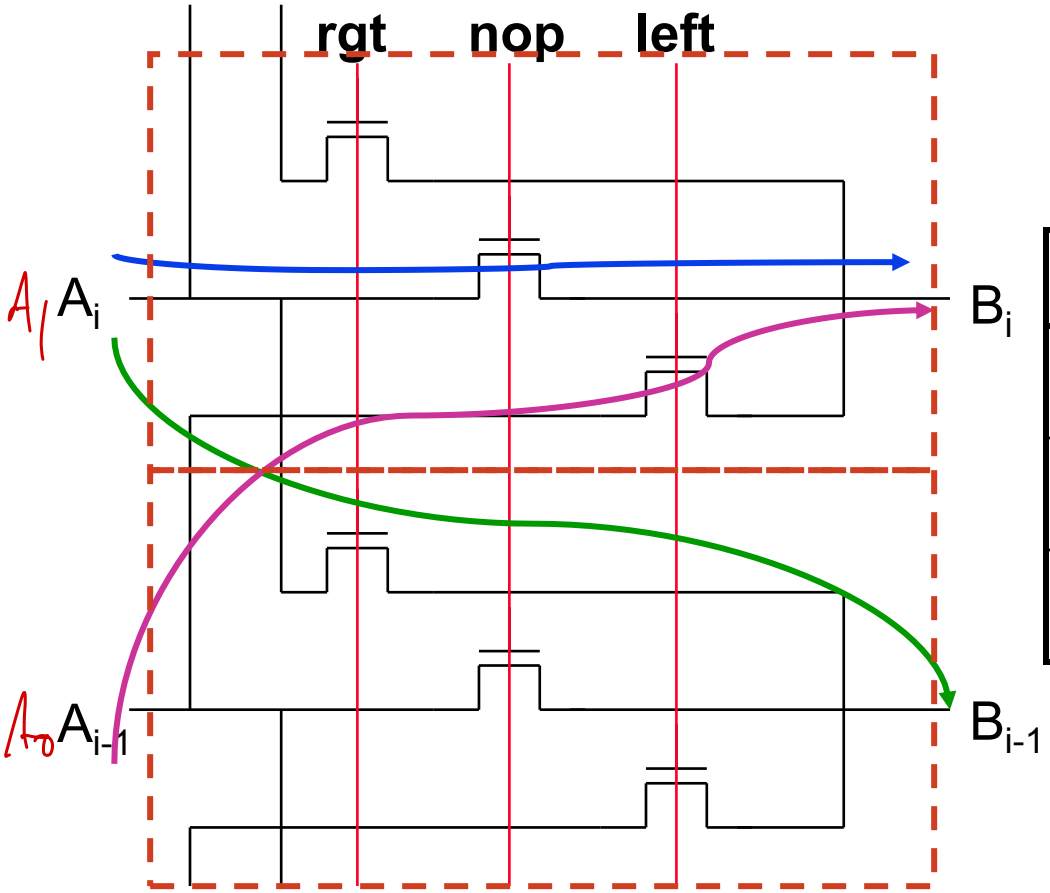
NMOS
strong 0
weak 1

PMOS
weak 0
strong 1

Building Big Muxes from Small

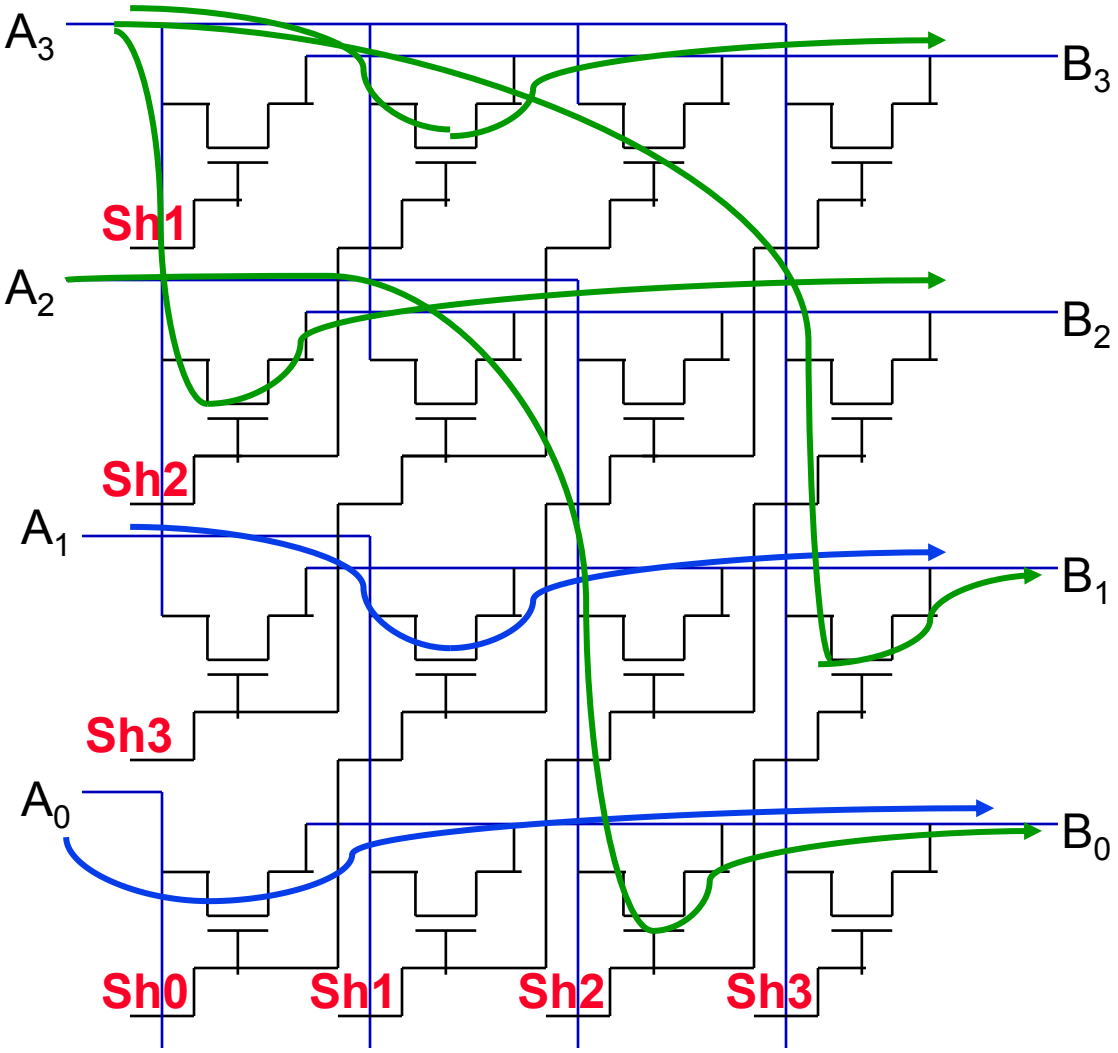


Shifter



A_i	A_{i-1}	rgt	nop	left	B_i	B_{i-1}
A_1	A_0	0	1	0	A_1	A_0
A_1	A_0	1	0	0	0	A_1
A_1	A_0	0	0	1	A_0	0

Barrel Shifter



Example: Sh0 = 1

$B_3B_2B_1B_0 = A_3A_2A_1A_0$

Sh1 = 1

$B_3B_2B_1B_0 = A_3A_3A_2A_1$

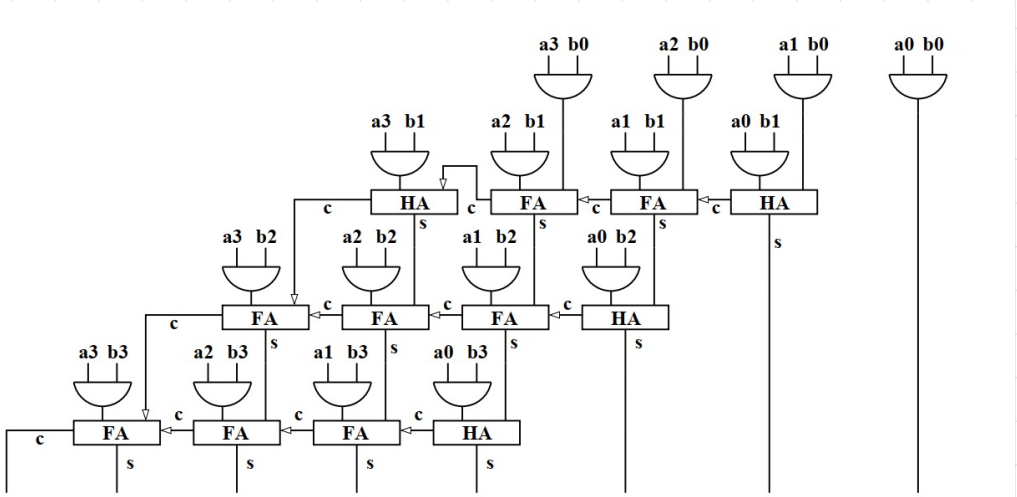
Sh2 = 1

$B_3B_2B_1B_0 = A_3A_3A_3A_2$

Sh3 = 1

$B_3B_2B_1B_0 = A_3A_3A_3A_3$

Area dominated by wiring


a3 b0
a2 b0
a1 b0
a0 b0
a3 b1
a2 b1
a1 b1
a0 b1
HA
FA
FA
HA
c
s
a3 b2
a2 b2
a1 b2
a0 b2
FA
FA
FA
HA
a3 b3
a2 b3
a1 b3
a0 b3
FA
FA
FA
HA