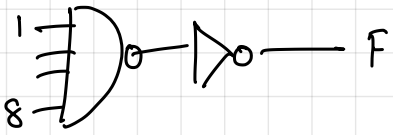
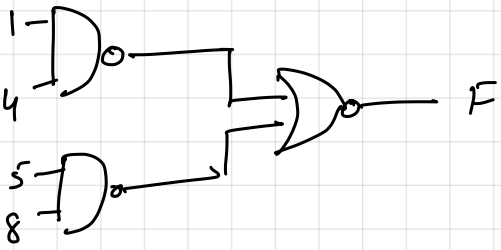
Introduction to VLSI Design
Lecture 15 - 12th Sep 2022

$F = \overline{X_1 X_2 \ldots X_8}$ → 8 input decoder

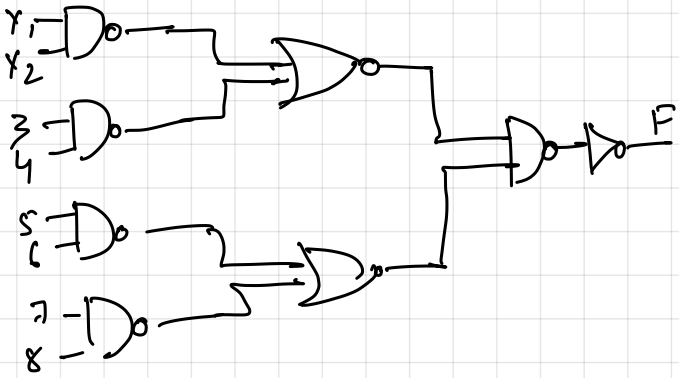
① 

② $\overline{X_1 \ldots X_4 + X_5 \ldots X_8}$



③ $\overline{\overline{X_1 X_2} + \overline{X_3 X_4} + \overline{X_5 X_6} + \overline{X_7 X_8}}$

$= \overline{\overline{X_1 X_2} + \overline{X_3 X_4}} \cdot \overline{\overline{X_5 X_6} + \overline{X_7 X_8}}$



Logical Effort

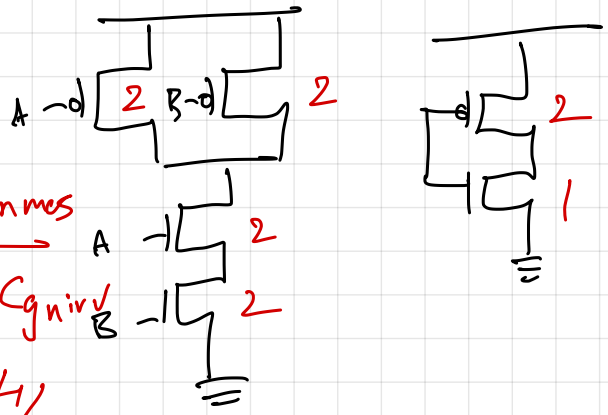
$LE(g) = \frac{R_{gate} C_{gate}}{R_{inv} C_{inv}}$ If $R_{gate} = R_{inv}$, $g = \frac{C_{gate}}{C_{inv}}$

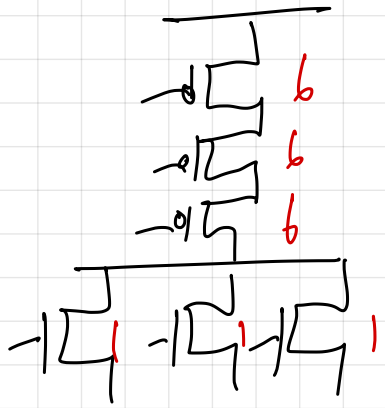
$g_{inv} = 1$

$g_{nand} = ?$

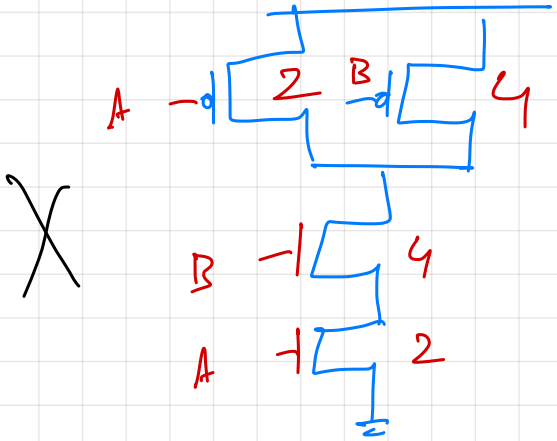
$= \frac{C_{g,PMOS} + C_{gnmos}}{C_{g,P,inv} + C_{gn,inv}}$

$= \frac{4C}{3C} = 4/3$



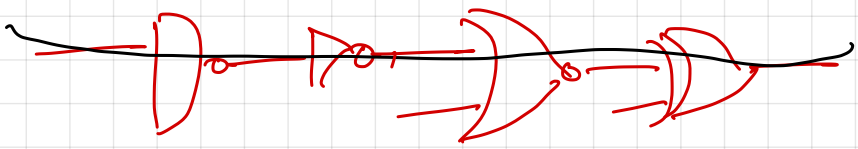


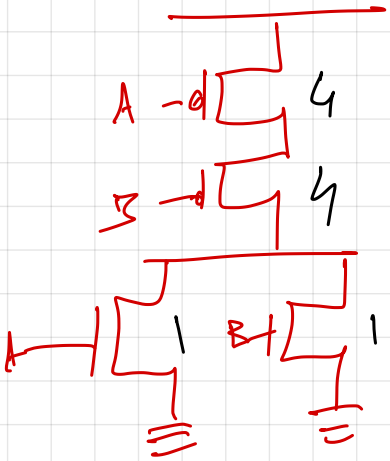
Nand	g	Nor	g
2	4/3	2	5/3
3	5/3	3	7/3
4	6/3	4	9/3
n	(n+1)/3		(2n+1)/3



$g_A = \frac{4}{3}$

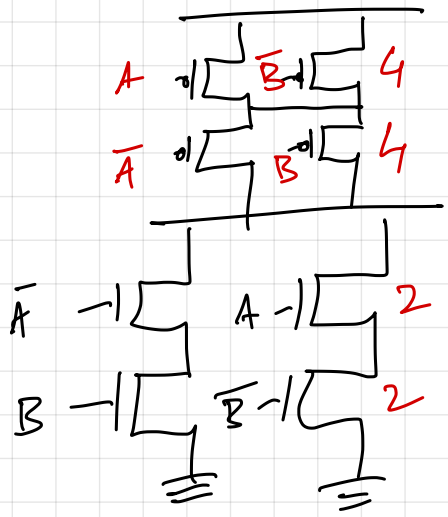
$g_B = \frac{8}{3}$





$g = \frac{5}{3}$

XNOR $F = \overline{A\bar{B} + \bar{A}B}$



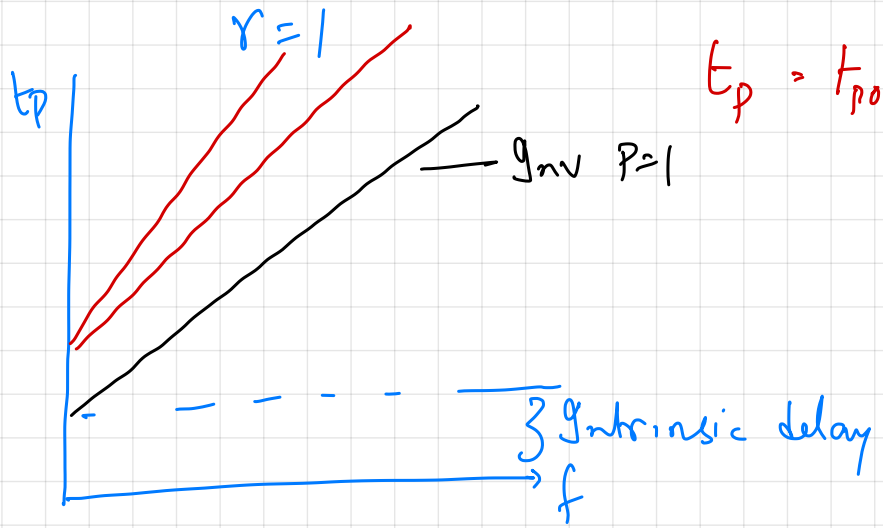
$g = \frac{6}{3} = 2$

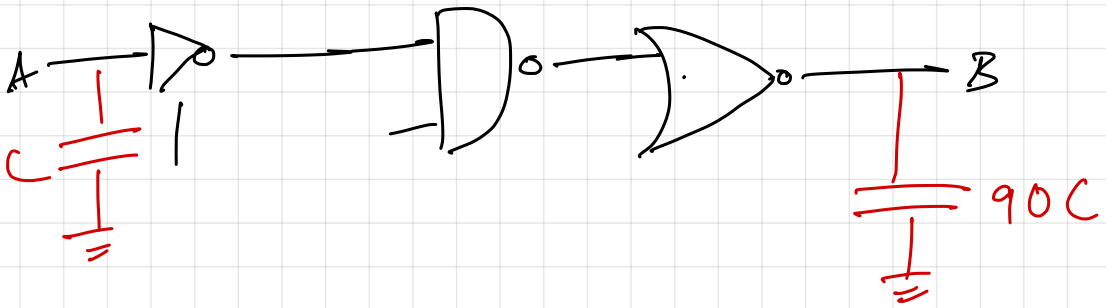
$g_{XOR} > g_{NOR} > g_{nand} > g_{inv}$

$t_p = t_{p0}\left(1 + \frac{f}{\gamma}\right)$

$t_p = t_{p0}\left(p + \frac{gf}{\gamma}\right)$

Logical Effort
Fan-out
No. of inputs





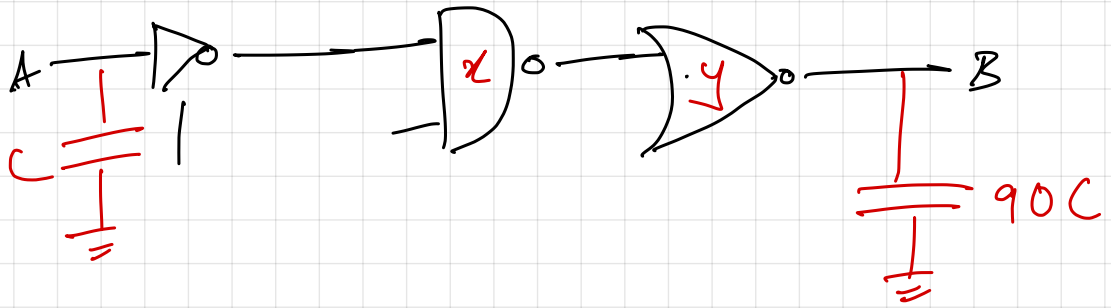
Path fanout = $F = 90$

Path Logical Effort $G = \prod g_i = 1 \times \frac{4}{3} \times \frac{5}{3} = \frac{20}{9}$

Stage Effort $= f_i g_i$

Path effort $= H = GF = \frac{20}{9} \times 90 = 200$

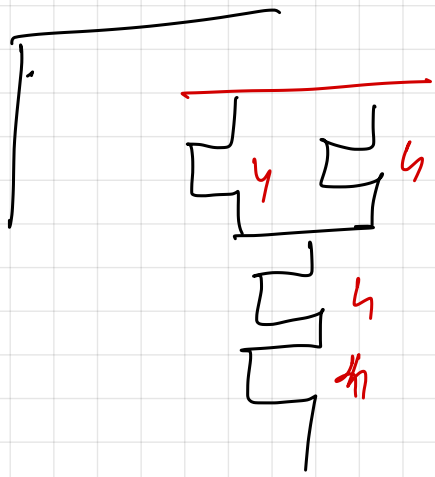
$h_{opt} = (200)^{1/3} = 5.9$



$h_{opt} = 5.91$

$h_3 = g_3 f_3 = \frac{5}{3} \times \frac{90}{y} = 5.91$ $\quad y = ?$ 25.3

$h_2 = g_2 f_2 = \frac{4}{3} \times \frac{y}{x} = 5.91 \Rightarrow x = ?$ 5.84



$LF = \frac{8C \times R/2}{3C \times R} = \frac{4}{3}$

Scaling doesnot change logical effort