Introduction to VLSI Design

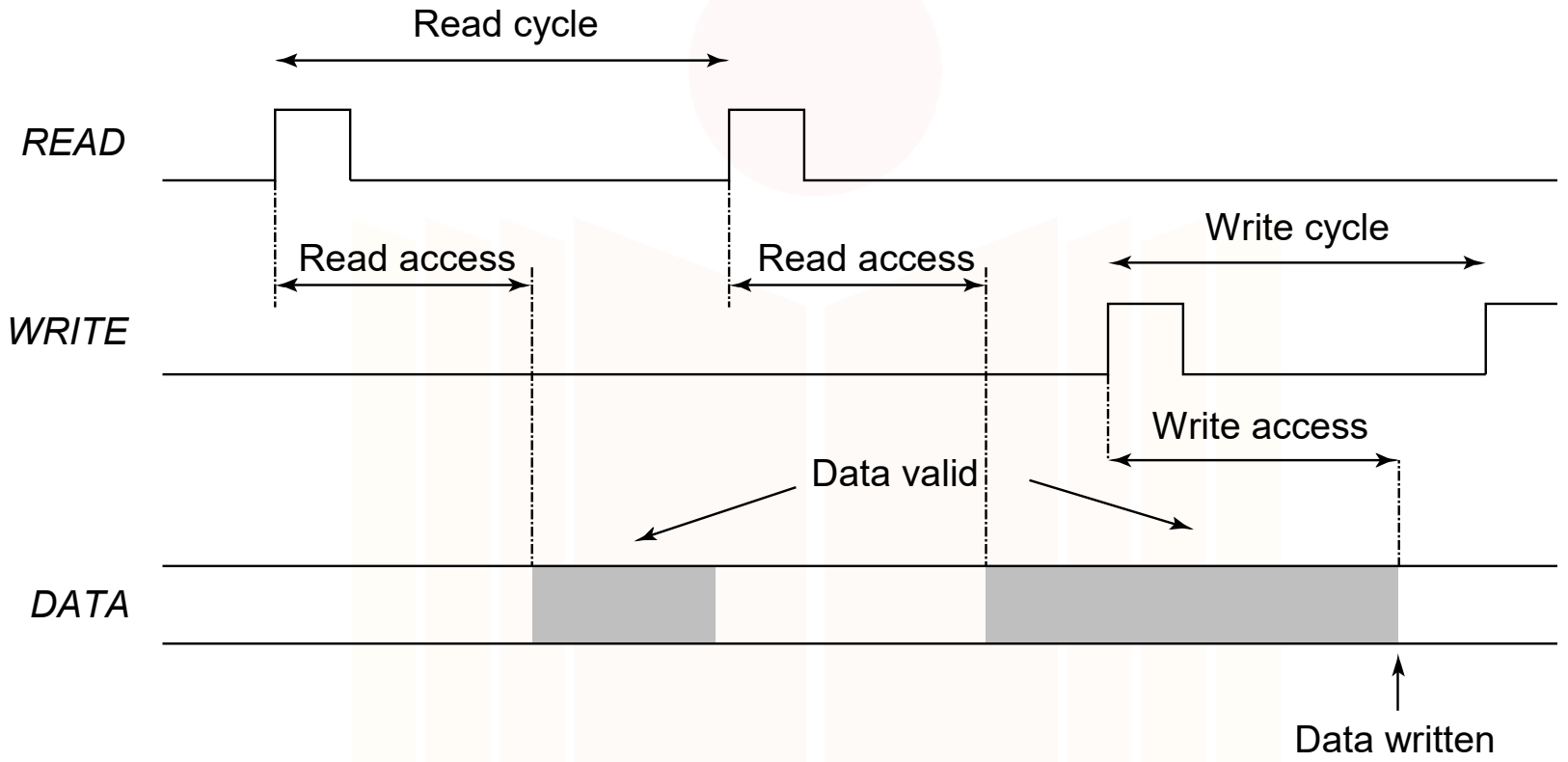
Memory Design

Material primarily form textbook and lecture slides for Rabaey et. al. Digital Integrated Circuits, 2nd Edition (2002) and other online resources

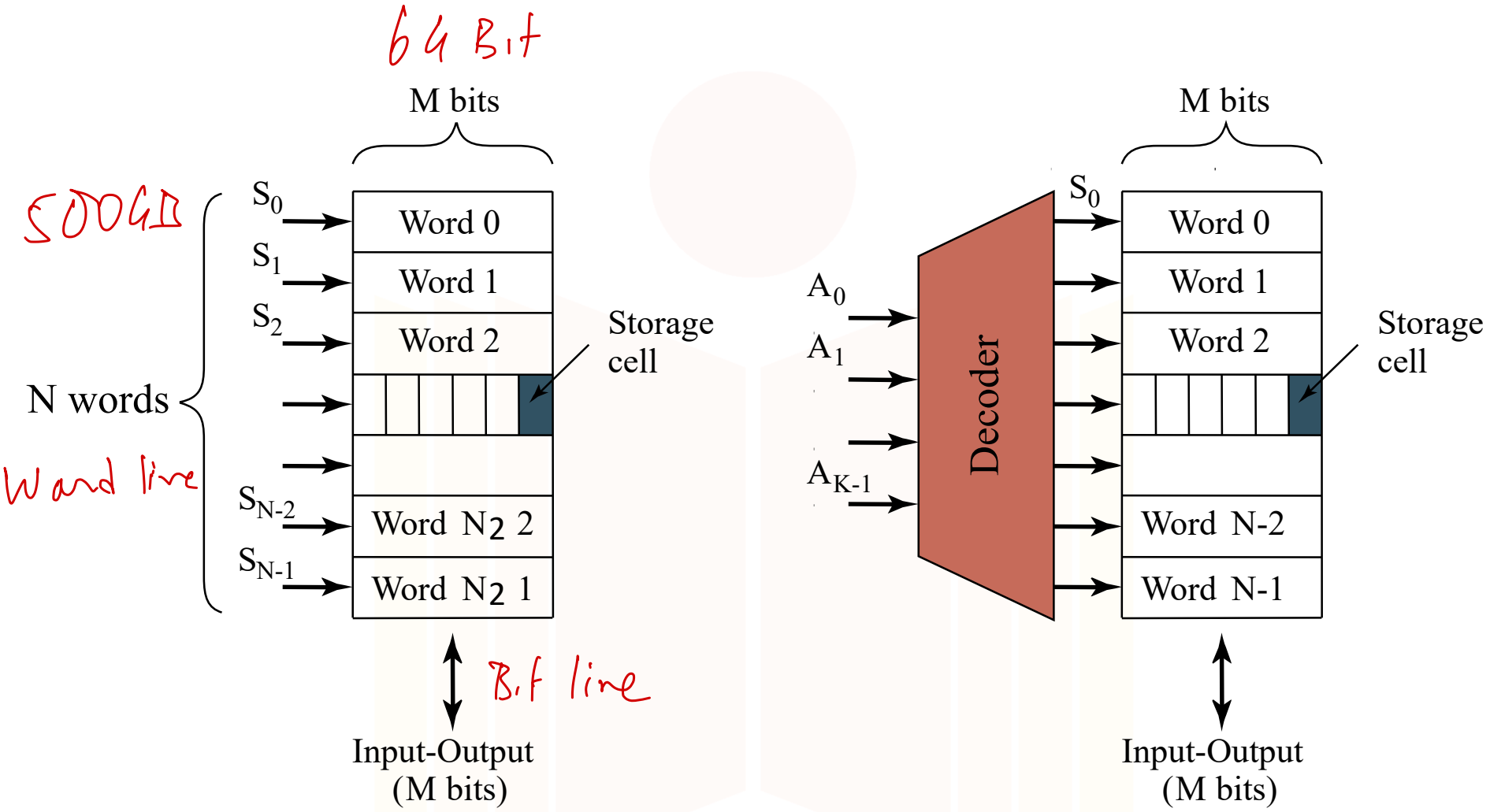
Memory Classification

- Size
- Timing – Read access time, write access time
- Function – Read only, RWM, CAM

Memory Timing: Definitions



Memory Architecture: Decoders



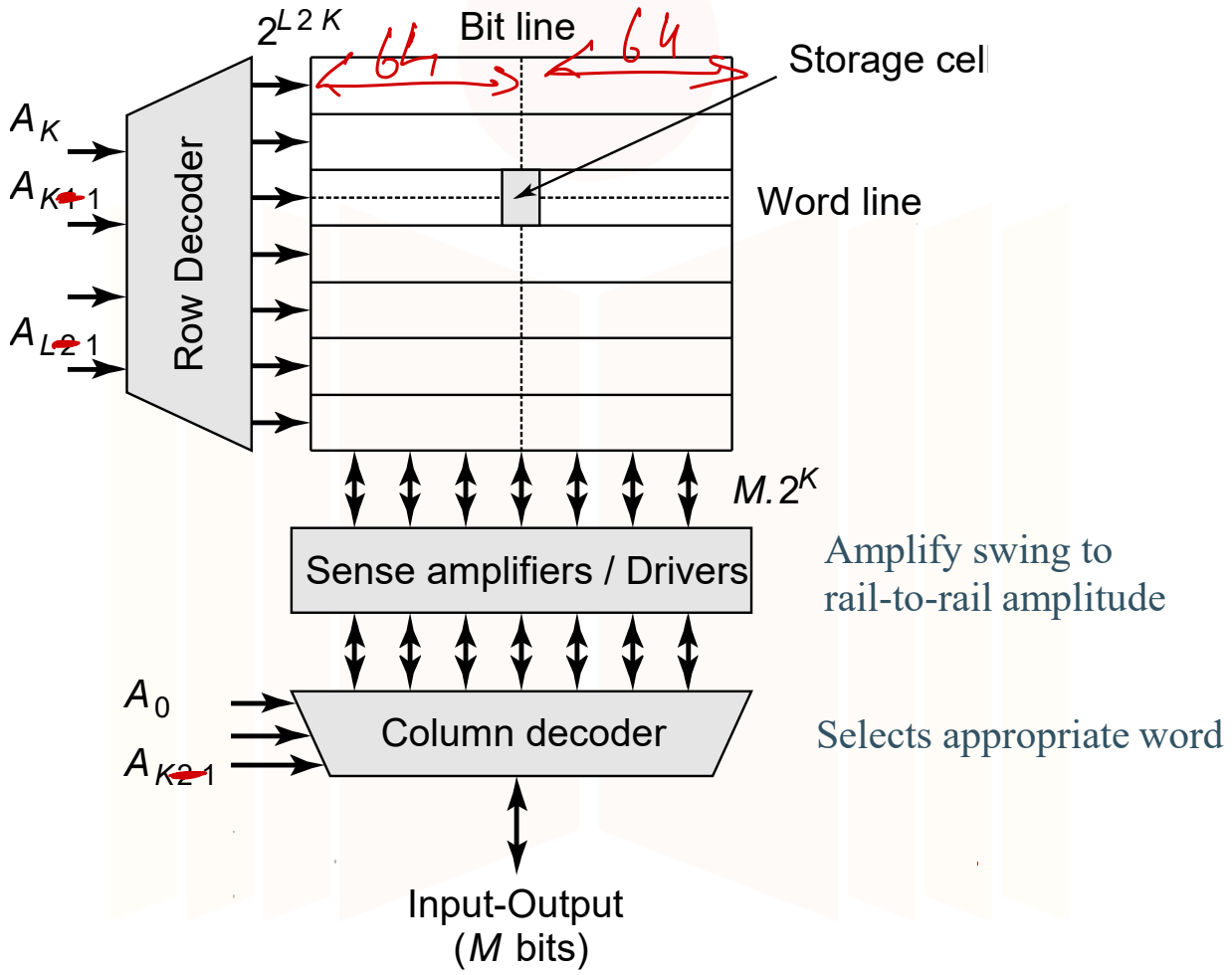
Intuitive architecture for N x M memory
Too many select signals:
N words == N select signals

Decoder reduces the number of select signals

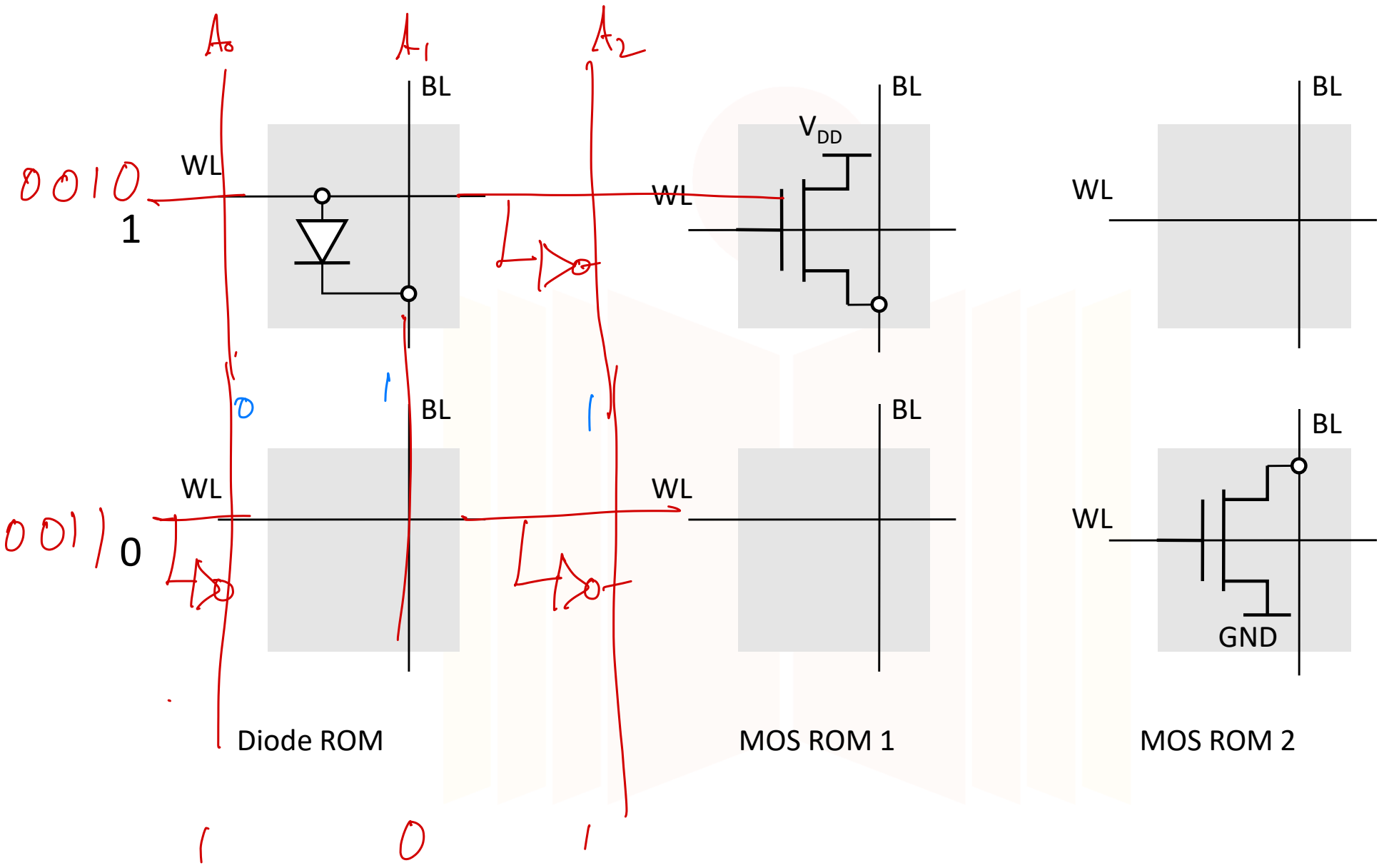
$$K = \log_2 N$$

Array-Structured Memory Architecture

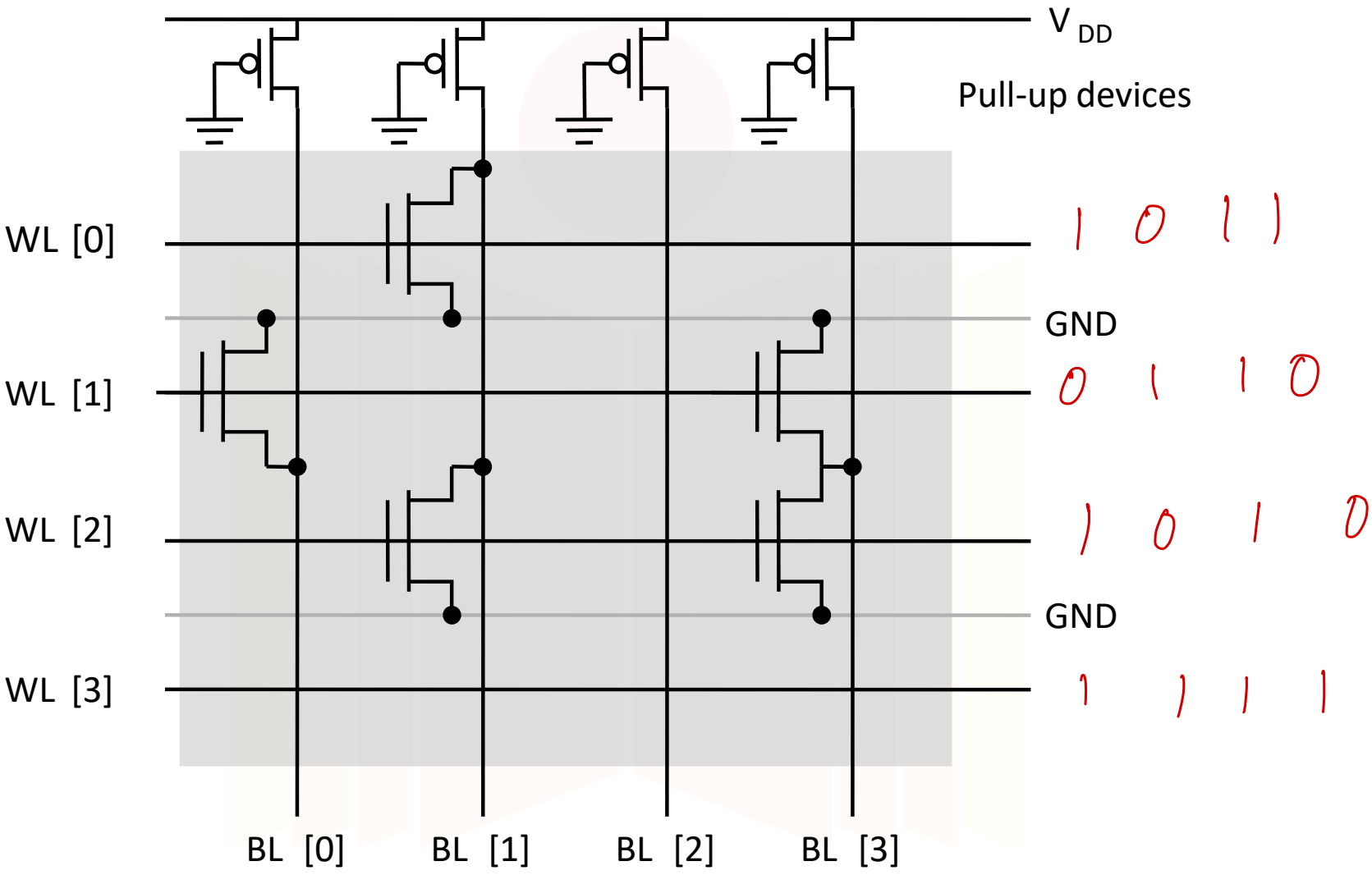
Problem: ASPECT RATIO or HEIGHT >> WIDTH



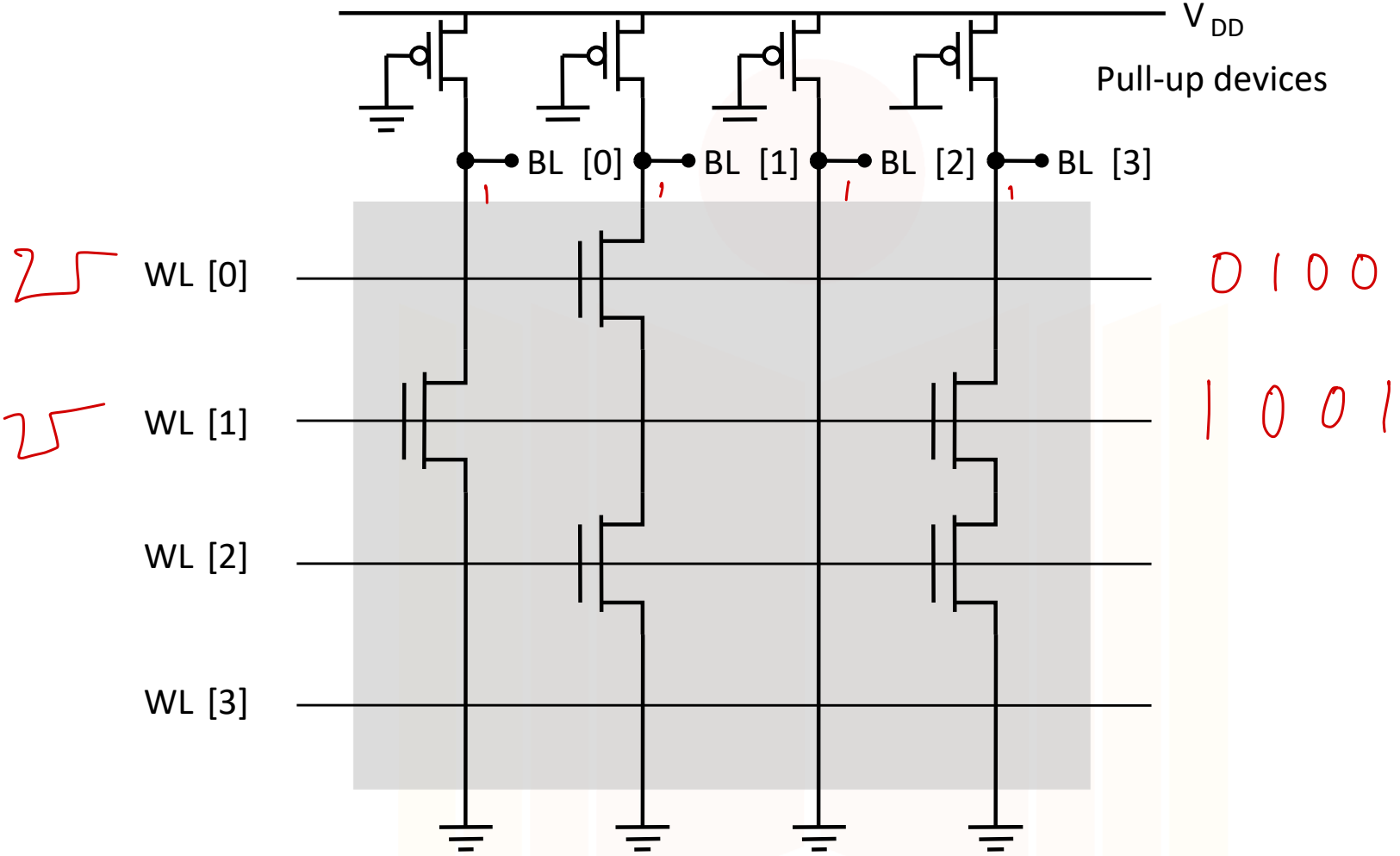
Read-Only Memory Cells



MOS NOR ROM

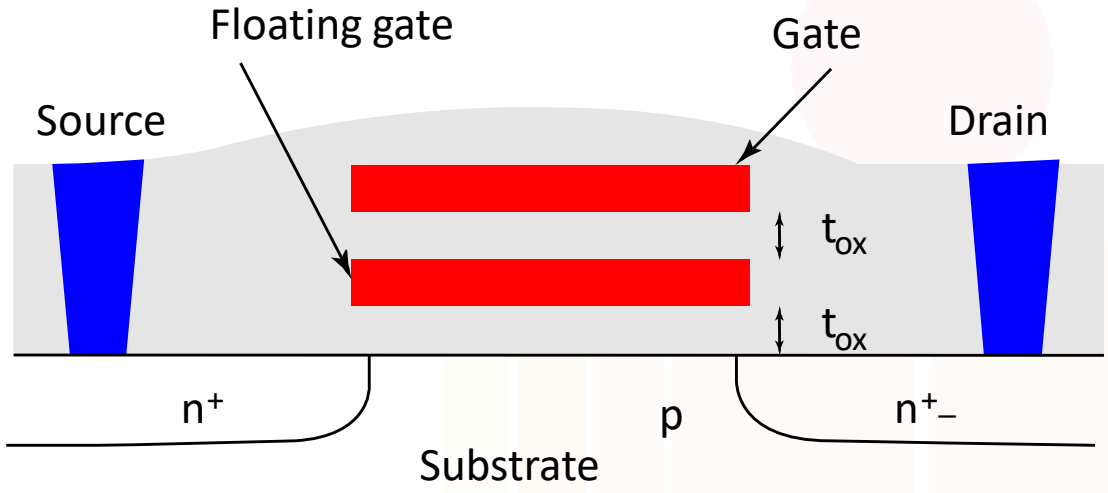

V DD
Pull-up devices
WL [0]
WL [1]
WL [2]
WL [3]
GND
GND
BL [0]
BL [1]
BL [2]
BL [3]
1 0 1 1
0 1 1 0
1 0 1 0
1 1 1 1

MOS NAND ROM

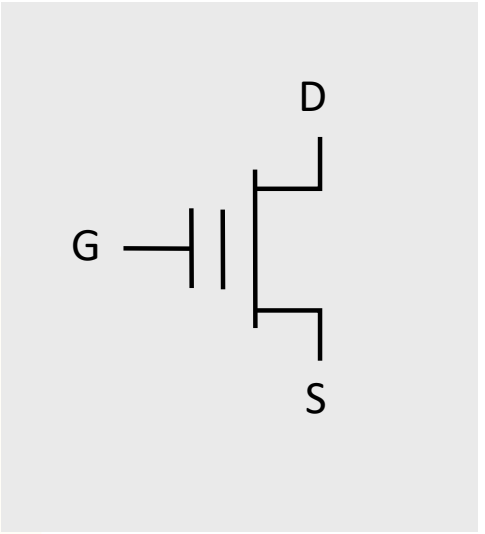


All word lines high by default with exception of selected row

Non-Volatile Memories

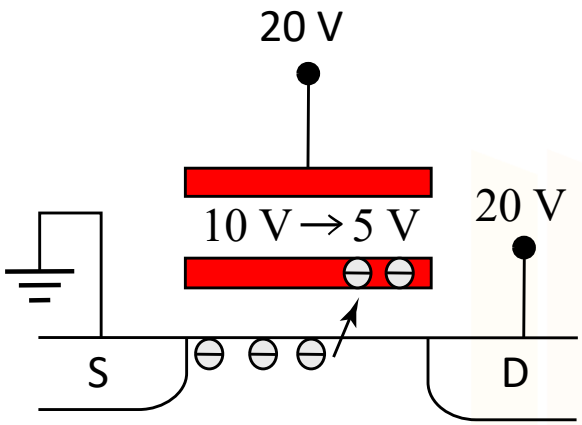


Device cross-section

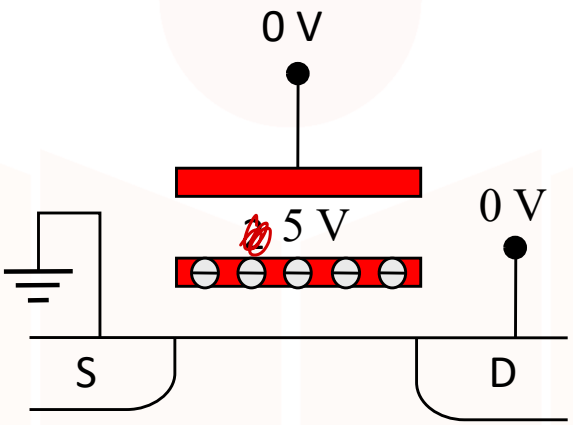


Schematic symbol

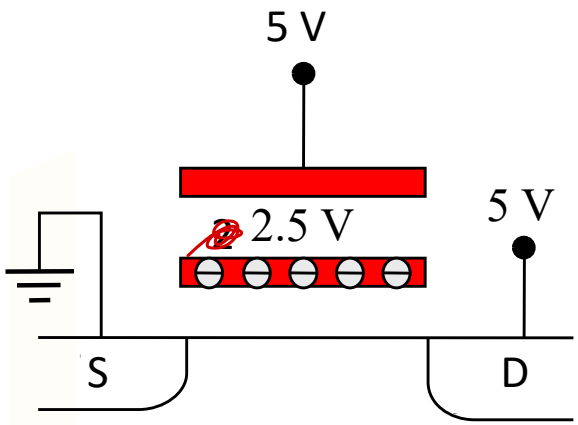
Floating-Gate Transistor Programming



Avalanche injection

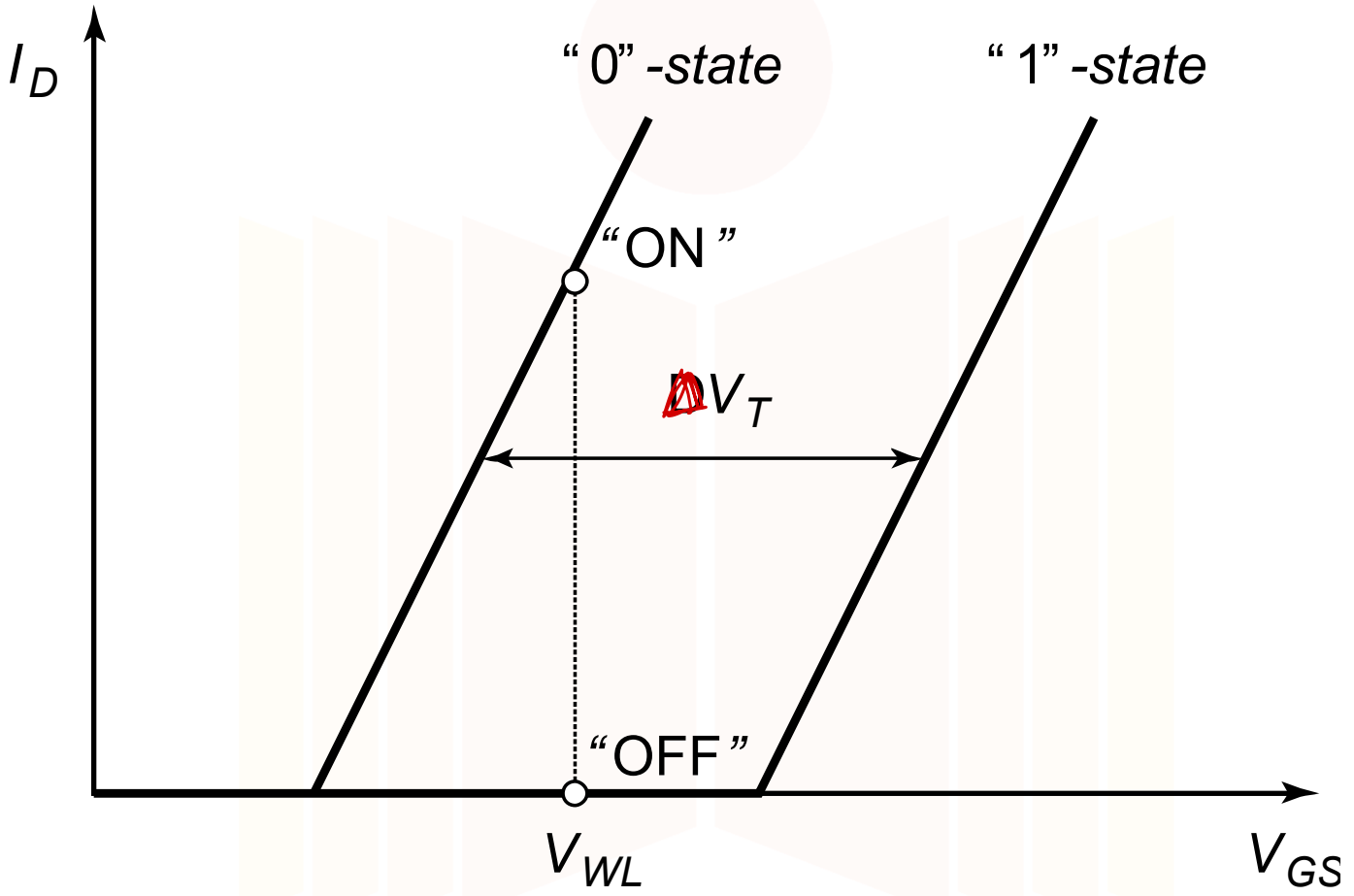


Removing programming voltage leaves charge trapped

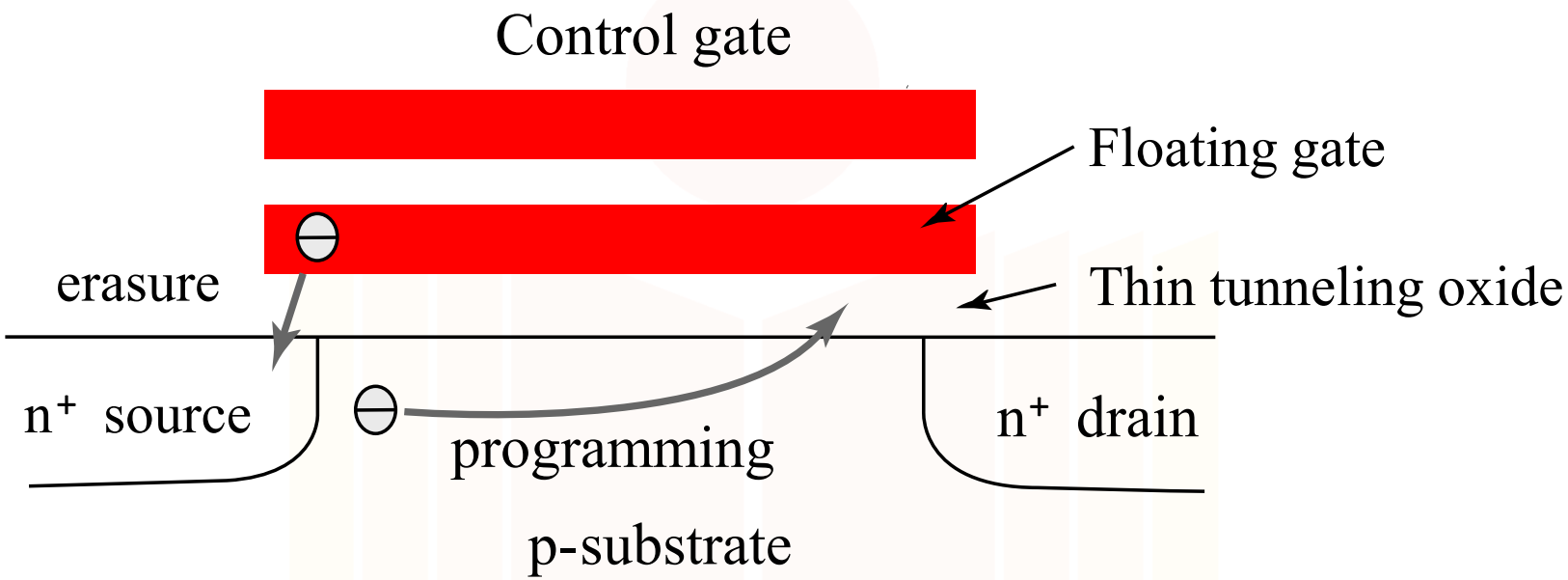


Programming results in higher V_T.

A “Programmable-Threshold” Transistor

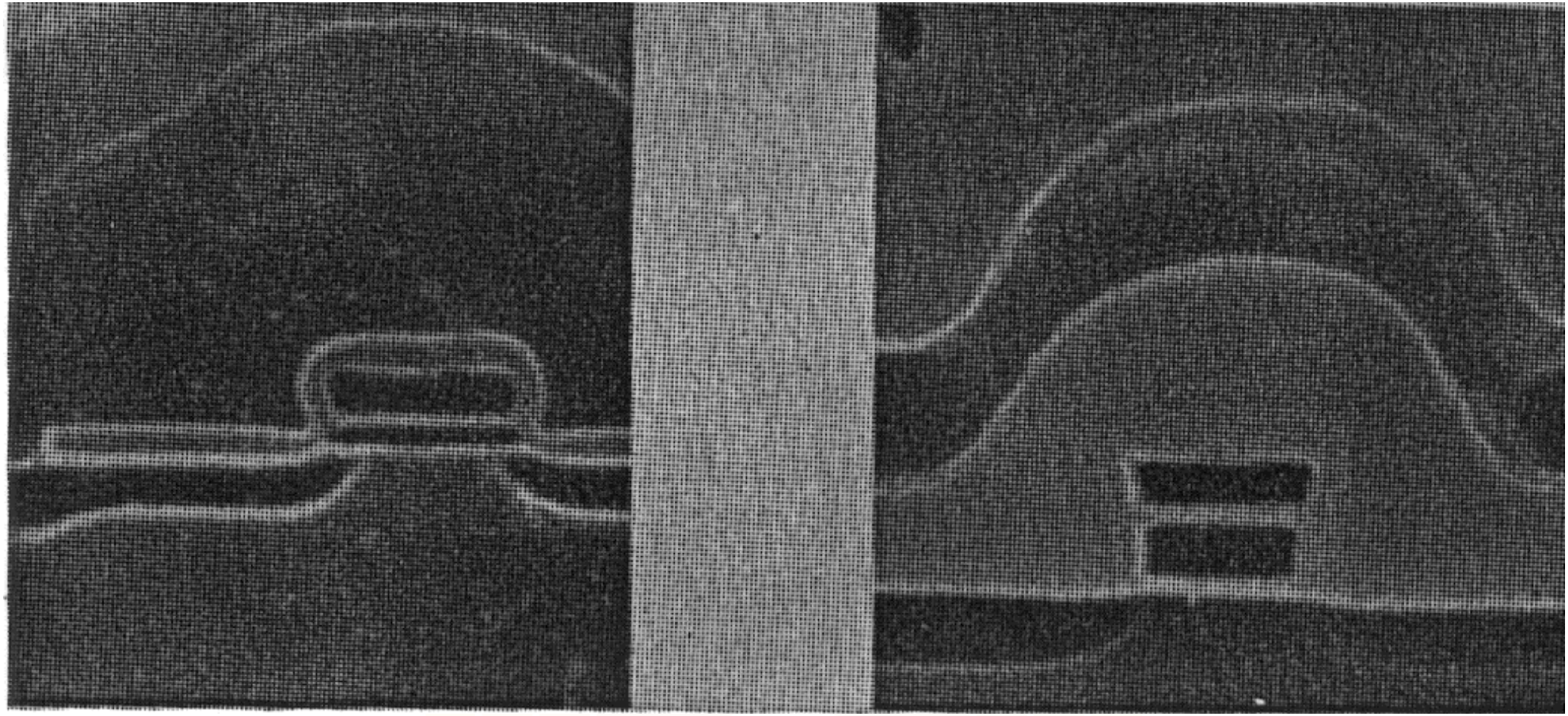


Flash EEPROM



Many other options …

Cross-sections of NVM cells



Flash

Courtesy Intel

EPROM