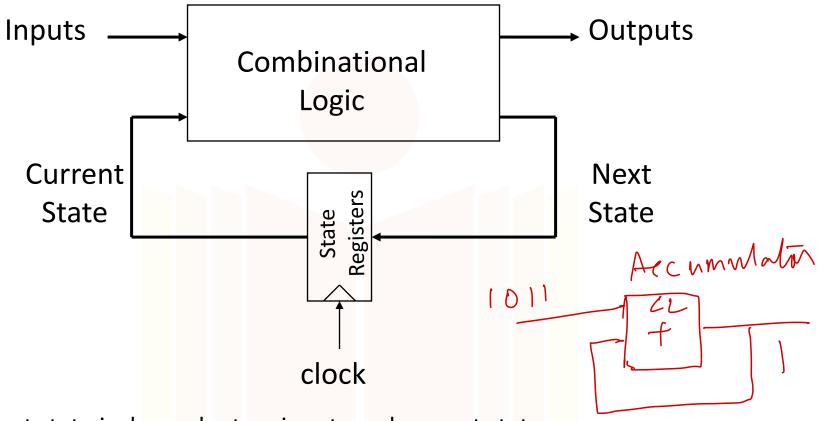
# **Introduction to VLSI Design**

Lecture 20 – Sequential circuits

Material primarily form textbook and lecture slides for Rabaey et. al. Digital Integrated Circuits, 2nd Edition (2002) and other online resources

### **Sequential Circuits**



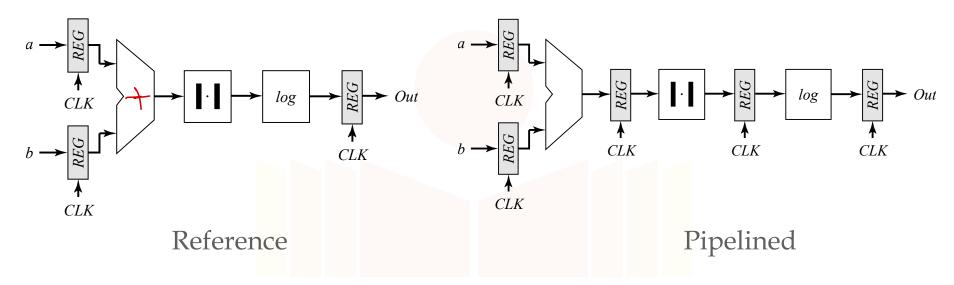
- Output state is dependent on inputs and current state
- □ Why do we need registers in feedback loop?
  - Know when output is ready, and next input can be applied
  - Avoid race conditions

# Why Sequential Logic?

IF	ID	EX	MEM	WB				
↓ <i>i</i>	IF	ID	EX	MEM	WB			
<i>t</i> →		IF	ID	EX	MEM	WB		
			IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB

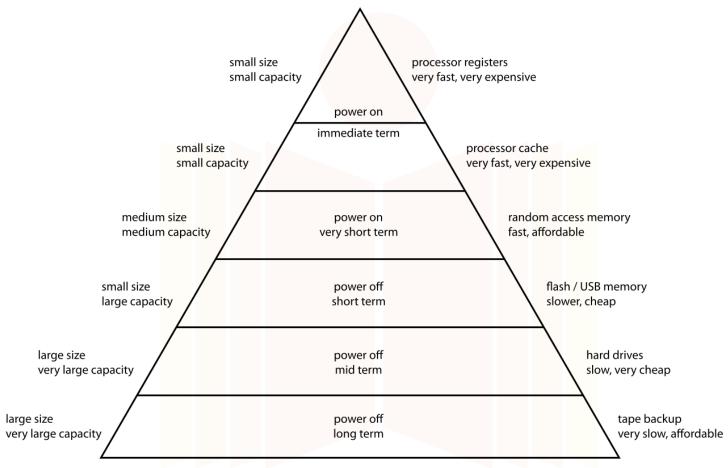
Basic five-stage pipeline in a RISC machine (IF = Instruction Fetch, ID = Instruction Decode, EX = Execute, MEM = Memory access, WB = Register write back).

# **Pipelining**



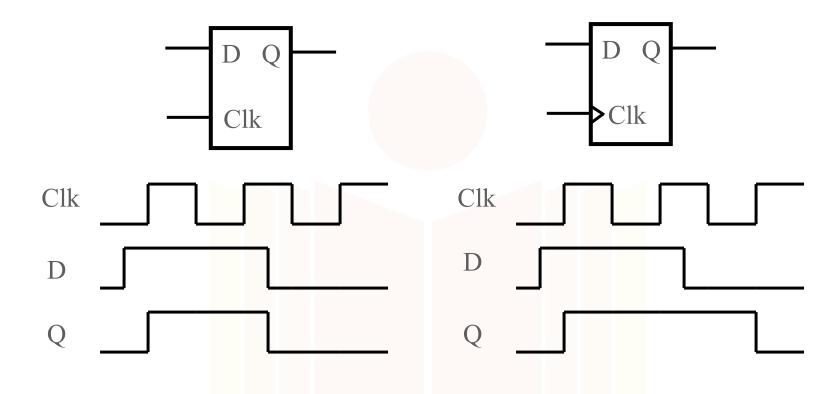
Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$ a_1 + b_1 $	
3	$a_3 + b_3$	$ a_2 + b_2 $	$\log( a_1 + b_1 )$
4	$a_4 + b_4$	$ a_3 + b_3 $	$\log( a_2 + b_2 )$
5	$a_5 + b_5$	$ a_4 + b_4 $	$\log( a_3 + b_3 )$

## **Memory Hierarchy**

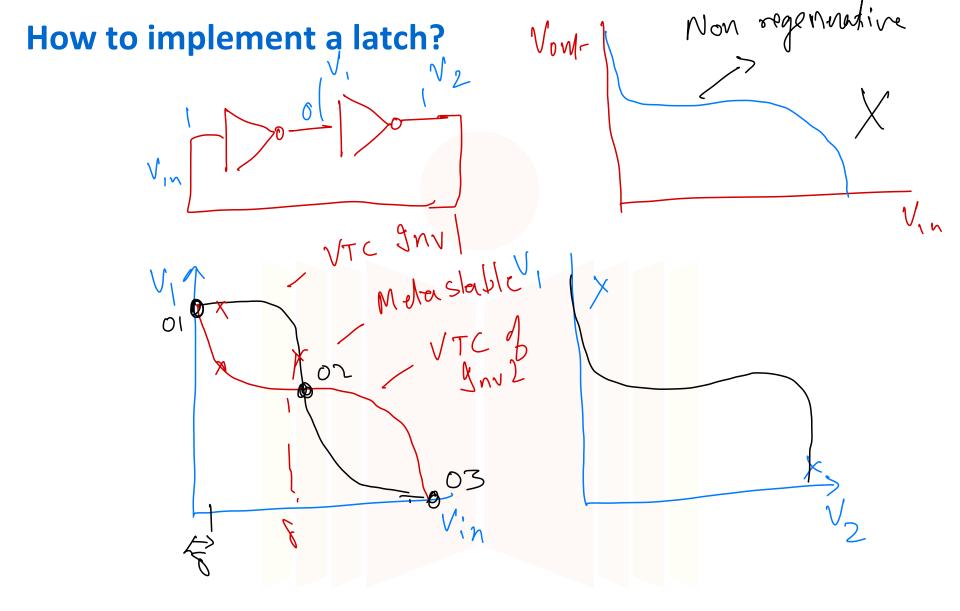


https://en.wikipedia.org/wiki/Memory\_hierarchy

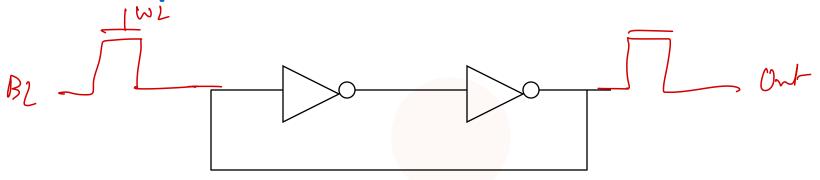
# Latch Vs Flipflop/Register



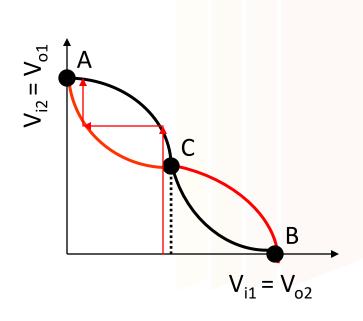
- □ Latch level sensitive
  - Transparent/Hold when CLK is high/Low
- □ Flipflop edge triggered
  - Samples input only when edge occurs



### How to implement a latch?

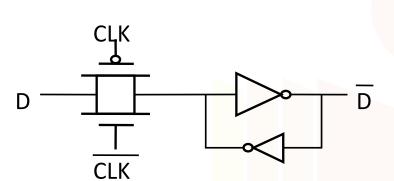


#### cascaded inverters

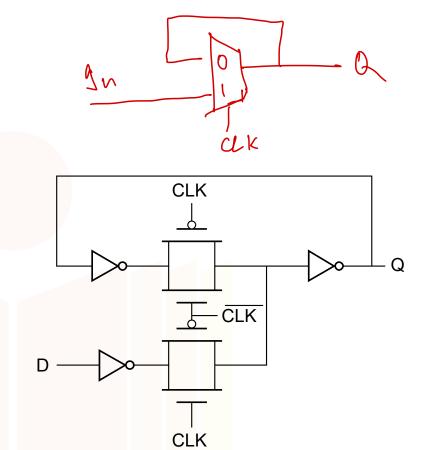


Two cascaded inverters show bistable operation. If the gain in the transient region is larger than 1, only A and B are stable operation points. C is a metastable operation point.

# Implementations of a latch



Forcing a state

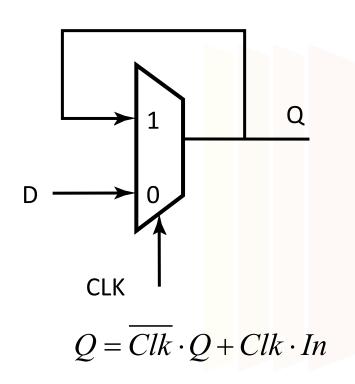


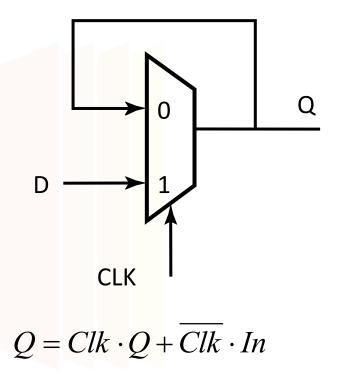
Converting a MUX into a latch

#### **Mux based Latches**

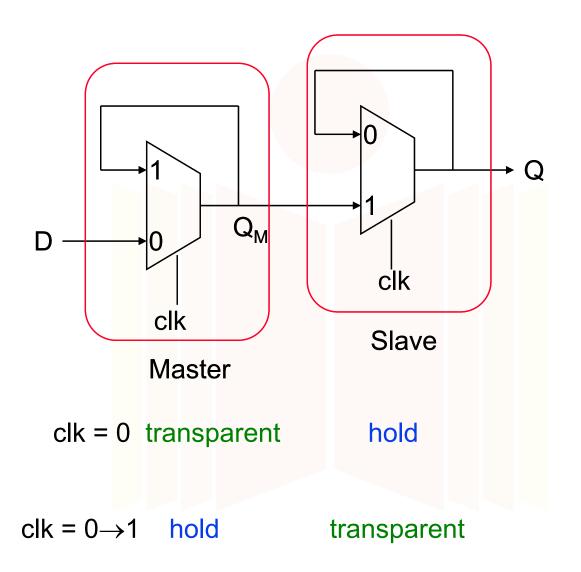
Negative latch (transparent when CLK= 0)

Positive latch (transparent when CLK= 1)





# **Edge triggered Flipflop**



# **Master Slave Flipflop Implementation**

