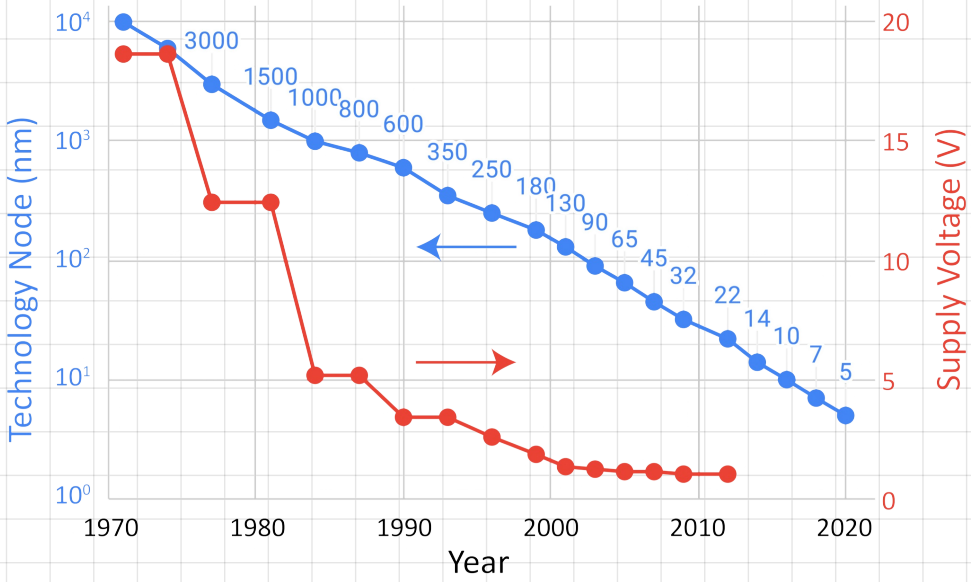
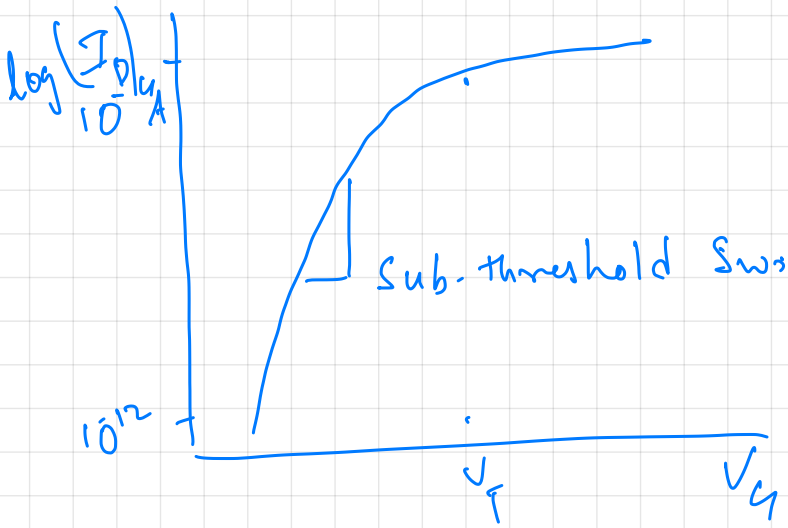
VLSI Design - Lecture 11

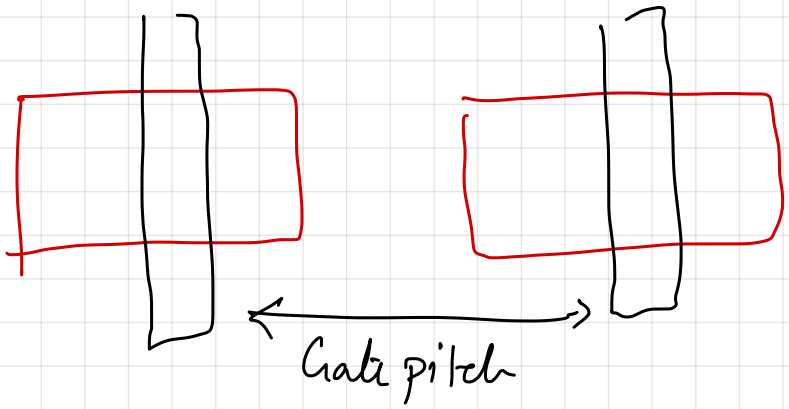
30th Aug 2022



90 - 2003
65 2005
45 2007
32 2009



90-100 mV/decade



MOSFET Scaling

- Proposed by Dennard *et. al.* in 1974
- Reduce vertical and lateral dimensions by α
- Reduce supply and threshold voltages by α
- Increase doping concentrations by α

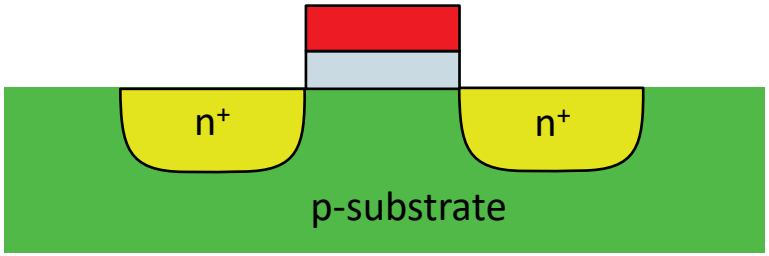
$L \rightarrow \alpha L \quad \alpha = 0.7$

$L \rightarrow 0.7L \quad W \rightarrow 0.7W$

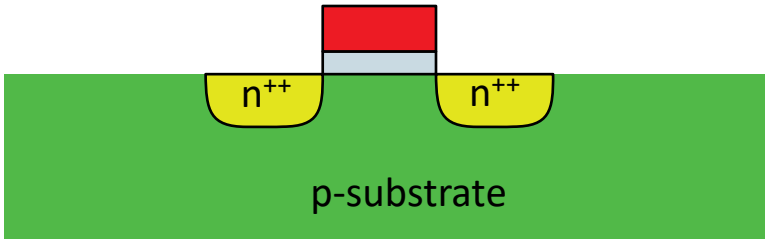
$t_{ox} \rightarrow 0.7 t_{ox}$

$V_{DD} \rightarrow 0.7 V_{DD} \quad V_t \rightarrow 0.7 V_t$

$N_{sub} \rightarrow \frac{N_{sub}}{\alpha}$



Original MOSFET



Scaled MOSFET

Scaling classical MOSFETs

Lateral and vertical dimensions reduce by 30% (W = 0.7, L = 0.7 and T_{ox}= 0.7)

Supply and threshold voltages reduced by 30% (V_{DD} = 0.7 and V_T = 0.7)

- ~~Die area~~ MOSFET $W \times L \rightarrow$ 50% reduction in area
- Total gate Capacitance $\frac{\epsilon_{ox}}{t_{ox}} W \times L$ $\frac{0.7 \times 0.7}{0.7}$ 30% ↓
- Gate Capacitance/unit area $\frac{\epsilon_{ox}}{t_{ox}} = \frac{1}{0.7}$ 40% ↑
- Current $I = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$ $\frac{1}{0.7} \times 0.7^2 = 30\%$ ↓
- Delay in circuit $t_d = \frac{CV}{I} : \frac{0.7 \times 0.7}{0.7} = 0.7$ 30% ↓
- Power dissipation $LCV^2f = \frac{0.7 \times 0.7^2}{0.7}$ 50% ↓

$P_{Tot} = P_{Static} + P_{Dynamic} + P_{direct\ path}$

$P_{Static} \rightarrow V_{DD} \times I_{Off}$

pW

Usually not significant

$P_{Dynamic} \rightarrow CV^2f$

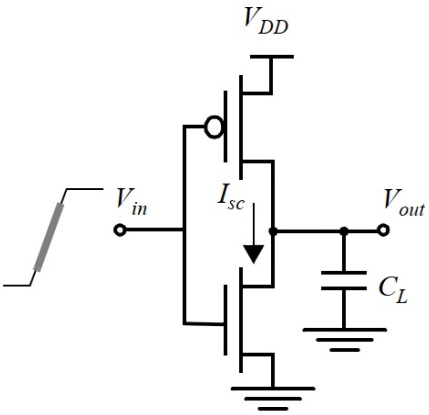
$6fF \times 2.5^2 \times 10^9$

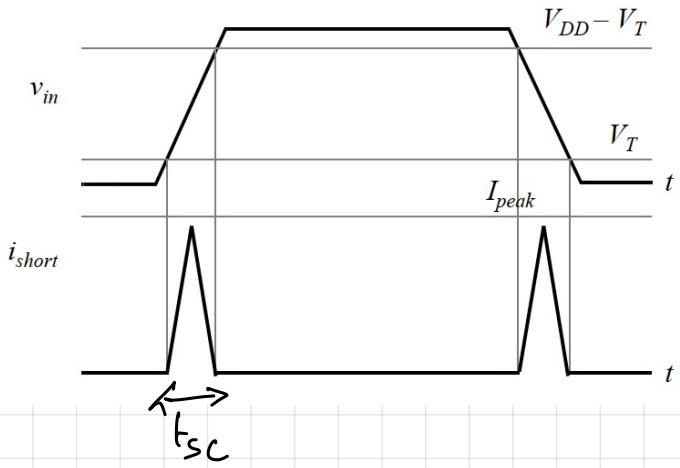
$\sim 37\ \mu W$

$37W$ (1 million gates)

Dominant source heat

$P_{direct\ path}$ → Direct short circuit current during switching

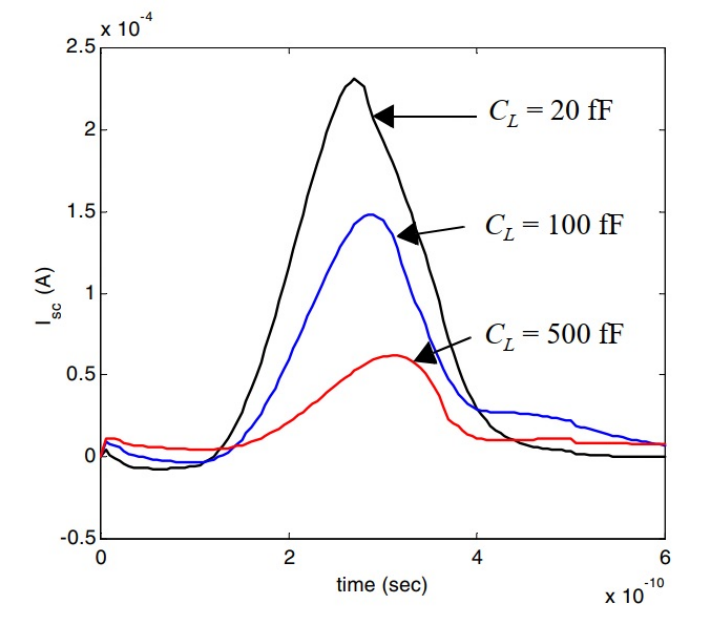


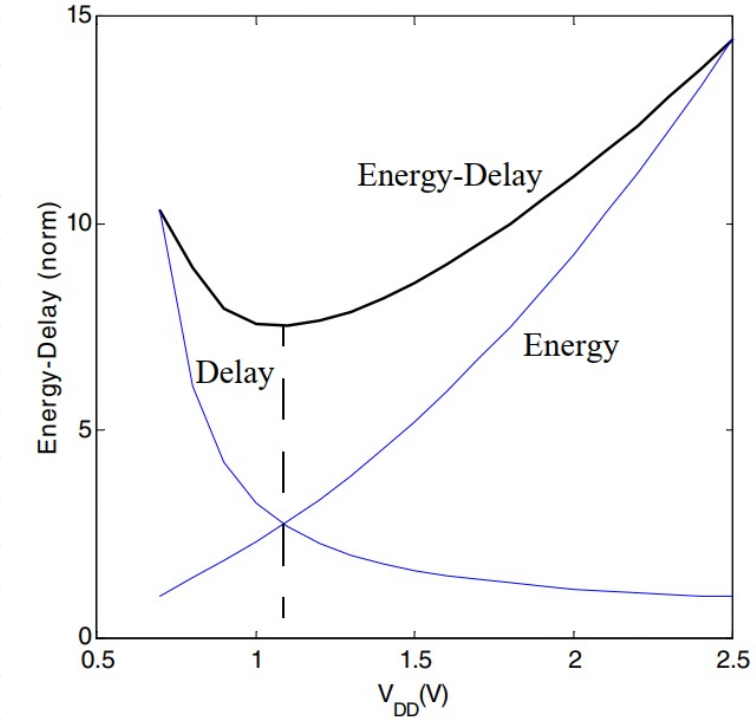


$P_{sp} = V_{DD} \times I_{sc}\ t_{sc} \cdot f$

$= 2.5 \times 100 \times 10^{-6} \times \frac{100ps \times}{1ns}$

$= 25\ \mu W$


x 10^-4
2.5
2
1.5
1
0.5
0
-0.5
I_sc (A)
C_L = 20 fF
C_L = 100 fF
C_L = 500 fF
0
2
4
6
time (sec)
x 10^-10


15
10
5
0
Energy-Delay (norm)
Energy-Delay
Energy
Delay
0.5
1
1.5
2
2.5
V_DD(V)