Analog Lab
Experiment 1: Inverter Characteristics

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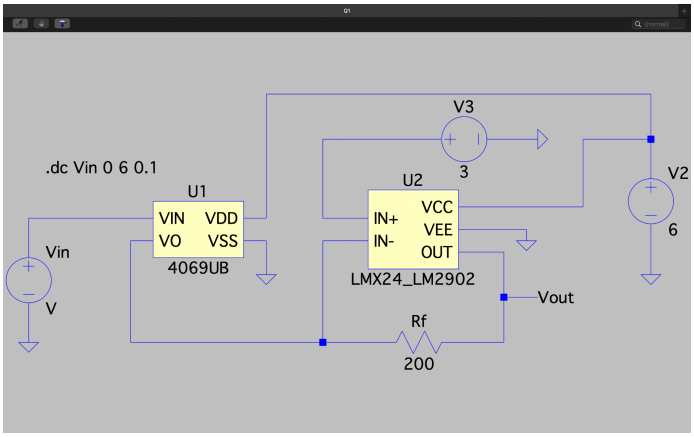
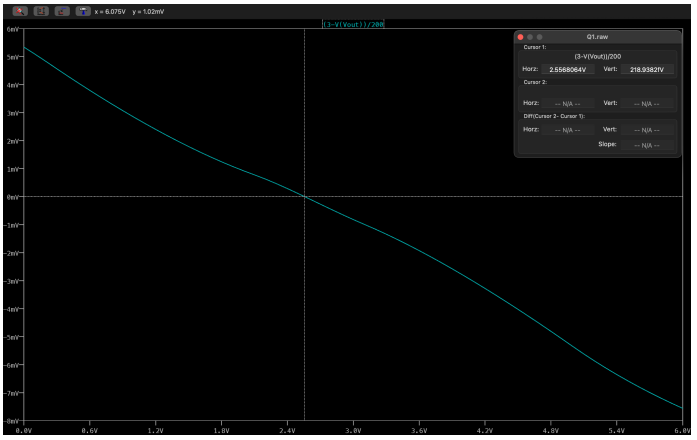
1. CMOS Inverter as Transconductor

1.1 Large Signal plot

Circuit used -



DC sweep gives -



We know that

$$V_{in-} = V_{in+} = \frac{V_{DD}}{2}$$

So writing KCL we get that

$$R_f * I_{out} = \frac{V_{DD}}{2} - V_{out}$$

Since we are advised not to use an ammeter, we can measure V_{out} and use the above equation to find out I_{out} .

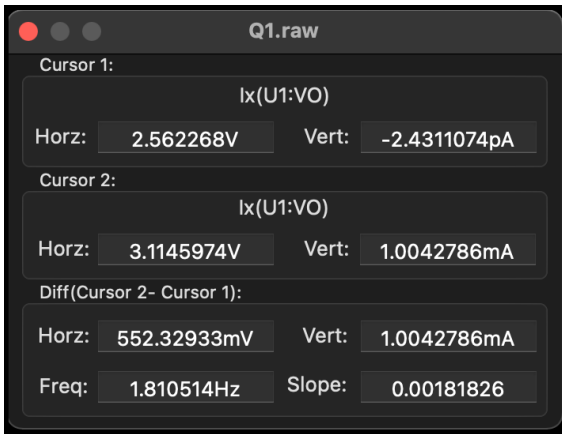
1.2 Self-Bias voltage of inverter-

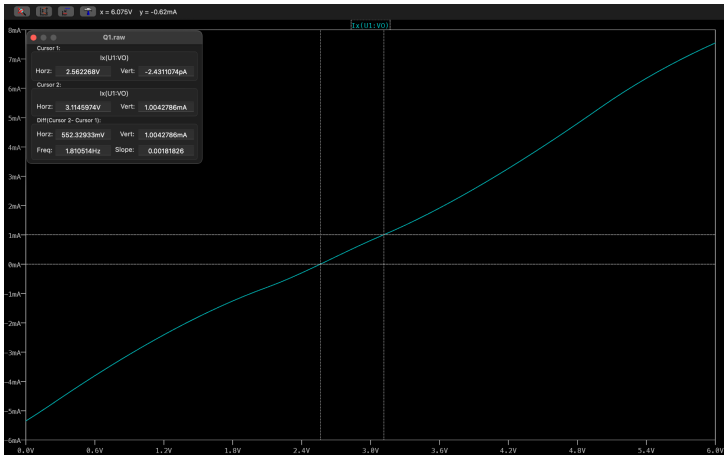
It is the input voltage (denoted as V_B) when $I_{out} = 0$. So from the graph, we get self-bias voltage V_B to be **2.5568V**.

1.3 Transconductance of inverter-

Transconductance is the small change in current divided by the small change in voltage around V_B . So it can be found by obtaining the slope of I_{out} vs V_{in} graph.

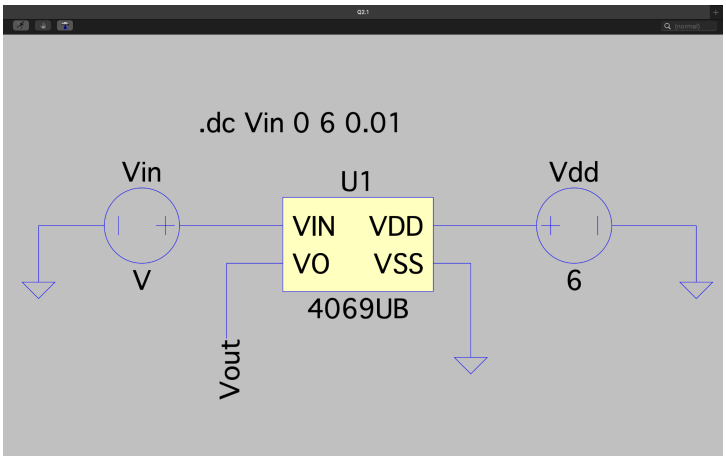
From the graph, we get $\mathbf{g_m = 1.81826\ mmho.}$



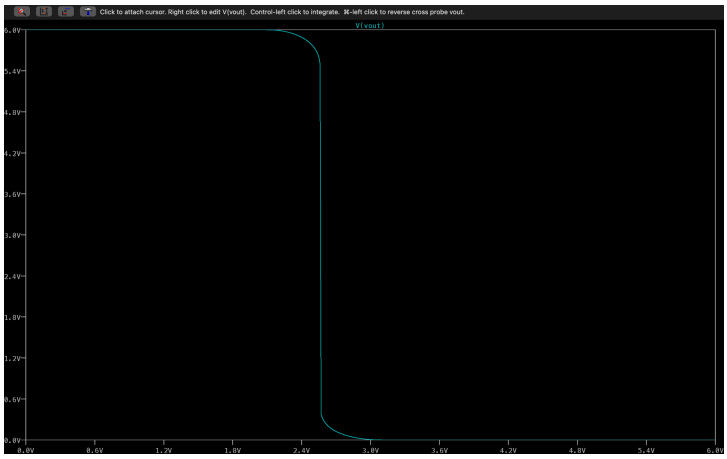


2.1 Large signal V_{out} vs V_{in} of CMOS inverter-

Circuit used-

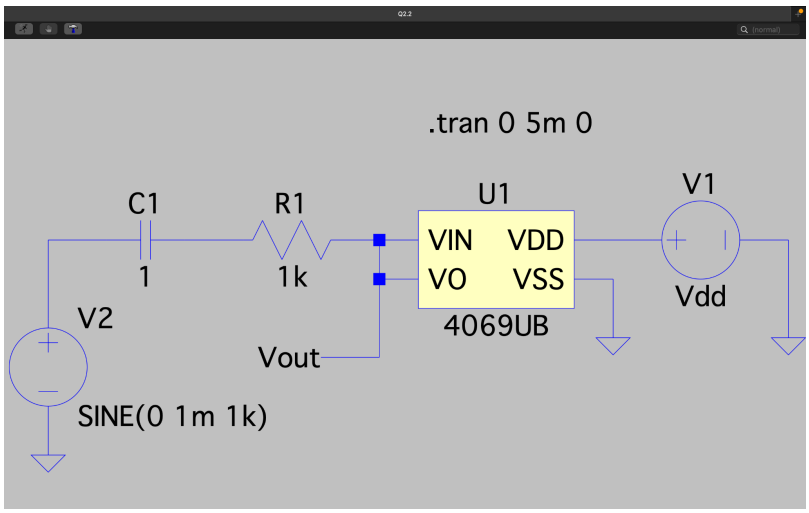


DC Sweep gives-



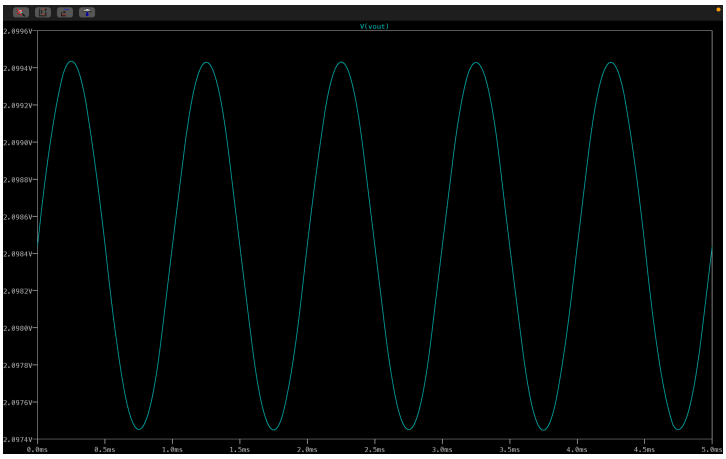
2.2 Small-Signal resistance using Self-Biased inverter-

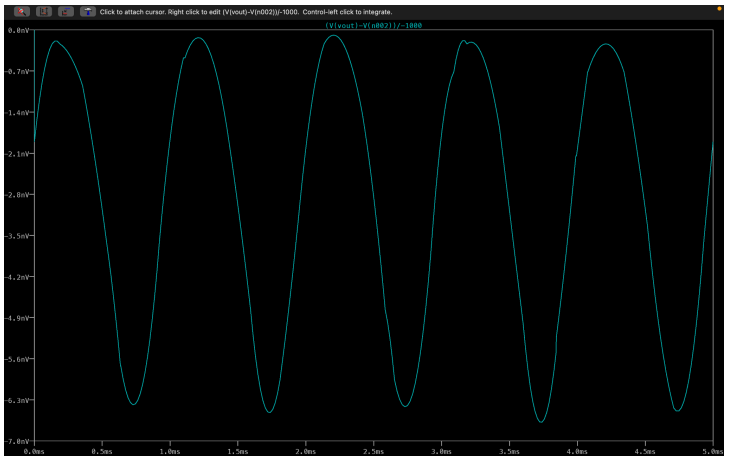
Circuit used-



Since we don't have an ammeter in the lab, we measure the voltages across the resistor (V_{out} and V_{n002}) and divide by 1 kΩ to obtain I_{out} (as from KCL at V_{out} we get $I_{in} = I_{out}$).

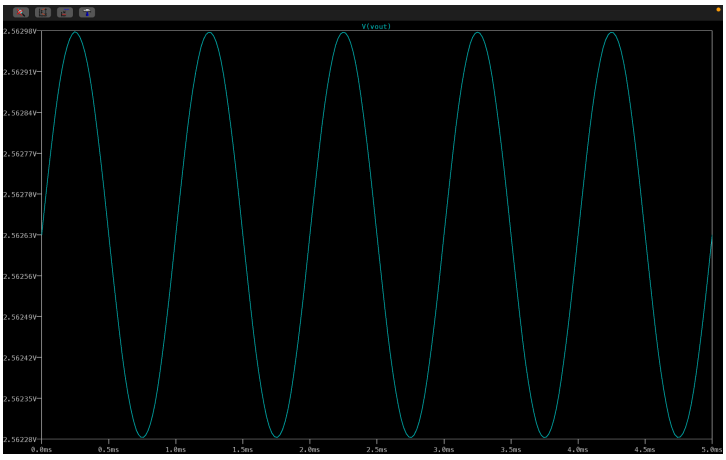
Small signal analysis at $V_{DD} = 5V$ gives-

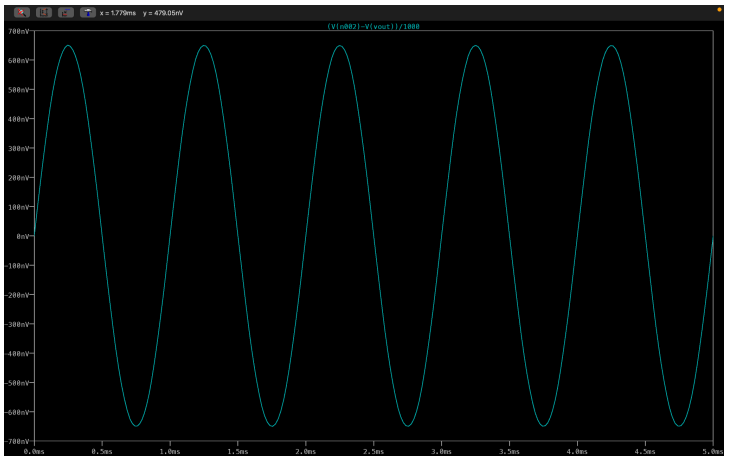




$$\text{Small signal resistance} = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{1.9812825\ mV}{6.3282885\ nA} = 313.08\ k\Omega$$

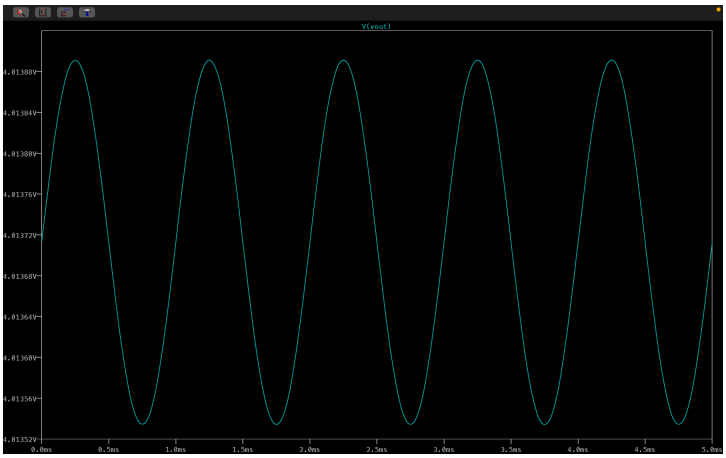
Small signal analysis at $V_{DD} = 6V$ gives-

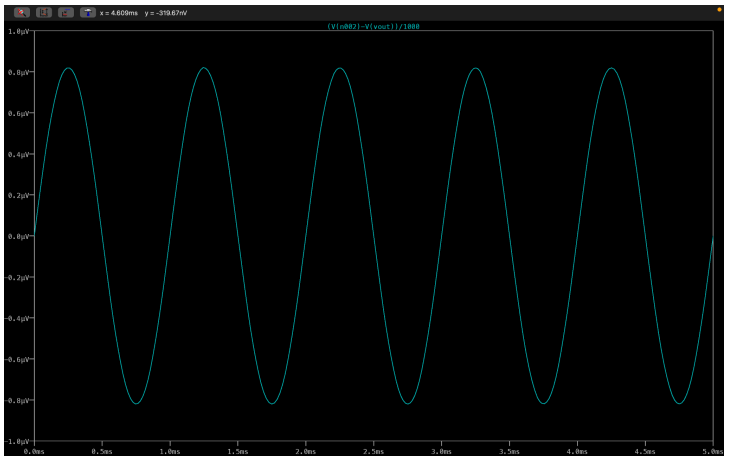




$$\text{Small signal resistance} = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{694.92356\ \mu V}{1.3000657\ \mu A} = 534.53\Omega$$

Small signal analysis at $V_{DD} = 9V$ gives-





$$\text{Small signal resistance} = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{356.61039\ \mu V}{1.6389857\ \mu A} = 217.58\Omega$$

Unusual observation-

The small signal resistance is unusually high for V_{DD}=5V. Also the CMOS characteristics curve is very sharp as well, so we can conclude that the time for which both MOSFETS will be in saturation is very less. So the CMOS inverter is not a good choice as a transconductor but a very good choice as a logical inverter.

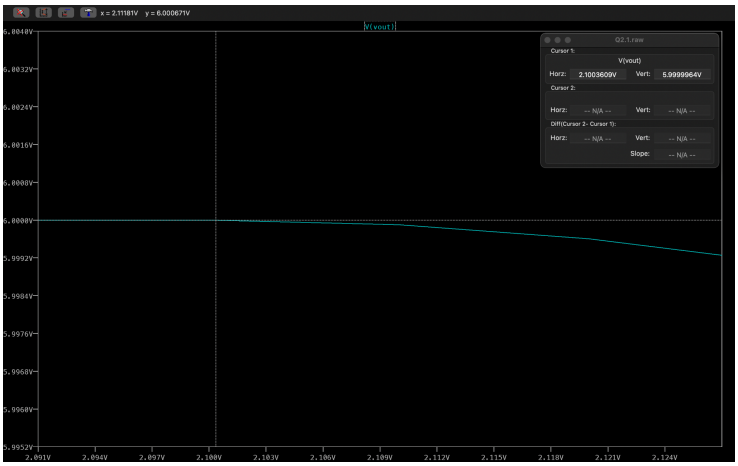
3. Finding the parameters of self-biased inverter, n-MOS and p-MOS

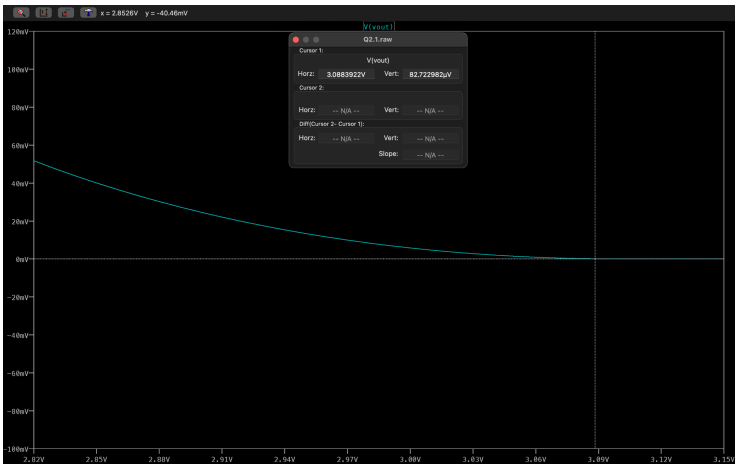
3.1 g_m of the self-biased inverter-

The transconductance g_m has already been found in 1.3, i.e. g_m =1.81826 mmho

3.2 V_T of the MOSFETs-

Before finding r_o and β we need to find V_{TH} of p-MOS and n-MOS transistors. We can do that graphically by using the same circuit from 2.1





We can find V_{THn} from the graph when the output voltage of the CMOS transistor starts reducing from V_{DD} to 0 (i.e. when n-MOS starts conducting). So from the first plot we get-

$$V_{THn} = 2.1V$$

We can find V_{THp} from the graph when the output voltage of the CMOS transistor almost reaches 0V (i.e. just before p-MOS stops conducting). So from the first plot we get-

$$V_{DD} - |V_{THp}| = 3.1V \quad => \quad V_{THp} = -2.9V$$

3.3 β values of the MOSFETs-

Also from KCL in the CMOS, we get-

$$I_{out} = I_{DSp} - I_{DSn}$$

So, β

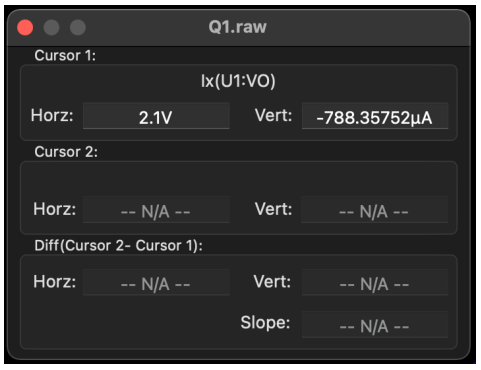
$$I_{out} = \frac{\beta_p}{2}(V_{SG} - |V_{THp}|)^2(1 + \lambda_p V_{SD}) - \frac{\beta_n}{2}(V_{GS} - V_{THn})^2(1 + \lambda_n V_{DS})$$

We know that $\lambda_p = \lambda_n = 1.87 \times 10^{-3}$(from the code) and using $I_{out} = 0 \ at \ V_{in} = V_{out} = V_B$

from 1.2, we get the ratio of β values as-

$$\frac{\beta_p}{\beta_n} = \frac{(2.5568 - 2.1)^2 \times (1 + 1.87 \times 10^{-3} \times 2.5568)}{(3.4432 - 2.9)^2 \times (1 + 1.87 \times 10^{-3} \times 3.4432)} = 0.706$$

At $V_{in} = V_{THn} = 2.1V$, we can say that $I_{DSn} = 0$. So finding out I_{out} experimentally we get-



$$788.3575 \times 10^{-6} = \frac{\beta_p}{2}(3.9 - 2.9)^2(1 + 1.87 \times 10^{-3} \times 0)$$

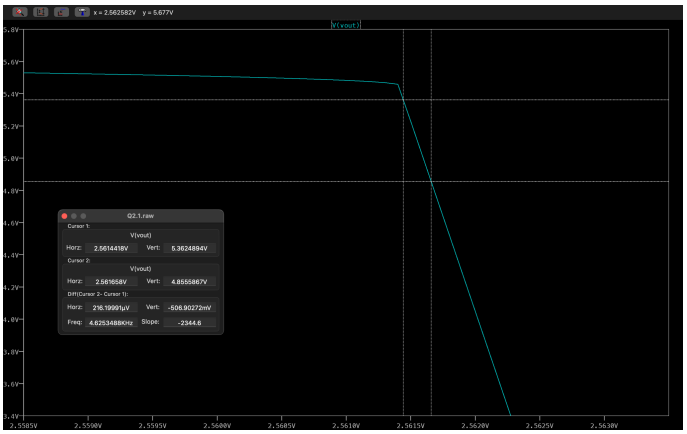
$$\beta_p = 1.58 \, mA/V^2$$

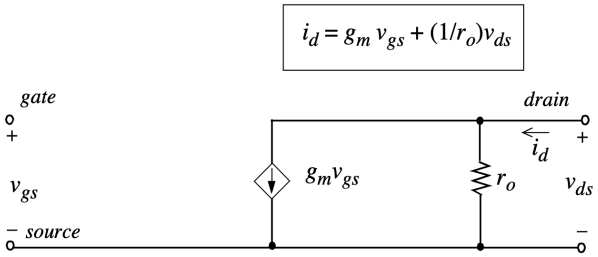
Therefore from the beta ratios, we get that

$$\beta_n = 2.24 \, mA/V^2$$

3.4 r_o of the CMOS inverter-

At the self-biased voltage of the CMOS inverter, the whole setup behaves as a transconductor and can be modeled as a VCCS in parallel with r_o .





Source webpage [link]

From the webpage at self-bias voltage,

$$\frac{\partial V_{out}}{\partial V_{in}} = -2344.6 = -r_o g_m$$

that gives $r_o = 1.289\ M\Omega$

(The UI is different as I am using a Mac)