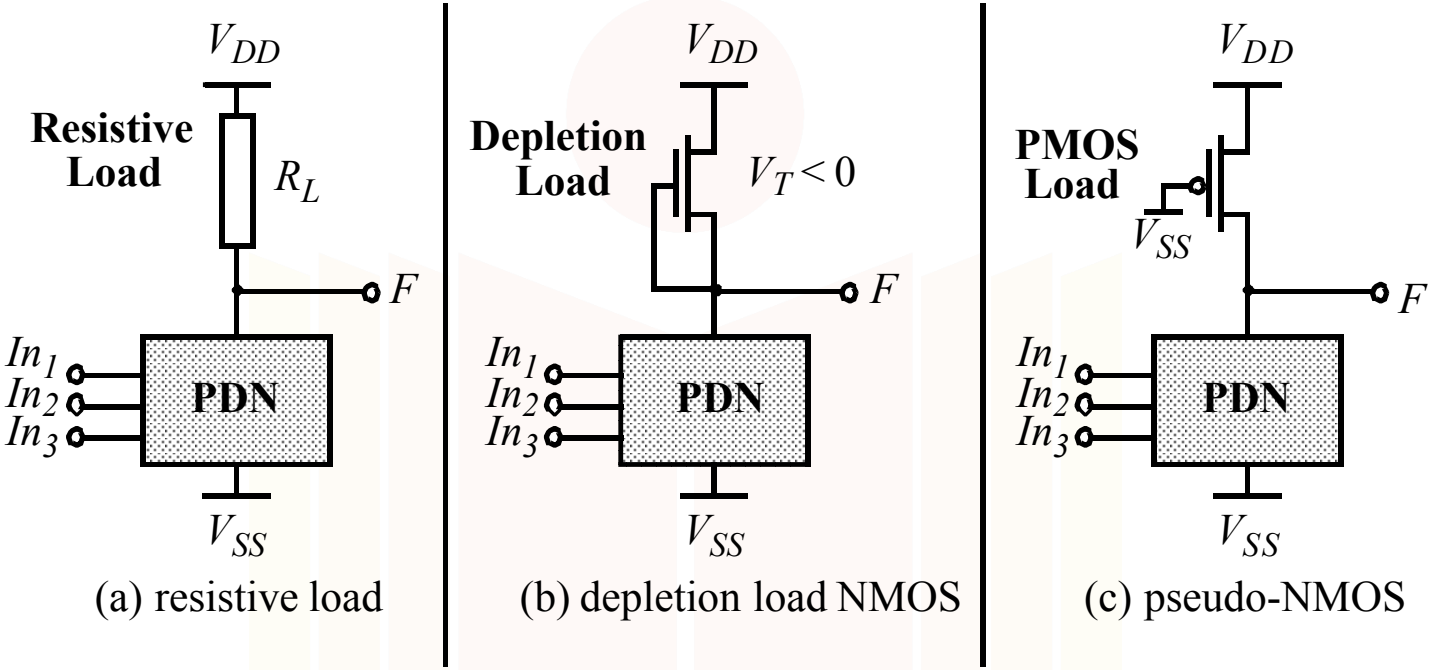
Introduction to VLSI Design

Lecture 19

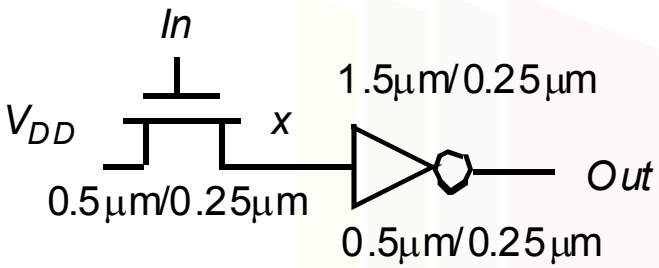
Material primarily form textbook and lecture slides for Rabaey et. al. Digital Integrated Circuits, 2nd Edition (2002) and other online resources

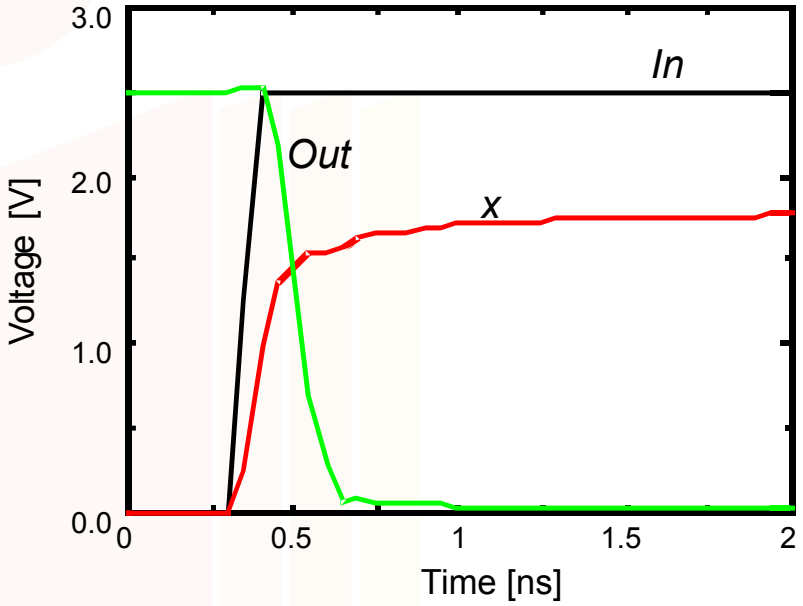
Ratioed Logic



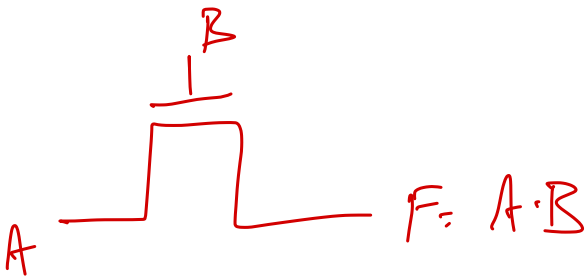
Goal: to reduce the number of devices over complementary CMOS

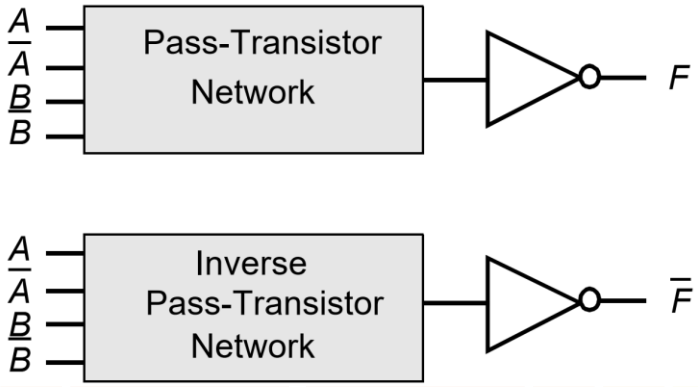
Pass Transistor Logic

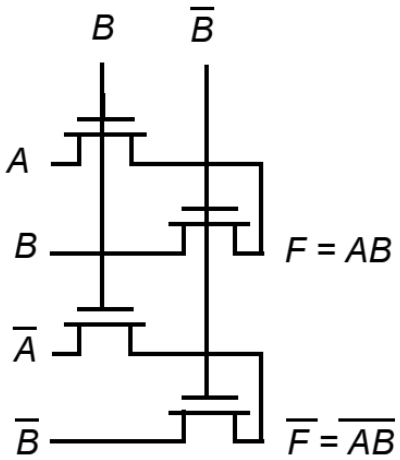




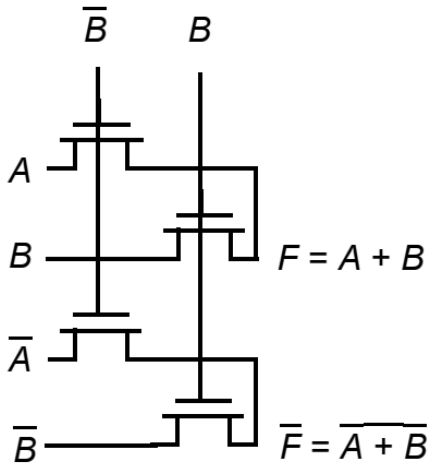
Complementary Pass Transistor Logic



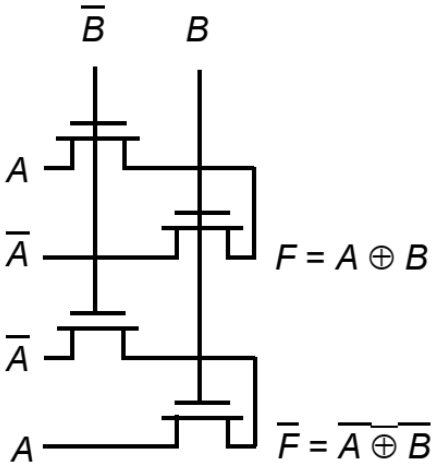




AND/NAND

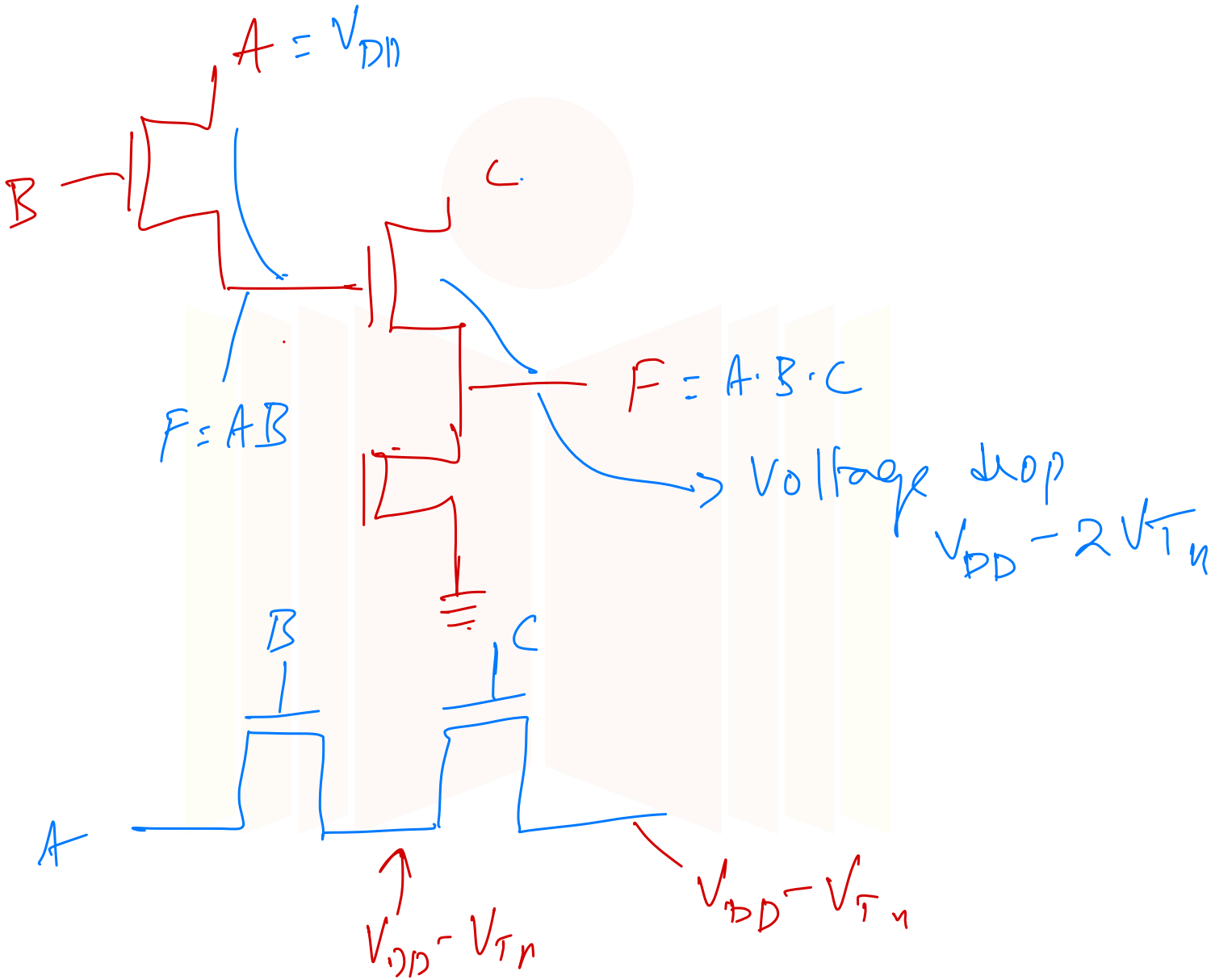


OR/NOR

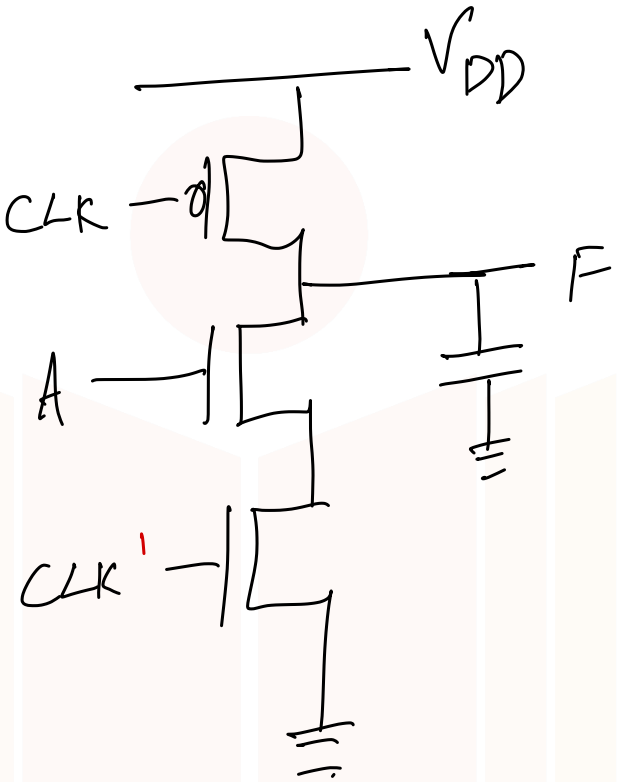


XOR/NXOR

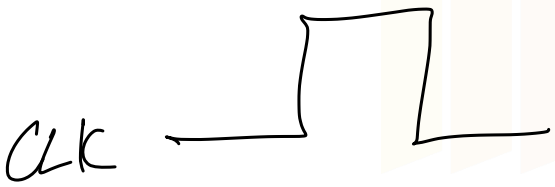
Cascading Pass Transistors



Dynamic CMOS



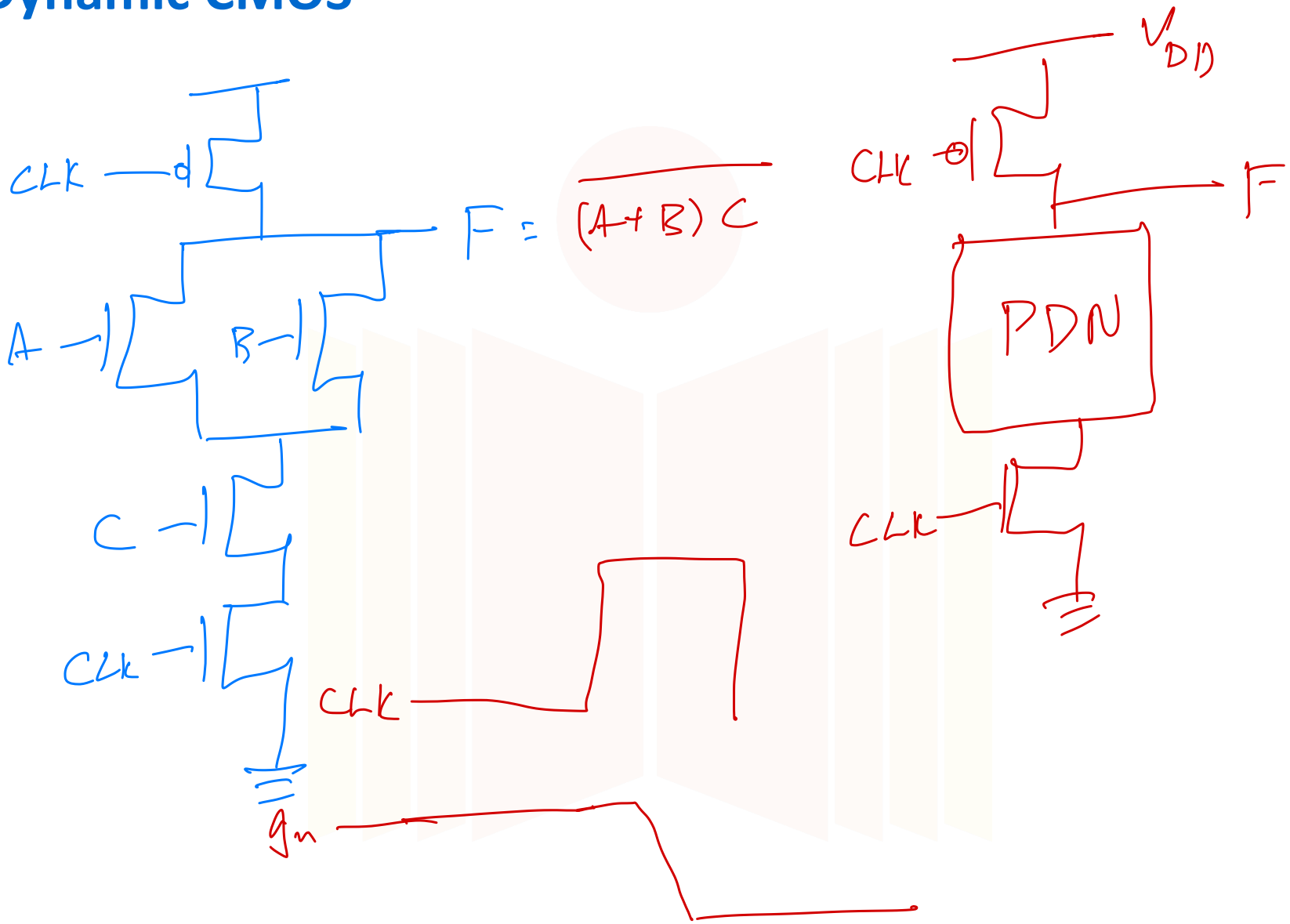
A	CLK	F
X	0	1
X	0	1
0	1	1
1	1	0



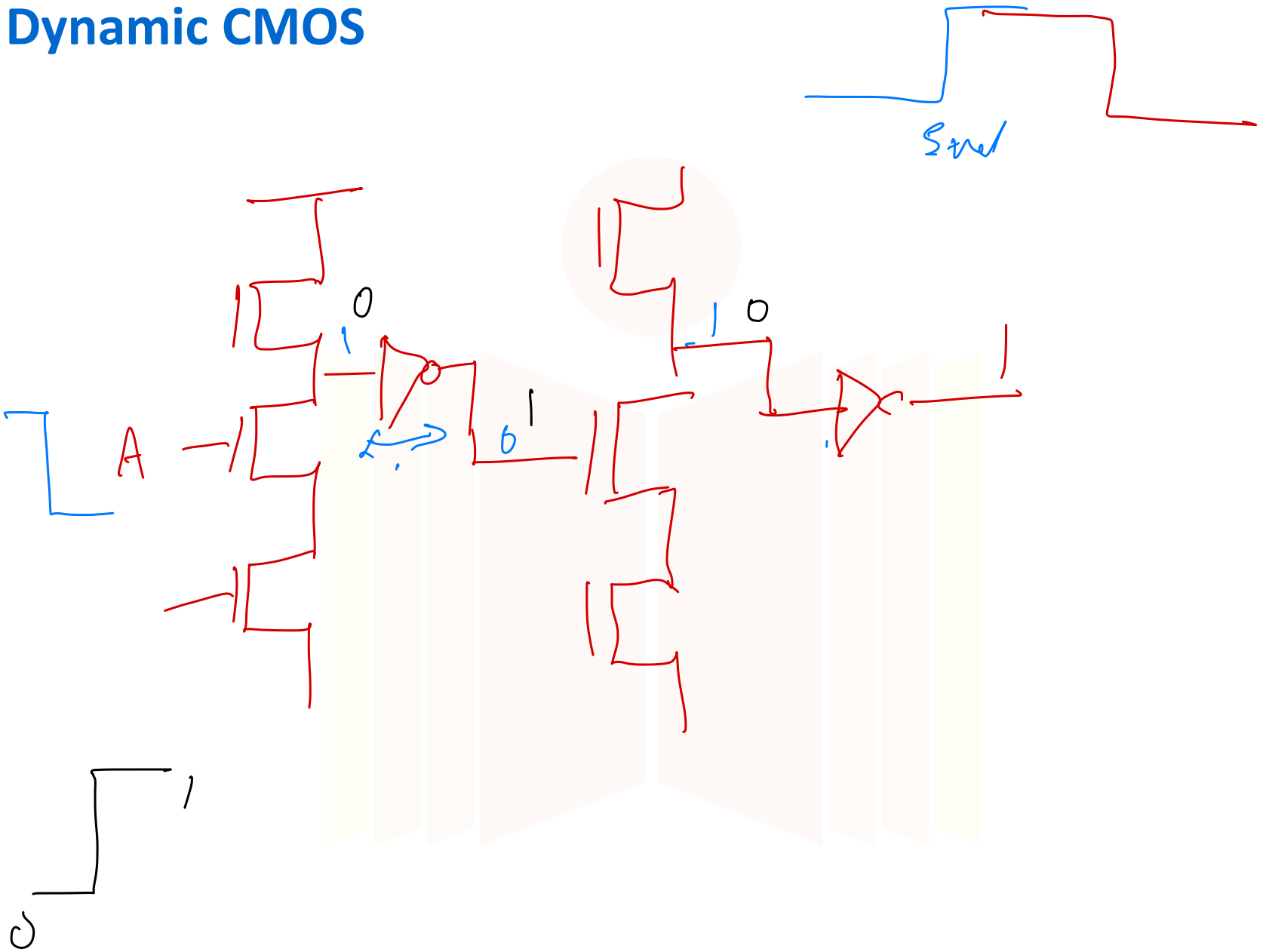
CLK = 0 F = 1 (Precharge)

CLK = 1 (Evaluate)

Dynamic CMOS

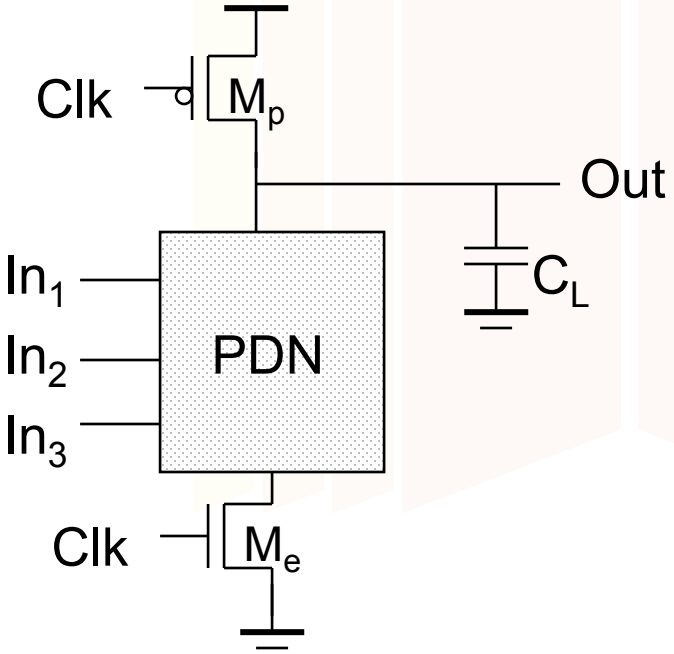


Dynamic CMOS



Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of n requires 2n (n N-type + n P-type) devices
- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on n + 2 (n+1 N-type + 1 P-type) transistors

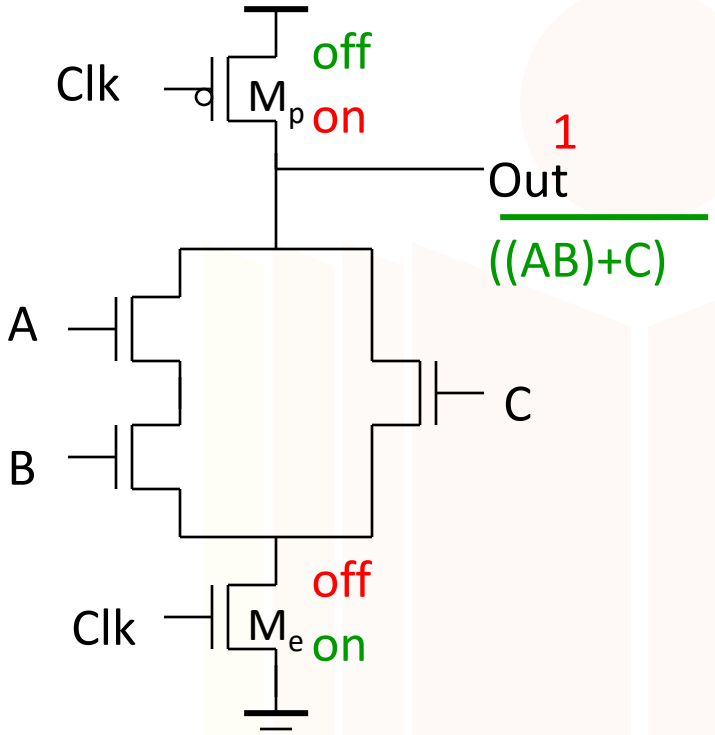


Two phase operation

Precharge (CLK = 0)

Evaluate (CLK = 1)

Dynamic Gate - Example



Two phase operation

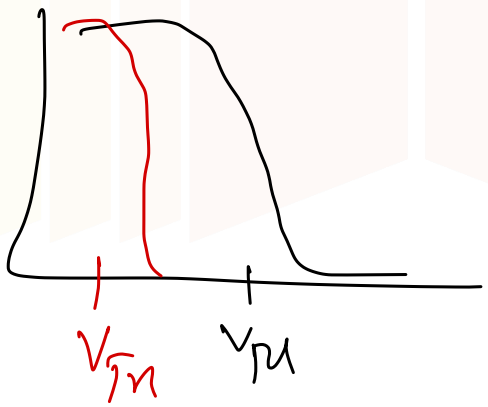
Precharge (Clk = 0)

Evaluate (Clk = 1)

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on CL

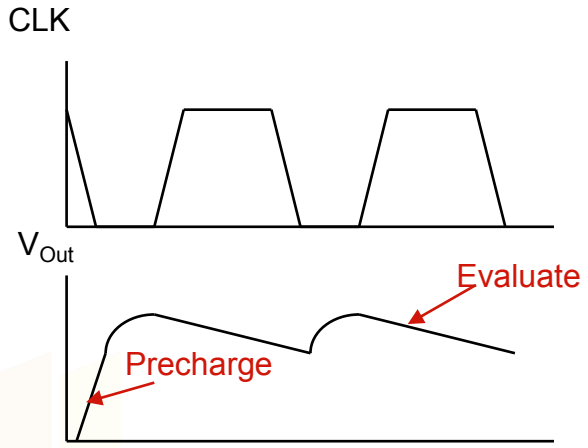
Properties of Dynamic Gates

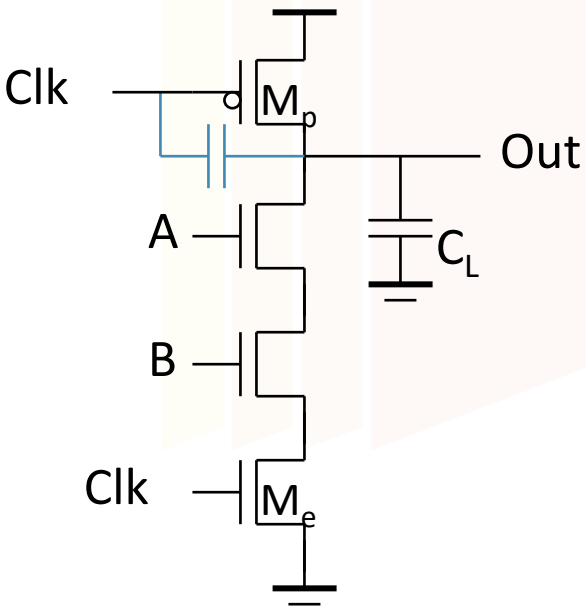
- Logic function is implemented by PDN only
  - N+2 transistors Vs 2N transistors for CMOS
- Full swing outputs (V_{OL}=GND and V_{OH}=V_{DD})
- Faster switching speeds (reduced C_{in} and C_{out})
- Overall power dissipation usually higher than CMOS
- PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}
- Needs a precharge/evaluate clock

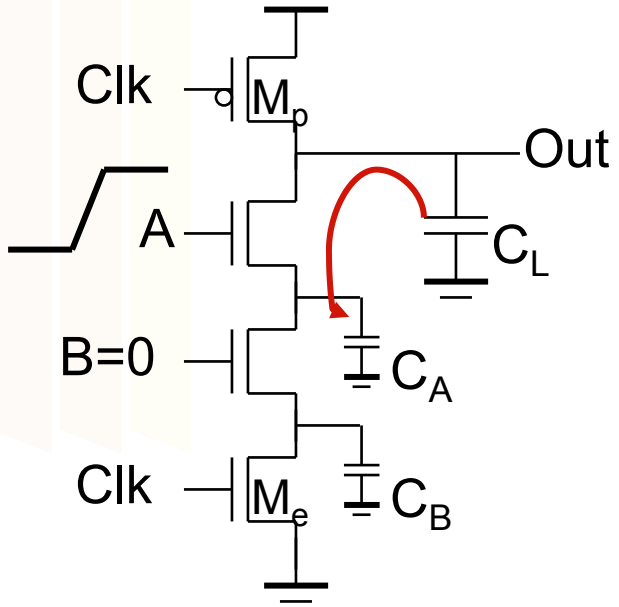


Issues with Dynamic Logic

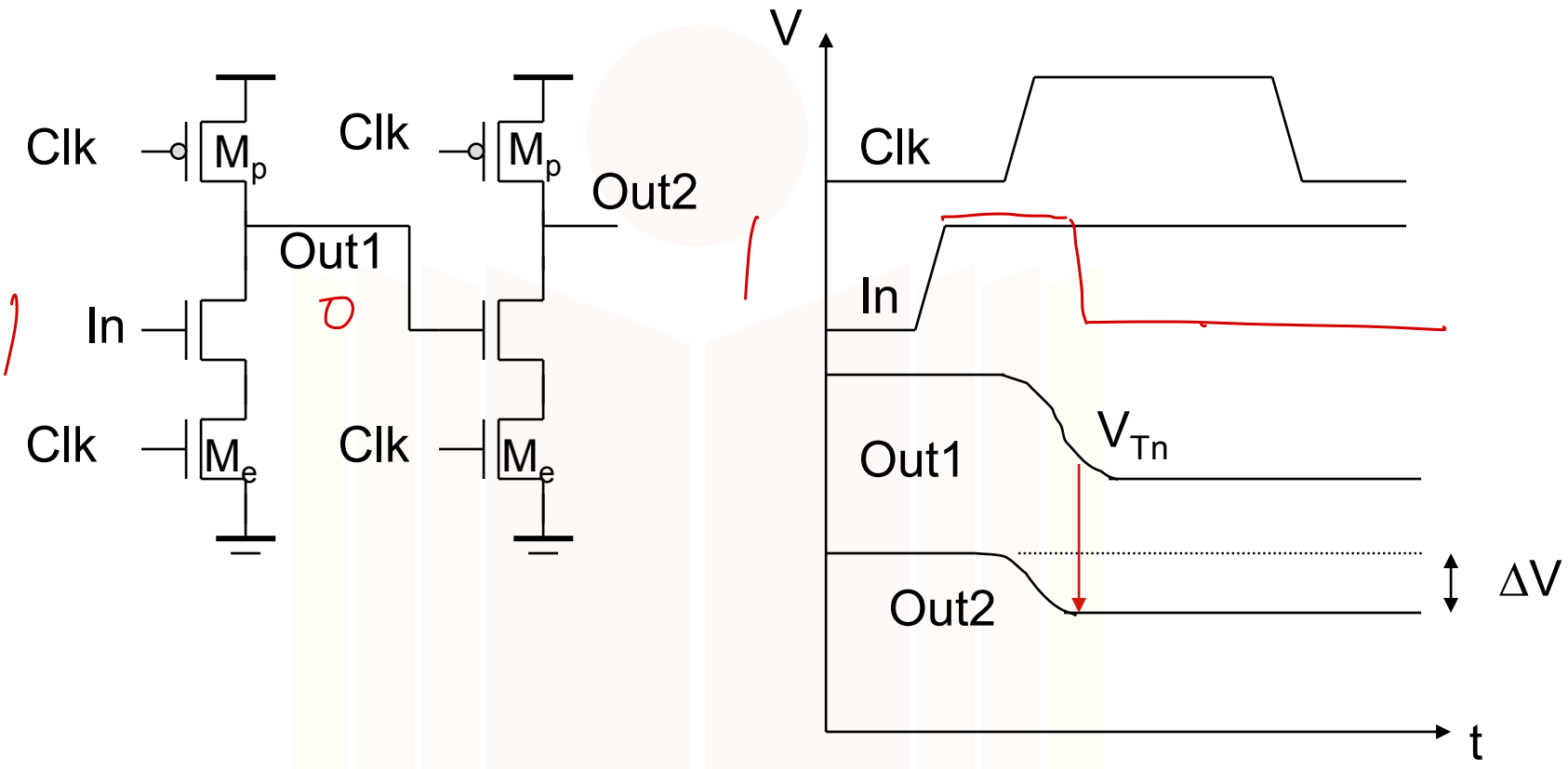
- Charge leakage due to sub-threshold conduction
  - Operate circuits at the highest possible frequency
  - Level restoring circuits
- Charge sharing between C_L and internal node capacitances
- Clock feedthrough





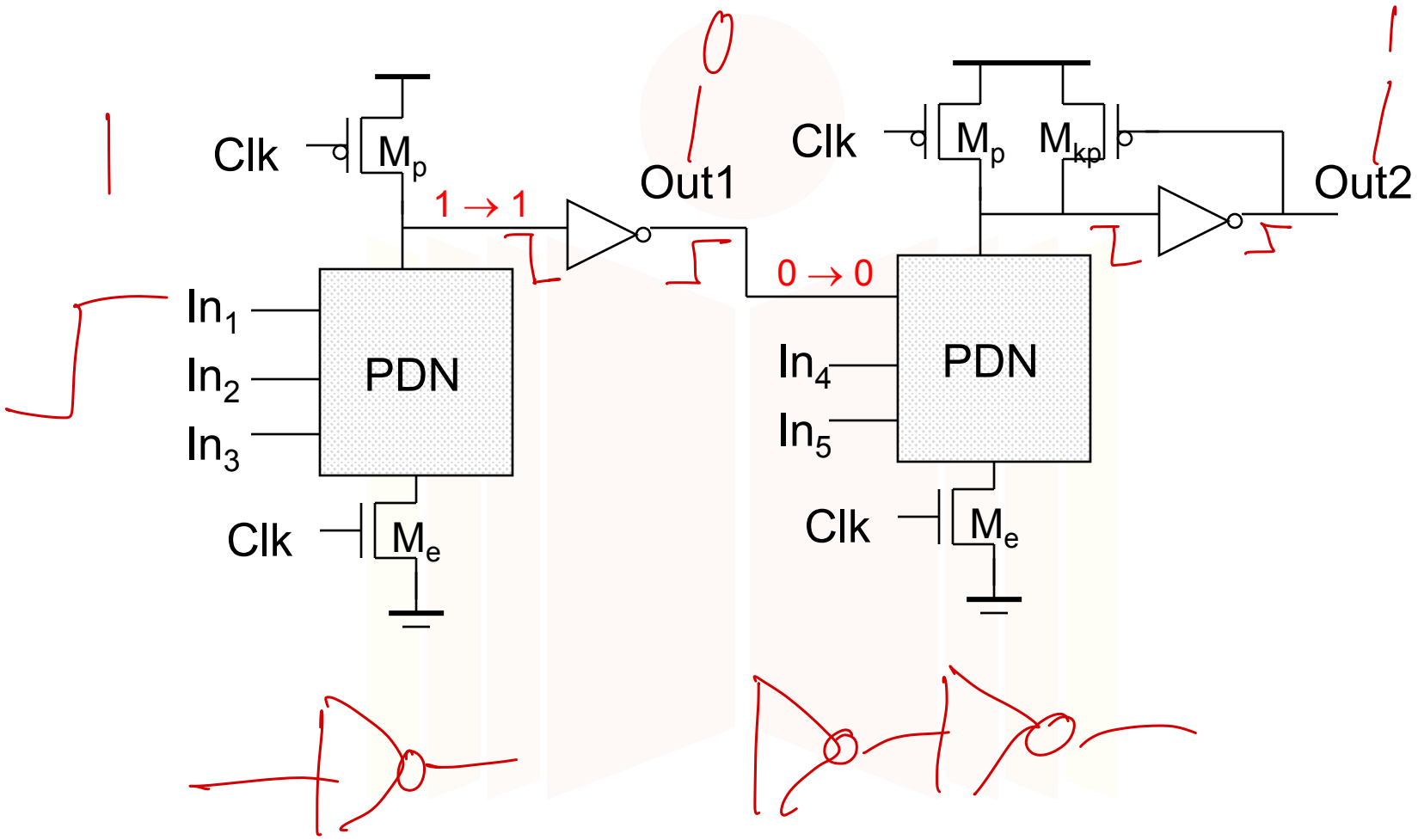


Cascading Dynamic Gates

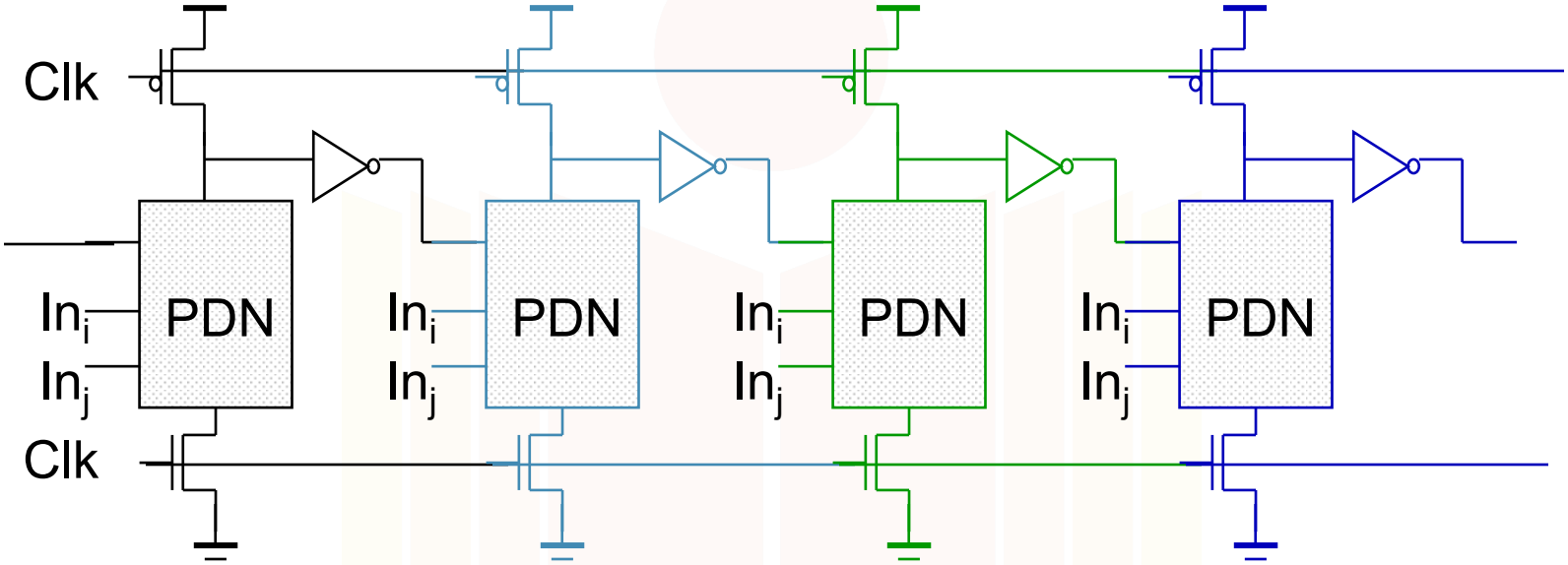


Only 0 → 1 transitions allowed at inputs!

Domino Logic



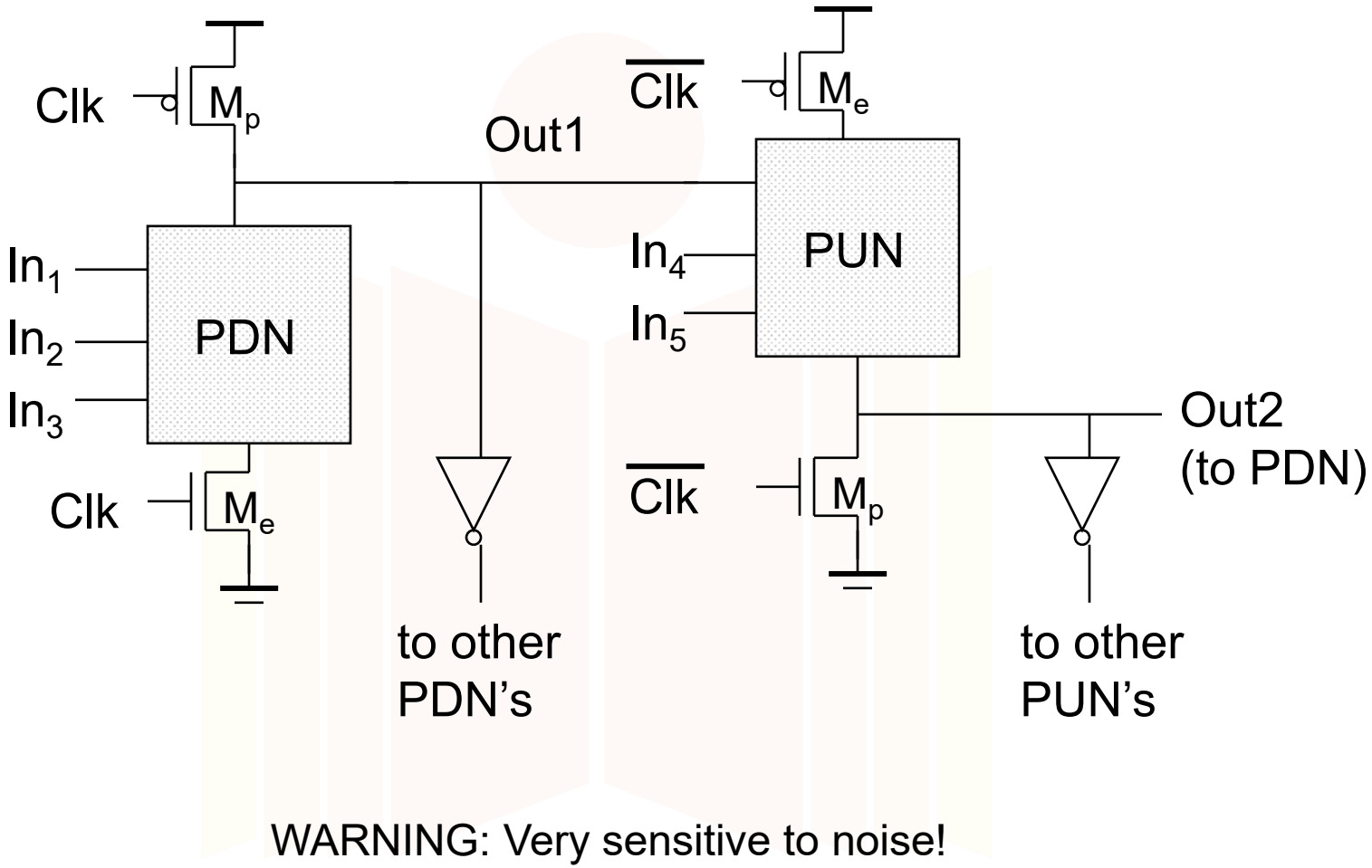
Why Domino?



Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - dynamic inverter can be skewed, only L-H transition
  - Input capacitance reduced – smaller logical effort

NORA Logic



WARNING: Very sensitive to noise!