Electronic Devices and Circuits Lab
Experiment 9- Group 2

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Aim-

To design a Common Source Amplifier with NMOS transistor having the following specifications

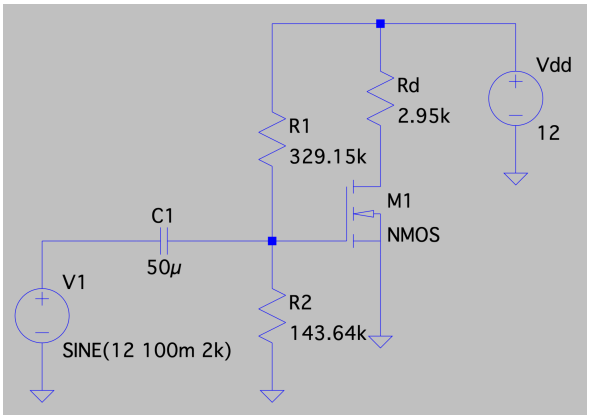
1) Specifications for NMOS are W=10μm and L=0.5μm
2) $V_{in,\,peak} = 100mV$ and Frequency = 2 kHz
3) $V_{DD} = 12V$, $I_{DQ} = 1.4mA$, $I_{DT} = 2.8mA$, $R_{in} = 100k\Omega$ and $V_{is} = 0\Omega$

Also calculate the gain of the amplifier.

Theory-

A linear amplifier is used to amplify the amplitude of the input signal without changing its frequency. We can use either Field Effect Transistors (FET's) or Bipolar Junction Transistors (BJT's). These transistors can be used in 3 different modes, namely for FET Common Source, Common Gate and Common Drain amplifiers and for BJT we have Common Collector, Common Emitter and Common Base amplifiers. We use FETs in amplifiers as they provide a higher gain in voltage compared to BJTs.

In this experiment we have to design an amplifier using NMOS transistor in common source configuration. Here the source-substrate terminal is grounded and input signal is given at the gate terminal (V_{GS}) and output is taken at drain (V_{DS}).



In this circuit, V_{DD} acts as a common power source and R_D is calculated in such a way that V_{DS} always lies in the middle of the saturation region to obtain maximum amplification. R_1 and R_2 are used as voltage dividers to provide the optimum voltage at the gate corresponding to V_{DD}. The capacitor C_1 is used as a coupling capacitor to prevent any current flowing from V_{DD} into the AC source.

This transistor is used in saturation mode, so we can say that-

$$I_D = K_n (V_{GS} - V_{T0})^2$$

To get the values of R_1 and R_2 we perform Small Signal Analysis as follows-
In this method we consider all DC sources to be 0V, and hence R_1 and R_2 are now in parallel connection as both are connected to the same nodes namely Gate and GND.
From the above diagram, $R_1 \,||\, R_2$ forms the input resistance R_{in} which is given as 100kΩ. So,

$$\frac{R1\,R2}{R1+R2} = 100k\Omega$$

The gain in this circuit (A_V) is defined as $\frac{Vout}{Vin}$ so using KVL across the resistor, we get

$$0V - I_D * R_D = V_{out}$$

In this circuit, as the transistor is used in saturation mode a very small change in V_{GS} results in a large change in I_d . Hence we can write $I_D = g_m V_{GS}$ (here g_m is called transconductance).

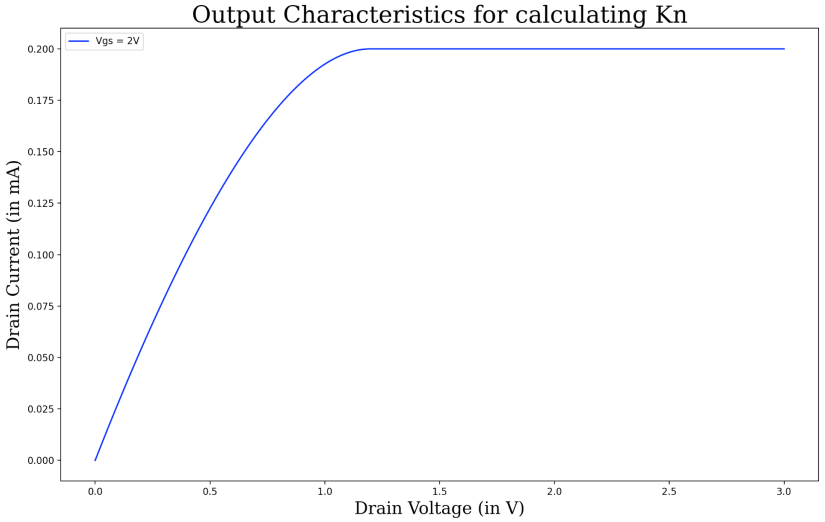
Now the above KVL becomes as - $V_{out} = -g_m * R_D * V_{GS} = -g_m * R_D * V_{in}$

$$\frac{Vout}{Vin} = A_v = -g_m R_D$$

So the gain of the circuit is negative.
Also note that the transconductance $g_m = 2\ (I_{DSQ} * k_n)^{1/2}$

Procedure-

The values of k_n , R_1 , R_2 and R_D are calculated as follows-



1) For k_n we can choose any arbitrary V_{GS} and obtain the saturation current from the graph. Here I have taken $V_{GS} = 2V$ and saturation current from the graph comes out as 0.2mA. Hence -

$0.2mA = k_n\ (2V - 1V)^2 = k_n$ (As $V_{T0} = 1V$)

$k_n = 0.2\ mA\ /\ V^2$

2) Now as we know the k_n value we can find V_{GSQ} from $I_{DQ} = 1.4mA$

$$1.4mA = 0.2\ mA/V^2\ (V_{GSQ} - 1)^2 \Rightarrow V_{GSQ} = 1 + (7)^{½} = 3.646V$$

So the voltage at the gate must be 3.646V, i.e. the voltage at the center of the voltage divider must be 3.646V. So,

$$\frac{12\ R2}{R1 + R2} = 3.646V$$

Combining this with $\frac{R1\ R2}{R1 + R2} = 100k\Omega$, we get $R_1 = 329.15k\Omega$ and $R_2 = 143.64k\Omega$

3) Transition point is the point where the load line intersects with the locus of pinchoff points. Now as we are given I_{DT} we can determine V_{GST} as-

$$2.8mA = 0.2\ mA/V^2\ (V_{GST} - 1)^2 \Rightarrow V_{GST} = 1 + (14)^{½} = 4.742V$$

From the pinchoff voltage relation between V_{DS} , V_{GST} and V_{T0} we have
$V_{DS} = V_1 = V_{GST} - V_{T0} = 4.742V - 1V = 3.742V$

So the coordinate of the transition point is (V_{DST} , I_{DT}) = (3.742V, 2.8mA).
The above coordinate must pass through the load line, so plugging that into the load line equation -

Slope = $\frac{2.8mA - 0}{3.742 - 12} = \frac{-1}{Rd} \Rightarrow R_d = 2.95k\Omega$

Observations-

1) Now that all parameters have been obtained, we can calculate the theoretical gain of the amplifier.

$$g_m = 2\ (I_{DSQ} * k_n)^{½} = 2 \text{ x } (\ 1.4 \text{ x } 10^{-3} \text{ x } 0.2 \text{ x } 10^{-3}\ )^{½}$$

$$g_m = 1.058 \text{ mA / V}$$

From theory, gain A_v is given by $A_v = -R_D * g_m = -\ 2.95k\Omega * 1.058 \text{ mA/V}$

$$A_v = -3.1219$$

2) From the output plot, we obtain amplification A_v = -3.092 which is approximately equal to the theoretical amplification

3) There is a DC bias in the output voltage due to the drain-source bias. Applying KVL across R_D-

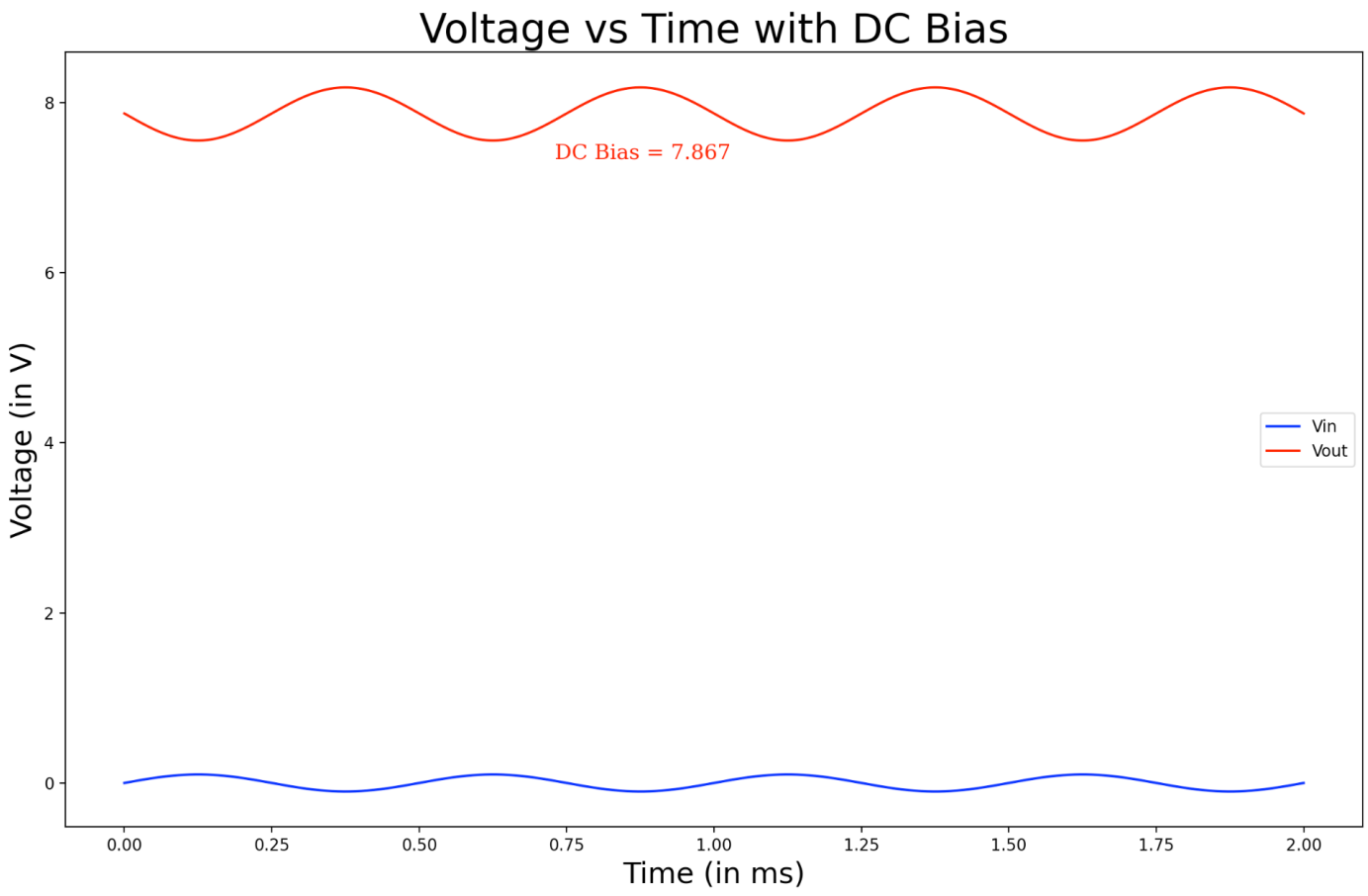
$$V_{DD} - I_{DQ} * R_D = V_{DS} = 12 - 1.4mA * 2.95k\Omega = 7.87V$$

From the simulation, we observe that the DC bias is 7.867V

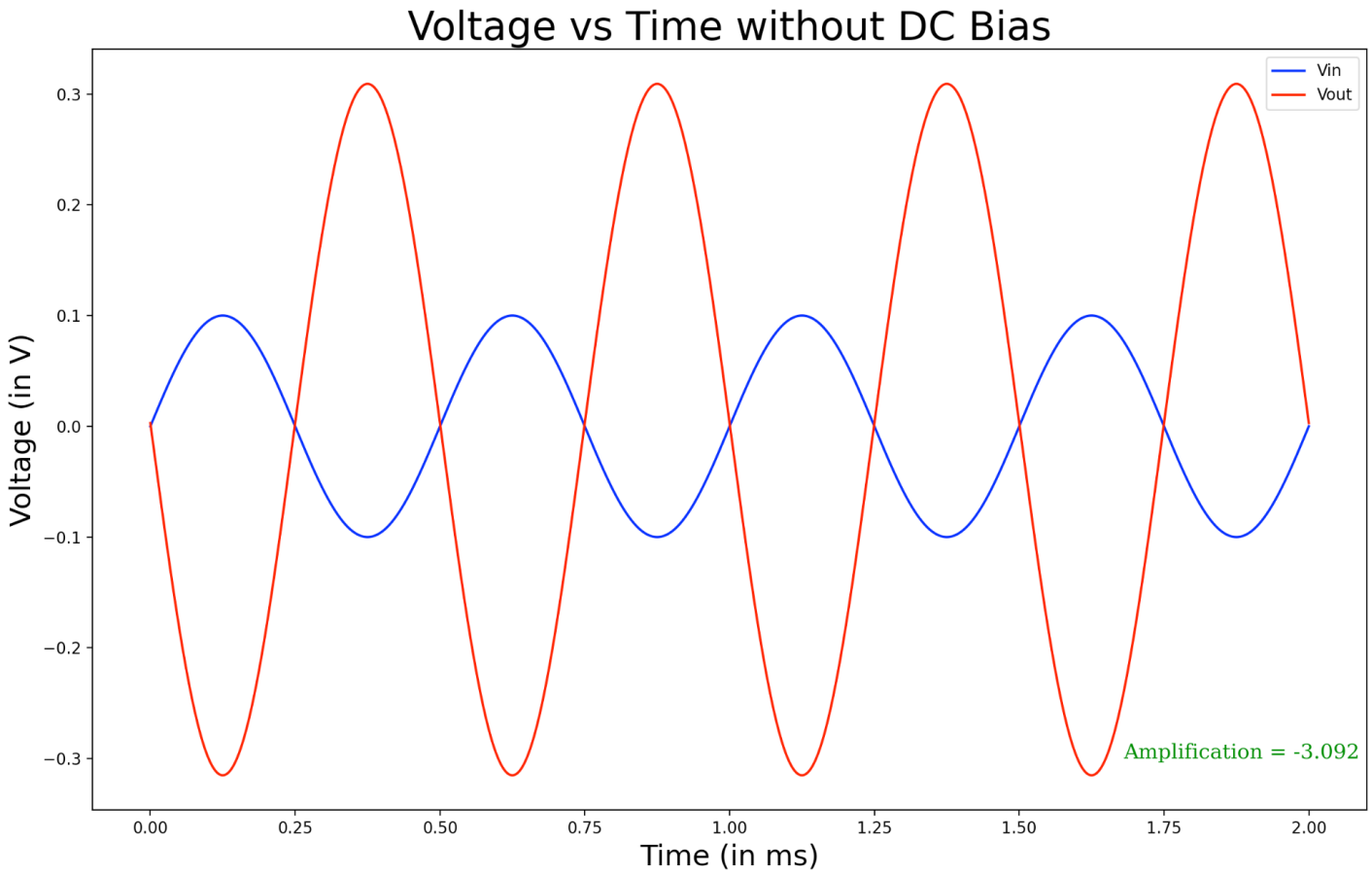
4) The amplifier has negative gain as expected which causes the output signal to have a 180° phase shift

Plots-

Output plot with DC bias -



Output Plot after removing DC bias-



Reference Image-

Reference image from Donald A. Neamen - Microelectronics Circuit Analysis and Design