

EE 3403

HDL Coding Assignment for DOT Product under various Design Constraints

MODULE: Digital Arithmetic, Architectures and VLSI for DSP

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Sum of Products/ Convolution/ FIR-alike Filtering in VLSI Signal Processing

ASSIGNMENT

$$Y = x0h0 + x1h1 + x2h2 \dots\dots\dots x9h9$$



Q1. Compute Y in one clock cycle.

Q2. Compute Y keeping in mind that no two different arithmetic operations will take place in same clock edge.

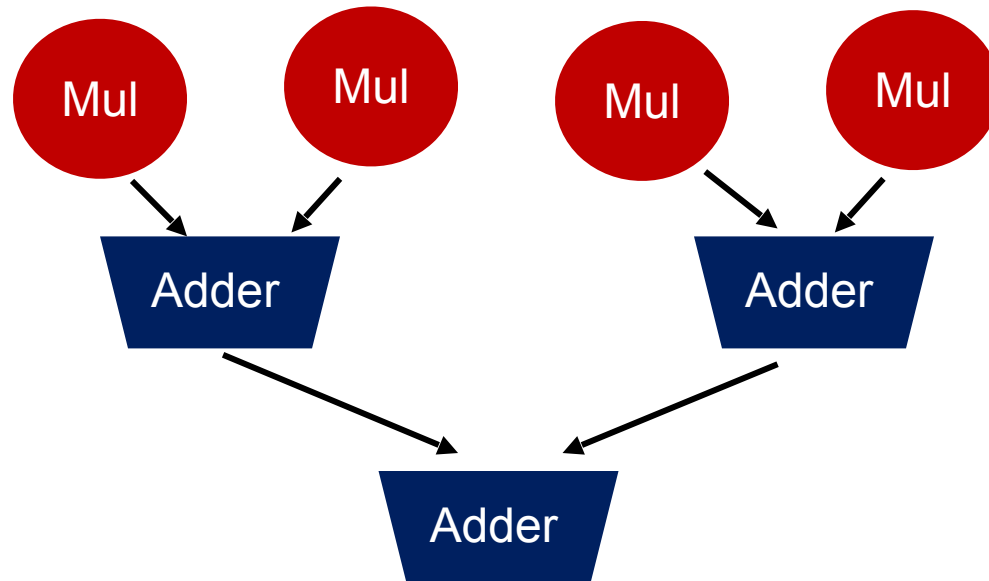
Q3. Compute Y assuming you have TWO multipliers and ONE adder.

Q4. Compute Y assuming there is no Multiplier module is available. You should not replace multiplier by shifted addition or repetitive additions. You can use memory. Consider the values of h_0, \dots, h_9 are known beforehand.

Q5. Compute Y assuming there is no multiplier module and no memory are available. Consider the values of h_0, \dots, h_9 are known beforehand. You should not replace multiplier by shifted addition or repetitive additions.

Sum of Products/ Convolution/ FIR-alike Filtering

$$Y = x_0h_0 + x_1h_1 + x_2h_2 + x_3h_3$$



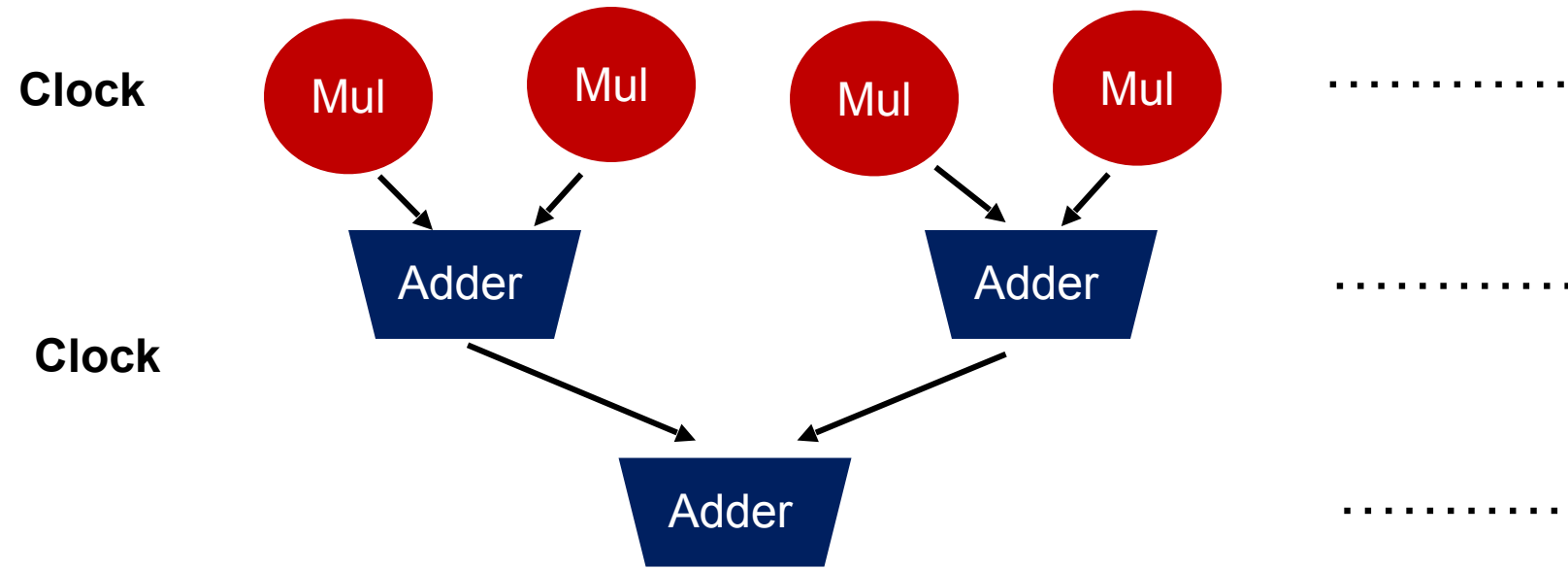


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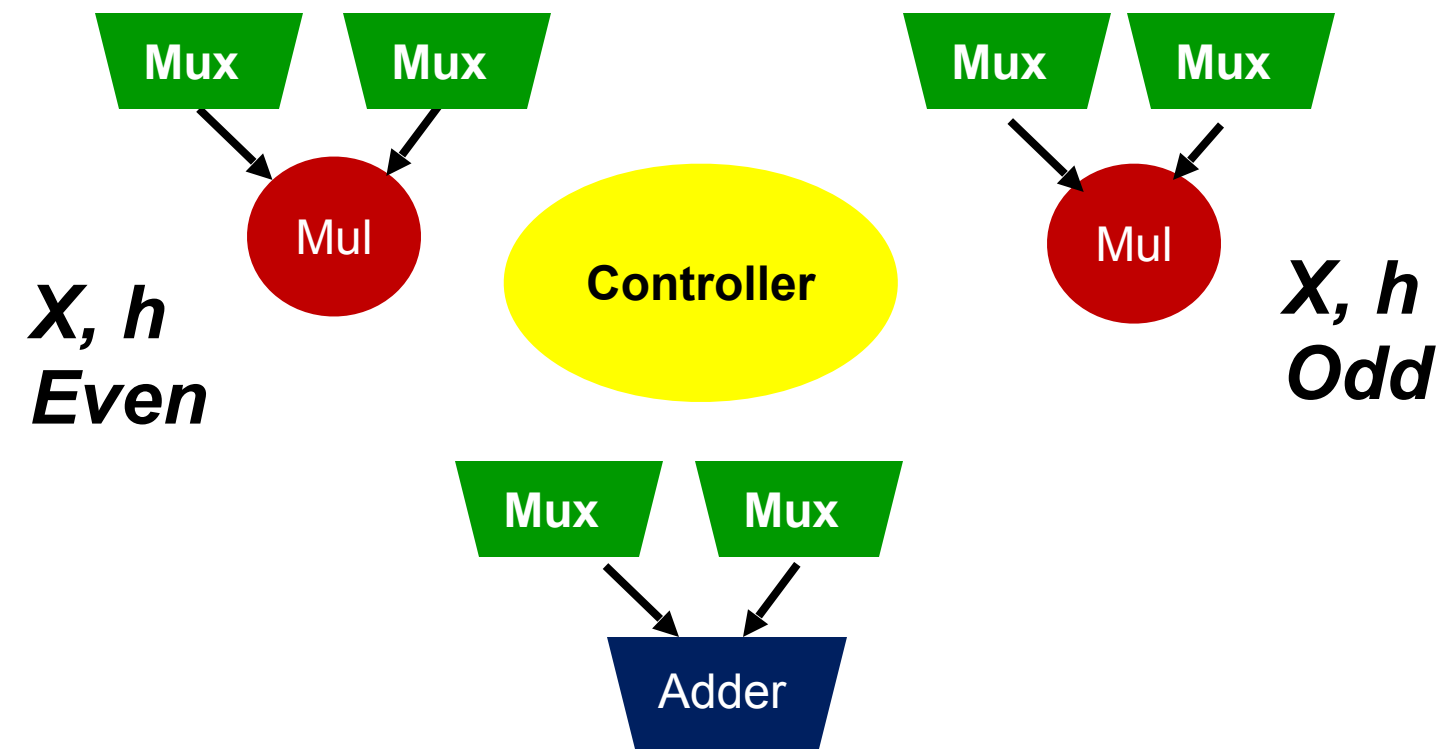
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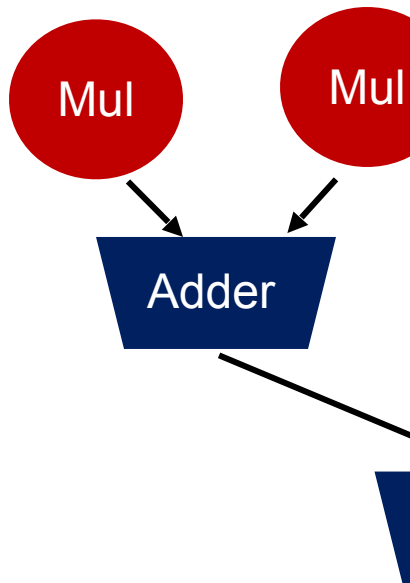
Q5. Compute Y assuming there is no multiplier module and no memory are available. Consider the values of h_0, \dots, h_9 are known beforehand. You should not replace multiplier by shifted addition or repetitive additions.

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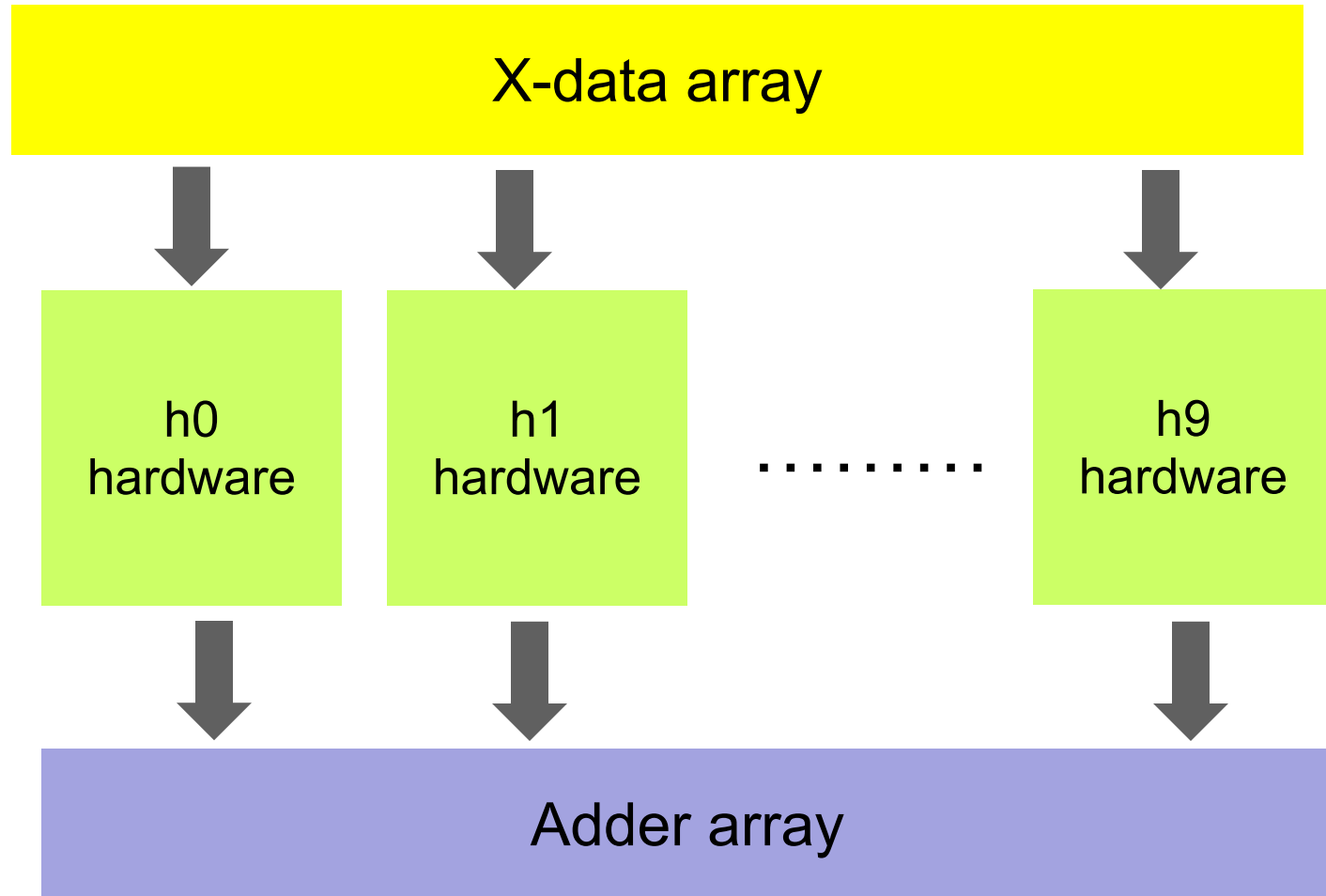
$$Y = x_0h_0 + x_1h_1 + x_2h_2 \dots\dots\dots x_9h_9$$



Not a solution

Hint: Different combinations of Filter Coefficients can be stored in the memory before-hand

Q5. Compute Y assuming there is no multiplier module and no memory are available. Consider the values of h_0, \dots, h_9 are known beforehand. You should not replace multiplier by shifted addition or repetitive additions.

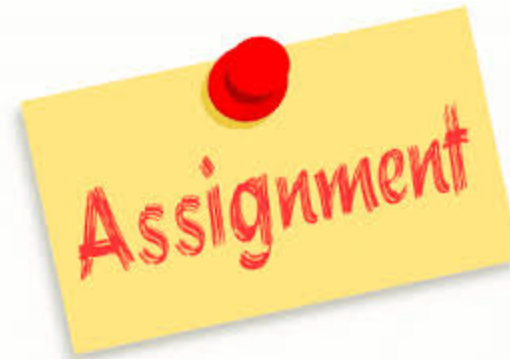




**Q1: Compute the circuit complexity
THEORETICALLY for prob.1 – 5 and compare. .
How will it vary with different word-length 4
to 64 bits?**



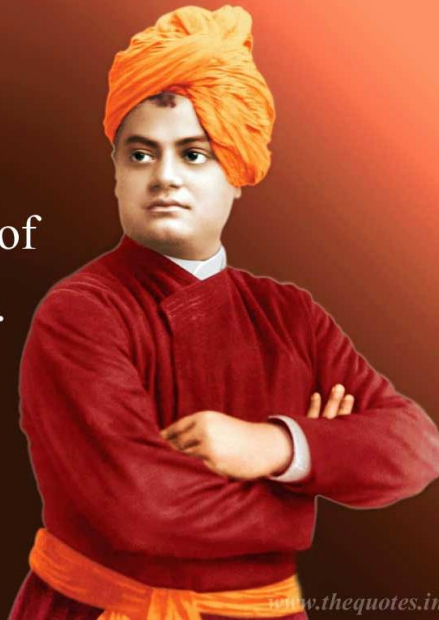
**Q2: Compute the numerical error
THEORETICALLY for prob. 1-5 and compare. How
will it vary with different word-length 4 to 64
bits?**



Q3: Connect answers of Q1 and Q2 and comment.

Education is the manifestation of
the perfection already in man.

Swami Vivekananda

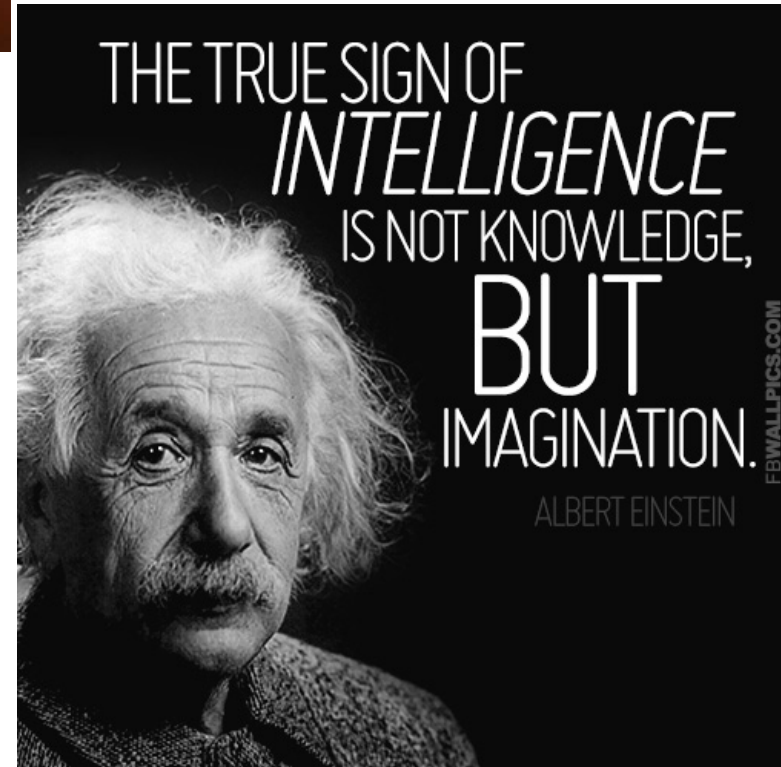


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Thank you

