Introduction to VLSI Design
Assignment 2

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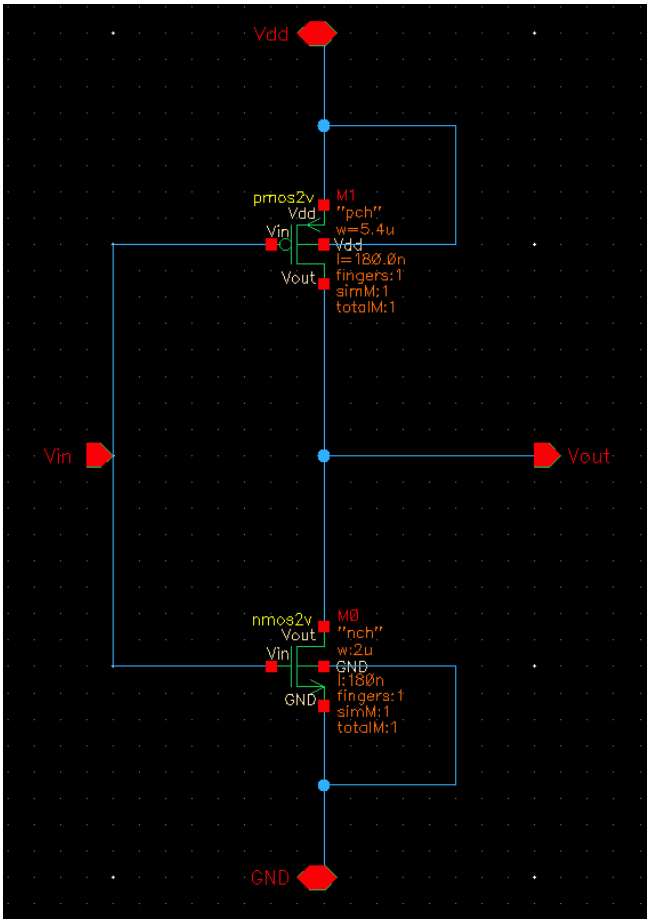
Design parameters of CMOS inverter

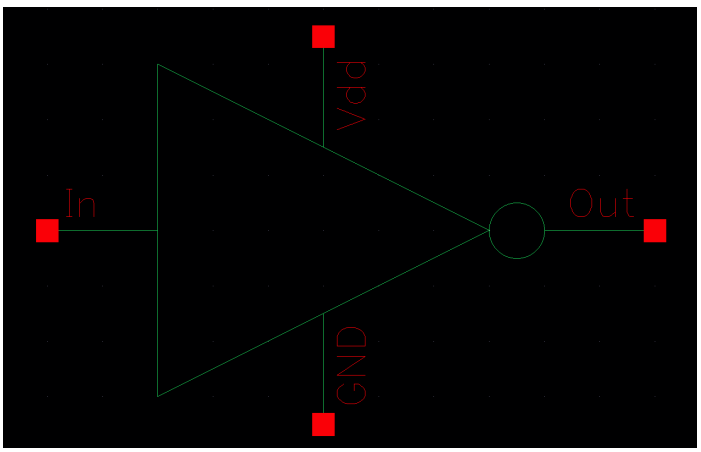
For NMOS: L = 180 nm and W = 2 µm
For PMOS: L = 180 nm and W = 4 µm

This schematic contains 4 pins: V_{DD} , GND , V_{in} and V_{out}



Schematic of CMOS inverter

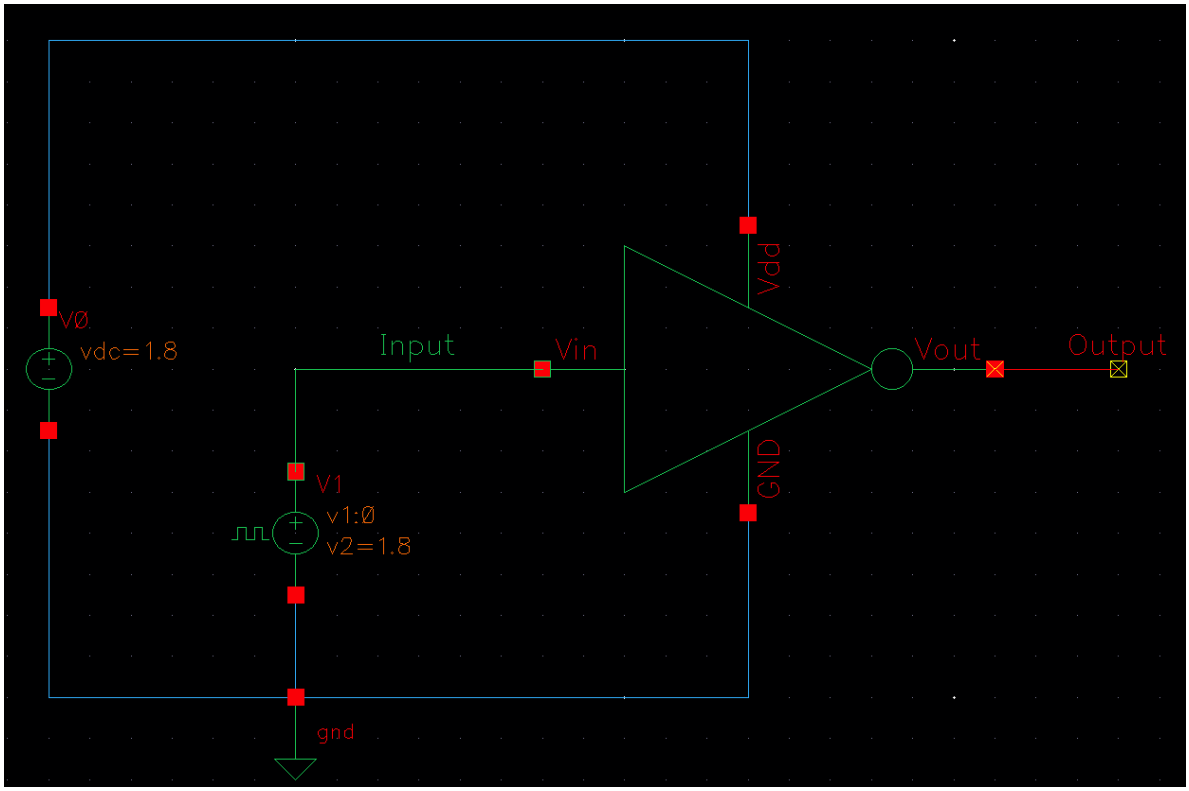
Symbol used for CMOS inverter



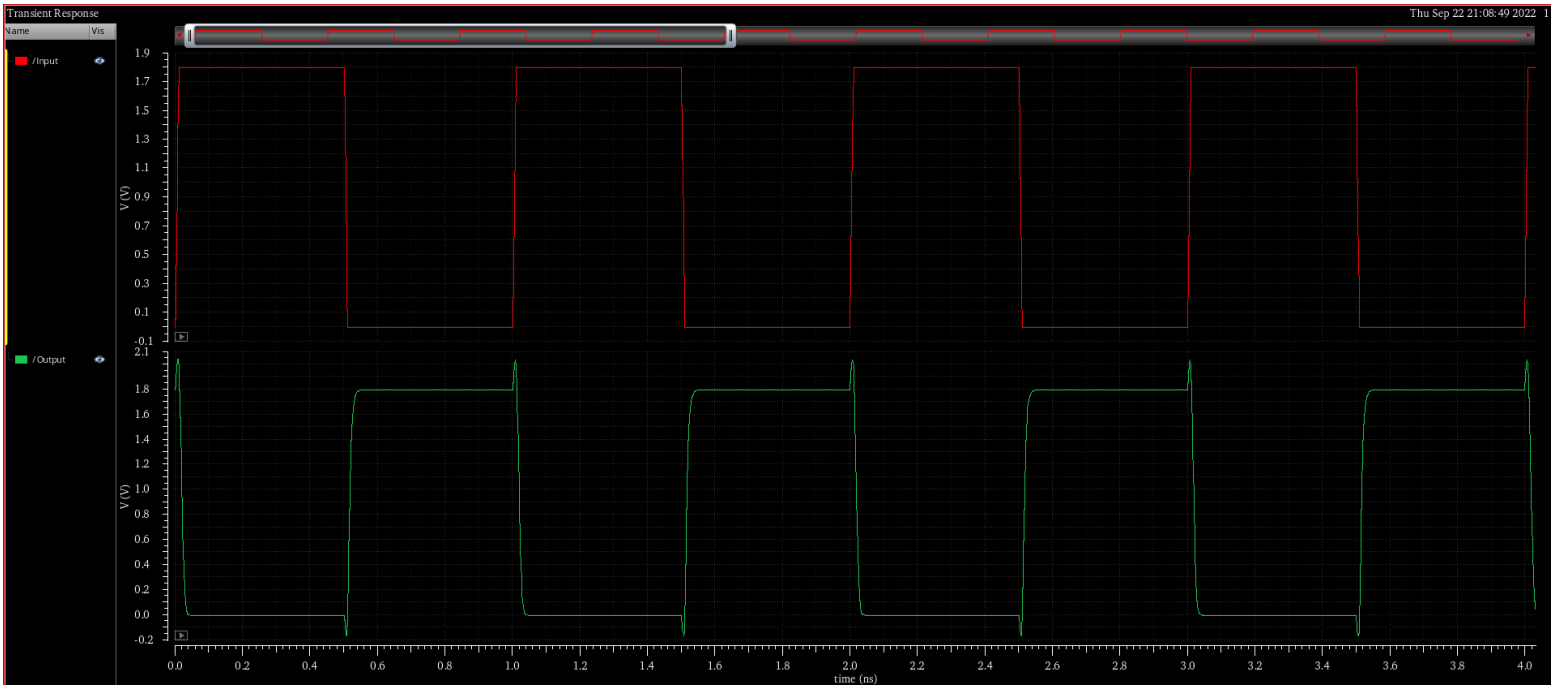
Testbench for verification of circuit

Here, V_{DD} is given at 1.8V and input is a pulse signal varying from 0V to 1.8V

Testbench circuit

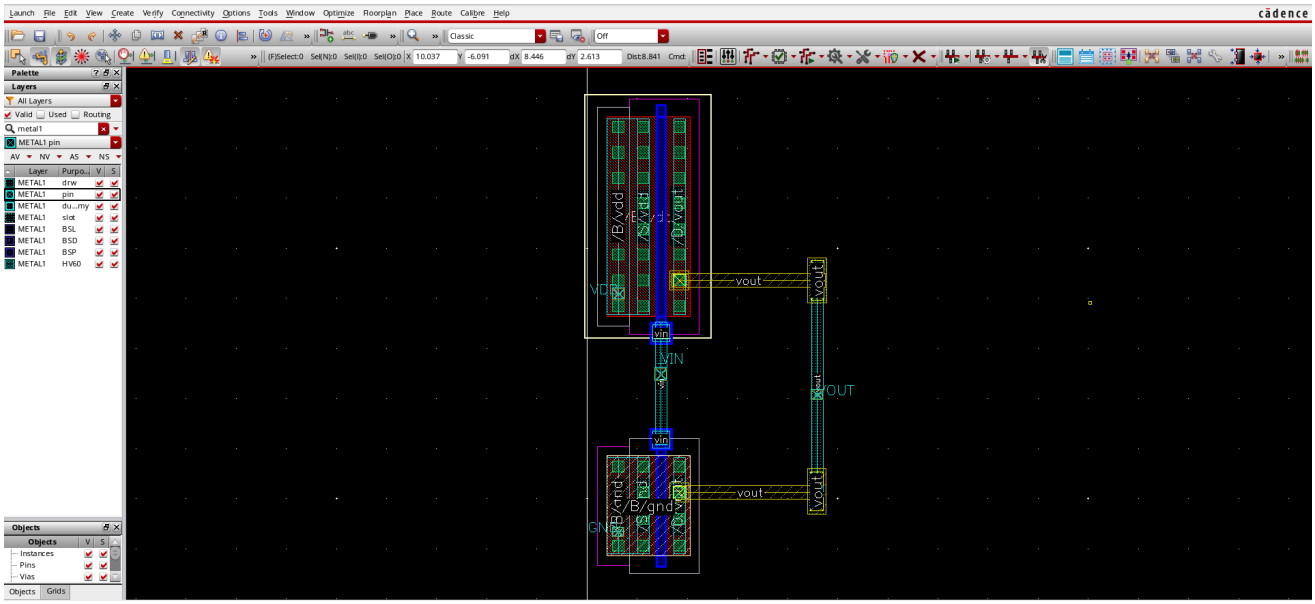


Corresponding output



Layout specifications

Two metal rails are used to interconnect the components, Metal 1 connects components vertically and Metal 2 connects components horizontally. Vias are metallic lined holes which are used to connect components across different layers, in this case connecting M1–M2 and M2 and polysilicon.

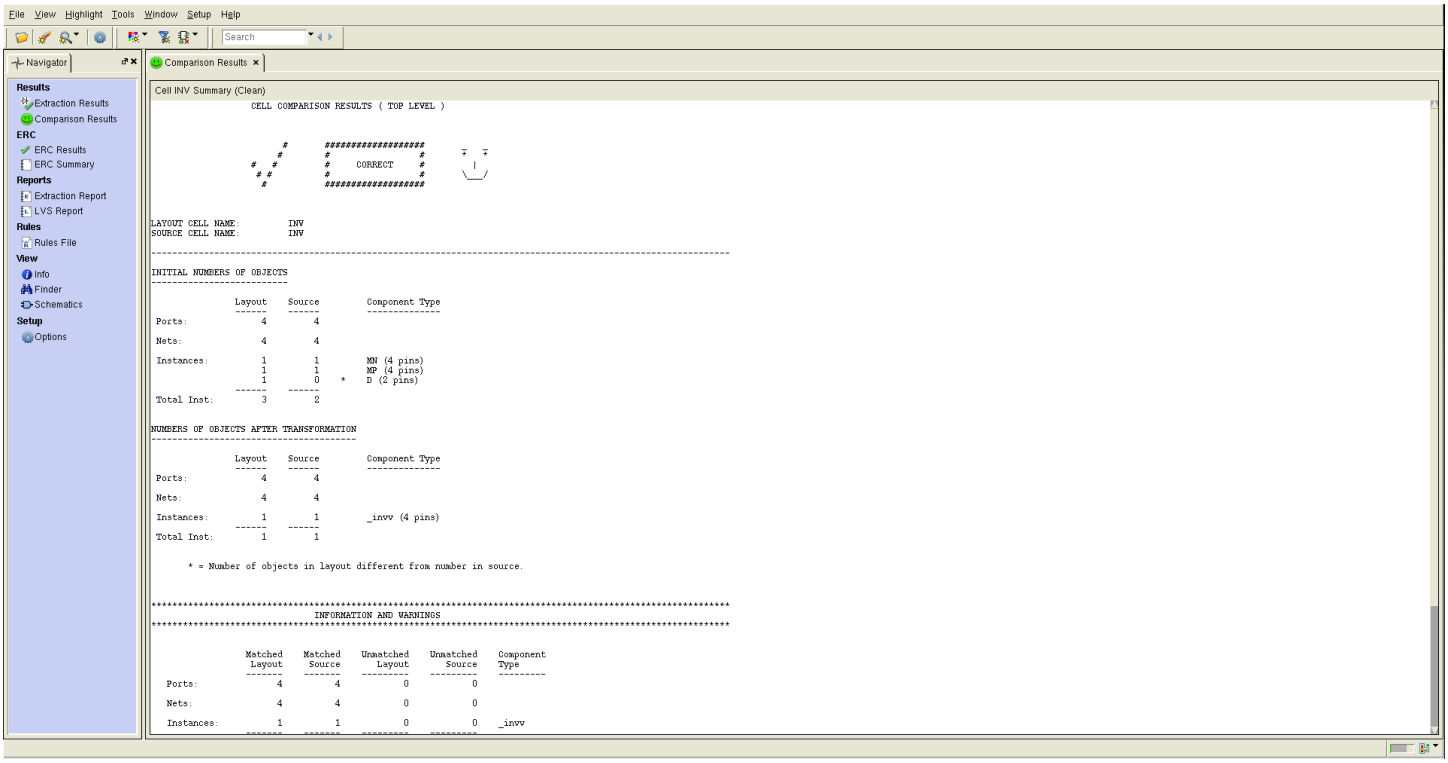


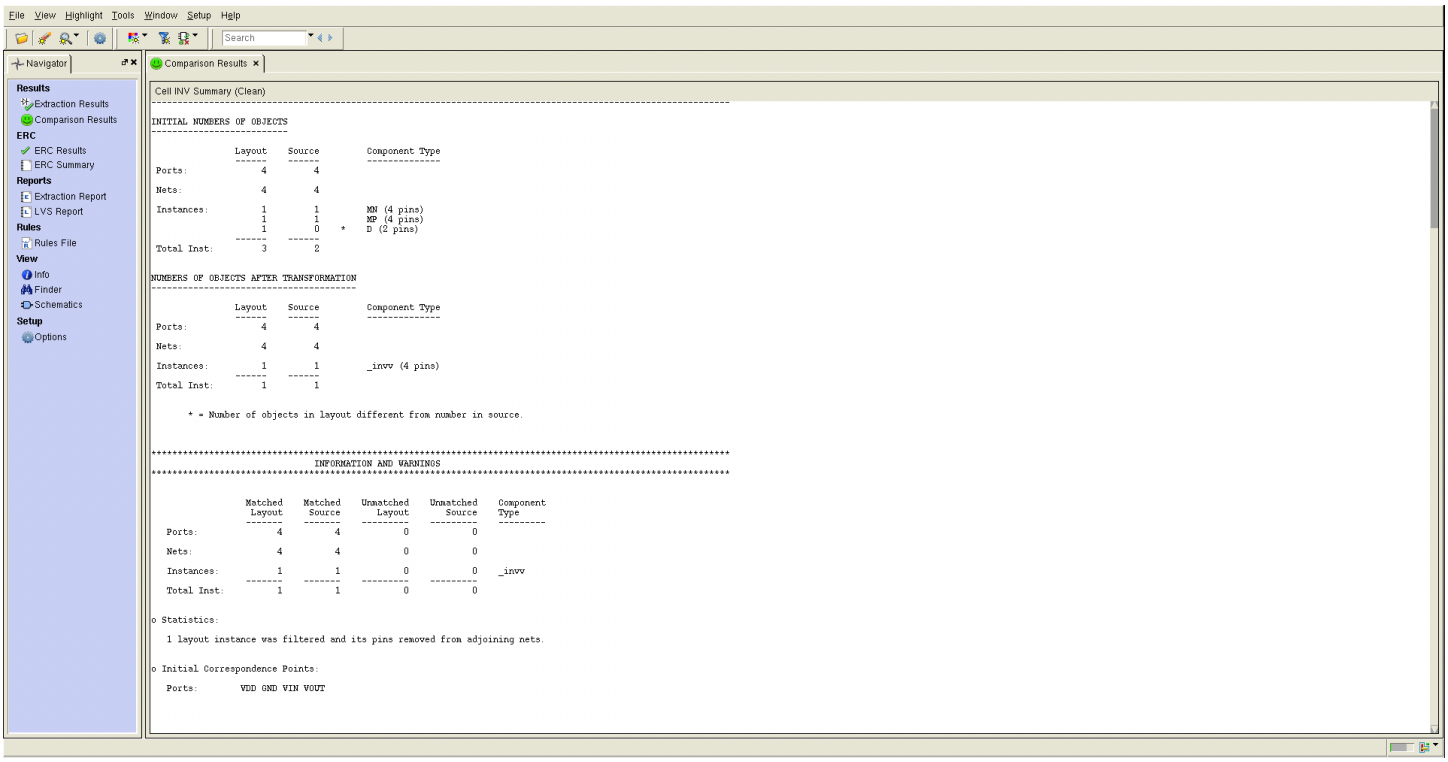
Design Rules Check (nm DRC)

Here are the results of the DRC check, there are 14 errors (which we couldn't resolve even after an all nighter).

Layout vs Schematic test (LVS)

LVS test verifies the connectivity of the circuit from the schematic and extracted connections from the GDS files and provides it in the form of a report. After running the LVS test from Calibre and setting appropriate rules, input, output, options for power and ground nets the following results were obtained –

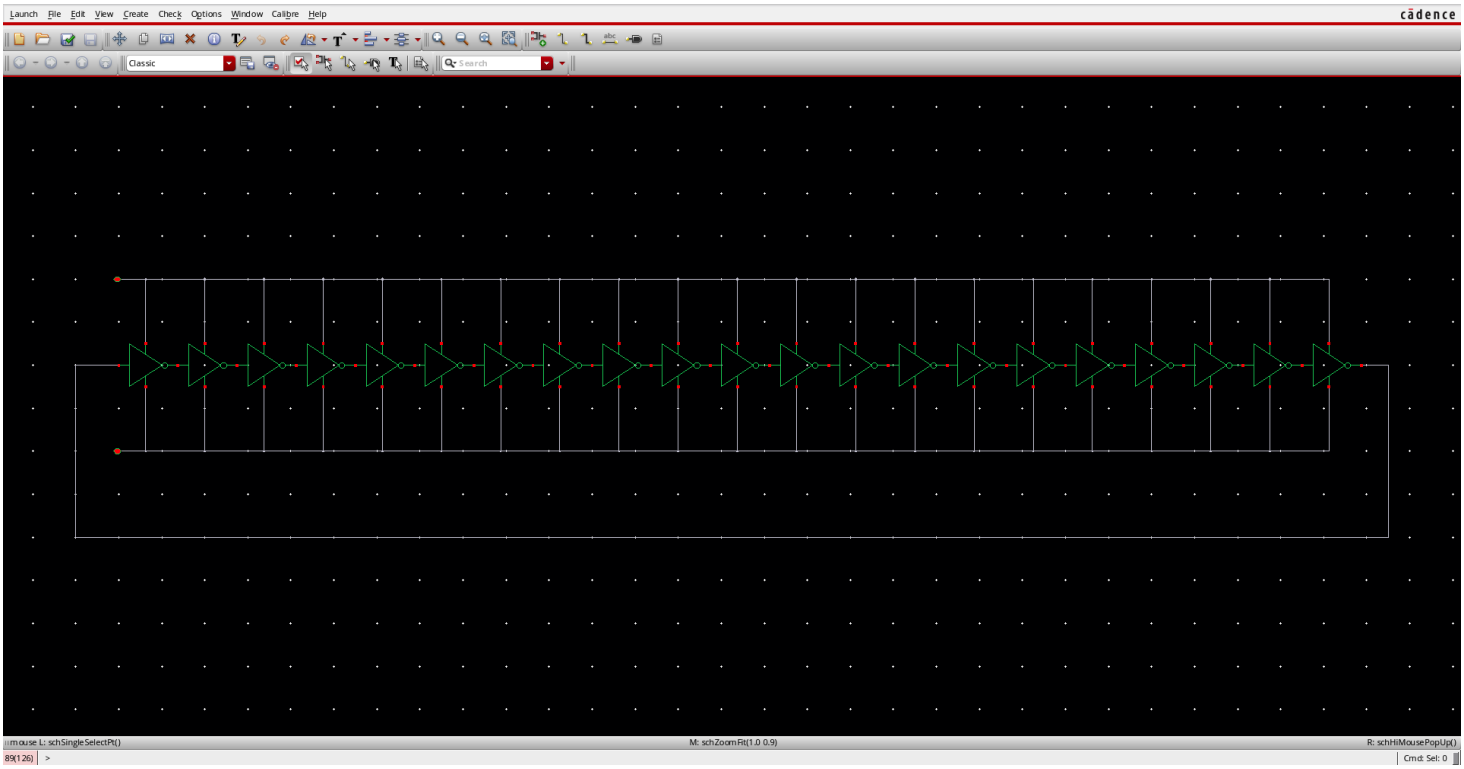




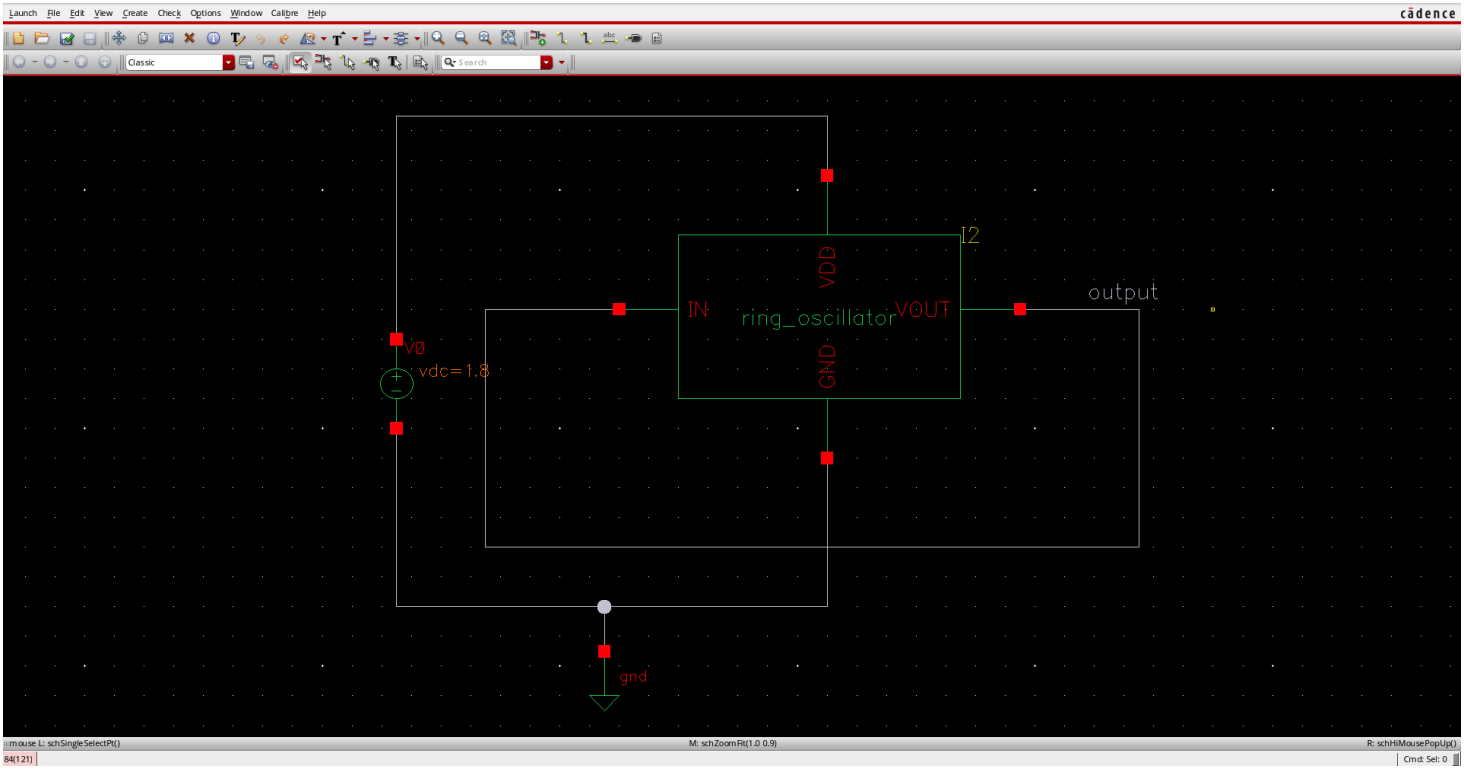
Ring Oscillator

It is a circuit composed of an odd number of NOT gates, whose output alternates between two voltage levels. Here we have used 21 CMOS inverters in series.

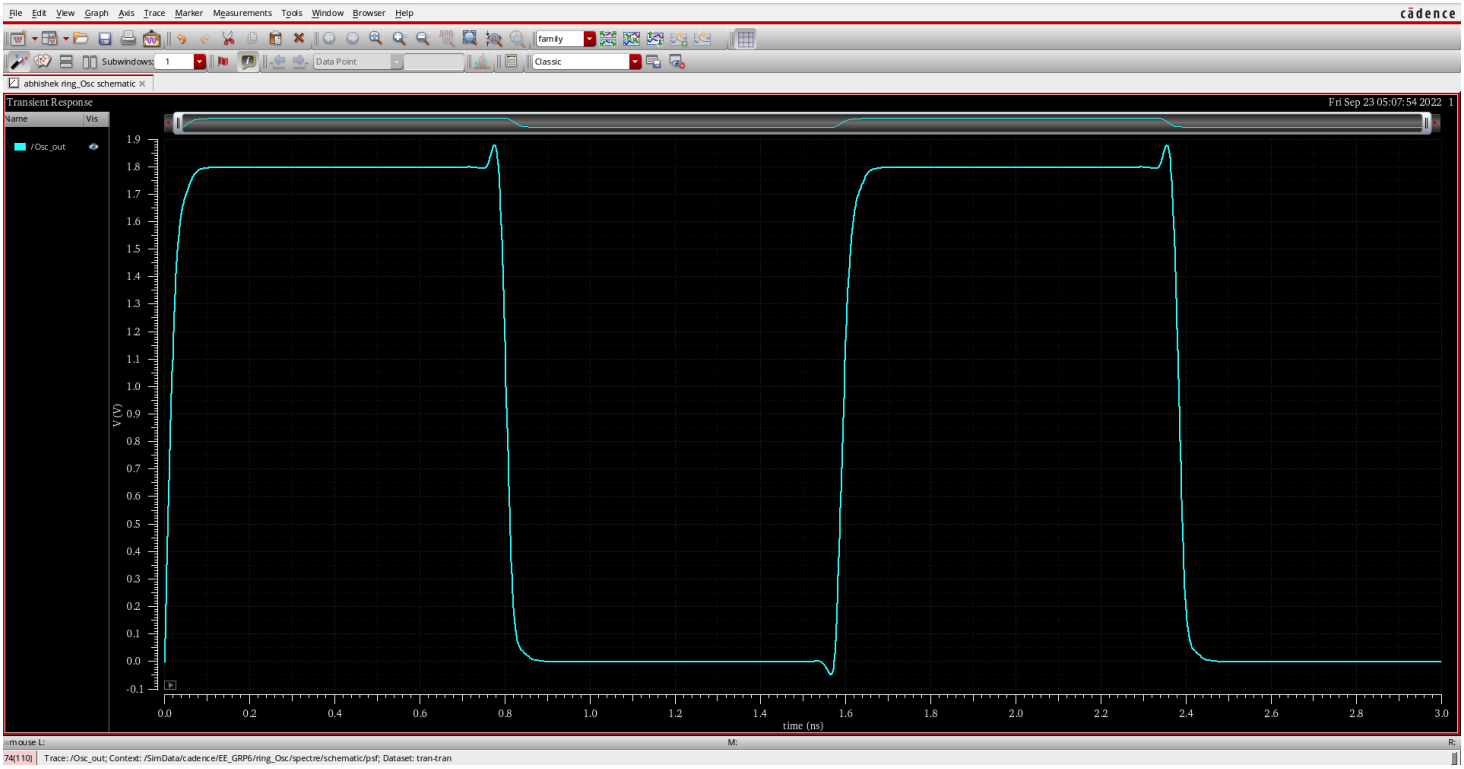
Schematic



Testbench



Output of the circuit



From the above circuit, the overall time period of the circuit is 1.5 ns which is equally distributed as delay in all inverters and in both cycles. Therefore the propagation delay of each inverter (T / 2N) is 24.19 ps.

Layout

We again use Metal 1 for vertical connections and Metal 2 for horizontal connections, vias are used to connect M1–M2 and M2–polysilicon. The layout is as follows –