

# Analog Electronics

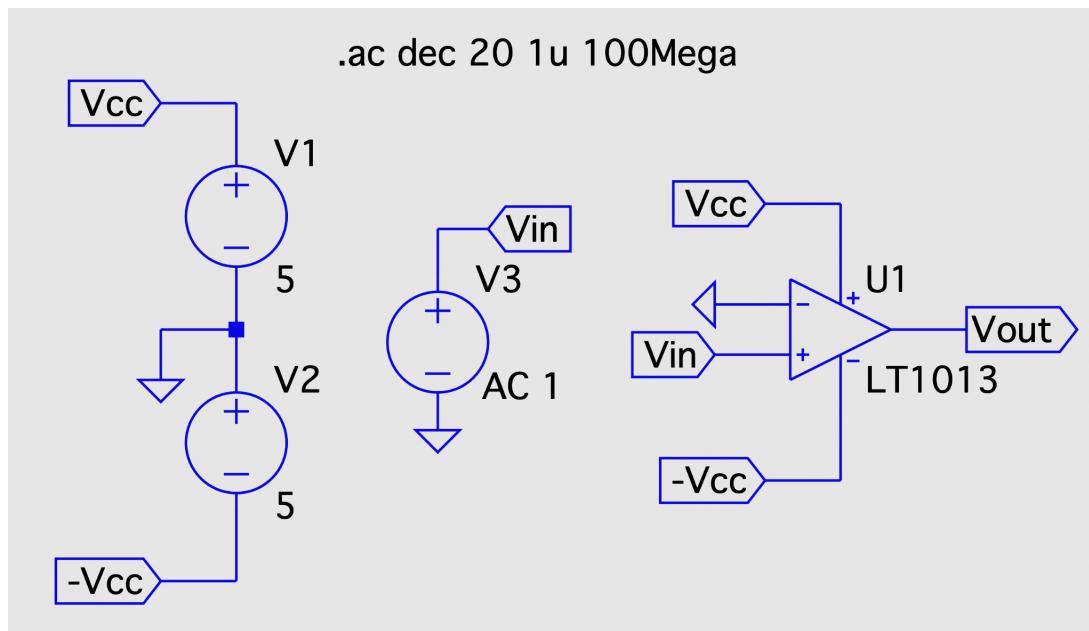
## Mini Project 2

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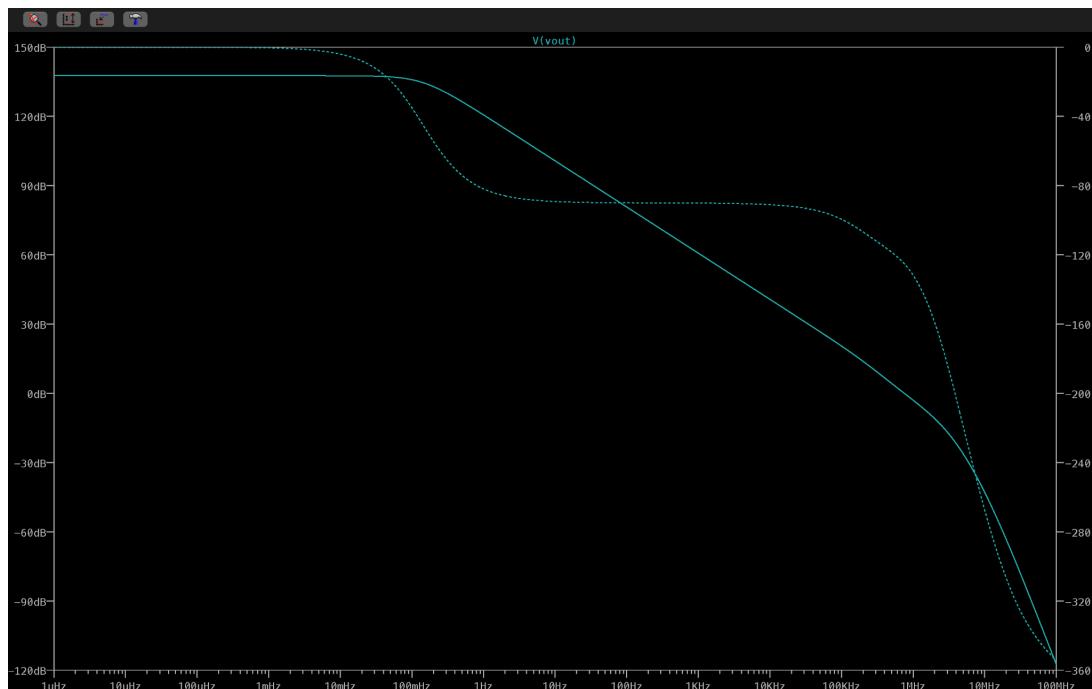
### 1. To find DC gain, UGB and macro model parameters of LT1013

We can use the AC analysis command in LTSpice to find out the bode plot of the transfer function of the Op-Amp in an open loop.

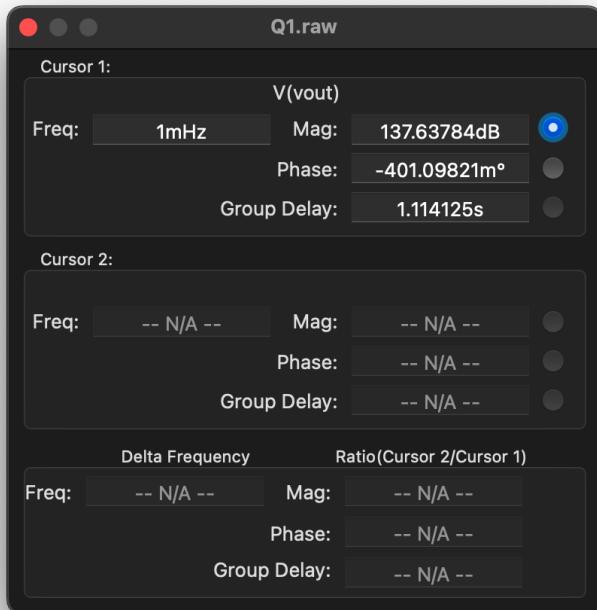
Testbench



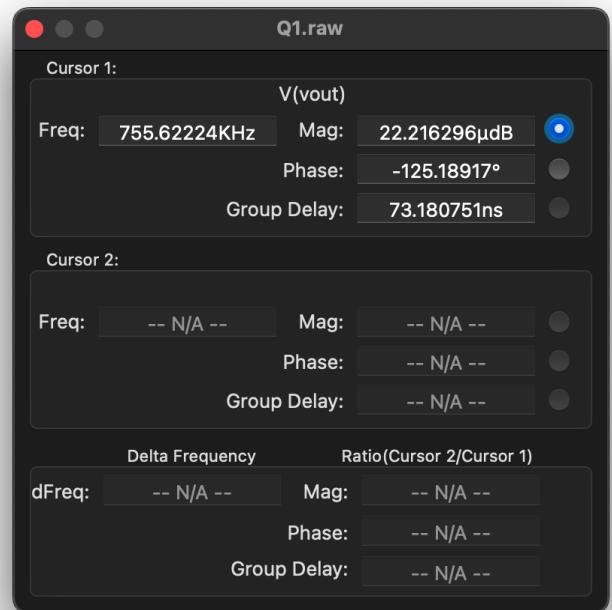
Bode Plot



For DC gain



For UGB



So DC gain:- 137.637dB or 7618158.42

UGB:- 755.62kHz

Macro model of the Op-Amp is as follows-

(Here we are designing for single pole upto UGB)

Writing KCL at node A-

$$i_R + i_C = g_m V_e$$

Also-

$$V_1 = i_R R = \frac{i_c}{sC}$$

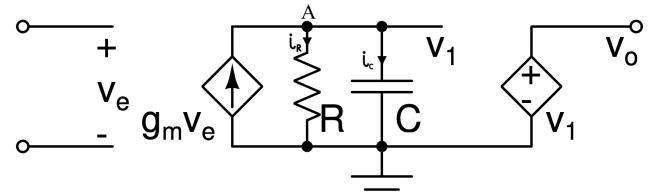
Using the above two equations, we get the following relation

$$\frac{V_1}{V_e} = \frac{g_m R}{1 + sRC}$$

The gain at DC is when  $s = 0$ , so  $g_m R = 7618158.42$

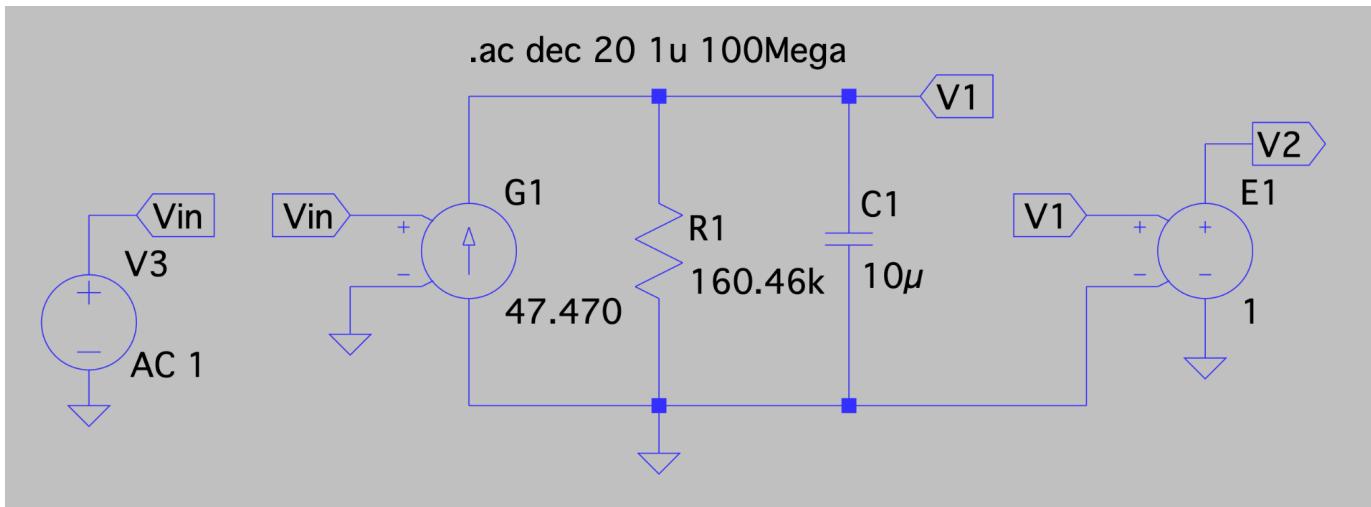
Now the UGB occurs at  $f = 755.62\text{kHz}$ , so substituting  $\omega = 2\pi * 755.62 * 10^3$  and value of  $g_m R$  in the gain equation we get  $RC = 1.604$

Dividing both the equations, we get  $\frac{g_m}{C} = 4747700.481$



For this experiment, I took C as  $10\mu F$ ,  $g_m$  as  $47.470$  and R as  $160.459k\Omega$ .

### Testbench for Macro-Model



Bode Plot



This is a good approximation for a single pole Op-Amp as both magnitude and phase plots overlap significantly upto  $\sim 25kHz$  but after that there are significant deviations in phase plot and slight deviation in magnitude from UGB frequency of Op-Amp due to the second pole in LT1013.

## 2. Design an instrumentation amplifier using LT1013 with

$$V_o = 4(V_1 - V_2)$$

Variation in Signal Frequency < 100m dB

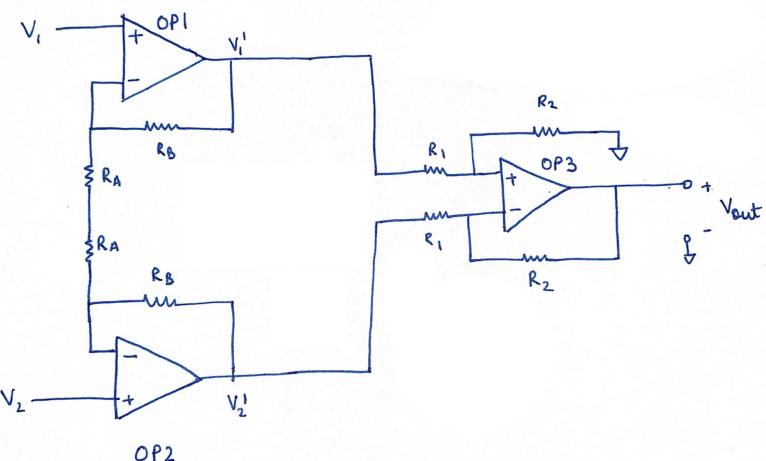
Load Resistance:  $10\text{k}\Omega$

Supply Voltage: 30V

Total Bias Current  $\leq 1\text{mA}$

Resistance Available:  $1\text{k}\Omega - 10\text{k}\Omega$

We can use the circuit from Lecture 30 as shown here-



Here, OP1 and OP2 act as voltage buffers and OP3 acts as a differential amplifier with gain  $\frac{R_2}{R_1}$ . The only issue with this circuit is that the supply voltage is from 0V to 30V but the above circuit is designed for negative voltages. So we can implement the method developed in Lecture 14 where we couple the input voltages with appropriate capacitors and biasing voltage and replace the GND of R<sub>2</sub> from OP3 with bias voltage.

An example has been shown in the adjacent image.

In our case, we have the supply voltage at 30V so we need V<sub>ss</sub> to be 15V.

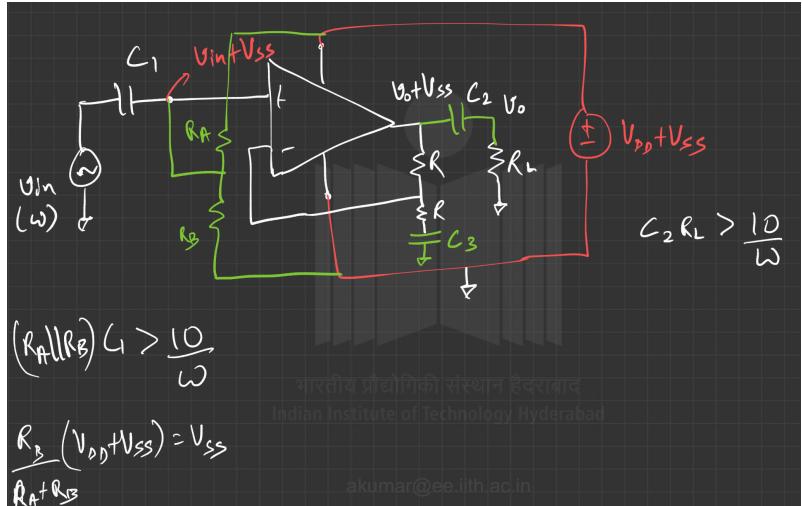
So we have to set  $R_A = R_B$ .

Now the condition on resistors and capacitors is that-

$$(R_A \parallel R_B) * C > \frac{10}{2\pi f}$$

As  $R_A = R_B$ ,  $R_A \parallel R_B = \frac{R_A}{2}$  and we have to maximize RHS so we take  $f = 1\text{kHz}$ .

(This condition is based on the fact that the time constant of the RC circuit must be much greater than the time period of input frequencies so that the capacitor does not discharge).



Now to minimize the capacitance used, we can maximize the resistance  $R_A$  to  $100k\Omega$  (this also helps in restricting bias current) as specified in the question. Plugging these values we get  $C > 31.83nF$ .

In this experiment, I took capacitance as  $0.2\mu F$ .

Now from class lectures, we had-

$$V_o \approx \left(1 + \frac{R_B}{R_A}\right) \frac{R_2}{R_1} (V_1 - V_2) \quad \& \quad CMRR = \frac{A_D}{A_{CM}} \left(1 + \frac{R_B}{R_A}\right)$$

We require the gain of the differential amplifier to be 4 and also to maximize CMRR. Assuming that the magnitude of input voltages do not exceed 1V (as it is required further in question and also to maximize CMRR), the maximum output voltage will be  $(15V+8V)$  when  $V_1$  is  $(15V+1V)$  and  $V_2$  is  $(15V-1V)$  which is acceptable as maximum voltage tolerable by Op-Amps is 30V. But for OP1 we have-

$$V'_1 = \left(1 + \frac{R_B}{2R_A}\right) V_1 - \frac{R_B}{2R_A} V_2$$

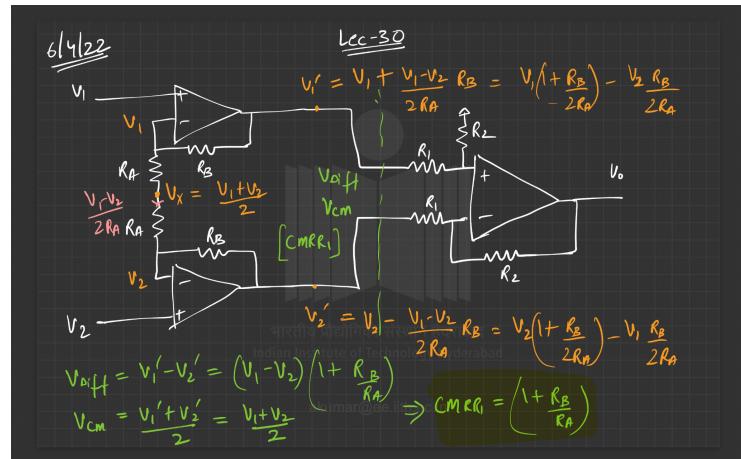
So  $V'_1$  is maximized when  $V_1$  is  $(15V+1V)$  and  $V_2$  is  $(15V-1V)$ , also  $V'_1$  must be less than 30V. So plugging in the values we get-

$$\frac{R_B}{R_A} \leq 14$$

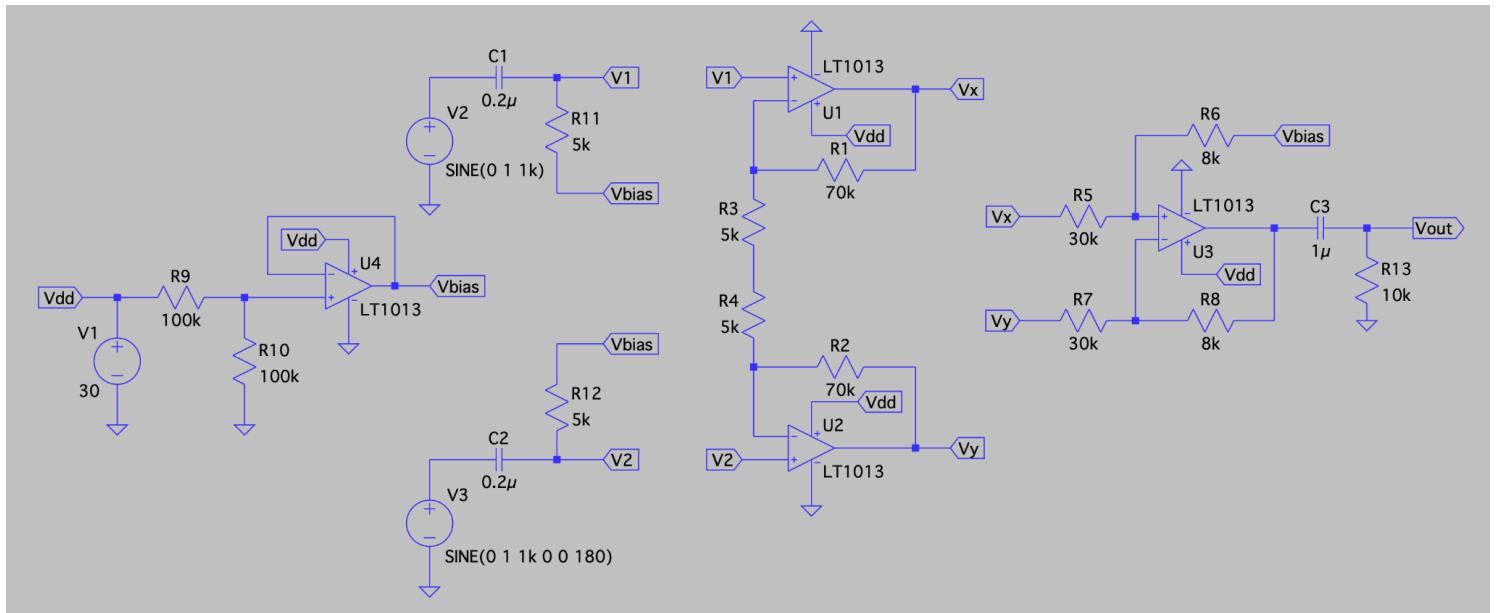
We get the same relation for  $V'_2$  by substituting  $V_2$  as  $(15V+1V)$  and  $V_1$  as  $(15V-1V)$ .

So for this experiment, I took  $R_A$  as  $5k\Omega$  and  $R_B$  as  $70k\Omega$ . Since the gain of the differential amplifier is required to be 4, substituting  $R_A$  and  $R_B$  values in the above expression we can take  $R_1$  as  $30k\Omega$  and  $R_2$  as  $8k\Omega$ . Also the CMRR for OP1 and OP2 is 15 and for OP3 is  $\frac{15A_D}{A_{CM}}$ .

(Note that I have mentioned  $15V+...$  or  $15V-...$  and that is due to the biasing voltages that we have to maintain for proper operation)

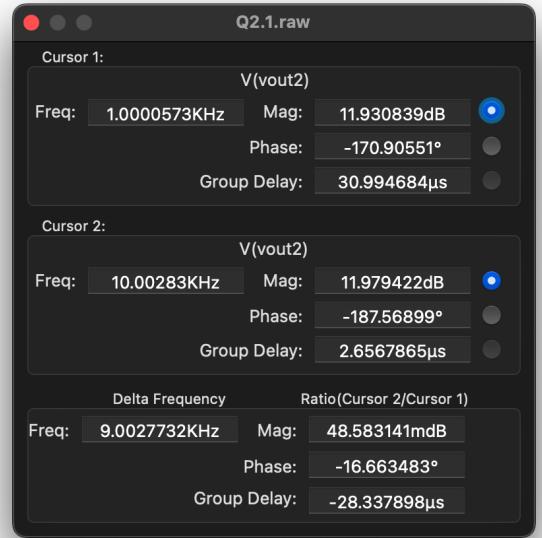
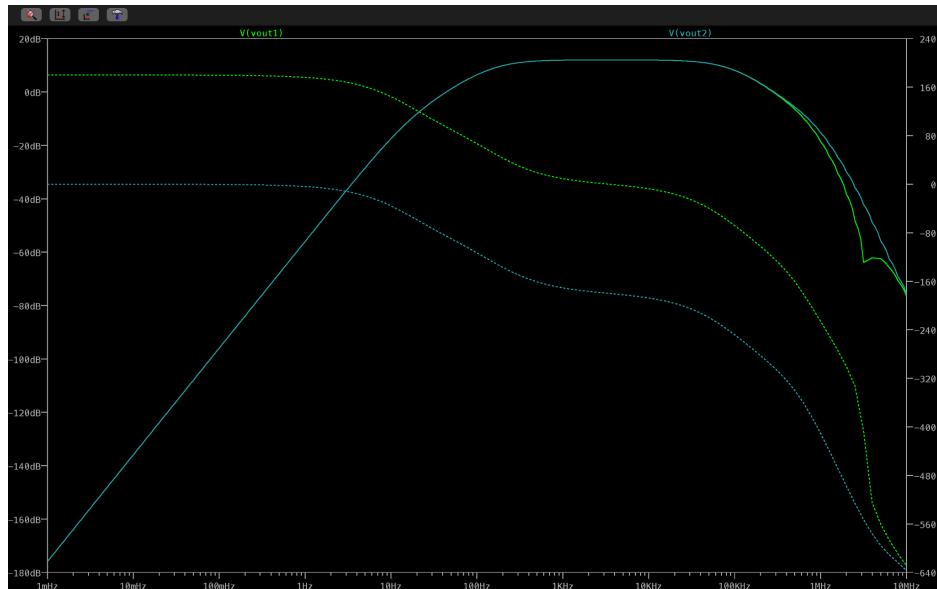


## Implementation in LTSpice



Also note that I have added a resistance before the biasing voltage to control the biasing current and have added a  $1\mu\text{F}$  capacitor before load resistance to remove the DC component (15V) from the signal otherwise the given relation will not follow as it would have a 15V DC component.

Frequency response for one input at a time

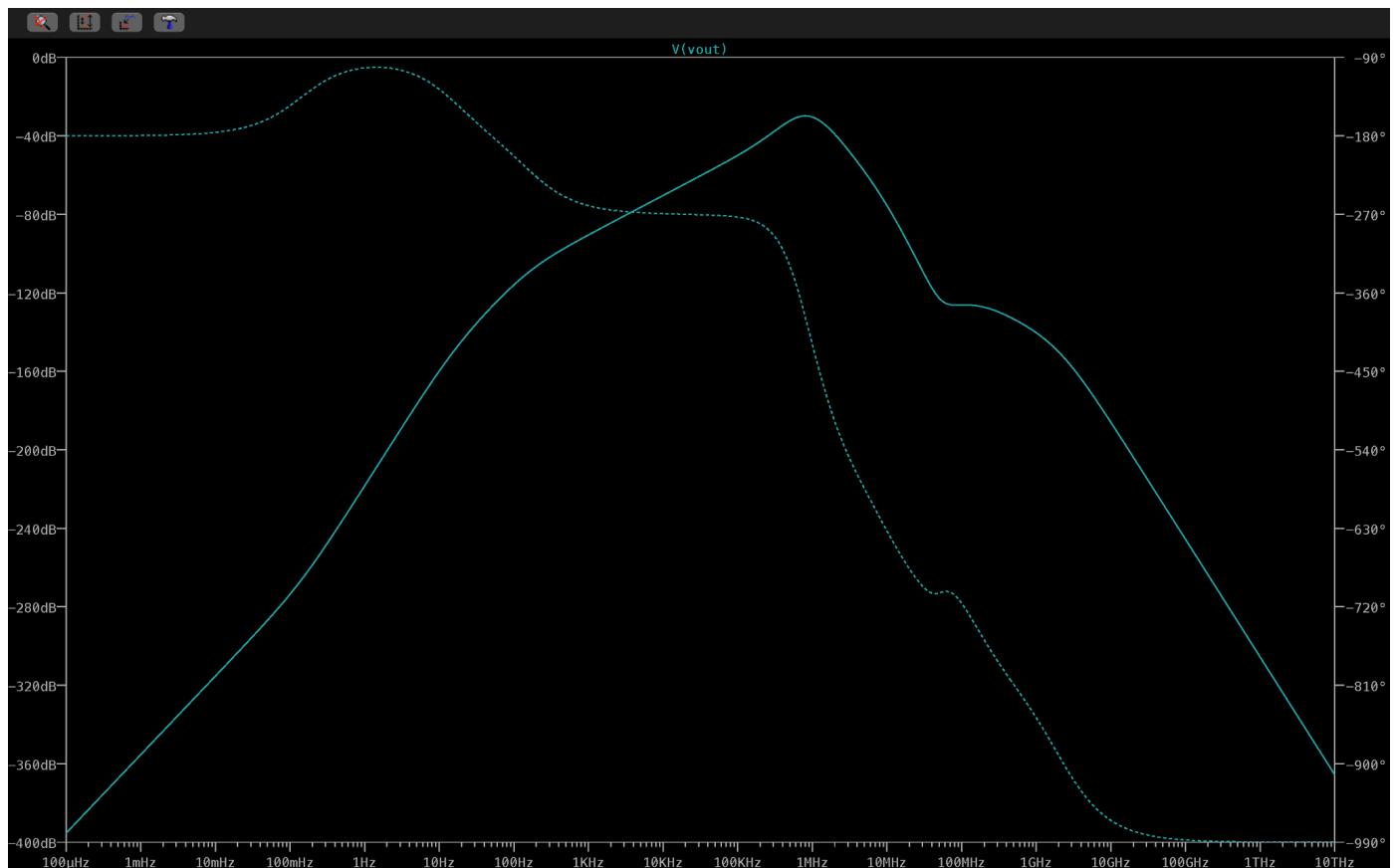


Some observations-

- When  $V_1$  is varied and  $V_2$  is 0V, we have  $V_{\text{out}} = 4V_1$  and when  $V_2$  is varied and  $V_1$  is 0V we have  $V_{\text{out}} = -4V_2$ . This means that the magnitude plots must be the same and phase plots should differ by  $180^\circ$  as  $-1 = e^{j\pi}$ .

- 2) The magnitude plots exactly trace each other as seen in the image except at higher frequencies due to unpredictable behavior of Op-Amps. Also they look similar to high pass filter response.
- 3) The phase plot of case 1 leads the phase plot of case 2 by  $180^\circ$  except at higher frequencies due to unpredictable behavior of Op-Amps.
- 4) Also the variation in gain at 1kHz and 10kHz is 48.583dB which is well under the required range.
- 5) So all results are as expected.

Frequency response when both inputs are varied



Some observations-

- 1) The magnitude and phase responses look like band pass filters but with very small gain (peak is around -40dB).
- 2) Due to the non-ideality of Op-Amp the output is not exactly 0 and hence there is small variation in voltage.
- 3) So we can say that the system subtracts the two voltages but since Op-Amp is non-ideal the output is not zero but close to zero.