

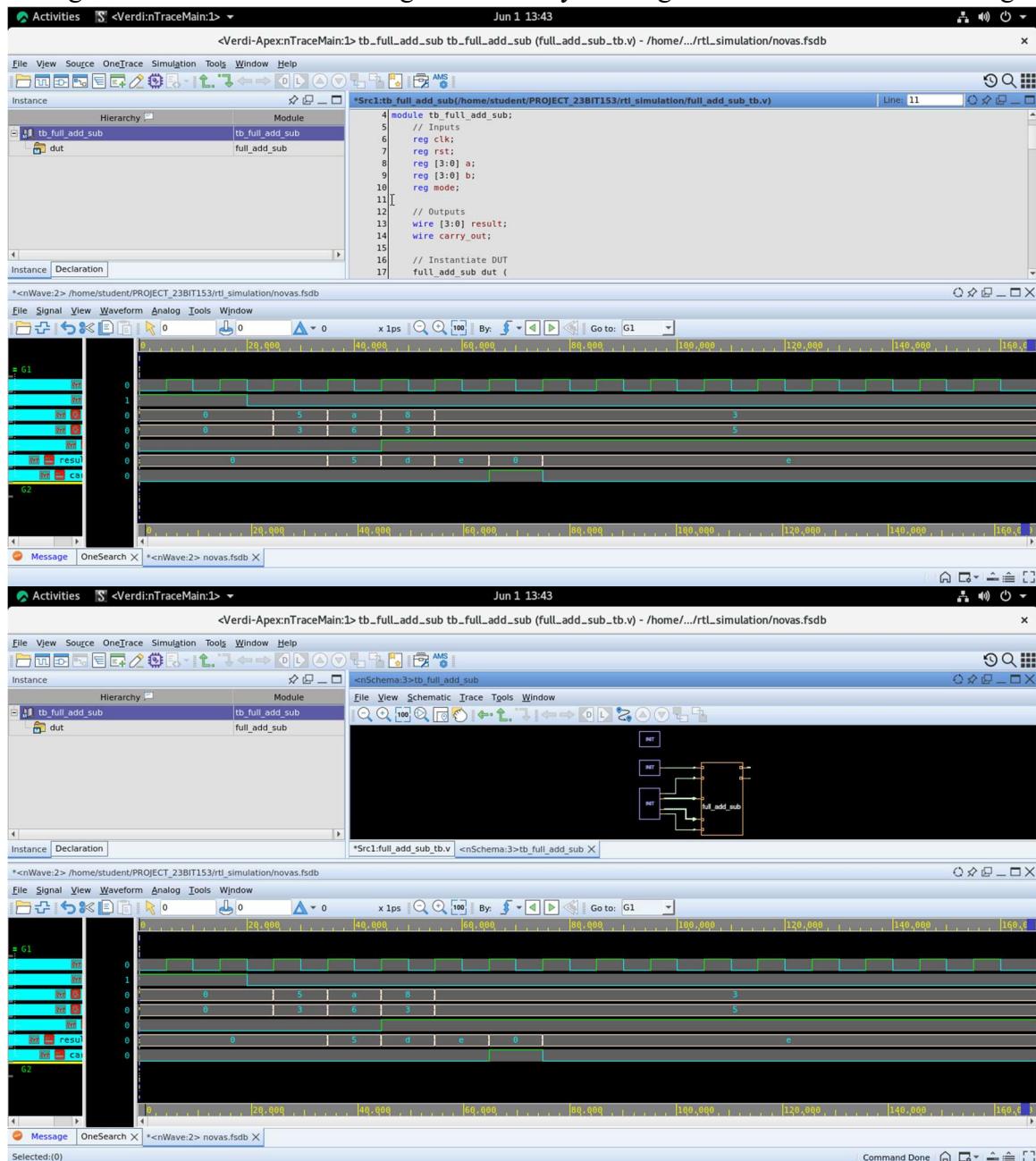
PROJECT REPORT

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Roll Number: 23BIT153

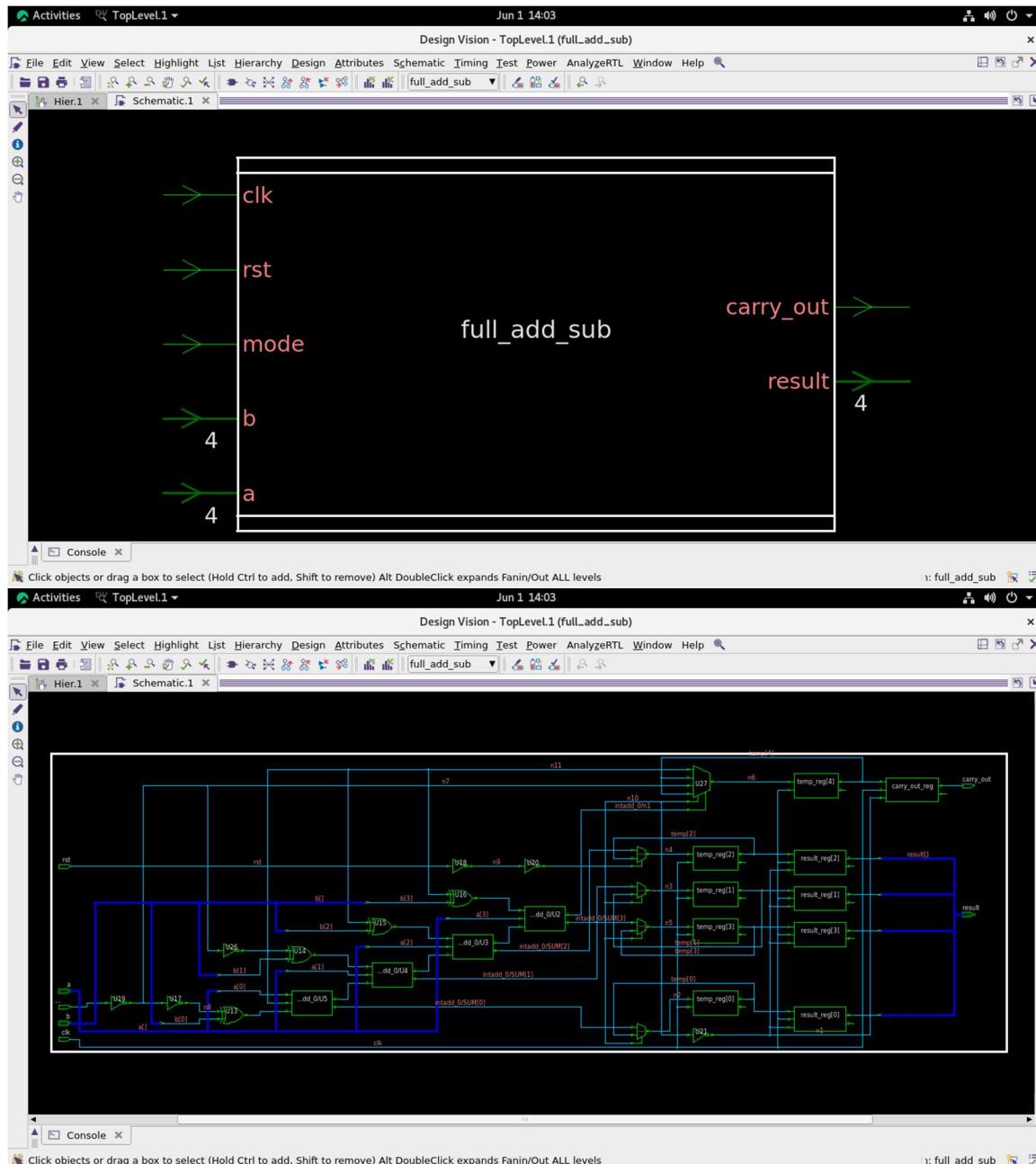
Topic: 4-bit Full Adder-Subtractor

We began the project by creating the RTL and testbench files for the 4-bit adder-subtractor circuit. Simulation was performed using Verdi, where we analyzed both the timing waveforms and block diagram to verify the logical correctness of our design.



Synthesis Phase (Design Compiler)

We used Design Compiler (DC) to synthesize the RTL into a gate-level netlist. Before synthesis, the constraints file (SDC) was updated with proper clock definitions and timing constraints. The primary goal was to ensure the slack remains positive and close to zero, ideally under 1 ns. This step enabled area and timing optimization for the synthesized design.



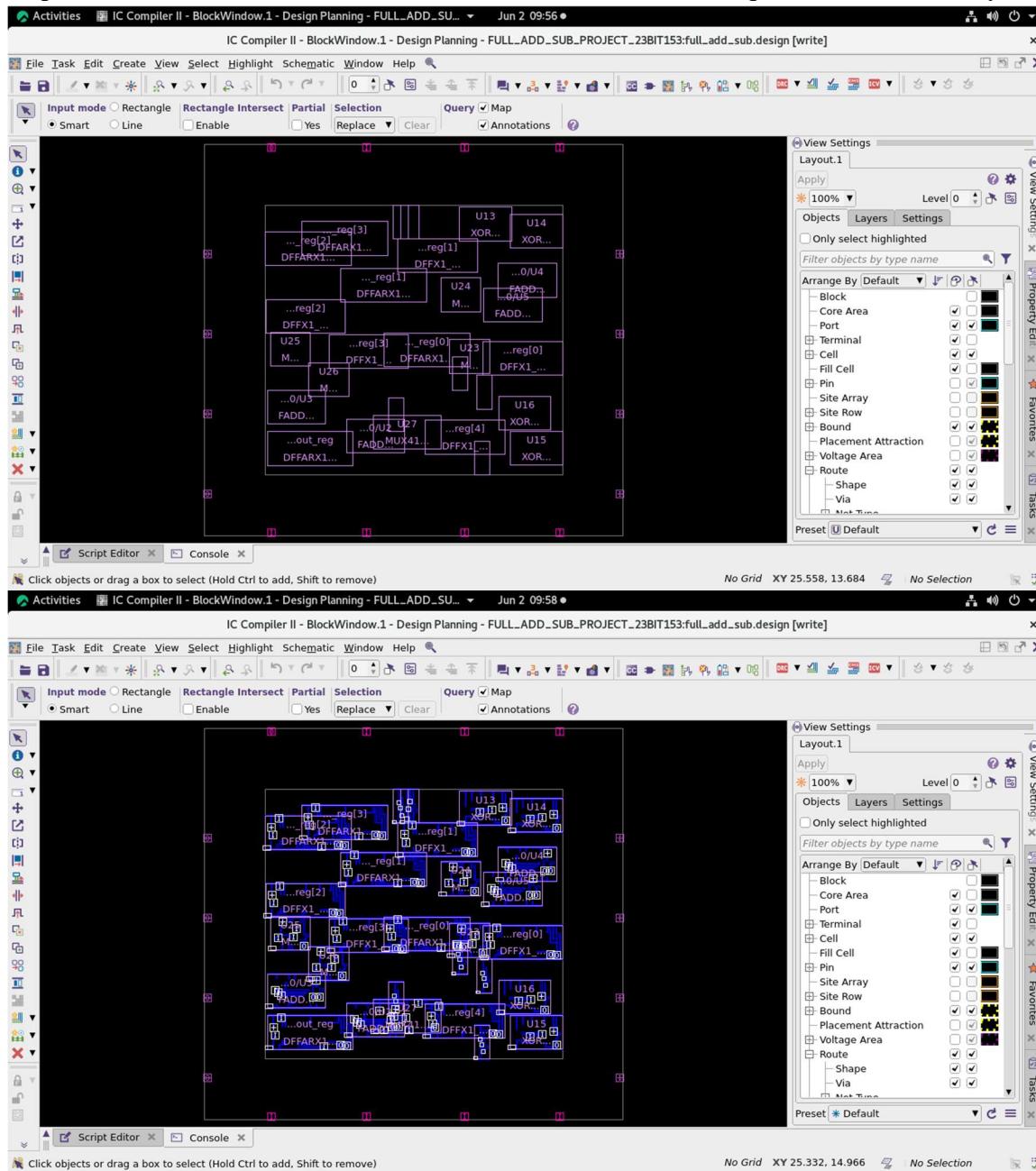
ICC2 Design Compiler

Library used: TT [typical Typical]

Clock time period constraint: 3ns

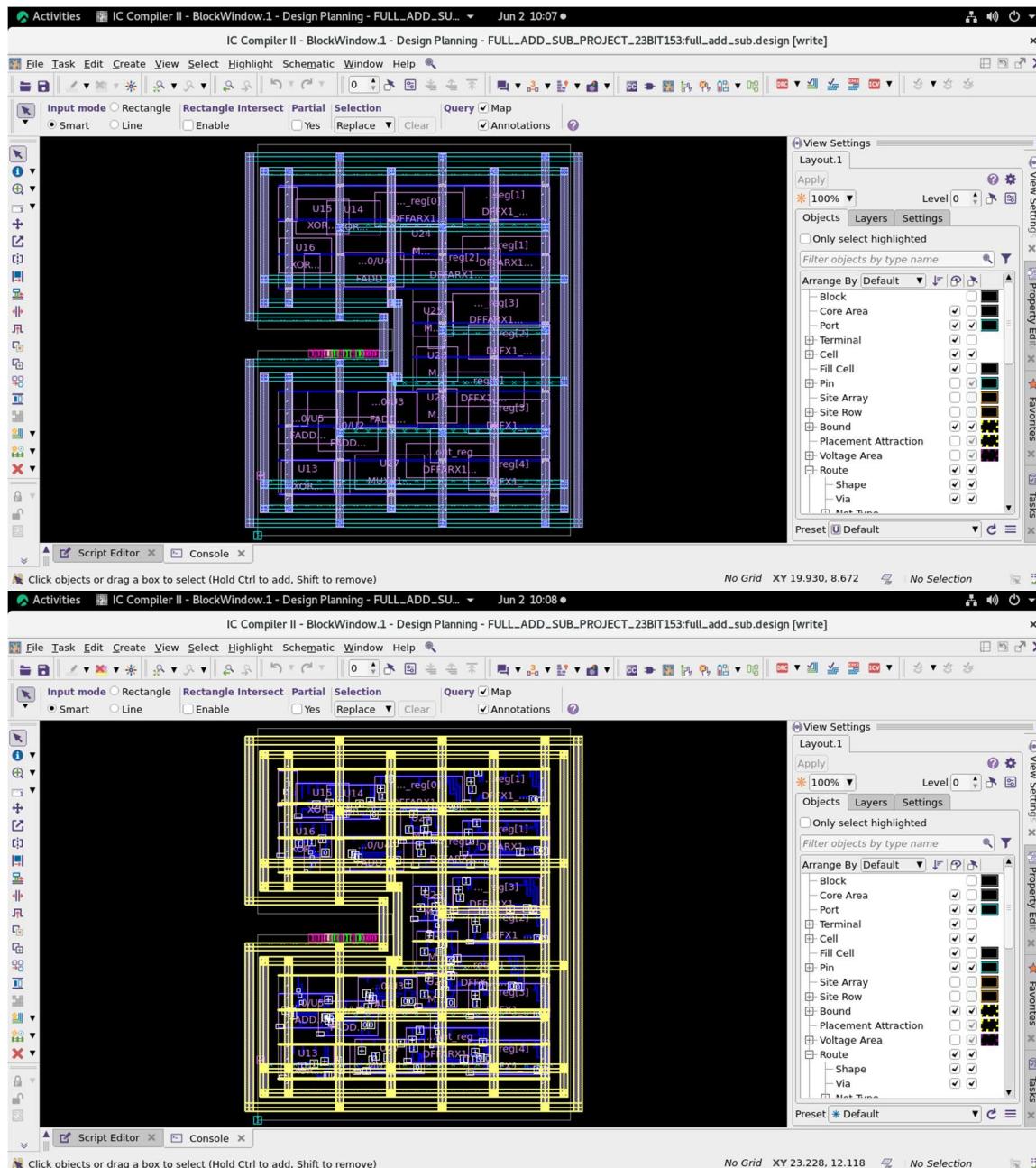
Floorplanning

After successful synthesis, we moved to ICC2 Shell to initiate the physical design flow. The floorplan script was executed to define the die size, core utilization, and IO pin placement. After that, the Graphical User Interface (GUI) was launched to visually inspect the initial floorplan layout.



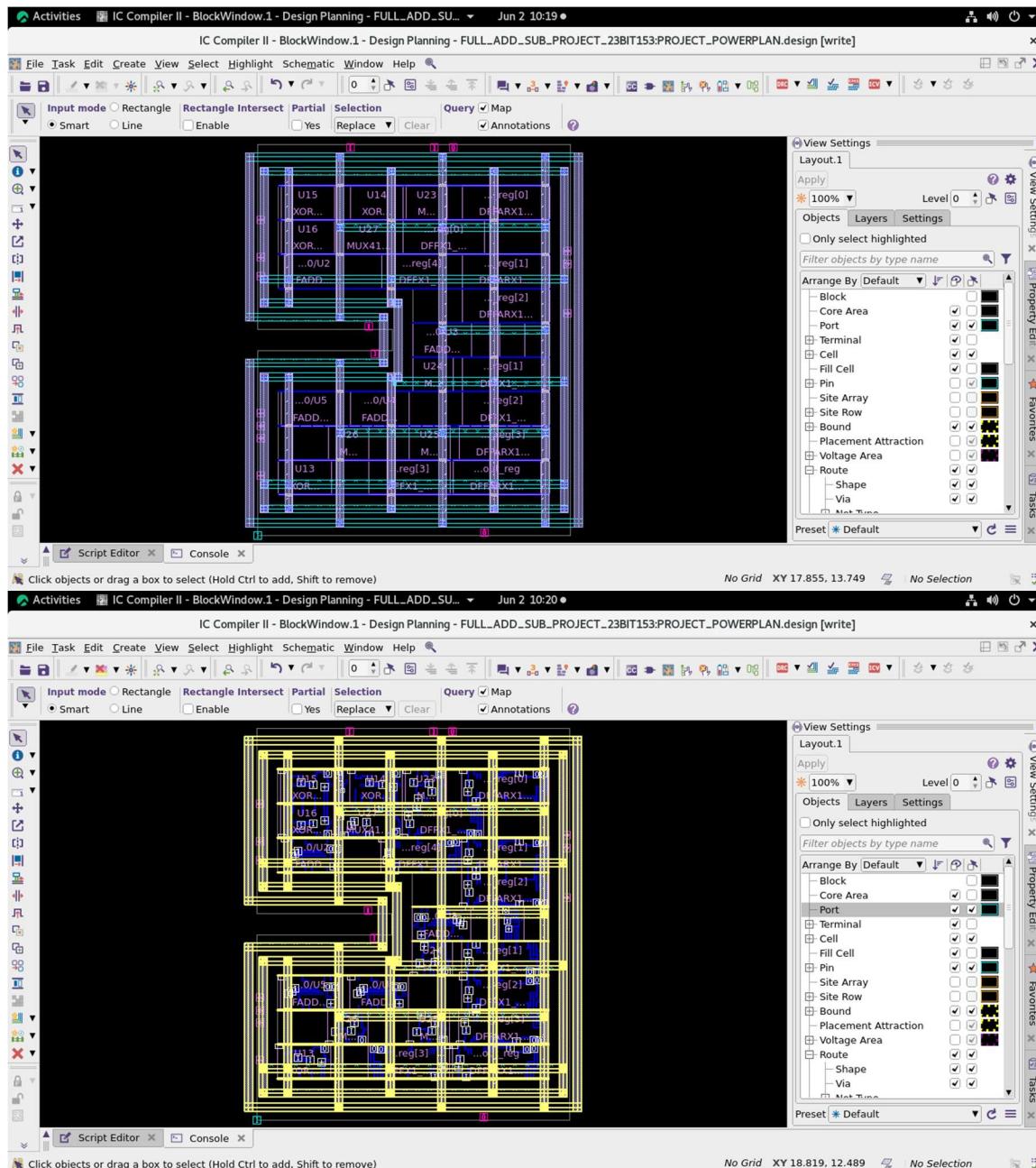
Power Planning

Power planning was implemented next using ICC2, where we executed the power planning script. This involved designing the power rings, straps, and rails to ensure even power distribution and support for dynamic switching activity across the 4-bit adder-subtractor blocks.



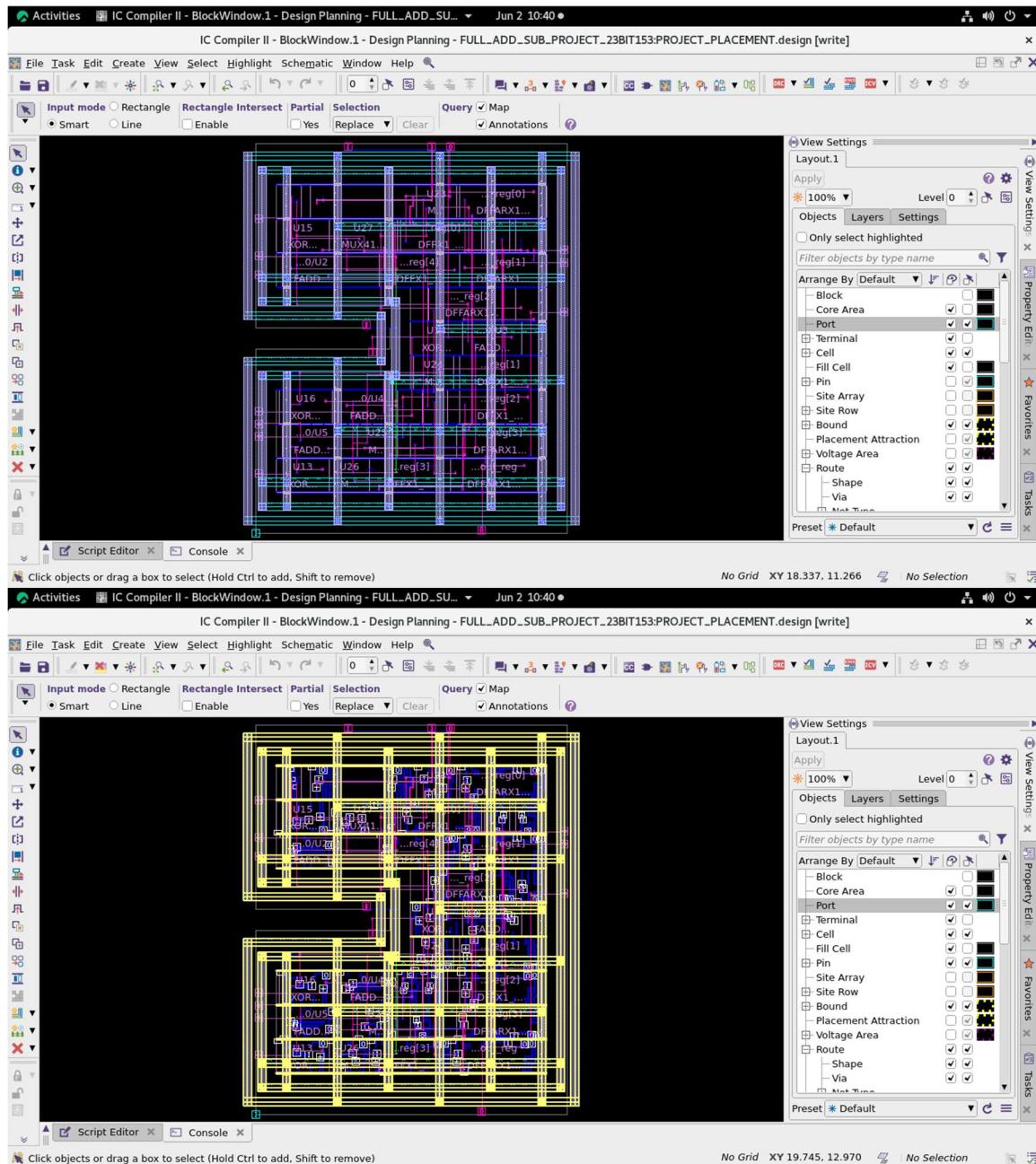
Placement

With power planning complete, we proceeded to standard cell placement. Using the placement script, the synthesized cells were legally placed within the defined floorplan. Placement optimization was guided by timing and congestion analysis to achieve minimal wirelength and better timing slack.



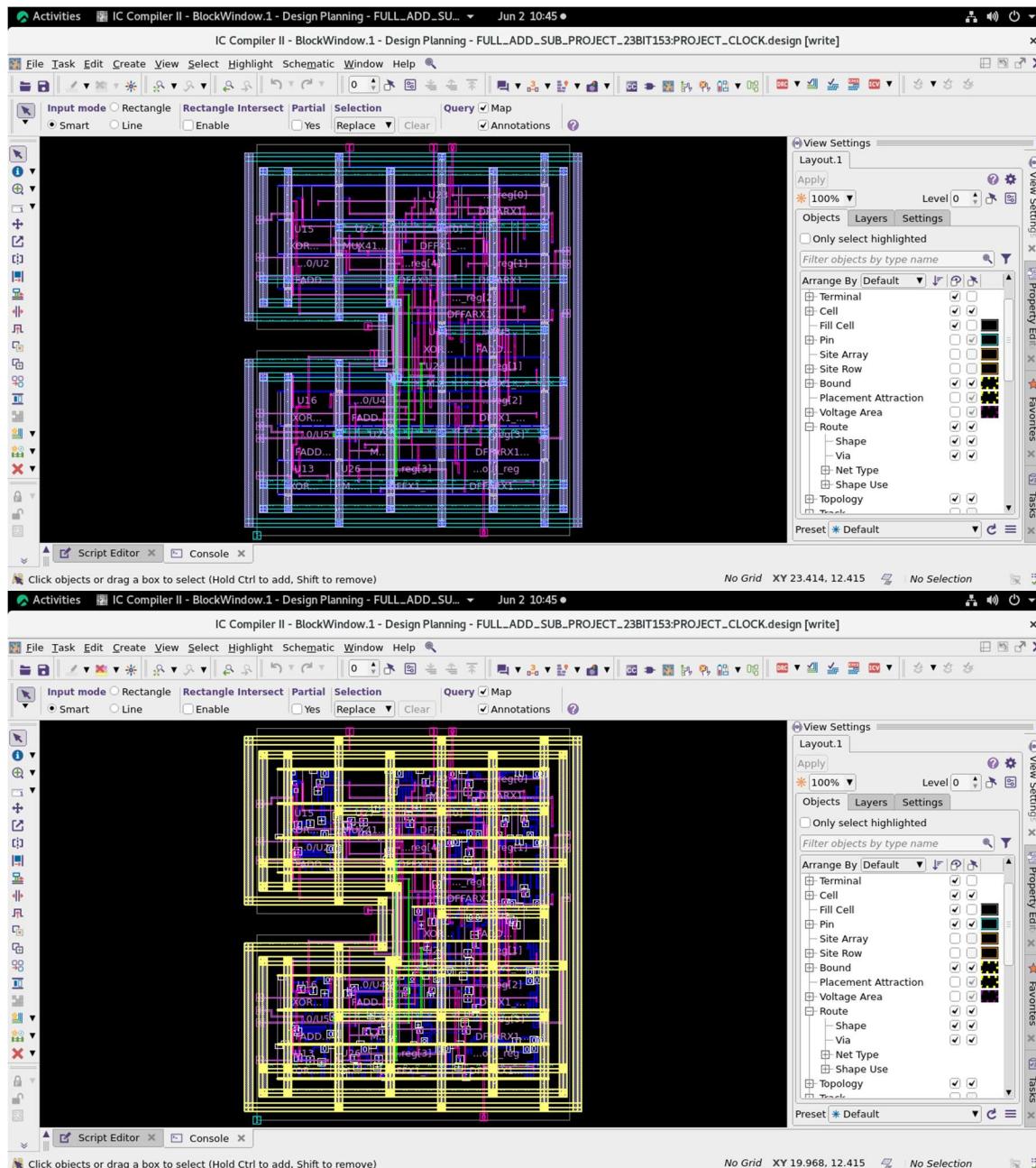
Clock Tree Synthesis (CTS)

The clock network was constructed using the CTS script. Buffers and inverters were strategically inserted to balance clock skew and latency, ensuring reliable clock distribution to all sequential elements of the design.



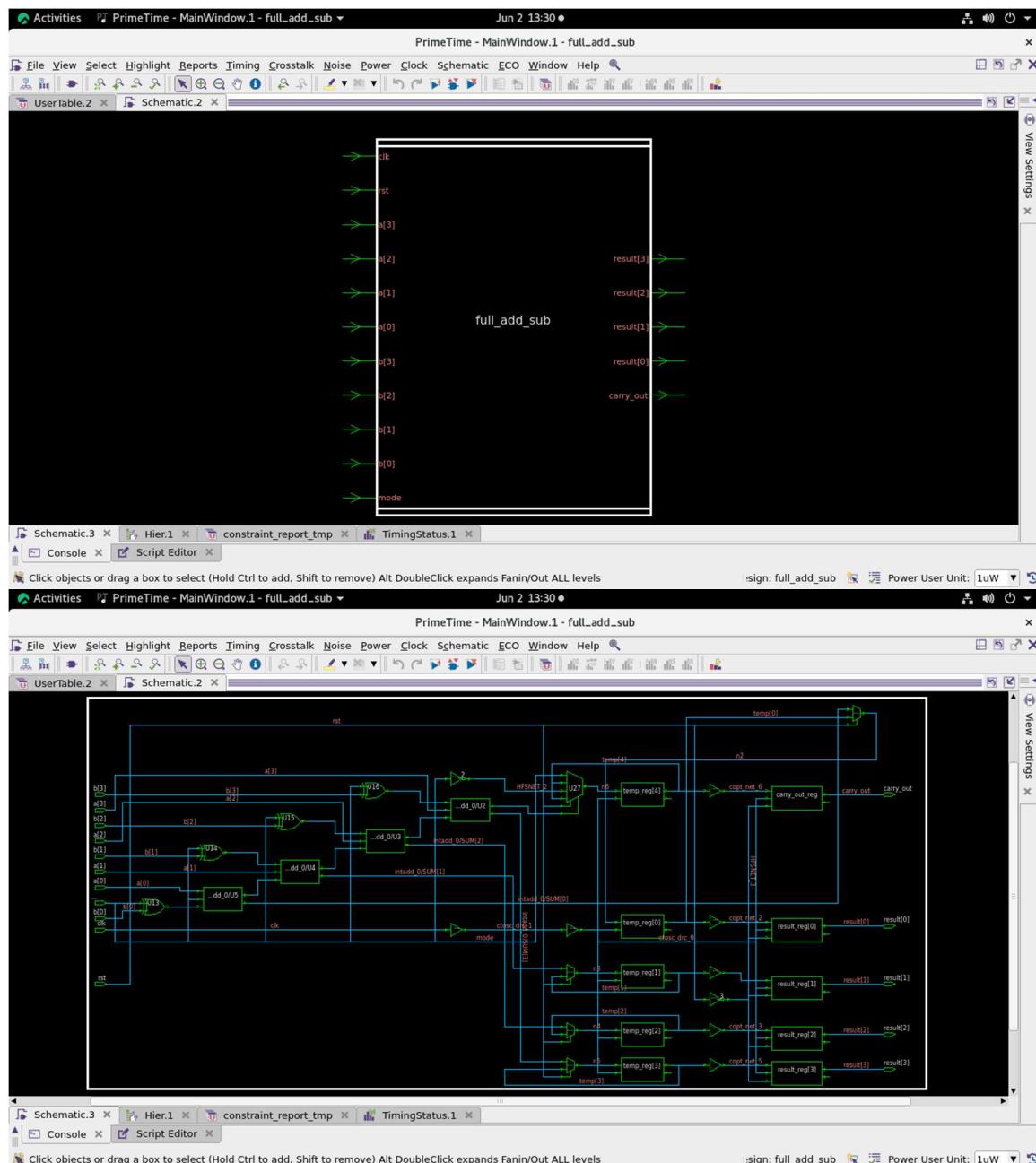
Routing

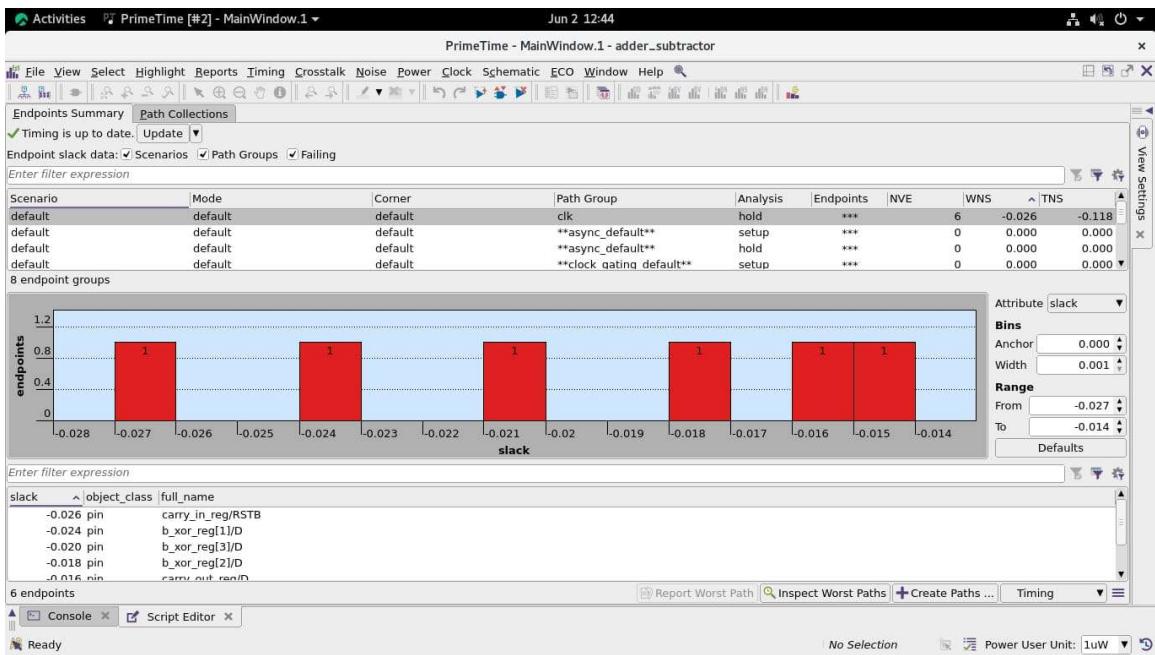
Routing was performed using the routing script in ICC2. Both global and detailed routing phases were completed, connecting all logic elements with minimal detours and respecting design rules. Special attention was given to avoid congestion and reduce crosstalk on critical nets.



Timing Analysis (PrimeTime)

After routing, PrimeTime (PT) was used to analyze final timing. Using PT Shell, we generated the timing report and confirmed that the final design has a positive slack, again kept under 1 ns to meet design constraints. This validated the timing closure for the full adder-subtractor implementation.





Conclusion

We successfully designed and implemented a 4-bit full adder-subtractor using RTL-to-GDSII flow. Each stage—starting from RTL simulation to final timing verification—was executed with a focus on design optimization and constraint satisfaction. The final design meets functional and timing requirements, and is ready for physical signoff.

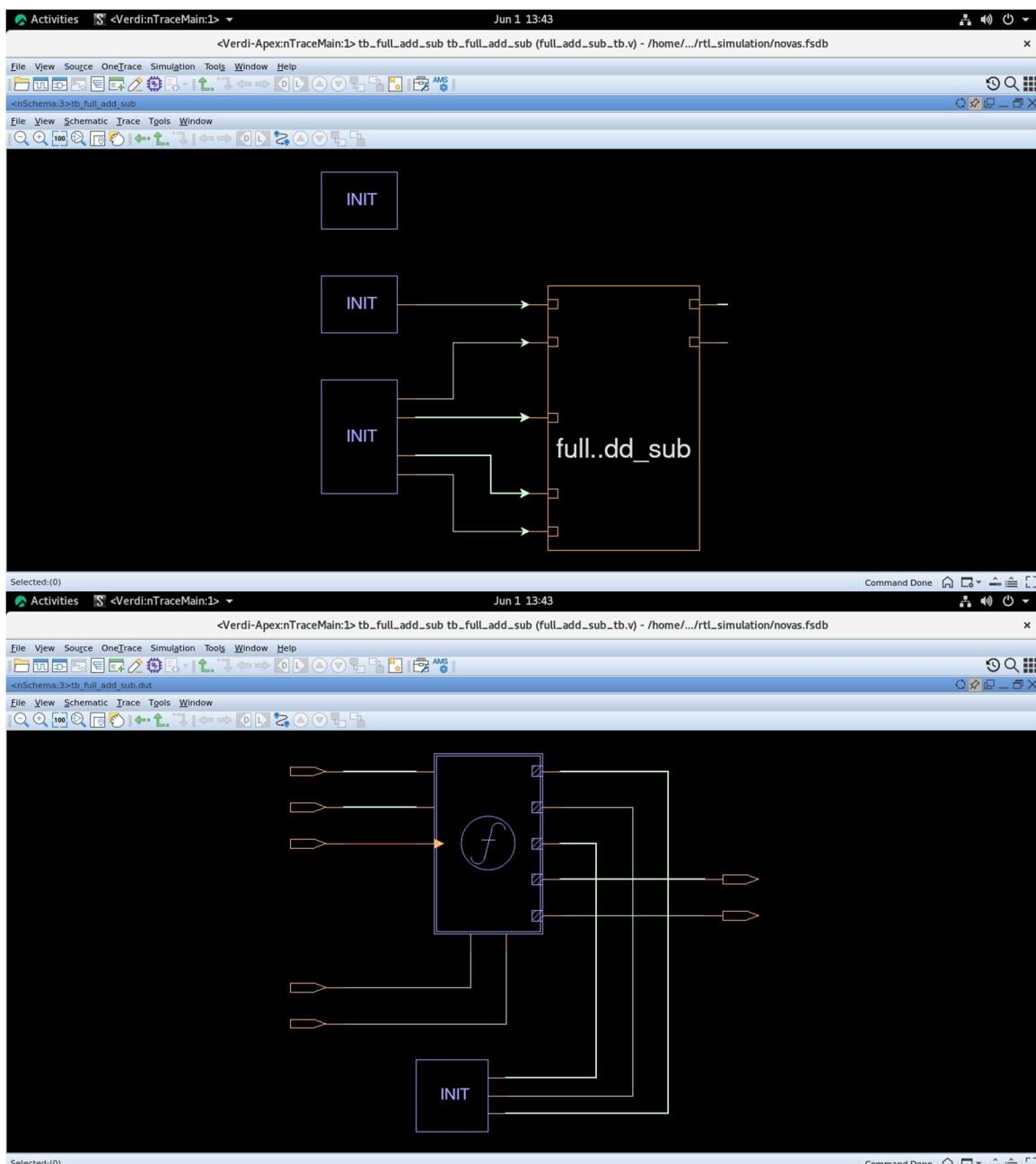
Introduction and Theoretical Background

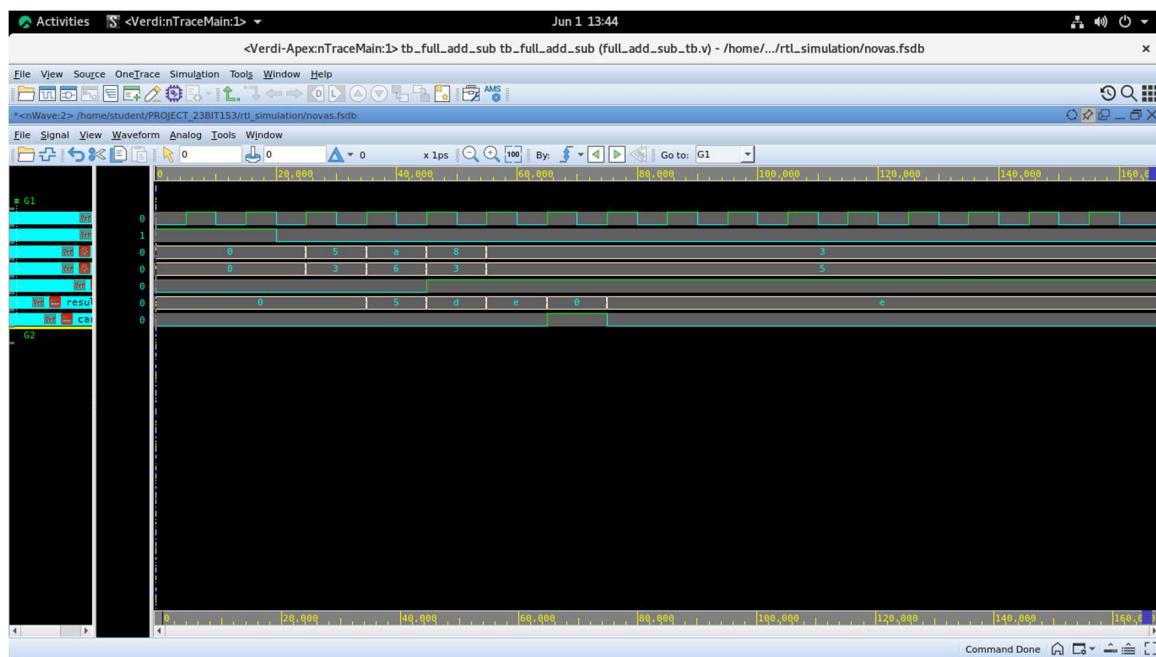
The 4-bit Full Adder-Subtractor is a combinational circuit capable of performing both addition and subtraction of binary numbers. The design uses basic logic gates to implement a series of full adders, with an XOR gate used to control the subtraction operation via a control input. When the control signal is active, the second operand is complemented, and a '1' is added to perform two's complement subtraction. This project involves implementing this functionality in Verilog HDL, followed by a complete RTL-to-GDSII flow to generate the physical layout.

Design Methodology

1. RTL Design and Simulation:

- The Verilog HDL code for the 4-bit Full Adder-Subtractor was written.
- Testbenches were created to validate the functionality.
- The design was compiled and simulated using **VCS** and **Verdi**, where timing waveforms and schematic diagrams were inspected for correctness.





2. Synthesis Using Design Compiler (DC):

- The synthesized gate-level netlist was generated using the `run.dc.tcl` script.
- Slack was analyzed at this step to ensure it remained between 0 and 1.
- Optimization was targeted towards area, timing, and power.

```

Activities Terminal Jun 2 09:49 ●
student@ict-chipin:~/PROJECT_23BIT153/DC

File Edit View Search Terminal Help
No. of Hold Violations: 0.00
-----
Cell Count
-----
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 29
Buf/Inv Cell Count: 6
Buf Cell Count: 0
Inv Cell Count: 6
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 19
Sequential Cell Count: 10
Macro Count: 0
-----
Area
-----
Combinational Area: 63.281855
Noncombinational Area: 68.618882
Buf/Inv Area: 7.878464
Total Buffer Area: 0.00
Total Inverter Area: 7.88
Macro/Black Box Area: 0.000000
Net Area: 7.209889
-----
Cell Area: 131.900737
Design Area: 139.118626

Design Rules
-----
Total Number of Nets: 44
Nets With Violations: 10
Max Trace Violations: 10
Activities Terminal Jun 2 09:49 ●
student@ict-chipin:~/PROJECT_23BIT153/DC

File Edit View Search Terminal Help
U27/Y (MUX4X1_RVT) 0.27 2.07 f
temp_reg[4]/D (DFFX1_RVT) 0.01 2.08 f
data arrival time 2.08
-----
clock clk (rise edge) 3.00 3.00
clock network delay (ideal) 0.00 3.00
clock uncertainty -0.30 2.70
temp_reg[4]/CLK (DFFX1_RVT) 0.00 2.70 r
library setup time -0.12 2.58
data required time 2.58
-----
data required time 2.58
data arrival time -2.08
-----
slack (MET) 0.49

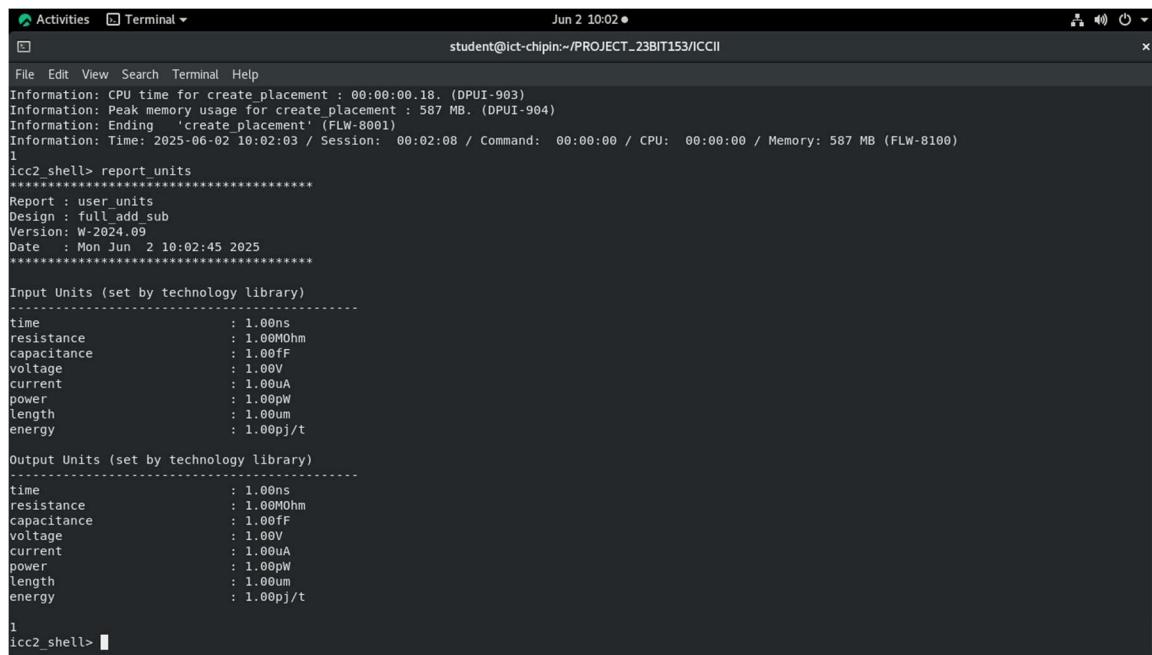
l
dc_shell>
dc_shell> report_units
*****
Report : units
Design : full_add_sub
Version: W-2024.09
Date : Mon Jun 2 09:49:57 2025
*****
Units
-----
Time_unit : 1.0e-09 Second(ns)
Capacitive_load_unit : 1.0e-15 Farad(fF)
Resistance_unit : 1.0e-6 Ohm(MOhm)
Voltage_unit : 1 Volt
Power_unit : N/A
Current_unit : 1.0e-06 Amp(uA)
1
dc_shell>

```

3. Physical Design in ICC2:

- **Floorplanning:** Defined die size, core area, and pin placement.

```
Activities Terminal Jun 2 09:59 ● student@ict-chipin:~/PROJECT_23BIT153/ICCI
File Edit View Search Terminal Help
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count: 0
Single-bit Sequential Cell Count: 10
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPerflip: 1.00
Macro Count: 0
-----
Area
-----
Combinational Area: 63.28
Noncombinational Area: 68.62
Buf/Inv Area: 7.88
Total Buffer Area: 0.00
Total Inverter Area: 7.88
Macro/Black Box Area: 0.00
Net Area: 0
Net Xlength: 218.17
Net Ylength: 159.38
-----
Cell Area (netlist): 131.90
Cell Area (netlist and physical only): 131.90
Net Length: 377.55
-----
Design Rules
-----
Total Number of Nets: 44
Nets with Violations: 0
Max Trans Violations: 0
Max Cap Violations: 0
-----
1
icc2_shell> [REDACTED]
Activities Terminal Jun 2 09:59 ● student@ict-chipin:~/PROJECT_23BIT153/ICCI
File Edit View Search Terminal Help
Smart Arc Optimization: disabled
*****
Cell Count
-----
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 29
Buf/Inv Cell Count: 6
Buf Cell Count: 0
Inv Cell Count: 6
Combinational Cell Count: 19
Single-bit Isolation Cell Count: 0
Multi-bit Isolation Cell Count: 0
Isolation Cell Banking Ratio: 0.00%
Single-bit Level Shifter Cell Count: 0
Multi-bit Level Shifter Cell Count: 0
Level Shifter Cell Banking Ratio: 0.00%
Single-bit ELS Cell Count: 0
Multi-bit ELS Cell Count: 0
ELS Cell Banking Ratio: 0.00%
Sequential Cell Count: 10
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count: 0
Single-bit Sequential Cell Count: 10
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPerflip: 1.00
Macro Count: 0
-----
Area
-----
Combinational Area: 63.28
Noncombinational Area: 68.62
```



```

Activities Terminal Jun 2 10:02 ●
student@ict-chipin:~/PROJECT_23BIT153/ICCI

File Edit View Search Terminal Help
Information: CPU time for create_placement : 00:00:00.18. (DPU1-903)
Information: Peak memory usage for create_placement : 587 MB. (DPU1-904)
Information: Ending 'create_placement' (FLW-8001)
Information: Time: 2025-06-02 10:02:03 / Session: 00:02:08 / Command: 00:00:00 / CPU: 00:00:00 / Memory: 587 MB (FLW-8100)
l
icc2_shell> report_units
*****
Report : user_units
Design : full_add_sub
Version: W-2024.09
Date : Mon Jun 2 10:02:45 2025
*****

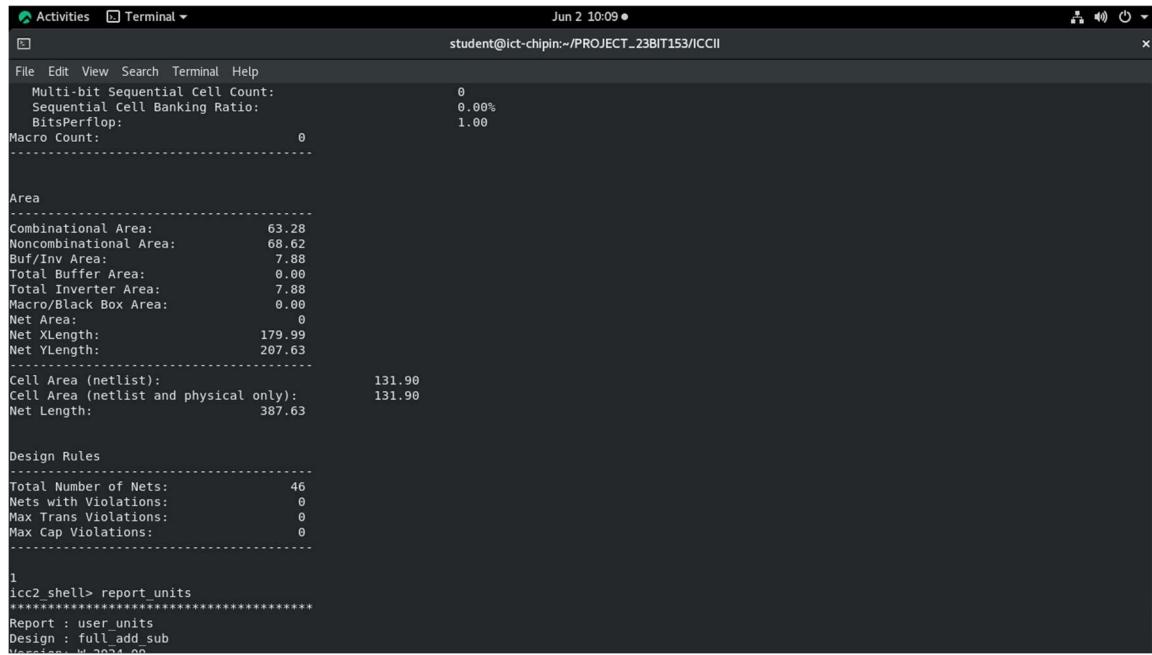
Input Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00Mohm
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

Output Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00Mohm
capacitance : 1.00ff
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

l
icc2_shell>

```

- Power Planning: Created power rings and straps for robust distribution.



```

Activities Terminal Jun 2 10:09 ●
student@ict-chipin:~/PROJECT_23BIT153/ICCI

File Edit View Search Terminal Help
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPer flop: 1.00
Macro Count: 0

Area
-----
Combinational Area: 63.28
Noncombinational Area: 68.62
Buf/Inv Area: 7.88
Total Buffer Area: 0.00
Total Inverter Area: 7.88
Macro/Black Box Area: 0.00
Net Area: 0
Net XLength: 179.99
Net YLength: 207.63

Cell Area (netlist): 131.90
Cell Area (netlist and physical only): 131.90
Net Length: 387.63

Design Rules
-----
Total Number of Nets: 46
Nets with Violations: 0
Max Trans Violations: 0
Max Cap Violations: 0

l
icc2_shell> report_units
*****
Report : user_units
Design : full_add_sub
Version: W-2024.09

```

The image shows two terminal windows side-by-side, both titled "Terminal". The top window displays a detailed report of cell counts for a design. The bottom window shows the ICC2 shell prompt, listing units and reporting no violations.

```
student@ict-chipin:~/PROJECT_23BIT153/ICCII
```

```
File Edit View Search Terminal Help
ML Acceleration: off
Smart Arc Optimization: disabled
*****
```

```
Cell Count
-----
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 29
Buf/Inv Cell Count: 6
Buf Cell Count: 0
Inv Cell Count: 6
Combinational Cell Count: 19
  Single-bit Isolation Cell Count: 0
  Multi-bit Isolation Cell Count: 0
  Isolation Cell Banking Ratio: 0.00%
  Single-bit Level Shifter Cell Count: 0
  Multi-bit Level Shifter Cell Count: 0
  Level Shifter Cell Banking Ratio: 0.00%
  Single-bit ELS Cell Count: 0
  Multi-bit ELS Cell Count: 0
  ELS Cell Banking Ratio: 0.00%
Sequential Cell Count: 10
  Integrated Clock-Gating Cell Count: 0
  Sequential Macro Cell Count: 0
  Single-bit Sequential Cell Count: 10
  Multi-bit Sequential Cell Count: 0
  Sequential Cell Banking Ratio: 0.00%
  BitsPer flop: 1.00
Macro Count: 0
```

```
Area
-----
Combinational Area: 62.20
```

```
student@ict-chipin:~/PROJECT_23BIT153/ICCII
```

```
File Edit View Search Terminal Help
Max Trans Violations: 0
Max Cap Violations: 0
-----
```

```
1
icc2 shell> report_units
*****
Report : user_units
Design : full_add_sub
Version: W-2024.09
Date : Mon Jun 2 10:08:57 2025
*****
```

```
Input Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MΩ
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t
```

```
Output Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MΩ
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t
```

```
1
icc2 shell>
```

- **Placement:** Legally placed standard cells while minimizing congestion.

```
Activities Terminal Jun 2 10:21 ● student@ict-chipin:~/PROJECT_23BIT153/ICCI
File Edit View Search Terminal Help
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count: 0
Single-bit Sequential Cell Count: 10
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPer flop: 1.00
Macro Count: 0

Area
-----
Combinational Area: 58.71
Noncombinational Area: 68.62
Buf/Inv Area: 3.30
Total Buffer Area: 0.00
Total Inverter Area: 3.30
Macro/Black Box Area: 0.00
Net Area: 0
Net XLength: 130.32
Net YLength: 188.36
-----
Cell Area (netlist): 127.33
Cell Area (netlist and physical only): 127.33
Net Length: 318.68

Design Rules
-----
Total Number of Nets: 42
Nets with Violations: 10
Max Trans Violations: 10
Max Cap Violations: 0
-----
1
icc2_shell> [REDACTED]
Activities Terminal Jun 2 10:21 ● student@ict-chipin:~/PROJECT_23BIT153/ICCI
File Edit View Search Terminal Help

Cell Count
-----
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 25
Buf/Inv Cell Count: 2
Buf Cell Count: 0
Inv Cell Count: 2
Combinational Cell Count: 15
    Single-bit Isolation Cell Count: 0
    Multi-bit Isolation Cell Count: 0
    Isolation Cell Banking Ratio: 0.00%
    Single-bit Level Shifter Cell Count: 0
    Multi-bit Level Shifter Cell Count: 0
    Level Shifter Cell Banking Ratio: 0.00%
    Single-bit ELS Cell Count: 0
    Multi-bit ELS Cell Count: 0
    ELS Cell Banking Ratio: 0.00%
Sequential Cell Count: 10
    Integrated Clock-Gating Cell Count: 0
    Sequential Macro Cell Count: 0
    Single-bit Sequential Cell Count: 10
    Multi-bit Sequential Cell Count: 0
    Sequential Cell Banking Ratio: 0.00%
    BitsPer flop: 1.00
Macro Count: 0

Area
-----
Combinational Area: 58.71
Noncombinational Area: 68.62
Buf/Inv Area: 3.30
Total Buffer Area: 0.00
Total Inverter Area: 3.30
Macro/Black Box Area: 0.00
```

The image shows two terminal windows side-by-side. Both windows have a dark theme and are titled 'Activities Terminal'. The top window shows the results of a timing analysis command:

```

File Edit View Search Terminal Help
Endpoint: temp_reg[4] (rising edge-triggered flip-flop clocked by clk)
Mode: func
Corner: nom
Scenario: func::nom
Path Group: **in2reg_default**
Path Type: max

Point Incr Path
-----
clock clk (rise edge) 0.00 0.00
clock network delay (ideal) 0.00 0.00
input external delay 0.50 0.50 f
b[0] (in) 0.00 0.50 f
U13/Y (XOR2X1_RVT) 0.17 0.67 f
intadd_0/U5/C0 (FAADDX1_RVT) 0.06 0.73 f
intadd_0/U4/C0 (FAADDX1_RVT) 0.06 0.79 f
intadd_0/U3/C0 (FAADDX1_RVT) 0.06 0.85 f
intadd_0/U2/C0 (FAADDX1_RVT) 0.07 0.91 f
U27/Y (MUX4X1X1_RVT) 0.07 0.99 f
temp_reg[4]/D (DFFX1_RVT) 0.00 0.99 f
data arrival time 0.99

clock clk (rise edge) 3.00 3.00
clock network delay (ideal) 0.00 3.00
temp_reg[4]/CLK (DFFX1_RVT) 0.00 3.00 r
clock uncertainty -0.30 2.70
library setup time -0.05 2.65
data required time 2.65
data arrival time -0.99

slack (MET) 1.66

```

The bottom window shows the results of a report command:

```

1
icc2_shell> [REDACTED]
Activities Terminal Jun 2 10:23 ● student@ict-chipin:~/PROJECT_23BIT153/ICCII
File Edit View Search Terminal Help
Max Cap Violations: 0
-----
1
icc2 shell> gui_change_highlight -remove -all_colors
icc2 shell> report_units
*****
Report : user_units
Design : full_add_sub
Version: W-2024.09
Date : Mon Jun 2 10:23:01 2025
*****
Input Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MΩ
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t
Output Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MΩ
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t
1
icc2_shell>

```

- **Clock Tree Synthesis (CTS):** Designed balanced clock trees to reduce skew.

```
Activities Terminal Jun 2 10:41 ● student@ict-chipin:~/PROJECT_23BIT153/ICCI
File Edit View Search Terminal Help
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count: 0
Single-bit Sequential Cell Count: 10
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPerflip: 1.00
Macro Count: 0
-----
Area
-----
Combinational Area: 74.46
Noncombinational Area: 68.62
Buf/Inv Area: 19.06
Total Buffer Area: 15.25
Total Inverter Area: 3.81
Macro/Black Box Area: 0.00
Net Area: 0
Net Xlength: 212.08
Net Ylength: 206.10
-----
Cell Area (netlist): 143.08
Cell Area (netlist and physical only): 143.08
Net Length: 418.18
-----
Design Rules
-----
Total Number of Nets: 49
Nets with Violations: 11
Max Trans Violations: 11
Max Cap Violations: 0
-----
1
icc2_shell>
Activities Terminal Jun 2 10:41 ● student@ict-chipin:~/PROJECT_23BIT153/ICCI
File Edit View Search Terminal Help
Total Hold Violation: 0.00
No. of Hold Violations: 0
-----
Cell Count
-----
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 32
Buf/Inv Cell Count: 9
Buf Cell Count: 7
Inv Cell Count: 2
Combinational Cell Count: 22
Single-bit Isolation Cell Count: 0
Multi-bit Isolation Cell Count: 0
Isolation Cell Banking Ratio: 0.00%
Single-bit Level Shifter Cell Count: 0
Multi-bit Level Shifter Cell Count: 0
Level Shifter Cell Banking Ratio: 0.00%
Single-bit ELS Cell Count: 0
Multi-bit ELS Cell Count: 0
ELS Cell Banking Ratio: 0.00%
Sequential Cell Count: 10
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count: 0
Single-bit Sequential Cell Count: 10
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPerflip: 1.00
Macro Count: 0
-----
Area
-----
Combinational Area: 74.46
Noncombinational Area: 68.62
```

```

Activities Terminal Jun 2 10:41 ●
student@ict-chipin:~/PROJECT_23BIT153/ICCI

File Edit View Search Terminal Help
Mode: func
Corner: nom
Scenario: func::nom
Path Group: **in2reg_default**
Path Type: max

Point Incr Path
-----
clock clk (rise edge) 0.00 0.00
clock network delay (propagated) 0.03 0.03
input external delay 0.50 0.53 f
b[0] (in) 0.00 0.53 f
U13/Y (XOR2X1_RVT) 0.17 0.70 f
intadd 0/U5/CO (FAADDX1_RVT) 0.06 0.76 f
intadd 0/U4/CO (FAADDX1_RVT) 0.06 0.82 f
intadd 0/U3/CO (FAADDX1_RVT) 0.06 0.88 f
intadd 0/U2/CO (FAADDX1_RVT) 0.07 0.95 f
U27/Y (MUX41X1_RVT) 0.07 1.02 f
temp_reg[4]/D (DFFX1_RVT) 0.00 1.02 f
data arrival time 1.02

clock clk (rise edge) 3.00 3.00
clock network delay (propagated) 0.07 3.07
temp_reg[4]/CLK (DFFX1_RVT) 0.00 3.07 r
clock uncertainty -0.30 2.77
library setup time -0.05 2.72
data required time 2.72
data arrival time -1.02

slack (MET) 1.70

1
icc2_shell> gui_change_highlight -remove -all_colors
icc2_shell> [REDACTED]

Activities Terminal Jun 2 10:42 ●
student@ict-chipin:~/PROJECT_23BIT153/ICCI

File Edit View Search Terminal Help
Max Trans Violations: 11
Max Cap Violations: 0
-----

1
icc2 shell> report_units
*****
Report : user_units
Design : full_add_sub
Version: W-2024.09
Date : Mon Jun 2 10:42:24 2025
*****
Input Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MΩ
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

Output Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MΩ
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

1
icc2_shell>

```

- **Routing:** Performed global and detailed routing while ensuring DRC compliance.

```
Activities Terminal Jun 2 10:46 ● student@ict-chipin:~/PROJECT_23BIT153/ICCII
File Edit View Search Terminal Help
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count: 0
Single-bit Sequential Cell Count: 10
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPerflip: 1.00
Macro Count: 0

Area
-----
Combinational Area: 74.46
Noncombinational Area: 68.62
Buf/Inv Area: 19.06
Total Buffer Area: 15.25
Total Inverter Area: 3.81
Macro/Black Box Area: 0.00
Net Area: 0
Net Xlength: 214.04
Net Ylength: 212.73
-----
Cell Area (netlist): 143.08
Cell Area (netlist and physical only): 143.08
Net Length: 426.77

Design Rules
-----
Total Number of Nets: 49
Nets with Violations: 11
Max Trans Violations: 11
Max Cap Violations: 0
-----
1
icc2_shell>
Activities Terminal Jun 2 10:46 ● student@ict-chipin:~/PROJECT_23BIT153/ICCII
File Edit View Search Terminal Help
Total Hold Violation: 0.00
No. of Hold Violations: 0
-----
Cell Count
-----
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 32
Buf/Inv Cell Count: 9
Buf Cell Count: 7
Inv Cell Count: 2
Combinational Cell Count: 22
Single-bit Isolation Cell Count: 0
Multi-bit Isolation Cell Count: 0
Isolation Cell Banking Ratio: 0.00%
Single-bit Level Shifter Cell Count: 0
Multi-bit Level Shifter Cell Count: 0
Level Shifter Cell Banking Ratio: 0.00%
Single-bit ELS Cell Count: 0
Multi-bit ELS Cell Count: 0
ELS Cell Banking Ratio: 0.00%
Sequential Cell Count: 10
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count: 0
Single-bit Sequential Cell Count: 10
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPerflip: 1.00
Macro Count: 0

Area
-----
Combinational Area: 74.46
Noncombinational Area: 68.62
```

```

Activities Terminal Jun 2 10:46 ●
student@ict-chipin:~/PROJECT_23BIT153/ICCII

File Edit View Search Terminal Help
Endpoint: temp_reg[4] (rising edge-triggered flip-flop clocked by clk)
Mode: func
Corner: nom
Scenario: func::nom
Path Group: **in2reg_default**
Path Type: max

Point Incr Path
-----
clock clk (rise edge) 0.00 0.00
clock network delay (propagated) 0.03 0.03
input external delay 0.50 0.53 f
b[0] (in) 0.00 0.53 f
U13/Y (XOR2X1_RVT) 0.17 0.70 f
intadd_0/U5/C0 (FAADDX1_RVT) 0.06 0.76 f
intadd_0/U4/C0 (FAADDX1_RVT) 0.06 0.82 f
intadd_0/U3/C0 (FAADDX1_RVT) 0.06 0.88 f
intadd_0/U2/C0 (FAADDX1_RVT) 0.07 0.95 f
U27/Y (MUX4X1X1_RVT) 0.07 1.02 f
temp_reg[4]/D (DFFX1_RVT) 0.00 1.02 f
data arrival time 0.00 1.02

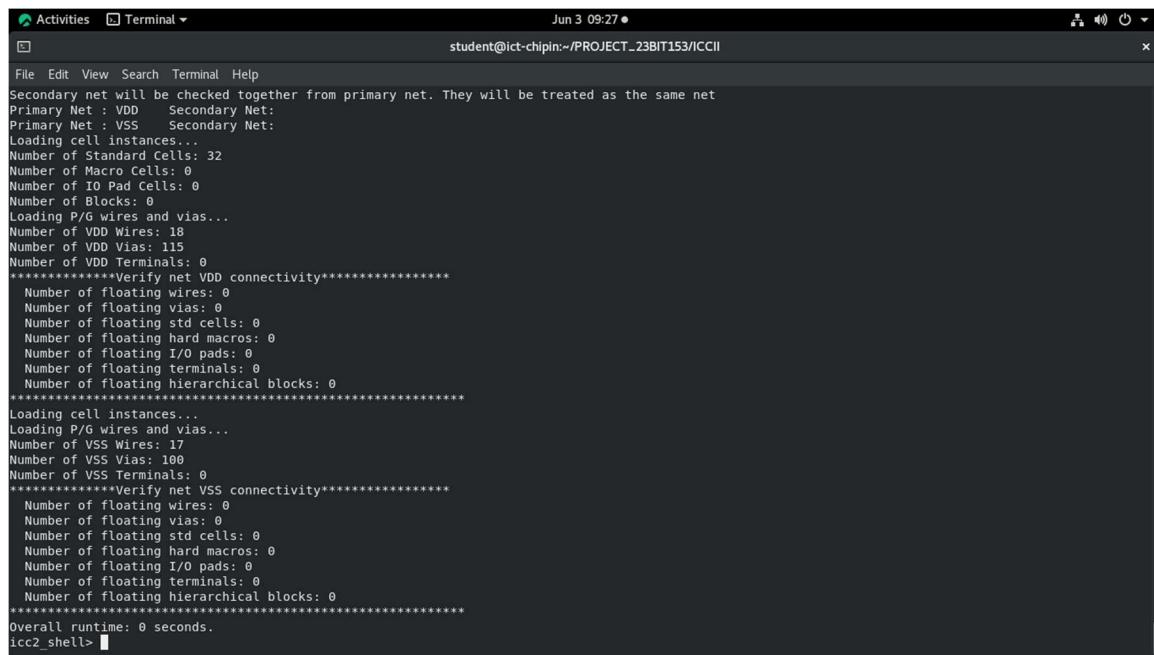
clock clk (rise edge) 3.00 3.00
clock network delay (propagated) 0.07 3.07
temp_reg[4]/CLK (DFFX1_RVT) 0.00 3.07 r
clock uncertainty -0.38 2.77
library setup time -0.05 2.72
data required time 2.72
-----
data required time 2.72
data arrival time -1.02
-----
slack (MET) 1.70

1
icc2_shell>
Activities Terminal Jun 2 10:46 ●
student@ict-chipin:~/PROJECT_23BIT153/ICCII

File Edit View Search Terminal Help
Max Trans Violations: 11
Max Cap Violations: 0
-----
1
icc2 shell> report_units
*****
Report : user_units
Design : full_add_sub
Version: W-2024.09
Date : Mon Jun 2 10:46:37 2025
*****
Input Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MΩ
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t
Output Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MΩ
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t
1
icc2_shell> 

```

- Slack was evaluated after each of these steps to maintain design constraints.



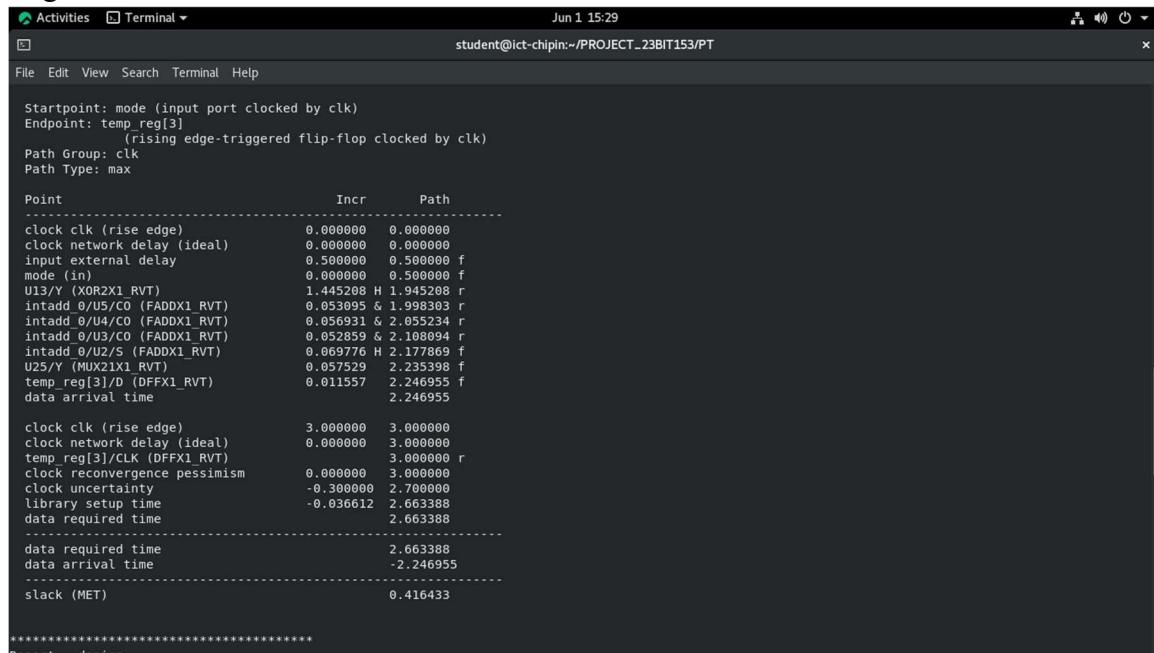
```

Activities Terminal Jun 3 09:27 ●
student@ict-chipin:~/PROJECT_23BIT153/ICCI
File Edit View Search Terminal Help
Secondary net will be checked together from primary net. They will be treated as the same net
Primary Net : VDD Secondary Net:
Primary Net : VSS Secondary Net:
Loading cell instances...
Number of Standard Cells: 32
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 18
Number of VDD Vias: 115
Number of VDD Terminals: 0
*****Verify net VDD connectivity*****
Number of floating wires: 0
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****Verify net VSS connectivity*****
Number of floating wires: 0
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Overall runtime: 0 seconds.
icc2_shell> █

```

4. Timing Analysis in PrimeTime:

- The routed design was analyzed in **PT shell** using timing reports.
- The final slack after routing was confirmed to be between 0 and 1 to meet the design target.



```

Activities Terminal Jun 1 15:29
student@ict-chipin:~/PROJECT_23BIT153/PT
File Edit View Search Terminal Help
Startpoint: mode (input port clocked by clk)
Endpoint: temp_reg[3]
(rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Point Incr Path
-----
clock clk (rise edge) 0.000000 0.000000
clock network delay (ideal) 0.000000 0.000000
input external delay 0.500000 0.500000 f
mode (in) 0.000000 0.500000 f
U13/Y (XOR2X1_RVT) 1.445208 H 1.945208 r
intadd_0/U3/CO (FADDX1_RVT) 0.053095 & 1.998303 r
intadd_0/U4/CO (FADDX1_RVT) 0.056931 & 2.055234 r
intadd_0/U3/CO (FADDX1_RVT) 0.052859 & 2.108094 r
intadd_0/U2/S (FADDX1_RVT) 0.069776 H 2.177869 f
U25/Y (MUX2X1X1_RVT) 0.057529 2.235398 f
temp_reg[3]/D (DFFX1_RVT) 0.011557 2.246955 f
data arrival time 2.246955
-----  

clock clk (rise edge) 3.000000 3.000000
clock network delay (ideal) 0.000000 3.000000
temp reg[3]/CLK (DFFX1_RVT) 3.000000 r
clock reconvergence pessimism 0.000000 3.000000
clock uncertainty -0.300000 2.700000
library setup time -0.036612 2.663388
data required time 2.663388
-----  

data required time 2.663388
data arrival time -2.246955
-----  

slack (MET) 0.416433
*****  

Done -> done

```

```
Activities Terminal Jun 2 10:50 ●
student@ict-chipin:~/PROJECT_23BIT153/PT

File Edit View Search Terminal Help

Timing Path Group 'clk' (min_delay/hold)
-----
Levels of Logic: 2
Critical Path Length: 0.126525
Critical Path Slack: 0.024616
Total Negative Slack: 0.000000
No. of Violating Paths: 0

Area
-----
Net Interconnect area: 7.455995
Total cell area: 143.083069
Design Area: 150.539062

Cell & Pin Count
-----
Pin Count: 118
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 32

Design Rule Violations
-----
Total No. of Pins in Design: 118
max_transition Count: 31
max_transition Cost: 7.750000
Total DRC Cost: 7.750000

1
pt_shell> [REDACTED]
Activities Terminal Jun 2 10:50 ●
student@ict-chipin:~/PROJECT_23BIT153/PT

File Edit View Search Terminal Help
Date : Mon Jun 2 10:50:40 2025
*****
Timing Path Group '**async_default**' (max_delay/setup)
-----
Levels of Logic: 1
Critical Path Length: 2.1223076
Critical Path Slack: 0.606782
Total Negative Slack: 0.000000
No. of Violating Paths: 0

Timing Path Group 'clk' (max_delay/setup)
-----
Levels of Logic: 6
Critical Path Length: 2.244950
Critical Path Slack: 0.418438
Total Negative Slack: 0.000000
No. of Violating Paths: 0

Timing Path Group 'clk' (min_delay/hold)
-----
Levels of Logic: 2
Critical Path Length: 0.126525
Critical Path Slack: 0.024616
Total Negative Slack: 0.000000
No. of Violating Paths: 0

Area
-----
Net Interconnect area: 7.455995
Total cell area: 143.083069
Design Area: 150.539062
```

```

Activities Terminal Jun 2 10:49 ●
student@ict-chipin:~/PROJECT_23BIT153/PT

File Edit View Search Terminal Help
(rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point Incr Path
-----
clock clk (rise edge) 0.000000 0.000000
clock network delay (ideal) 0.000000 0.000000
input external delay 0.500000 0.500000 f
mode (in) 0.000000 0.500000 f
U13/Y (XOR2X1_RVT) 1.442985 H 1.942985 r
intadd 0/U5/CO (FADDX1_RVT) 0.052220 & 1.995206 r
intadd 0/U4/CO (FADDX1_RVT) 0.054908 & 2.050114 r
intadd 0/U3/CO (FADDX1_RVT) 0.055589 & 2.105703 r
intadd 0/U2/S (FADDX1_RVT) 0.070161 H 2.175863 r
U25/Y (MUX2X1X1_RVT) 0.057529 2.233393 f
temp_reg[3]/D (DFFX1_RVT) 0.011557 2.244950 f
data arrival time 2.244950

clock clk (rise edge) 3.000000 3.000000
clock network delay (ideal) 0.000000 3.000000
temp_reg[3]/CLK (DFFX1_RVT) 3.000000 r
clock reconvergence pessimism 0.000000 3.000000
clock uncertainty -0.300000 2.700000
library setup time -0.036612 2.663388
data required time 2.663388

data required time 2.663388
data arrival time -2.244950
-----
slack (MET) 0.418438

*****
Report : design
Design : full_add_sub
Version: W-2024.09
Date : Mon Jun 2 10:49:30 2025
Activities Terminal Jun 2 10:51 ●
student@ict-chipin:~/PROJECT_23BIT153/PT

File Edit View Search Terminal Help

Cell & Pin Count
-----
Pin Count: 118
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 32
-----

Design Rule Violations
-----
Total No. of Pins in Design: 118
max_transition Count: 31
max_transition Cost: 7.750000
Total DRC Cost: 7.750000

1
pt_shell> report_units
*****
Report : units
Design : full_add_sub
Version: W-2024.09
Date : Mon Jun 2 10:51:03 2025
*****
Units
-----
Capacitive_load_unit : 1e-15 Farad
Current_unit : 1e-06 Amp
Resistance_unit : 1e+06 Ohm
Time_unit : 1e-09 Second
Voltage_unit : 1 Volt
1
pt_shell>

```

- Report for power analysis is attached below, calculated after **Prime Time Analysis**

```

Activities Terminal Jun 2 11:12 ●
student@ict-chipin:~/PROJECT_23BIT153/GDSII
File Edit View Search Terminal Help
ue = inf, value = 0.081367 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port QN on cell temp_reg[2] for parameter Cout. Lowest table value = 0.000100, highest table value = 0.008000, value = 0.000000 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port D on cell temp_reg[1] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.079918 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port QN on cell temp_reg[1] for parameter Cout. Lowest table value = 0.000100, highest table value = 0.008000, value = 0.000000 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port D on cell temp_reg[0] for parameter Tinp. Lowest table value = inf, highest table value = inf, value = 0.080872 (POW-046)
Warning: Power table extrapolation (extrapolation mode) for port QN on cell temp_reg[0] for parameter Cout. Lowest table value = 0.000100, highest table value = 0.008000, value = 0.000000 (POW-046)
Note - message 'POW-046' limit (10) exceeded. Remainder will be suppressed.

Cell Internal Power      = 2.23e+07 pW ( 85.4%)
Net Switching Power     = 3.79e+06 pW ( 14.6%)
Total Dynamic Power     = 2.61e+07 pW (100.0%)

Cell Leakage Power       = 3.70e+08 pW

Attributes
-----
    u - User defined power group
    i - Includes clock pin internal power

Power Group      Internal Power      Switching Power      Leakage Power      Total Power      ( % )      Attrs
-----
io_pad          0.00e+00           0.00e+00           0.00e+00           0.00e+00      ( 0.0%)
memory         0.00e+00           0.00e+00           0.00e+00           0.00e+00      ( 0.0%)
black_box       0.00e+00           0.00e+00           0.00e+00           0.00e+00      ( 0.0%)
clock_network   3.11e+07           2.64e+06           3.26e+07           6.64e+07      ( 16.8%)      i
register        -1.59e+07          1.96e+05           2.00e+08           1.84e+08      ( 46.5%)
sequential       0.00e+00           0.00e+00           0.00e+00           0.00e+00      ( 0.0%)
combinational   7.10e+06           9.56e+05           1.38e+08           1.46e+08      ( 36.7%)
-----
Total           2.23e+07 pW      3.79e+06 pW      3.70e+08 pW      3.96e+08 pW
1
icarus shells report power consumption

```

Conclusion

Through the implementation of the **4-bit Full Adder-Subtractor** using the complete RTL-to-GDSII flow, we gained hands-on experience in the digital IC design cycle. Each step, from Verilog coding to final timing verification, was performed with strict adherence to industry practices. The project not only validated the functional correctness of the design but also ensured timing closure and layout compliance, preparing the design for real-world ASIC fabrication.