CERTIFICATE
OF PROJECT COMPLETION

VYORIUS

THIS CERTIFICATE IS PROUDLY PRESENTED TO

Pushpal Das

has successfully undergone Industrial Program on VLSI..
from VYORIUS from 20th Nov, 2021 to 20th Jan, 2022 and
successfully completed the projects on

- Basic Circuits written in Verilog HDL implemeted on the FPGA
- UART Communication to print a single character
- FSM Designs : Mealy & Moore Machines and Up Down Counter

Under the guidance of the mentor and company representative

23-Jan-2022

DATE

istop
Keep Growing

PROJECT HEAD

VYO-2201000146