VLSI DESIGN PROJECTS/INTERNSHIP

College Name

→SRM Institute of Science and Technology.

Company Name

→Vyorius.

Domain

→VLSI design.

Project topics

1. Basic circuits written in Verilog/VHDL, simulated and implemented on the FPGA
2. UART communication to print a single character
3. FSM Designs: Mealy & Moore Machines and Up Down Counter

Hardware and software used

Hardware,

Mimas A7 Mini FPGA Development Board
Mimas A7 Mini is an easy-to-use FPGA Development board featuring Artix 7 FPGA (XC7A35T – FTG256C package) with FTDI's FT2232H Dual-Channel USB device. It is an Artix-7 based replacement and upgrades of Mimas Spartan 6 FPGA Board. It is specially designed for the development and integration of FPGA based accelerated features to other designs. The USB 2.0 host

interface based on popular FT2232H offers high bandwidth data transfer and board programming without the need for any external programming adapters.

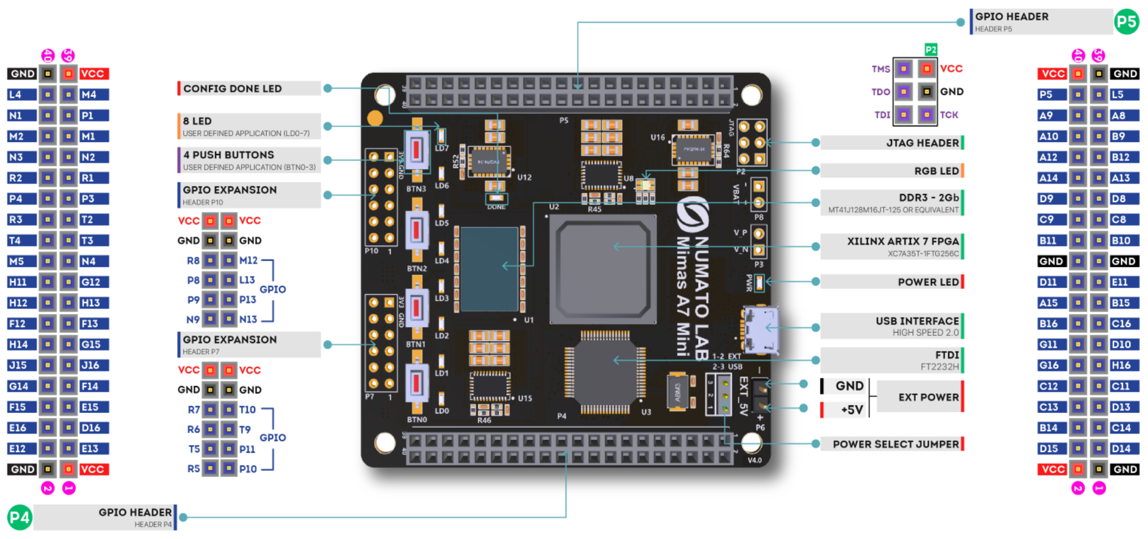
Features,

→ Device: Xilinx Artix 7 FPGA (XC7A35T-1FTG256C)
→ DDR3: 2Gb DDR3 (MT41J128M16JT-125 or equivalent)
→ Built-in programming interface. No expensive JTAG adapters needed for programming the board
→ Onboard 128Mb flash memory for FPGA configuration storage and custom user data storage
→ High-Speed USB 2.0 interface for On-board flash programming. FT2232H Channel B is dedicated to JTAG Programming. Channel A can be used for custom applications
→ 100MHz CMOS oscillator
→ 8 LEDs, 1 RGB LED and 4 Push Buttons for user-defined purposes
→ FPGA configuration via JTAG and USB
→ Maximum IOs for user-defined purposes

FPGA – 70 IOs (35 professionally length matched Differential Pairs) and two 2×6 Expansion Headers

Applications,

→ Product Prototype Development
→ Accelerated computing integration
→ Development and testing of custom embedded processors
→ Communication devices development
→ Educational tool for Schools and Universities



Specifications,

Attribute	Value
Dimensions	6 × 4 × 1 in
FPGA	XC7A35T – 1FTG256C
Memory	DDR3 – 2Gb
Configuration Options	JTAG, USB
Host Interface	USB 2.0
Primary Clock Frequency	100MHz
Number Of GPIOs (Max)	70
Number Of Diff Pairs	35

Software

Icarus Verilog is a Verilog simulation and synthesis tool. It operates as a compiler, compiling source code written in Verilog (IEEE-1364) into some target format. For batch simulation, the compiler can generate an intermediate form called *vvp assembly*. This intermediate form is executed by the ``vvp'' command. For synthesis, the compiler generates netlists in the desired format.

The compiler proper is intended to parse and elaborate design descriptions written to the IEEE standard *IEEE Std 1364-2005*. This is a fairly large and complex standard, so it will take some time to fill all the dark alleys of the standard, but that's the goal.

Icarus Verilog is a work in progress, and since the language standard is not standing still either, it probably always will be. That is as it should be. However, I will make stable releases from time to time, and will endeavour to not retract any features that appear in these stable releases. The quick links above will show the current stable release.

The main porting target is Linux, although it works well on many similar operating systems. Various people have contributed precompiled binaries of stable releases for a variety of targets. These releases are ported by volunteers, so what binaries are available depends on who takes the time to do the packaging. *Icarus Verilog* has been ported to That Other Operating System, as a command line tool, and there are installers for users without compilers. You can compile it entirely with free tools, too, although there are precompiled binaries of stable releases.

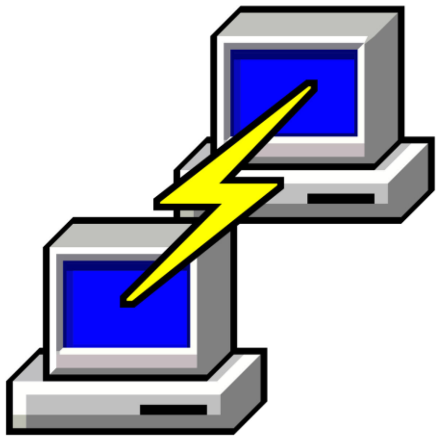
Vivado Design Suite is a software suite produced by Xilinx for synthesis and analysis of HDL designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis.[1][5][6][7] Vivado represents a ground-up rewrite and re-thinking of the entire design flow (compared to ISE).[8][9][10]

Like the later versions of ISE, Vivado includes the in-built logic simulator ISIM.[11] Vivado also introduces high-level synthesis, with a toolchain that converts C code into programmable logic.[6]

Replacing the 15-year-old ISE with Vivado Design Suite took 1000 person-years and cost US$200 million.

Tenagra is an FPGA System management tool for configuring and communicating with Numato Lab's supported FPGA modules and development platforms. This software is designed to be a single interface for managing the devices and exercising some of the available features. Currently, Tenagra supports configuring the FPGA module/board (programming) and Memory Exerciser that can transfer data between various memories on the device. This includes both external DDR Memory and Block RAM available within the FPGA device. With Tenagra, you can create multiple configuration setups with different bitstreams and settings for each device model so that switching between multiple bitstreams is a breeze. This is especially helpful during development where the device may need to be reprogrammed with various bitstreams repeatedly.

Driver for Mimas A7 Mini Module



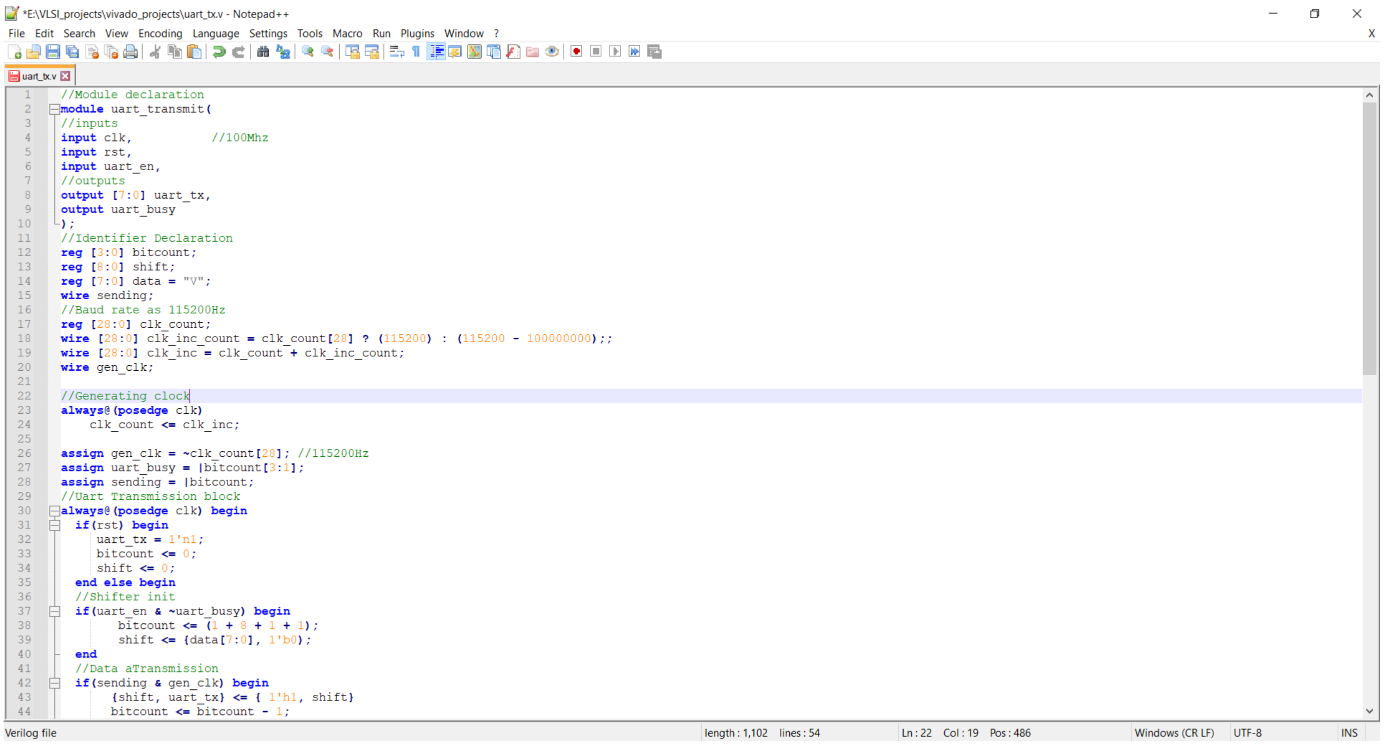
PuTTY is a free implementation of SSH **(and telnet) for PCs running Microsoft Windows** (it also includes an xterm terminal emulator). You will find PuTTY useful if you want to access an account on a Unix or other multi-user system from a PC (for example your own or one in an internet cafe).

2. UART communication to print a single character

Software to download

- Notepad++

Step 1- Write the verilog program in notepad ++ .

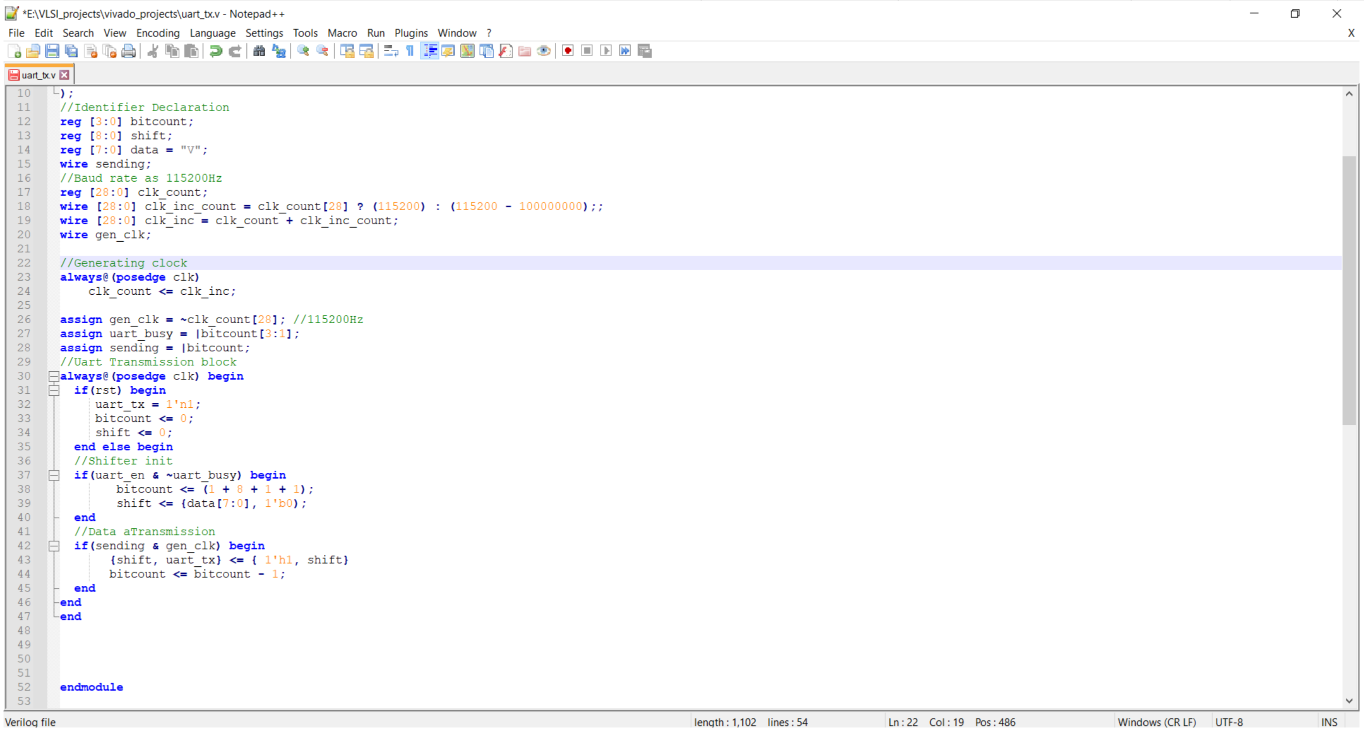


*E:\VLSI_projects\vivado_projects\uart_tx.v - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
uart_tx.v
Verilog file
length : 1,102 lines : 54
Ln : 22 Col : 19 Pos : 486
Windows (CR LF)
UTF-8
INS

```verilog
//Module declaration
module uart_transmit(
//inputs
input clk,           //100Mhz
input rst,
input uart_en,
//outputs
output [7:0] uart_tx,
output uart_busy
);
//Identifier Declaration
reg [3:0] bitcount;
reg [8:0] shift;
reg [7:0] data = "V";
wire sending;
//Baud rate as 115200Hz
reg [28:0] clk_count;
wire [28:0] clk_inc_count = clk_count[28] ? (115200) : (115200 - 100000000);;
wire [28:0] clk_inc = clk_count + clk_inc_count;
wire gen_clk;

//Generating clock
always@(posedge clk)
    clk_count <= clk_inc;

assign gen_clk = ~clk_count[28]; //115200Hz
assign uart_busy = |bitcount[3:1];
assign sending = |bitcount;
//Uart Transmission block
always@(posedge clk) begin
  if(rst) begin
     uart_tx = 1'n1;
     bitcount <= 0;
     shift <= 0;
  end else begin
  //Shifter init
  if(uart_en & ~uart_busy) begin
        bitcount <= (1 + 8 + 1 + 1);
        shift <= {data[7:0], 1'b0);
  end
  //Data aTransmission
  if(sending & gen_clk) begin
       {shift, uart_tx} <= { 1'h1, shift}
       bitcount <= bitcount - 1;
```



*E:\VLSI_projects\vivado_projects\uart_tx.v - Notepad++
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//Generating clock
always@(posedge clk)
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assign gen_clk = ~clk_count[28]; //115200Hz
assign uart_busy = |bitcount[3:1];
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     uart_tx = 1'n1;
     bitcount <= 0;
     shift <= 0;
  end else begin
  //Shifter init
  if(uart_en & ~uart_busy) begin
        bitcount <= (1 + 8 + 1 + 1);
        shift <= {data[7:0], 1'b0);
  end
  //Data aTransmission
  if(sending & gen_clk) begin
       {shift, uart_tx} <= { 1'h1, shift}
       bitcount <= bitcount - 1;
```

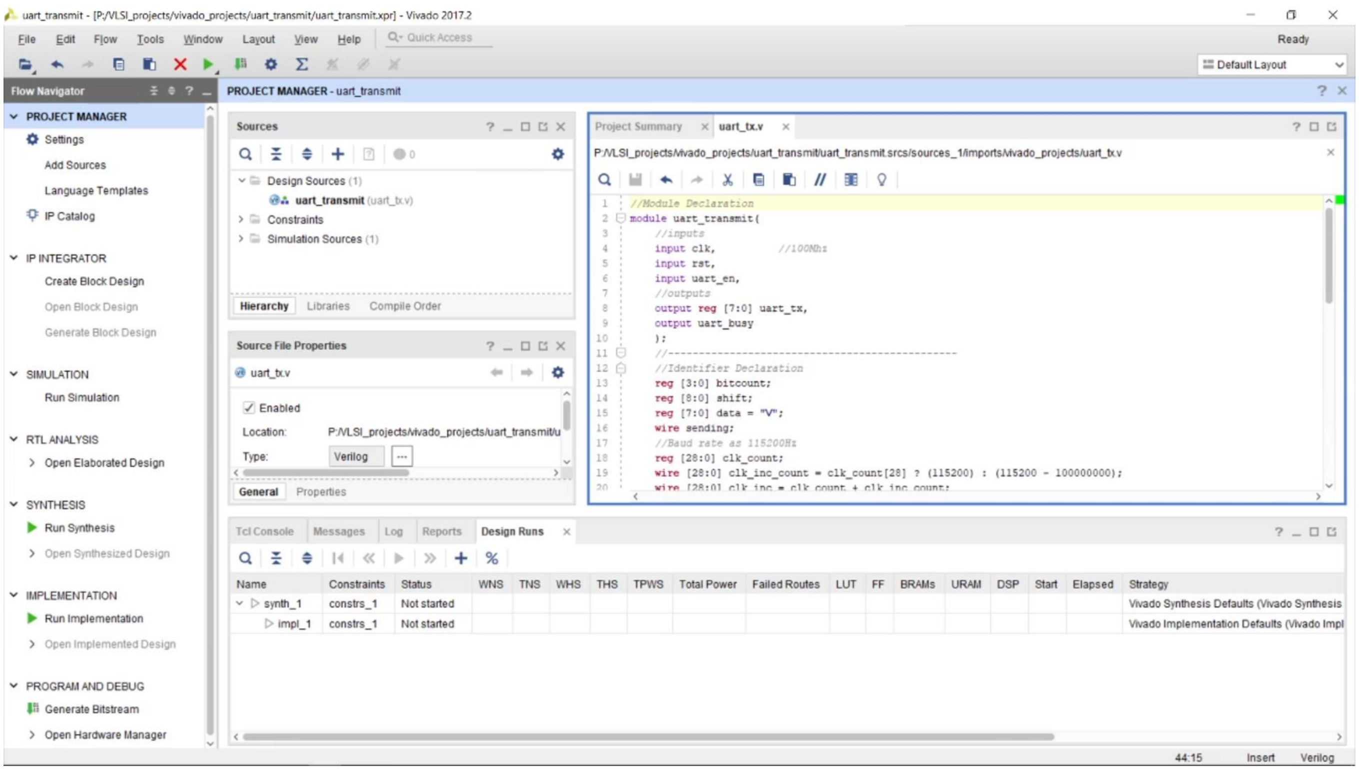
```verilog
  end
end
end




endmodule

```

Step 2-Open Vivado software create a new project and add this notepad verilog extension to it

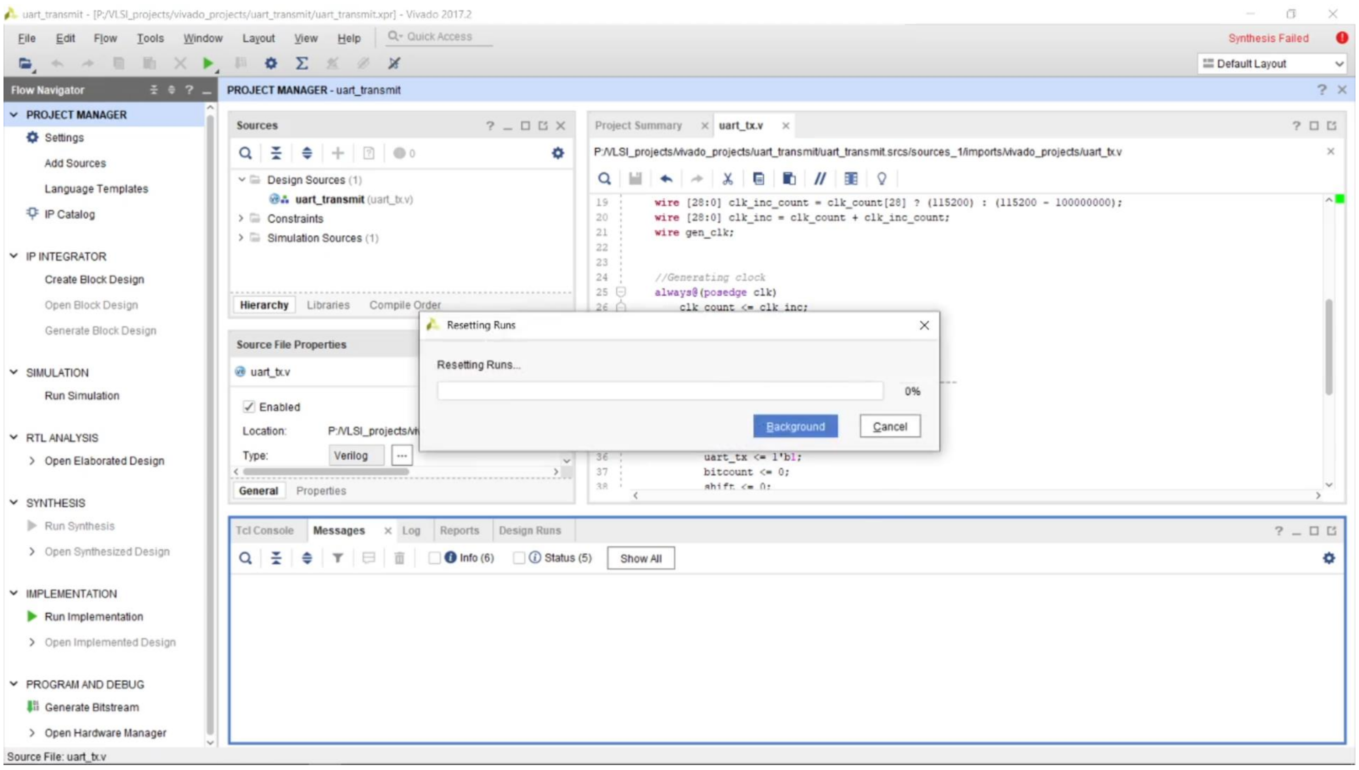


P:/VLSI_projects/vivado_projects/uart_transmit/uart_transmit.srcs/sources_1/imports/vivado_projects/uart_tx.v

```
//Module Declaration
module uart_transmit(
    //inputs
    input clk,          //100Mhz
    input rst,
    input uart_en,
    //outputs
    output reg [7:0] uart_tx,
    output uart_busy
    );
    //-------------------------------------------
    //Identifier Declaration
    reg [3:0] bitcount;
    reg [8:0] shift;
    reg [7:0] data = "V";
    wire sending;
    //Baud rate as 115200Hz
    reg [28:0] clk_count;
    wire [28:0] clk_inc_count = clk_count[28] ? (115200) : (115200 - 100000000);
    wire [28:0] clk_inc = clk_count + clk_inc_count;
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Impl

Synthesis the code extracted and compile the errors if there are any.

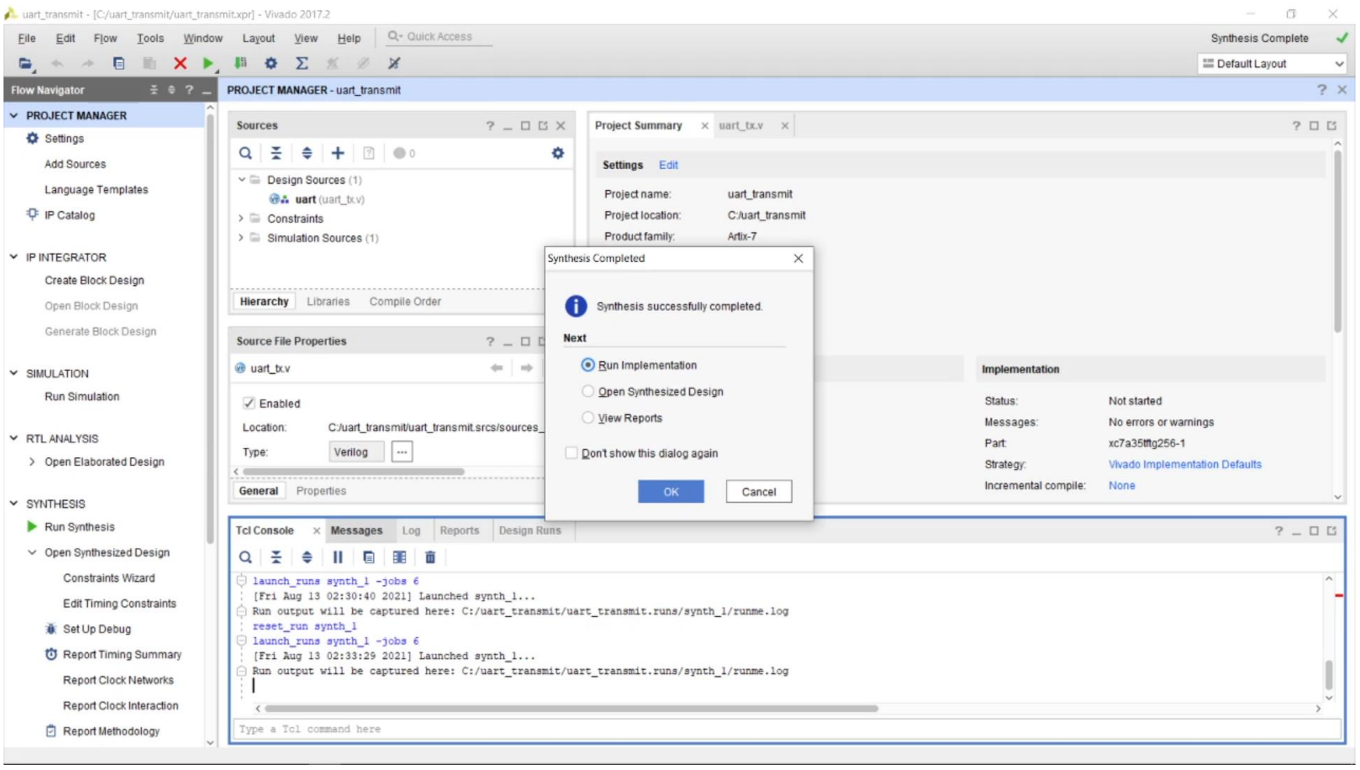


P:/VLSI_projects/vivado_projects/uart_transmit/uart_transmit.srcs/sources_1/imports/vivado_projects/uart_tx.v

```
    wire [28:0] clk_inc_count = clk_count[28] ? (115200) : (115200 - 100000000);
    wire [28:0] clk_inc = clk_count + clk_inc_count;
    wire gen_clk;


    //Generating clock
    always@(posedge clk)
        clk_count <= clk_inc;
...
            uart_tx <= 1'b1;
            bitcount <= 0;
            shift <= 0;
```

After synthesis run implementation


uart_transmit - [C:/uart_transmit/uart_transmit.xpr] - Vivado 2017.2
File Edit Flow Tools Window Layout View Help
Synthesis Complete
Default Layout
Flow Navigator
PROJECT MANAGER - uart_transmit
Sources
Project Summary
uart_tx.v
Hierarchy Libraries Compile Order
Source File Properties
General Properties
Tcl Console Messages Log Reports Design Runs

Project name: uart_transmit
Project location: C:/uart_transmit
Product family: Artix-7

Synthesis Completed

Synthesis successfully completed.

Next
- [✓ Run Implementation]
- Open Synthesized Design
- View Reports

Don't show this dialog again

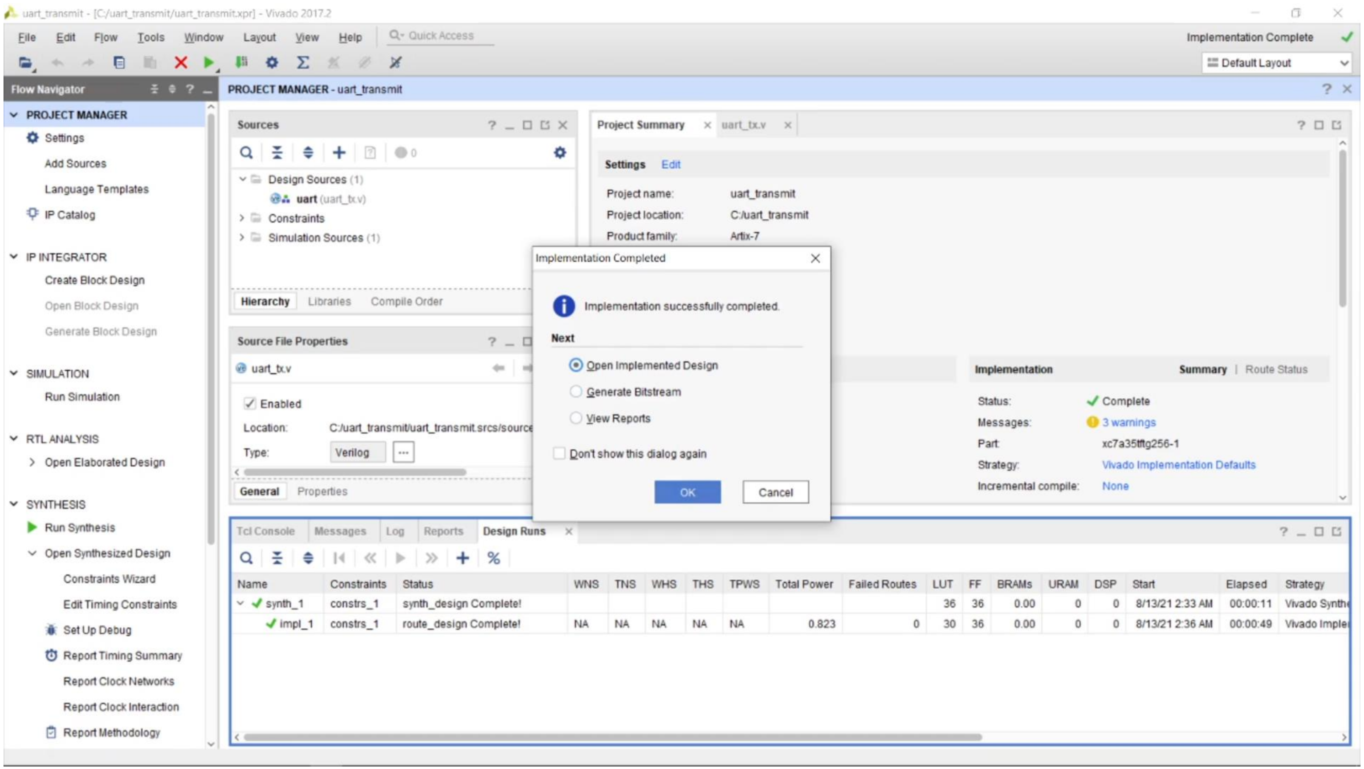
OK Cancel

Implementation

Status:	Not started
Messages:	No errors or warnings
Part:	xc7a35tftg256-1
Strategy:	Vivado Implementation Defaults
Incremental compile:	None

```
launch_runs synth_1 -jobs 6
[Fri Aug 13 02:30:40 2021] Launched synth_1...
Run output will be captured here: C:/uart_transmit/uart_transmit.runs/synth_1/runme.log
reset_run synth_1
launch_runs synth_1 -jobs 6
[Fri Aug 13 02:33:29 2021] Launched synth_1...
Run output will be captured here: C:/uart_transmit/uart_transmit.runs/synth_1/runme.log
```

Open synthesis implemented design


uart_transmit - [C:/uart_transmit/uart_transmit.xpr] - Vivado 2017.2
File Edit Flow Tools Window Layout View Help
Implementation Complete
Default Layout
Flow Navigator
PROJECT MANAGER - uart_transmit
Sources
Project Summary
uart_tx.v
Tcl Console Messages Log Reports Design Runs

Implementation Completed

Implementation successfully completed.

Next
- [✓ Open Implemented Design]
- Generate Bitstream
- View Reports

Don't show this dialog again

OK Cancel

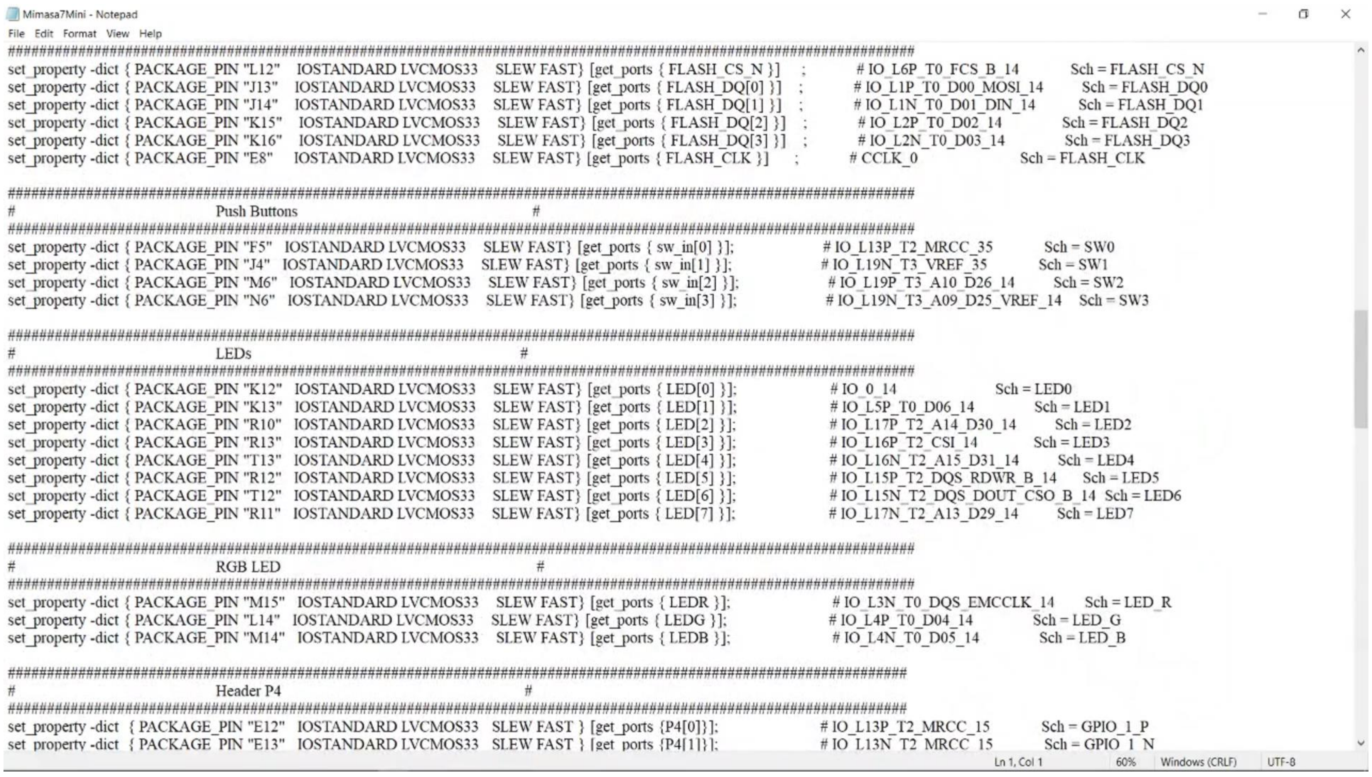
Implementation — Summary | Route Status

Status:	✓ Complete
Messages:	3 warnings
Part:	xc7a35tftg256-1
Strategy:	Vivado Implementation Defaults
Incremental compile:	None

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Strategy
✓ synth_1	constrs_1	synth_design Complete!								36	36	0.00	0	0	8/13/21 2:33 AM	00:00:11	Vivado Synthe
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	0.823	0	30	36	0.00	0	0	8/13/21 2:36 AM	00:00:49	Vivado Imple

Now one of the most vital part we have to change port design with respect to the XDC file we got for vivado designs from the link Mimas A7 Mini FPGA Development Board | Numato Lab

After downloading it open up with the notepad where we can view the XDC file


Mimasa7Mini - Notepad
File Edit Format View Help
Ln 1, Col 1 60% Windows (CRLF) UTF-8

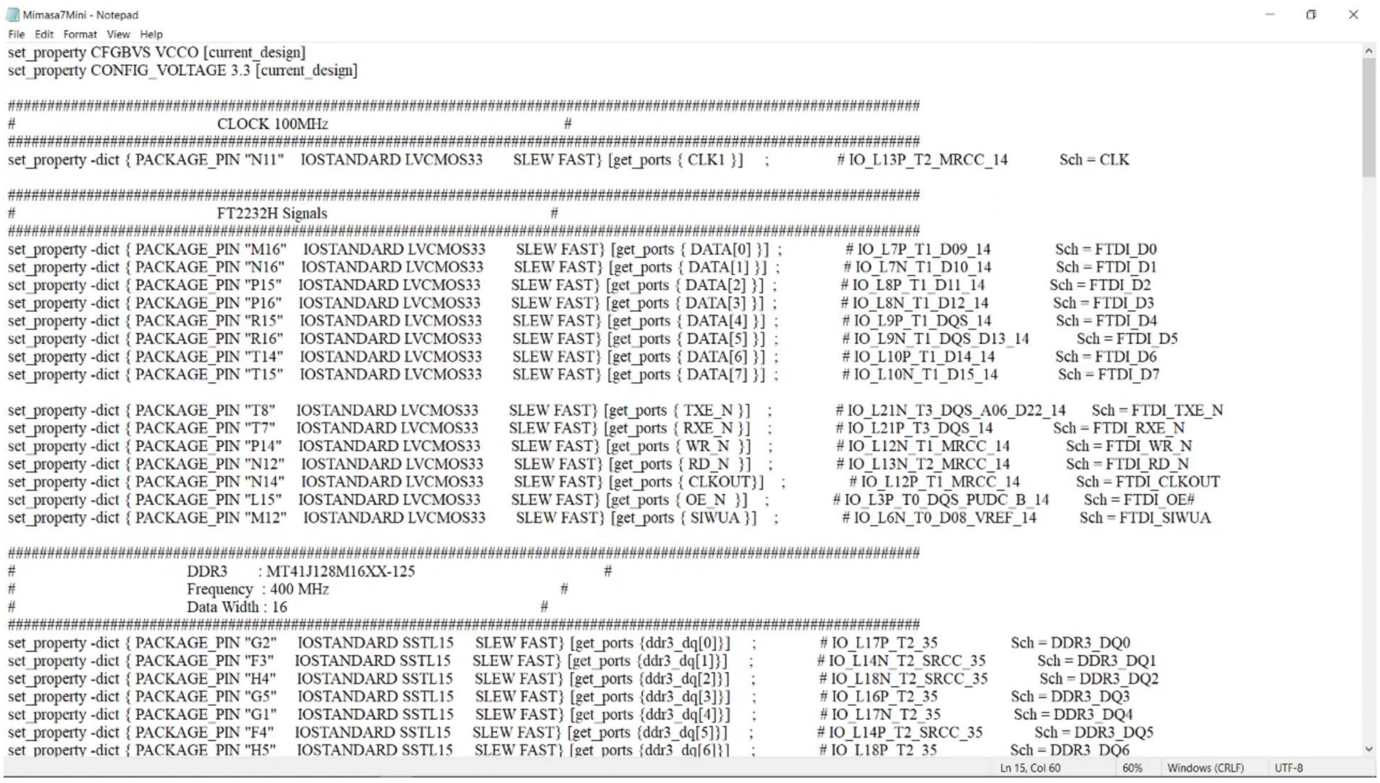
```
##############################################################################################################
set_property -dict { PACKAGE_PIN "L12"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { FLASH_CS_N }]   ;        # IO_L6P_T0_FCS_B_14        Sch = FLASH_CS_N
set_property -dict { PACKAGE_PIN "J13"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { FLASH_DQ[0] }]  ;        # IO_L1P_T0_D00_MOSI_14     Sch = FLASH_DQ0
set_property -dict { PACKAGE_PIN "J14"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { FLASH_DQ[1] }]  ;        # IO_L1N_T0_D01_DIN_14      Sch = FLASH_DQ1
set_property -dict { PACKAGE_PIN "K15"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { FLASH_DQ[2] }]  ;        # IO_L2P_T0_D02_14          Sch = FLASH_DQ2
set_property -dict { PACKAGE_PIN "K16"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { FLASH_DQ[3] }]  ;        # IO_L2N_T0_D03_14          Sch = FLASH_DQ3
set_property -dict { PACKAGE_PIN "E8"    IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { FLASH_CLK }]    ;        # CCLK_0                    Sch = FLASH_CLK

##############################################################################################################
#                         Push Buttons                                      #
##############################################################################################################
set_property -dict { PACKAGE_PIN "F5"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { sw_in[0] }];          # IO_L13P_T2_MRCC_35         Sch = SW0
set_property -dict { PACKAGE_PIN "J4"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { sw_in[1] }];          # IO_L19N_T3_VREF_35         Sch = SW1
set_property -dict { PACKAGE_PIN "M6"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { sw_in[2] }];          # IO_L19P_T3_A10_D26_14      Sch = SW2
set_property -dict { PACKAGE_PIN "N6"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { sw_in[3] }];          # IO_L19N_T3_A09_D25_VREF_14  Sch = SW3

##############################################################################################################
#                         LEDs                                      #
##############################################################################################################
set_property -dict { PACKAGE_PIN "K12"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LED[0] }];          # IO_0_14                  Sch = LED0
set_property -dict { PACKAGE_PIN "K13"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LED[1] }];          # IO_L5P_T0_D06_14         Sch = LED1
set_property -dict { PACKAGE_PIN "R10"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LED[2] }];          # IO_L17P_T2_A14_D30_14     Sch = LED2
set_property -dict { PACKAGE_PIN "R13"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LED[3] }];          # IO_L16P_T2_CSI_14        Sch = LED3
set_property -dict { PACKAGE_PIN "T13"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LED[4] }];          # IO_L16N_T2_A15_D31_14     Sch = LED4
set_property -dict { PACKAGE_PIN "R12"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LED[5] }];          # IO_L15P_T2_DQS_RDWR_B_14   Sch = LED5
set_property -dict { PACKAGE_PIN "T12"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LED[6] }];          # IO_L15N_T2_DQS_DOUT_CSO_B_14 Sch = LED6
set_property -dict { PACKAGE_PIN "R11"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LED[7] }];          # IO_L17N_T2_A13_D29_14     Sch = LED7

##############################################################################################################
#                         RGB LED                                      #
##############################################################################################################
set_property -dict { PACKAGE_PIN "M15"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LEDR }];          # IO_L3N_T0_DQS_EMCCLK_14    Sch = LED_R
set_property -dict { PACKAGE_PIN "L14"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LEDG }];          # IO_L4P_T0_D04_14           Sch = LED_G
set_property -dict { PACKAGE_PIN "M14"   IOSTANDARD LVCMOS33   SLEW FAST} [get_ports { LEDB }];          # IO_L4N_T0_D05_14           Sch = LED_B

#############################################################################################################
#                         Header P4                                      #
#############################################################################################################
set_property -dict  { PACKAGE_PIN "E12"   IOSTANDARD LVCMOS33   SLEW FAST } [get_ports {P4[0]}];          # IO_L13P_T2_MRCC_15        Sch = GPIO_1_P
set_property -dict  { PACKAGE_PIN "E13"   IOSTANDARD LVCMOS33   SLEW FAST } [get_ports {P4[1]}];          # IO_L13N_T2_MRCC_15        Sch = GPIO_1_N
```


Mimasa7Mini - Notepad
File Edit Format View Help
Ln 15, Col 60 60% Windows (CRLF) UTF-8

```
set_property CFGBVS VCCO [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]

##############################################################################################################
#                         CLOCK 100MHz                                      #
##############################################################################################################
set_property -dict { PACKAGE_PIN "N11"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { CLK1 }]   ;        # IO_L13P_T2_MRCC_14       Sch = CLK

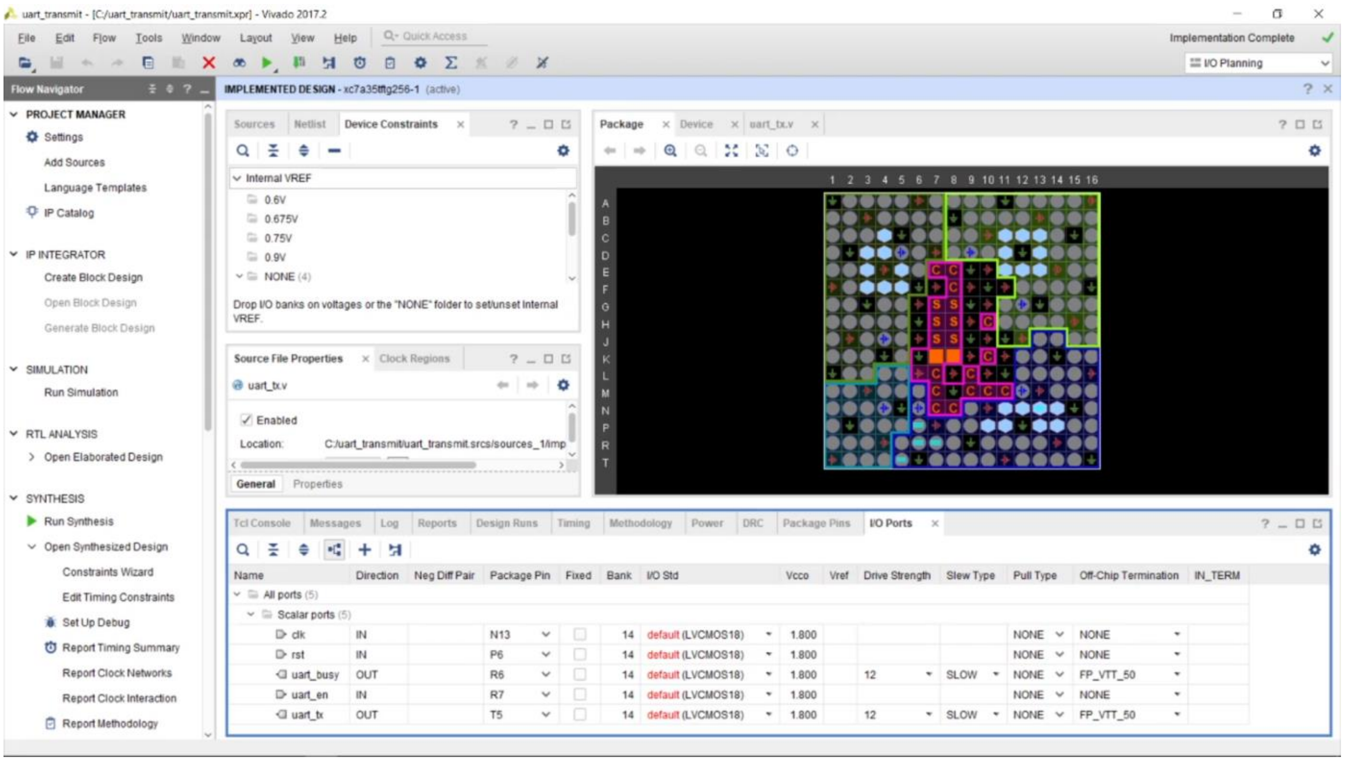
##############################################################################################################
#                         FT2232H Signals                                      #
##############################################################################################################
set_property -dict { PACKAGE_PIN "M16"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { DATA[0] }] ;        # IO_L7P_T1_D09_14         Sch = FTDI_D0
set_property -dict { PACKAGE_PIN "N16"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { DATA[1] }] ;        # IO_L7N_T1_D10_14         Sch = FTDI_D1
set_property -dict { PACKAGE_PIN "P15"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { DATA[2] }] ;        # IO_L8P_T1_D11_14         Sch = FTDI_D2
set_property -dict { PACKAGE_PIN "P16"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { DATA[3] }] ;        # IO_L8N_T1_D12_14         Sch = FTDI_D3
set_property -dict { PACKAGE_PIN "R15"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { DATA[4] }] ;        # IO_L9P_T1_DQS_14         Sch = FTDI_D4
set_property -dict { PACKAGE_PIN "R16"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { DATA[5] }] ;        # IO_L9N_T1_DQS_D13_14      Sch = FTDI_D5
set_property -dict { PACKAGE_PIN "T14"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { DATA[6] }] ;        # IO_L10P_T1_D14_14        Sch = FTDI_D6
set_property -dict { PACKAGE_PIN "T15"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { DATA[7] }] ;        # IO_L10N_T1_D15_14        Sch = FTDI_D7

set_property -dict { PACKAGE_PIN "T8"    IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { TXE_N }]   ;        # IO_L21N_T3_DQS_A06_D22_14   Sch = FTDI_TXE_N
set_property -dict { PACKAGE_PIN "T7"    IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { RXE_N }]   ;        # IO_L21P_T3_DQS_14          Sch = FTDI_RXE_N
set_property -dict { PACKAGE_PIN "P14"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { WR_N  }]   ;        # IO_L12N_T1_MRCC_14         Sch = FTDI_WR_N
set_property -dict { PACKAGE_PIN "N12"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { RD_N  }]   ;        # IO_L13N_T2_MRCC_14         Sch = FTDI_RD_N
set_property -dict { PACKAGE_PIN "N14"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { CLKOUT}]   ;        # IO_L12P_T1_MRCC_14         Sch = FTDI_CLKOUT
set_property -dict { PACKAGE_PIN "L15"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { OE_N  }]   ;        # IO_L3P_T0_DQS_PUDC_B_14     Sch = FTDI_OE#
set_property -dict { PACKAGE_PIN "M12"   IOSTANDARD LVCMOS33     SLEW FAST} [get_ports { SIWUA }]   ;        # IO_L6N_T0_D08_VREF_14      Sch = FTDI_SIWUA

##############################################################################################################
#                     DDR3       : MT41J128M16XX-125                           #
#                     Frequency  : 400 MHz                          #
#                     Data Width : 16                          #
##############################################################################################################
set_property -dict { PACKAGE_PIN "G2"   IOSTANDARD SSTL15   SLEW FAST} [get_ports {ddr3_dq[0]}]   ;        # IO_L17P_T2_35          Sch = DDR3_DQ0
set_property -dict { PACKAGE_PIN "F3"   IOSTANDARD SSTL15   SLEW FAST} [get_ports {ddr3_dq[1]}]   ;        # IO_L14N_T2_SRCC_35      Sch = DDR3_DQ1
set_property -dict { PACKAGE_PIN "H4"   IOSTANDARD SSTL15   SLEW FAST} [get_ports {ddr3_dq[2]}]   ;        # IO_L18N_T2_SRCC_35      Sch = DDR3_DQ2
set_property -dict { PACKAGE_PIN "G5"   IOSTANDARD SSTL15   SLEW FAST} [get_ports {ddr3_dq[3]}]   ;        # IO_L16P_T2_35          Sch = DDR3_DQ3
set_property -dict { PACKAGE_PIN "G1"   IOSTANDARD SSTL15   SLEW FAST} [get_ports {ddr3_dq[4]}]   ;        # IO_L17N_T2_35          Sch = DDR3_DQ4
set_property -dict { PACKAGE_PIN "F4"   IOSTANDARD SSTL15   SLEW FAST} [get_ports {ddr3_dq[5]}]   ;        # IO_L14P_T2_SRCC_35      Sch = DDR3_DQ5
set_property -dict { PACKAGE_PIN "H5"   IOSTANDARD SSTL15   SLEW FAST} [get_ports {ddr3_dq[6]}]   ;        # IO_L18P_T2_35          Sch = DDR3_DQ6
```

And have the necessary requirements, and when I say requirements, we need many ports for signals(user and programmimg chaneel), clock, Mimas A7 Mini does not have any reset we will use the push button pins,LED

We will use low voltage CMOS, LVCMOS33



Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.

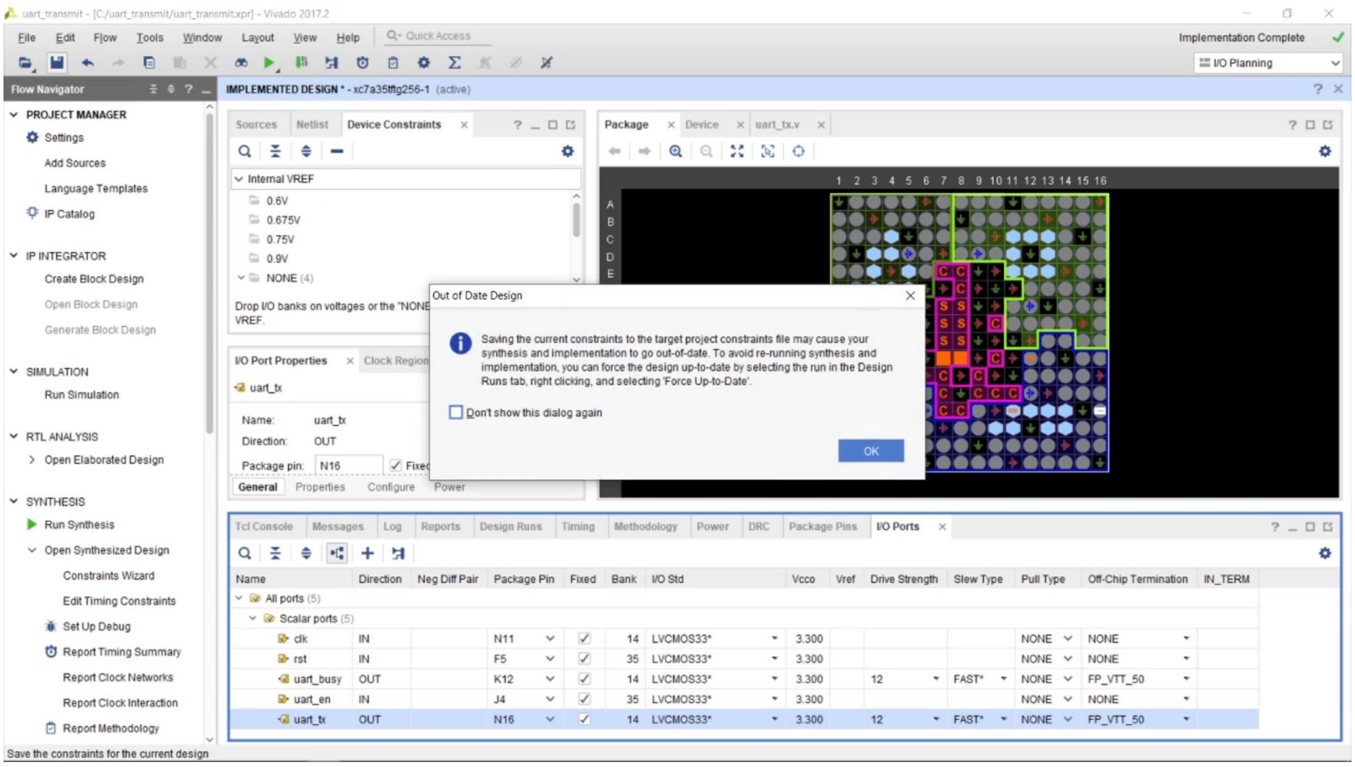
uart_tx.v

✓ Enabled

Location: C:/uart_transmit/uart_transmit.srcs/sources_1/imp

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
All ports (5)													
Scalar ports (5)													
clk	IN		N13	☐	14	default (LVCMOS18)	1.800				NONE	NONE	
rst	IN		P6	☐	14	default (LVCMOS18)	1.800				NONE	NONE	
uart_busy	OUT		R6	☐	14	default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_50	
uart_en	IN		R7	☐	14	default (LVCMOS18)	1.800				NONE	NONE	
uart_tx	OUT		T5	☐	14	default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_50	

After the necessary changes save it and name the file as "uart_tx"



Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.

uart_tx

Name: uart_tx

Direction: OUT

Package pin: N16 ✓ Fixed

Out of Date Design

Saving the current constraints to the target project constraints file may cause your synthesis and implementation to go out-of-date. To avoid re-running synthesis and implementation, you can force the design up-to-date by selecting the run in the Design Runs tab, right clicking, and selecting 'Force Up-to-Date'.

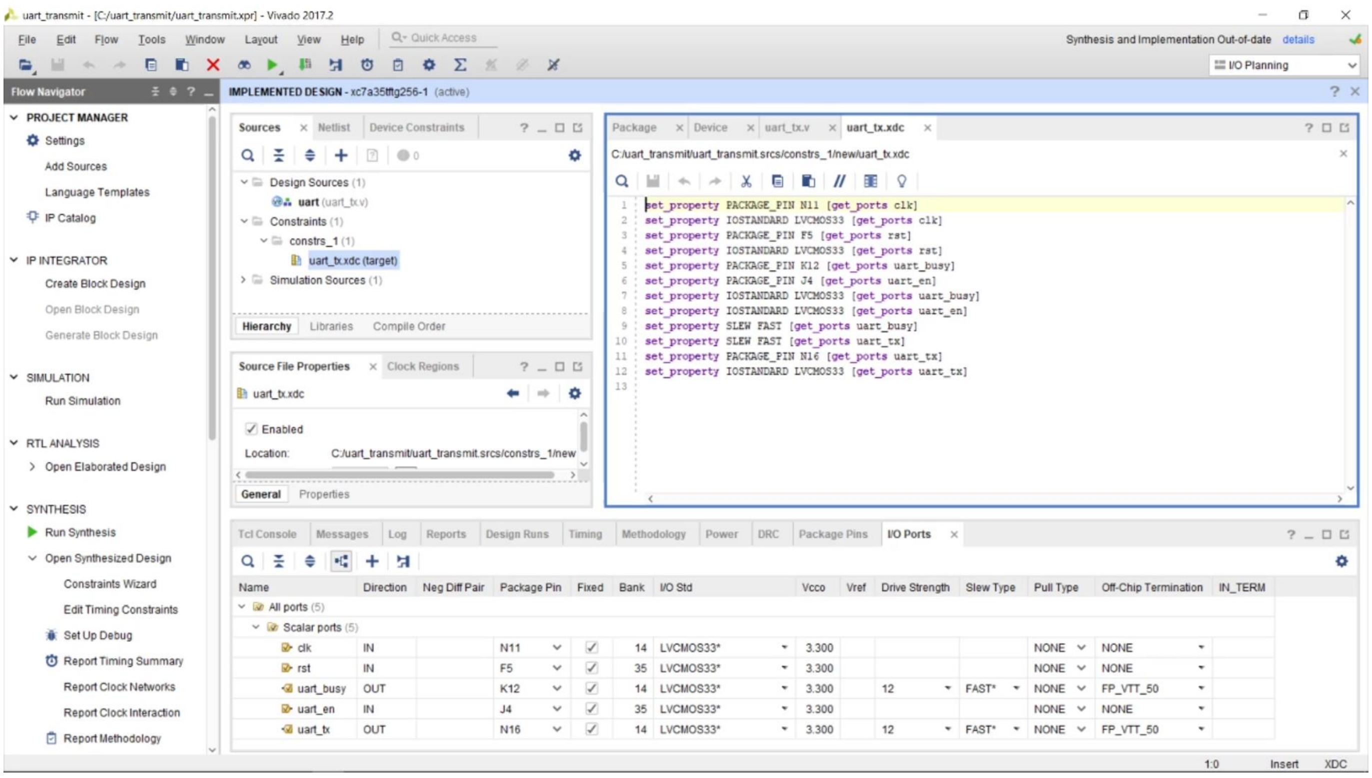
☐ Don't show this dialog again

OK

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
All ports (5)													
Scalar ports (5)													
clk	IN		N11	✓	14	LVCMOS33*	3.300				NONE	NONE	
rst	IN		F5	✓	35	LVCMOS33*	3.300				NONE	NONE	
uart_busy	OUT		K12	✓	14	LVCMOS33*	3.300		12	FAST*	NONE	FP_VTT_50	
uart_en	IN		J4	✓	35	LVCMOS33*	3.300				NONE	NONE	
uart_tx	OUT		N16	✓	14	LVCMOS33*	3.300		12	FAST*	NONE	FP_VTT_50	

Save the constraints for the current design

After that we can see in the source file under constrains and the I/O standards are given



uart_transmit - [C:/uart_transmit/uart_transmit.xpr] - Vivado 2017.2

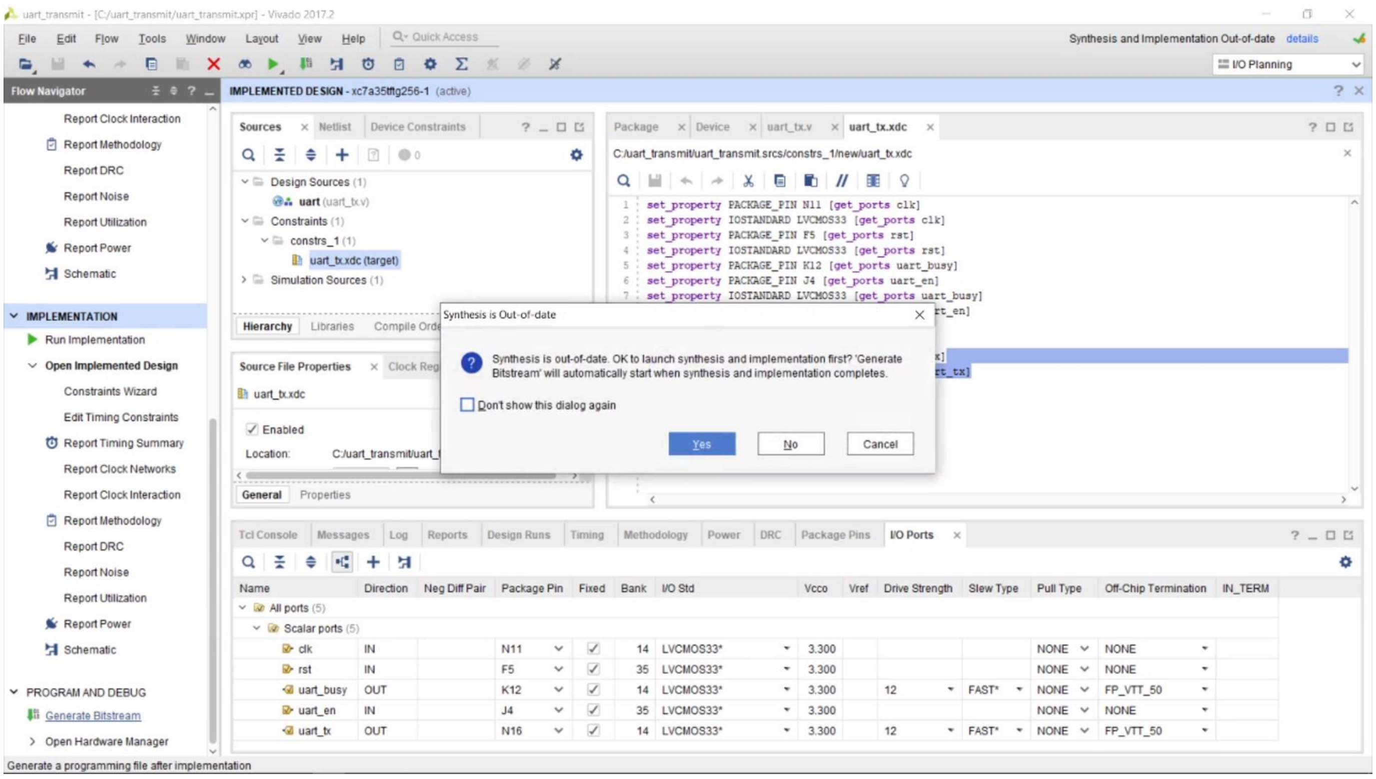
IMPLEMENTED DESIGN - xc7a35tftg256-1 (active)

C:/uart_transmit/uart_transmit.srcs/constrs_1/new/uart_tx.xdc

```
set_property PACKAGE_PIN N11 [get_ports clk]
set_property IOSTANDARD LVCMOS33 [get_ports clk]
set_property PACKAGE_PIN F5 [get_ports rst]
set_property IOSTANDARD LVCMOS33 [get_ports rst]
set_property PACKAGE_PIN K12 [get_ports uart_busy]
set_property PACKAGE_PIN J4 [get_ports uart_en]
set_property IOSTANDARD LVCMOS33 [get_ports uart_busy]
set_property IOSTANDARD LVCMOS33 [get_ports uart_en]
set_property SLEW FAST [get_ports uart_busy]
set_property SLEW FAST [get_ports uart_tx]
set_property PACKAGE_PIN N16 [get_ports uart_tx]
set_property IOSTANDARD LVCMOS33 [get_ports uart_tx]
```

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
All ports (5)													
Scalar ports (5)													
clk	IN		N11	✓	14	LVCMOS33*	3.300				NONE	NONE	
rst	IN		F5	✓	35	LVCMOS33*	3.300				NONE	NONE	
uart_busy	OUT		K12	✓	14	LVCMOS33*	3.300		12	FAST*	NONE	FP_VTT_50	
uart_en	IN		J4	✓	35	LVCMOS33*	3.300				NONE	NONE	
uart_tx	OUT		N16	✓	14	LVCMOS33*	3.300		12	FAST*	NONE	FP_VTT_50	

Generate bit stream after that, resulting in synthesis and implementation

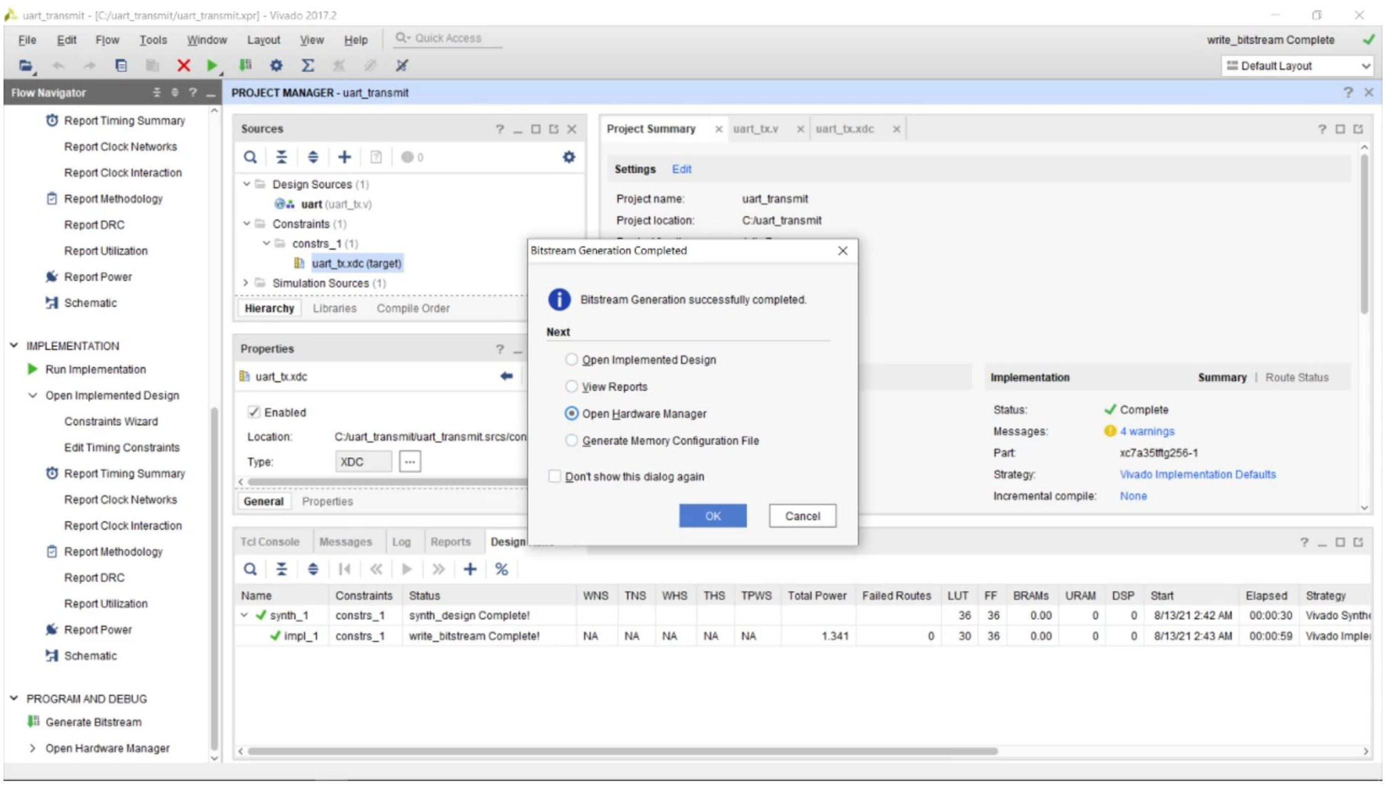


Synthesis is Out-of-date

Synthesis is out-of-date. OK to launch synthesis and implementation first? 'Generate Bitstream' will automatically start when synthesis and implementation completes.

Don't show this dialog again

After the generation of bit stream open hardware manager



Enabled

Location: C:/uart_transmit/uart_transmit.srcs/con

Type: XDC

Project name: uart_transmit

Project location: C:/uart_transmit

Status: ✓ Complete

Messages: 4 warnings

Part: xc7a35tftg256-1

Strategy: Vivado Implementation Defaults

Incremental compile: None

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

Open Implemented Design

View Reports

[✓ Open Hardware Manager]

Generate Memory Configuration File

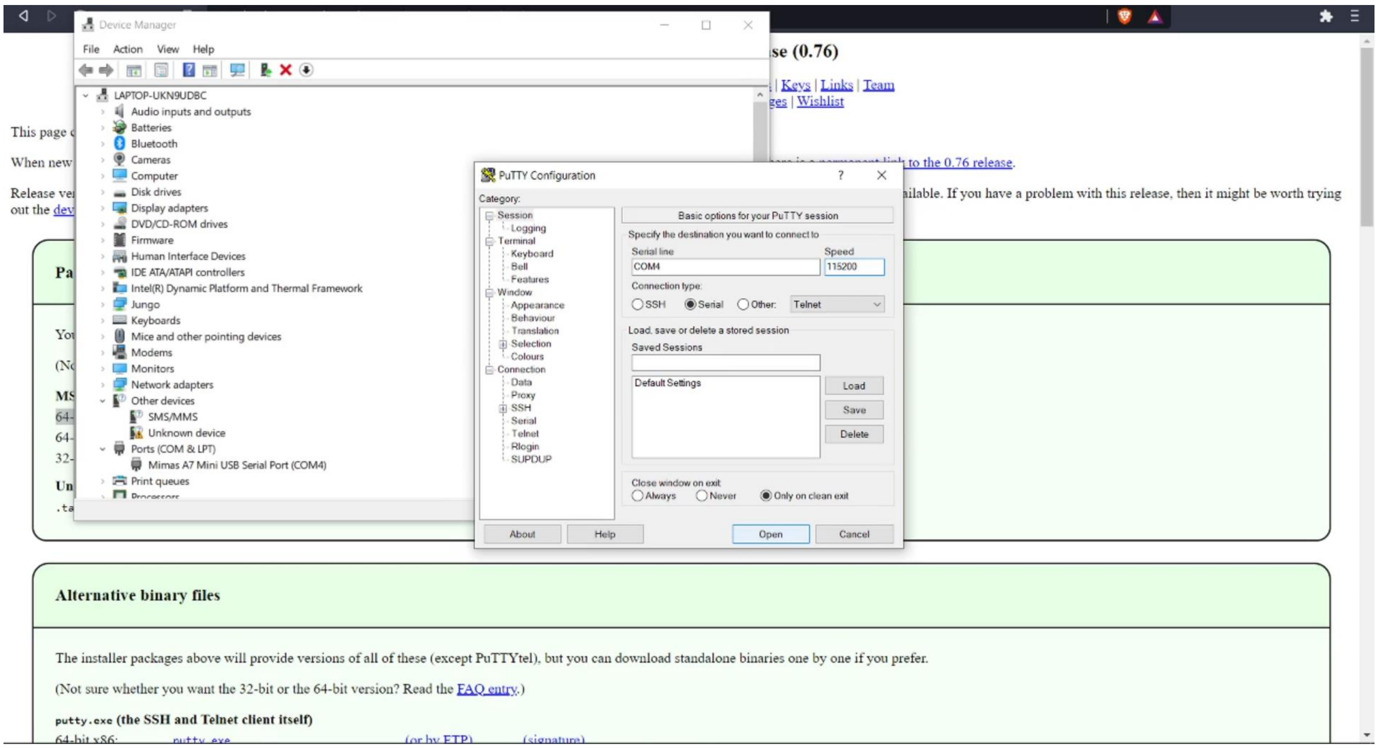
Don't show this dialog again

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Strategy
✓ synth_1	constrs_1	synth_design Complete!								36	36	0.00	0	0	8/13/21 2:42 AM	00:00:30	Vivado Synth
✓ impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	1.341	0	30	36	0.00	0	0	8/13/21 2:43 AM	00:00:59	Vivado Imple

Step 3- Download a serial monitor , we will be using a light weight serial monitor software

Download PuTTY - a free SSH and telnet client for Windows link to download

After that launch Putty with a a serial line as "COM 4" shown in device manager used in the following case , and the speed we know set as 15200, and then open the termnal.


Device Manager

LAPTOP-UKN9UDBC
- Audio inputs and outputs
- Batteries
- Bluetooth
- Cameras
- Computer
- Disk drives
- Display adapters
- DVD/CD-ROM drives
- Firmware
- Human Interface Devices
- IDE ATA/ATAPI controllers
- Intel(R) Dynamic Platform and Thermal Framework
- Jungo
- Keyboards
- Mice and other pointing devices
- Modems
- Monitors
- Network adapters
- Other devices
  - SMS/MMS
  - Unknown device
- Ports (COM & LPT)
  - Mimas A7 Mini USB Serial Port (COM4)
- Print queues

PuTTY Configuration

Basic options for your PuTTY session

Specify the destination you want to connect to

Serial line: COM4

Speed: 115200

Connection type: SSH [✓ Serial] Other: Telnet

Load, save or delete a stored session

Saved Sessions: Default Settings

Close window on exit: Always Never [✓ Only on clean exit]

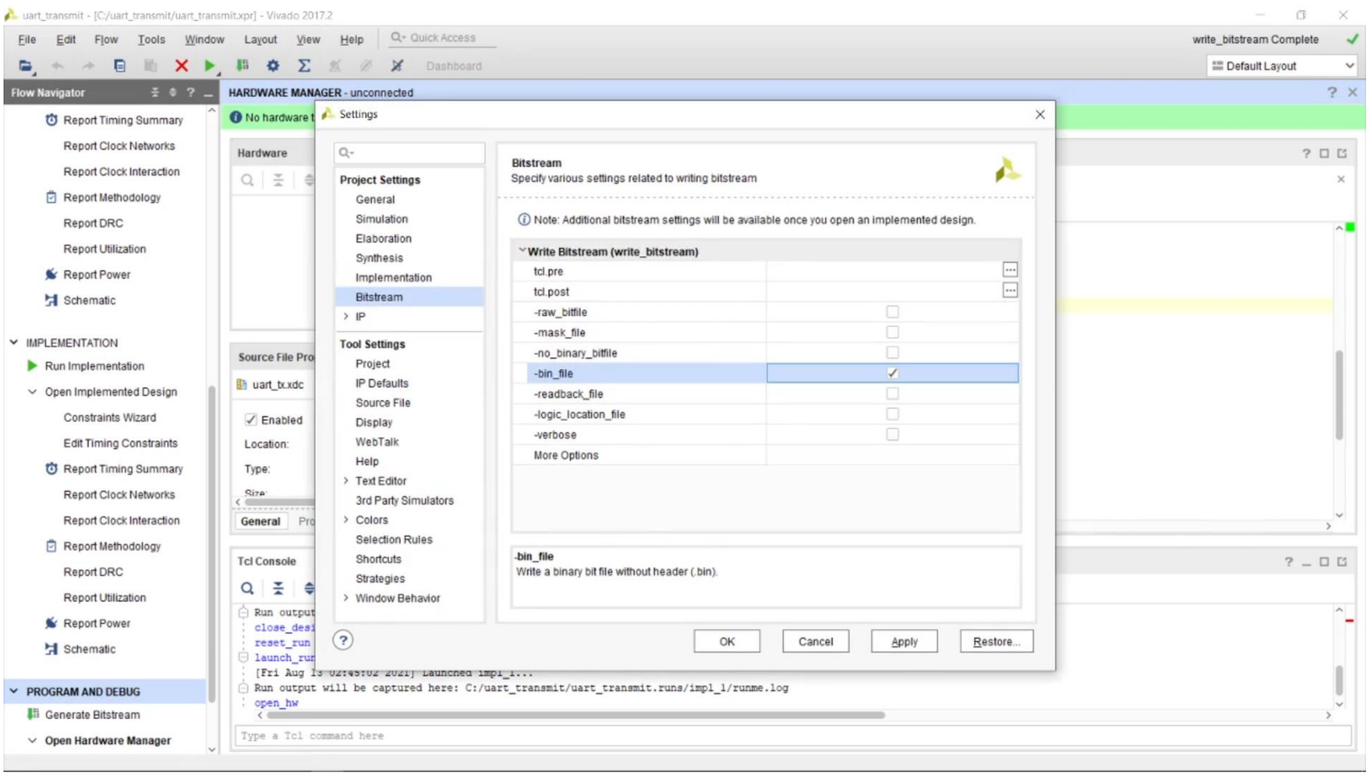
Alternative binary files

The installer packages above will provide versions of all of these (except PuTTYtel), but you can download standalone binaries one by one if you prefer.

(Not sure whether you want the 32-bit or the 64-bit version? Read the FAQ entry.)

putty.exe (the SSH and Telnet client itself)

Step 4- Open Tenegra application and synch vivado bitstream file , you can go to setting and create one .



uart_transmit - [C:/uart_transmit/uart_transmit.xpr] - Vivado 2017.2

Settings

Bitstream
Specify various settings related to writing bitstream

Note: Additional bitstream settings will be available once you open an implemented design.

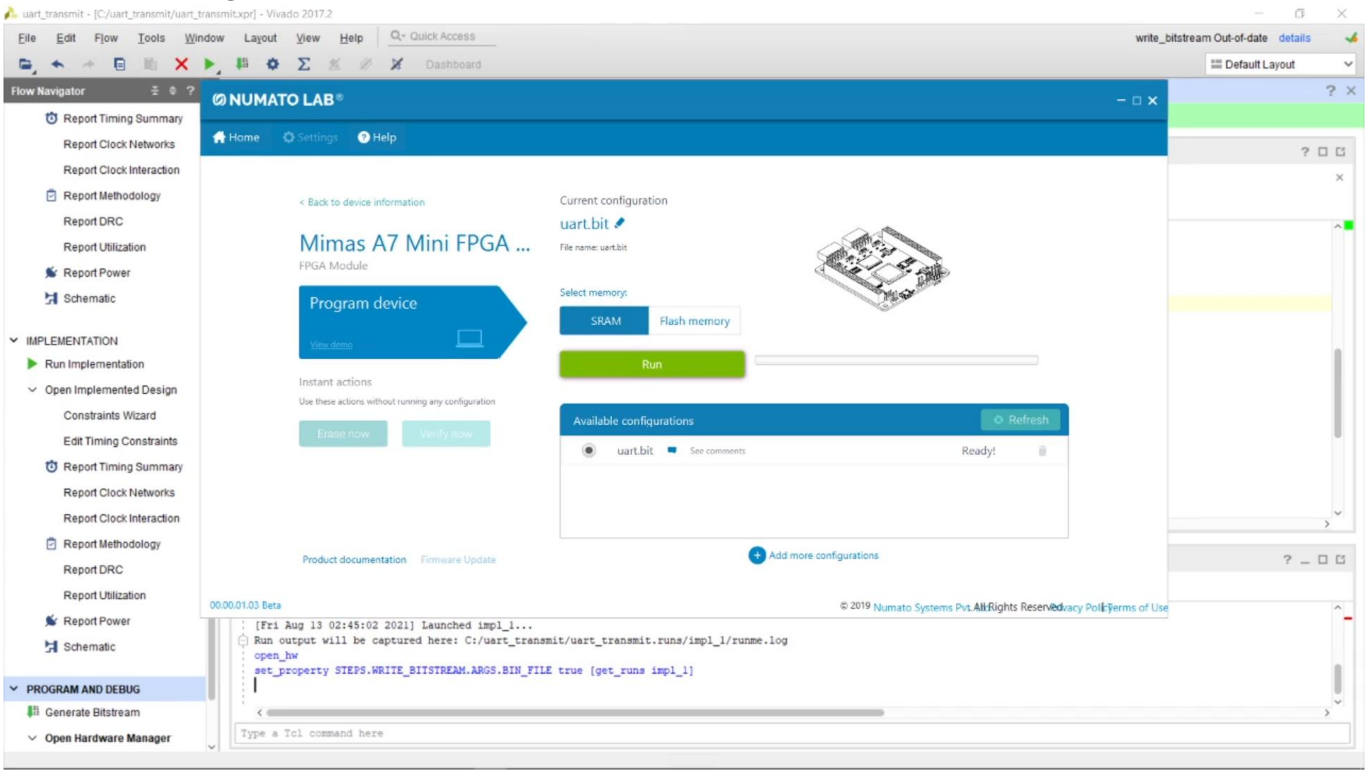
Write Bitstream (write_bitstream)

tcl.pre	
tcl.post	
-raw_bitfile	☐
-mask_file	☐
-no_binary_bitfile	☐
-bin_file	✓
-readback_file	☐
-logic_location_file	☐
-verbose	☐
More Options	

-bin_file
Write a binary bit file without header (.bin).

```
[Fri Aug 13 02:45:02 2021] Launched impl_1...
Run output will be captured here: C:/uart_transmit/uart_transmit.runs/impl_1/runme.log
open_hw
```

After chosing the file select SRAM and run it



uart_transmit - [C:/uart_transmit/uart_transmit.xpr] - Vivado 2017.2

Mimas A7 Mini FPGA ...
FPGA Module

Current configuration
uart.bit
File name: uart.bit

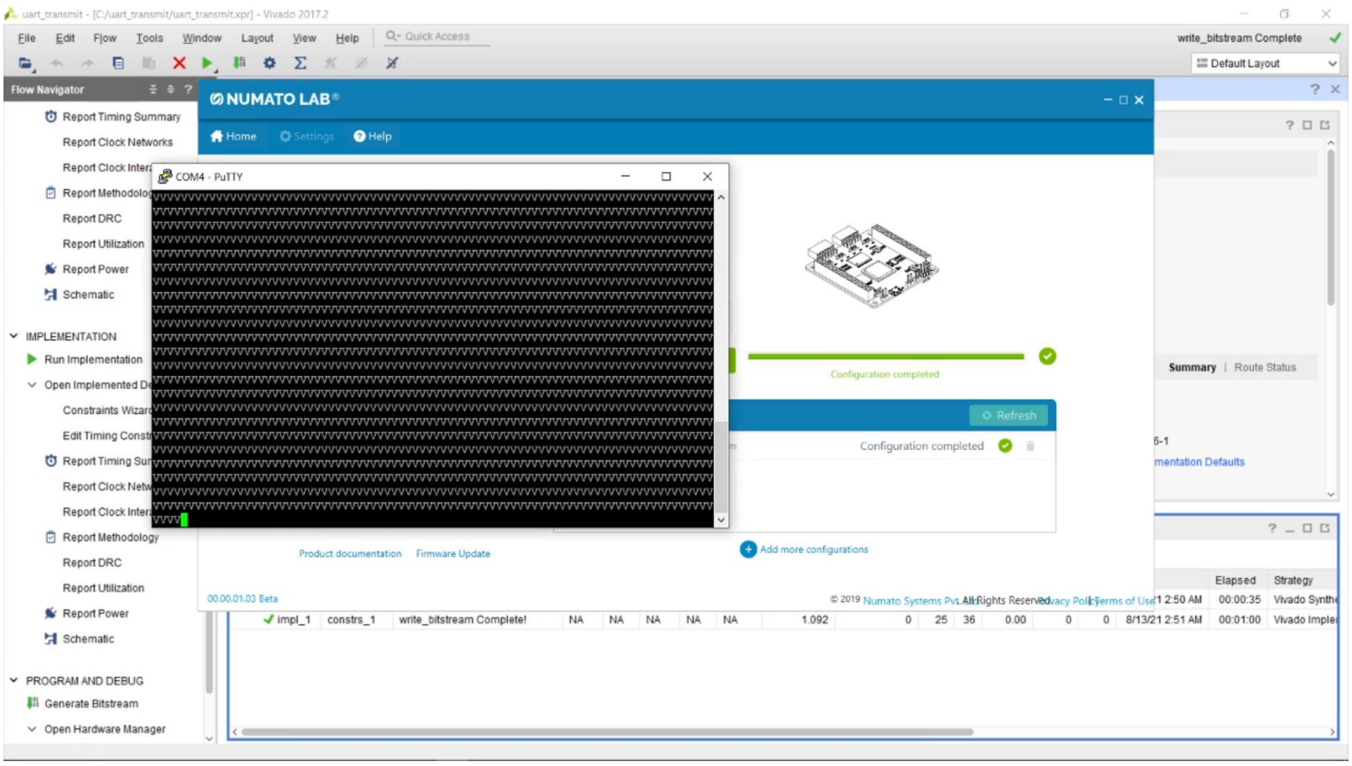
Select memory: [✓ SRAM] Flash memory

Available configurations

●	uart.bit	Ready!

```
[Fri Aug 13 02:45:02 2021] Launched impl_1...
Run output will be captured here: C:/uart_transmit/uart_transmit.runs/impl_1/runme.log
open_hw
set_property STEPS.WRITE_BITSTREAM.ARGS.BIN_FILE true [get_runs impl_1]
```

As we know that with push button is enabled with the input of letter we have created so in our case push button will work that way.Every time we press the push button the letter V gets automatically printed in its own.



uart_transmit - [C:/uart_transmit/uart_transmit.xpr] - Vivado 2017.2

write_bitstream Complete

COM4 - PuTTY

```
VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
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NUMATO LAB®

Configuration completed

Configuration completed

00.00.01.03 Beta

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																Elapsed	Strategy
															1 2:50 AM	00:00:35	Vivado Synth
✓ impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	1.092	0	25	36	0.00	0	0	8/13/21 2:51 AM	00:01:00	Vivado Imple