EE517: ANALOG VLSI LAB

Final course Project

Design and analysis of a 2-stage op-amp considering area optimization.

Submitted by,
Pushpendra Gurjar
Roll No - 234102414
Batch no:3

EEE - VLSI & Nanoelectronics

Contents

1 OBJECTIVE

Design a 2-stage Op-amp in 180 nm technology for low area(area should be minimum).

1.1 Design Specification:

Supply voltage (VDD) = 1.8 V
Reference current source (Iref) = 20 µA
Slew rate >= 1V/µs
Phase margin >= 60
Load Capacitance (CL) = 10pF
ICMR = 0.6- 1.4 V

Gain >= 40dB
GBW >=10MHz
Pdiss <=1mW
Lmax <= 2µm

1.2 Observations

1.2.1 DC Analysis

• Report the schematic of the diff pair with DC OP point annotated: Id, Vgs, Vds, Vth, Vdsat, gm, gds, gmb, region.
• Check that all transistors operate in saturation

1.2.2 AC Analysis

• Observe pole-zero analysis of your circuit.
• Frequency response of your circuit.
• Find Av, PM, Bandwidth, CMRR, PSRR.
• Give a proper reason for selecting any value of any parameter.

1.2.3 Transient Analysis

• Slew rate.
• ICMR, OCMR.

2 Theory

Since there are three high impedance nodes after cascading the two stages, we have stability issues even though we have only recently linked the two stages.Thus, the two poles that will be below the unit gain cross over frequency are listed. It will bring about instability.So, in order to make one pole dominant over the other poles, we must connect one capacitor.

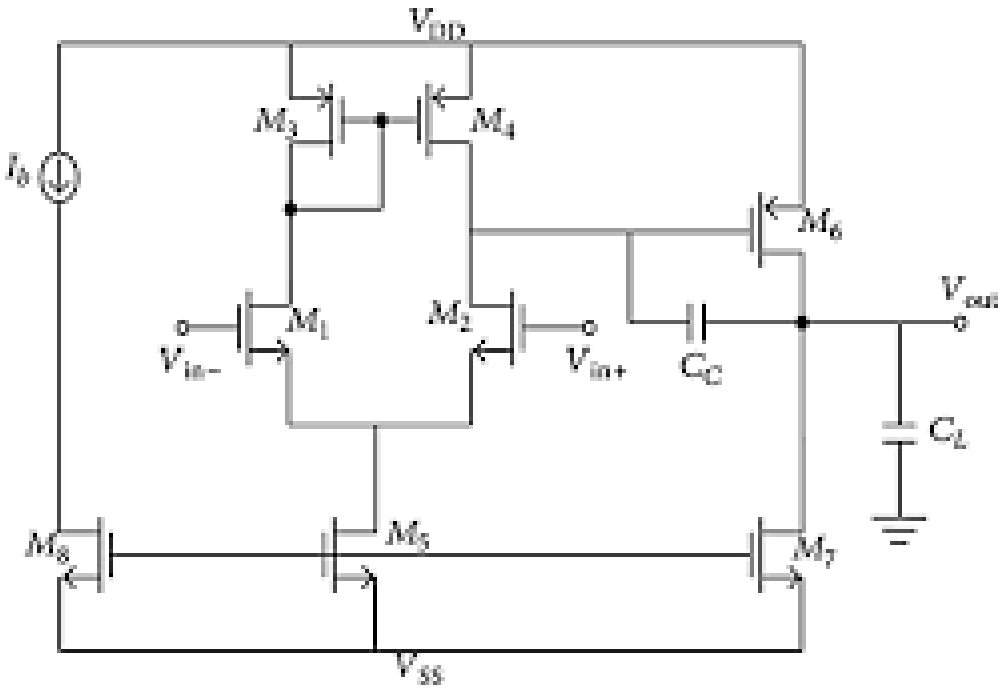

Figure 1: 2 stage OP AMP

In order for the increase cross over frequency to only be experienced by one pole.since the pole and capacitance are known to be inversely correlated.We must therefore link the high capacitance in order to create the dominating pole.Therefore, we just apply the Miller Theorem's one capacitance.For the above circuit, this means that it will offer a big capacitance with a tiny value (Cc).

3 Parameters to be measured

3.1 Slew Rate

For a large input step voltage, some transistors in the op-amp may be driven out of their saturation regions or completely cut-off. As a result the output will follow the input at a slower finite rate. The maximum rate of change dVo/dt is called slew rate.
General formula for slew rate is

$$slewrate = (\frac{dV_{out}}{dt})_{max} \tag{1}$$

3.2 ICMR

ICMR means nothing but Input the common mode range.In general, it is defined as the range of common mode inputs that can be applied to that circuit while keeping all transistors saturated.Maximum ICMR refers to the maximum common mode input values that can be applied.

3.3 GBWP

Gain Band Width Product ,of an amplifier ,product of Open Loop gain times frequency range at which amplifier gain attenuated to -20dB.

3.4 CMRR

The Common-Mode Rejection Ratio (CMRR) indicates the ability of a differential amplifier to suppress signals common to the two inputs. Desired signals should appear on only one input or with opposite polarities on both inputs. These desired signals are amplified and appear on the outputs.

3.5 PSRR

The power supply rejection ratio (PSRR) describes the ability of a circuit to suppress any power supply variations from passing to its output signal and is typically measured in dB.

4 Design approach for low area

- first, we find Maximum current Vdd can provide without failing power constraint (Idd = 550uA).
- Components of Idd are Iref, I5, I6. We know that Iref = 20uA, then I5 + I7 at max can be 530uA.
- since design procedure started from SR which is a function of I5 and CC we decide on them initially based on dependencies.
- I5 $\propto \frac{1}{S1}, \frac{1}{S8}, \frac{1}{S2}$,S3,$\frac{1}{S5}, \sqrt{Gm1}$,SR
- CC $\propto \frac{1}{GBW}$,Gm1,Gm6
- There is more Area dependence on I5 than on CC. Higher I5, Lower S1,S8,S2,S5.
- I5 will proportionally effect S3,S4 but both are limited by ICMR hence we can keep it up to 2.5.
- I5 is also proportional to I7(I6). But I5 and I6 both are limited by power constraints. Hence we cannot increase I5 as much as we want.
- since give SR(min) = 1, we have designed it for SR = 2.
- CC $\geq$ 0.22 CL, given CL = 10pf. Hence CC $\geq$ 22pf
- for SR = 2, We need I5 = 20uA.
- for safe stability , we need Zero ¿ 10 Pole_2. Hence we need CC $\geq$ 0.22 CL and Gm6 $\geq$ 10 Gm1.
- Above given constraints are not standardized but will ensure that circuit will not be unstable.
- we designed for Gm6 = 4 Gm1, still circuit is stable.
- using the above stated design procedure, we obtained values which are mentioned in the following sections.

5 Design Approach for 2-stage

5.0.1 Step 1

We assumed a 60-degree phase margin and zero frequency at more than ten times the Gain Band width product.So, using the foregoing assumptions, we solved the equation of a one zero and two pole system to obtain the equation.

$$(millercapacitance)C_c > 0.22C_L \tag{2}$$

They given C_L is 10 pF.so we got miller capacitance is

$$C_c > 2.2pF \tag{3}$$

so we have taken minimum value 4.5pF

5.0.2 Step 2

The design specification specifies a slew rate of 10 volts per microsecond. In the circuit above, the maximum output value occurs when M1 is turned off and M2 is turned on. As M3 and M1 are in series, the M1 current is also zero. M3 and M4 are joined in

If the current is mirrored, then the M4 current is also zero.The entire VDD will be at the drain of M2, with M5 current flowing via the Cc capacitor.The slew rate for the above circuit will be

$$slewrate = \frac{I_5}{C_c} \tag{4}$$

we know slew rate and C_L from equation 8.so

$$I_5 = 20\mu A \tag{5}$$

5.0.3 Step 3

we have the gain band width product will be the voltage unit gain frequency .because we have dominent pole ,so we have 20 db decay will happens at unit gain frequency.

$$gm_1 = GBW * 2\pi C_c \tag{6}$$

we have the GBW ,cc values so we got gm_1

$$gm_1 = 622.03\mu A \tag{7}$$

we have the gm equation

$$gm_1 = \sqrt{2I_d\mu_n C_{ox}\frac{W}{L}_1} \tag{8}$$

if you substitute the values in above equation we got

$$\frac{W}{L}_1 = 56.55 \tag{9}$$

as we know M1 and M2 are need to be symmetric so we have taken

$$\frac{W}{L}_1 = \frac{W}{L}_2 = 56.55 \tag{10}$$

5.0.4 Step 4

They given maximum ICMR value 1.6.so from above circuit we for M1 in saturation

$$V_{d1} > V_g - V_{th1} \tag{11}$$

$$V_g < V_{d1} + V_{th1} \tag{12}$$

$$V_g < (V_{dd} - V_{sg3}) + V_{th1} \tag{13}$$

$$V_g < (V_{dd} - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox}\frac{W}{L}3}}) + Vth1 \tag{14}$$

here gate voltage is the maximum ICMR voltage .so if you you substitute the all values you got the (WŁ) of M3

$$ICMRmax = (Vdd - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox}\frac{W}{L}3}}) + Vth1 \tag{15}$$

$$\frac{W}{L}_3 = 2.5 \tag{16}$$

as we know M3 and M4 are need to be symmetric so we have taken

$$\frac{W}{L}_3 = \frac{W}{L}_4 = 2.5 \tag{17}$$

5.0.5 Step 5

we know the ICMR minimum value.it will be taken from minimum gate voltage so all transistor are in saturation.so

$$V_{dsat} = ICMR_{min} - \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}1}} - Vthn \tag{18}$$

if you substitute all the values you got the Vdsat value.

$$V_{dast} = 0.147 \tag{19}$$

if you substitute the value on the current equation you got the

$$\frac{W}{L}_5 = 11.609 \tag{20}$$

so we have taken

$$\frac{W}{L}_5 = 11.609 \tag{21}$$

5.0.6 Step 6

as we taken the assumption zero frequency is 10 times of the GBW. we got the

$$gm_6 > 4 * gm_1 \tag{22}$$

we know the gm_1 from the eqution 12

$$gm_6 > 2488.12\mu A \tag{23}$$

we know M6 and M4 are in current mirror so .

$$\frac{(W/l)_6}{(W/l)_4} = \frac{I_6}{I_4} = \frac{gm_6}{gm_4} \tag{24}$$

so we know the $(w/l)_4$ and I_4 so from gm equation we got the

$$gm_4 = 58.561\mu A \tag{25}$$

from equation 29, we got

$$(w/l)_6 = 106.22 \tag{26}$$

from equation 29 we can calculate the

$$Id_6 = 424.8\mu A \tag{27}$$

5.0.7 Step 7

$$\frac{(W/l)_7}{(W/l)_5} = \frac{I_7}{I_5} \tag{28}$$

M6 and M7 are in series so both currents are equal.so we got

$$(w/l)_7 = 248.27 \tag{29}$$

we got the all the (wł) ratios ,we need to calculate the lengths.we know gain of two stage op amp is

$$gain = gm_1 gm_2 (r01||r04)(ro6||ro7) \tag{30}$$

6 CIRCUIT DIAGRAM

6.1 DC ANALYSIS

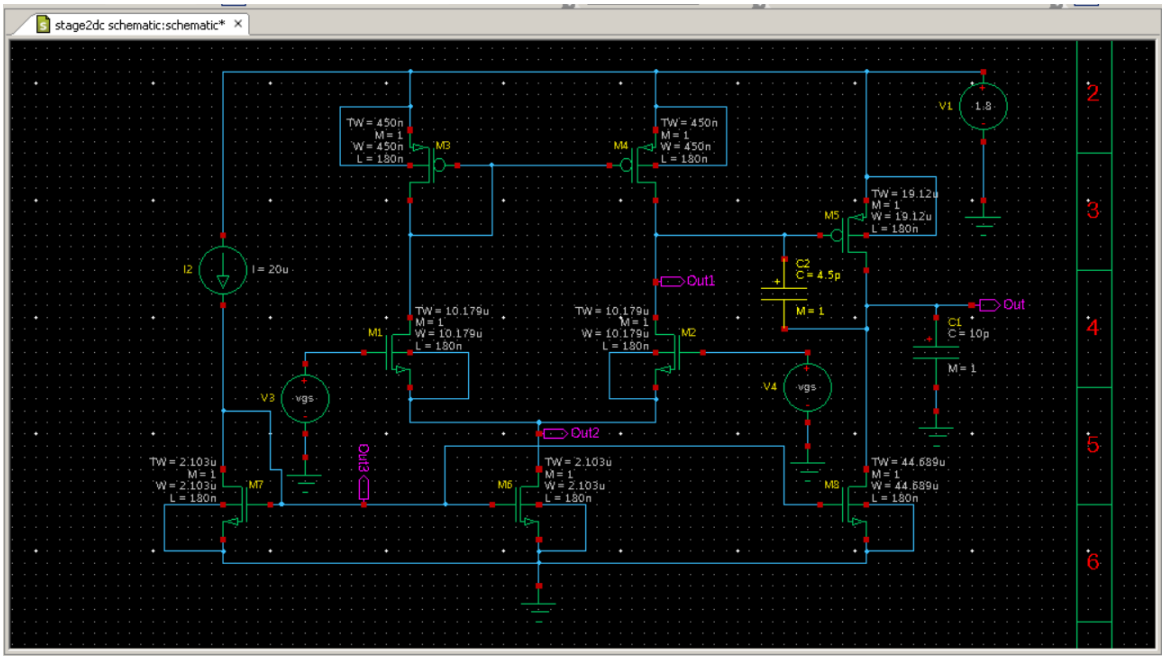

Figure 2: DC analysis schematic

6.2 AC ANALYSIS

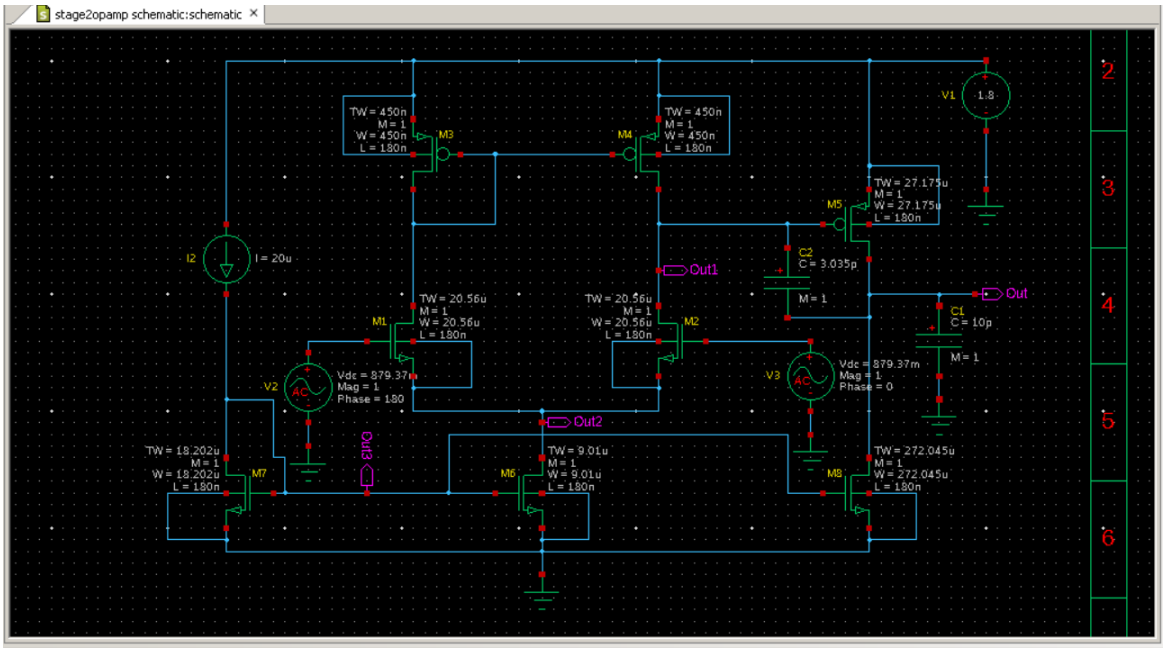

Figure 3: AC analysis schematic

7 SIMULATION RESULTS

7.0.1 DC Analysis

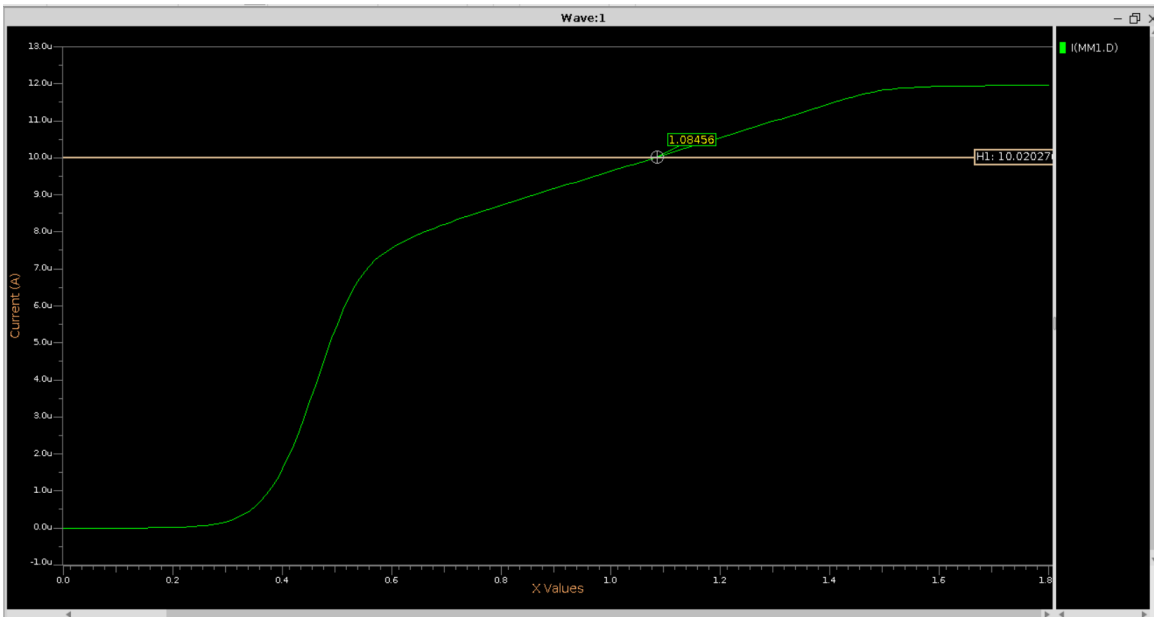

Figure 4: graph of dc analysis of 2-stage op-amp

7.0.2 AC analysis

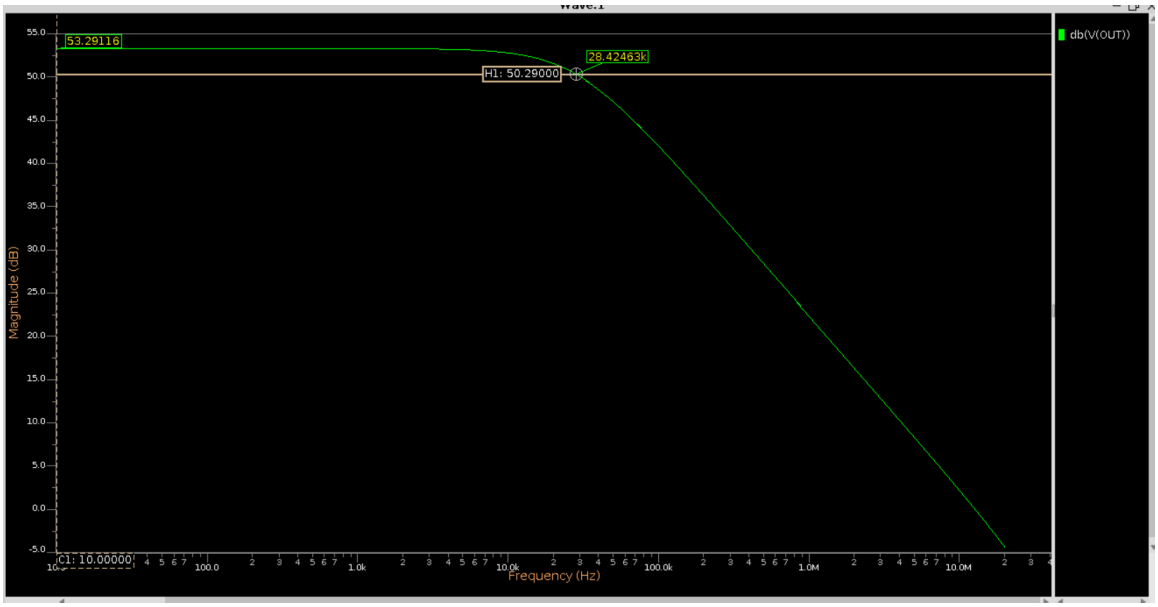

Figure 5: AC analysis Gain,3db bandwidth

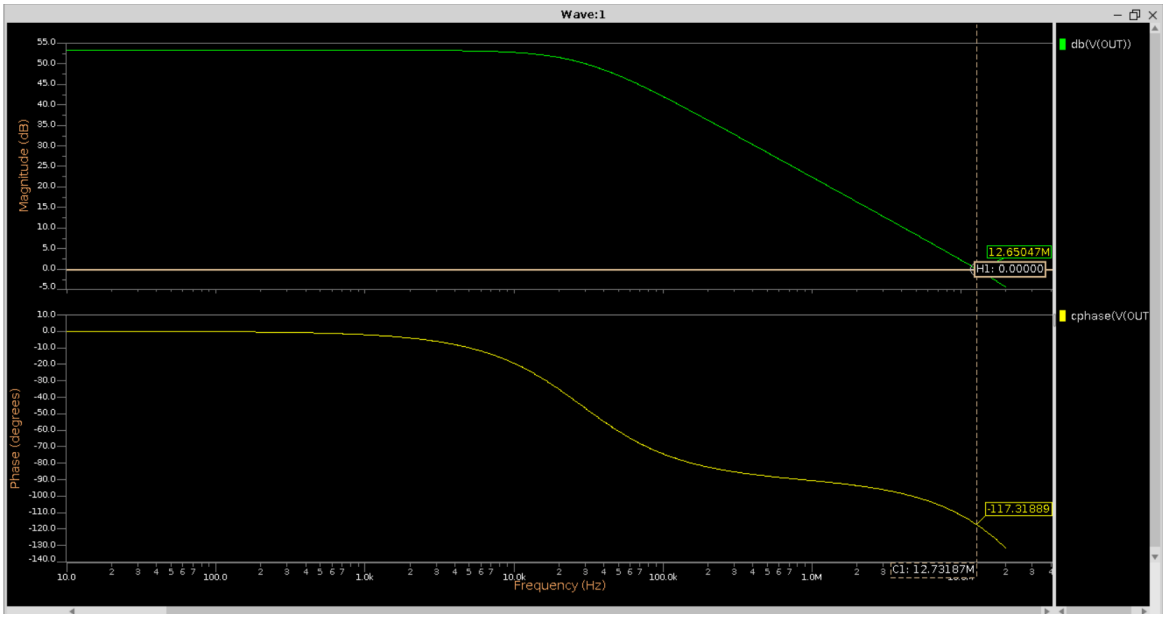

Figure 6: AC analysis GBW,Phase margin

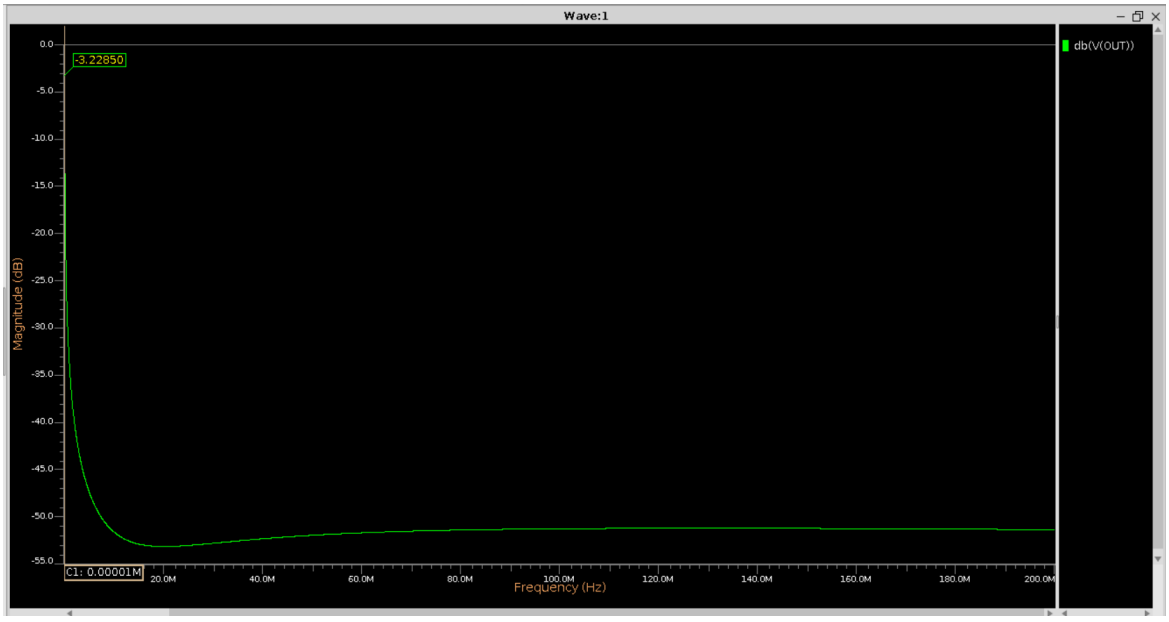

Figure 7: Common Mode gain

7.0.3 PSRR

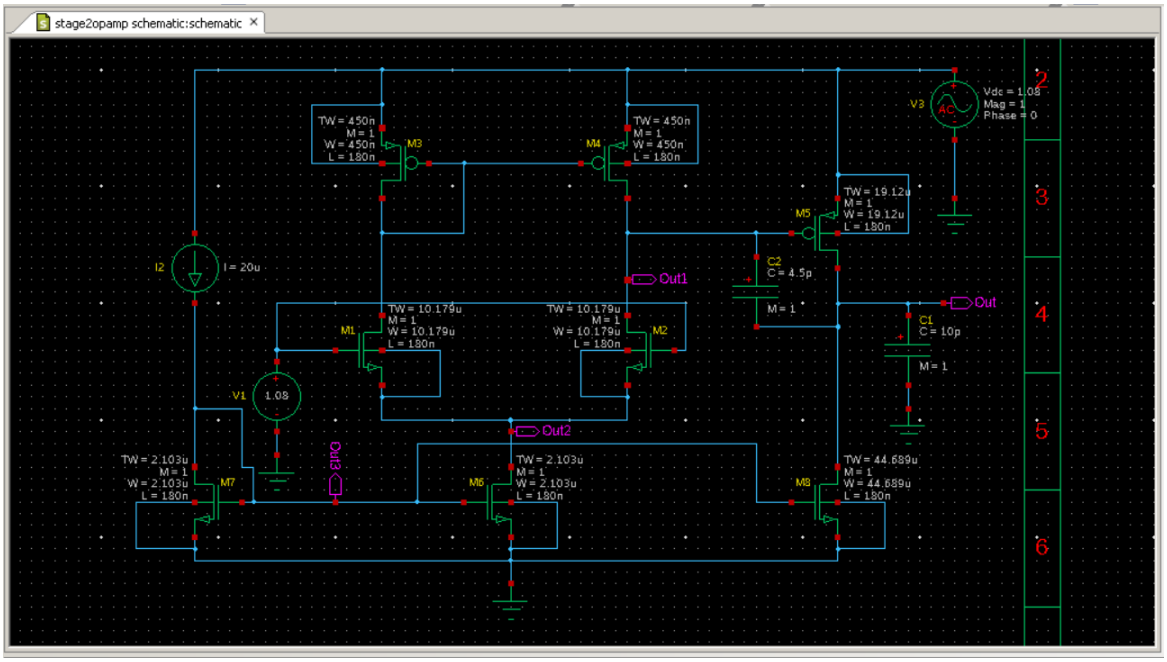

Figure 8: schematic of PSRR analysis

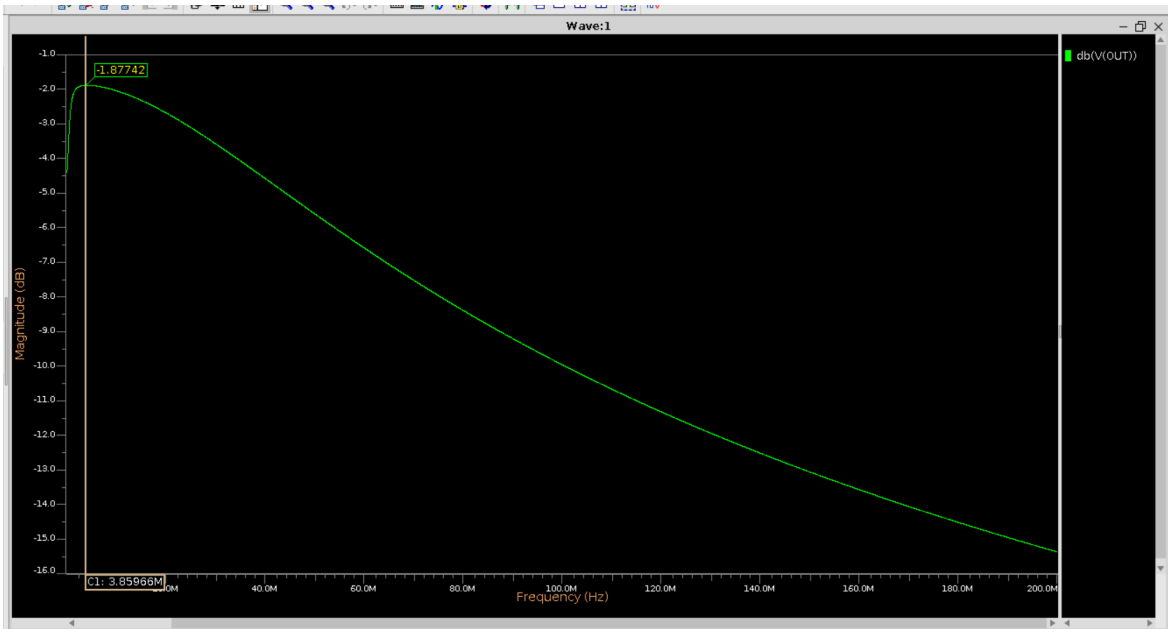

Figure 9: PSRR

7.0.4 Transient Analysis

7.0.5 Slew Rate

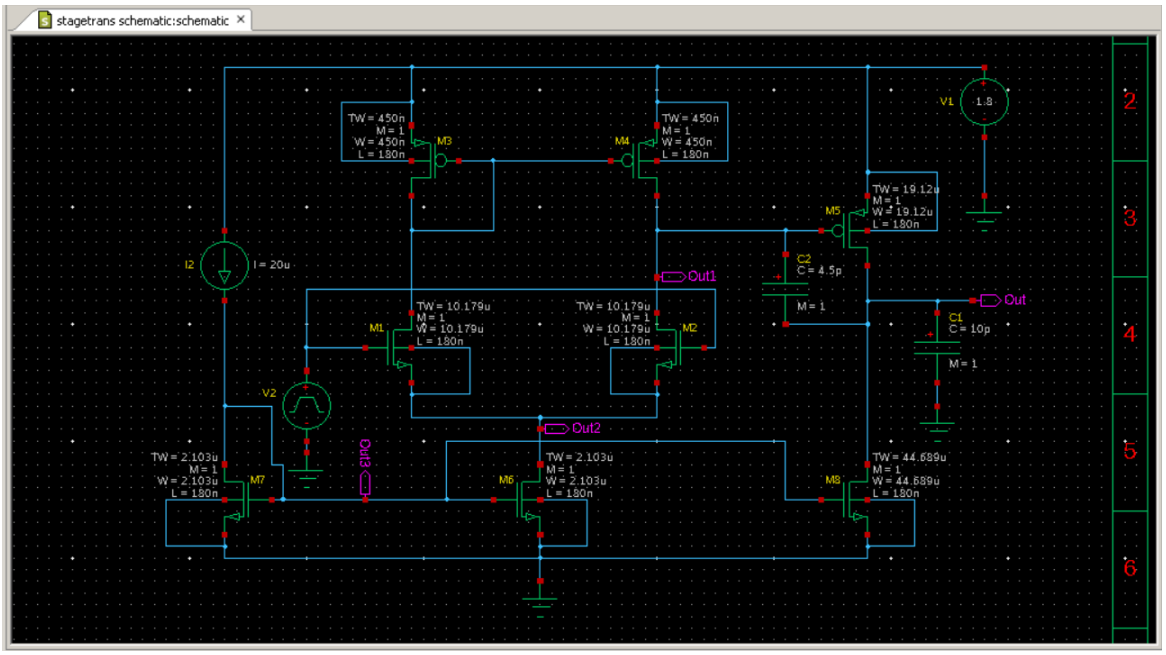

Figure 10: schematic for slew rate

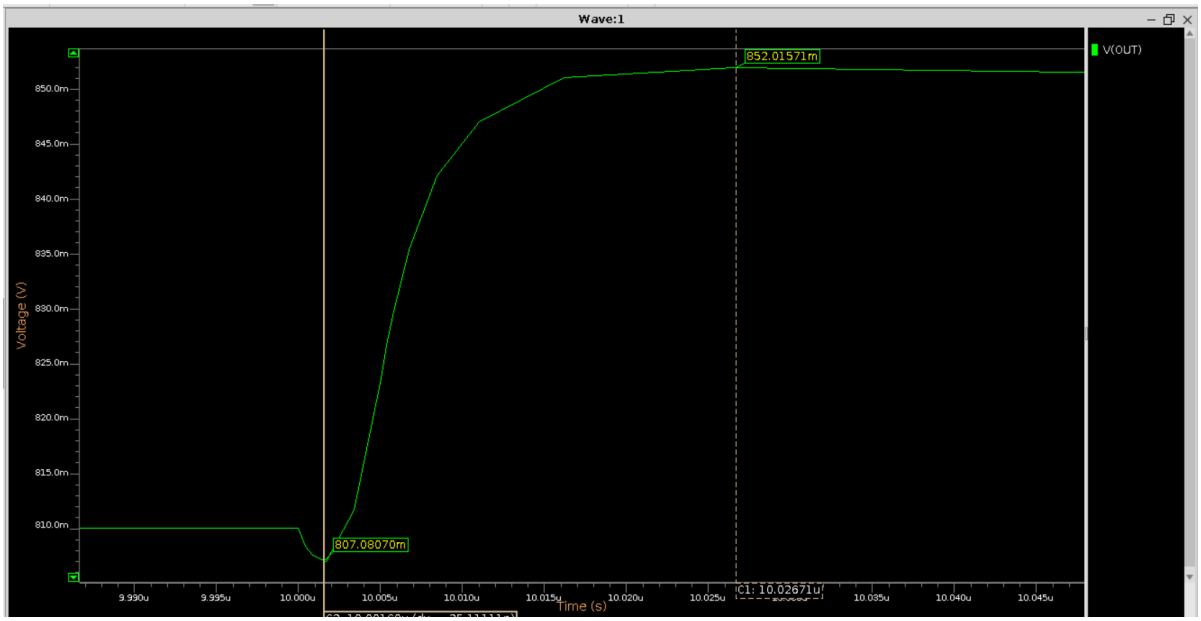

Figure 11: slew rate

7.0.6 ICMR and OCMR

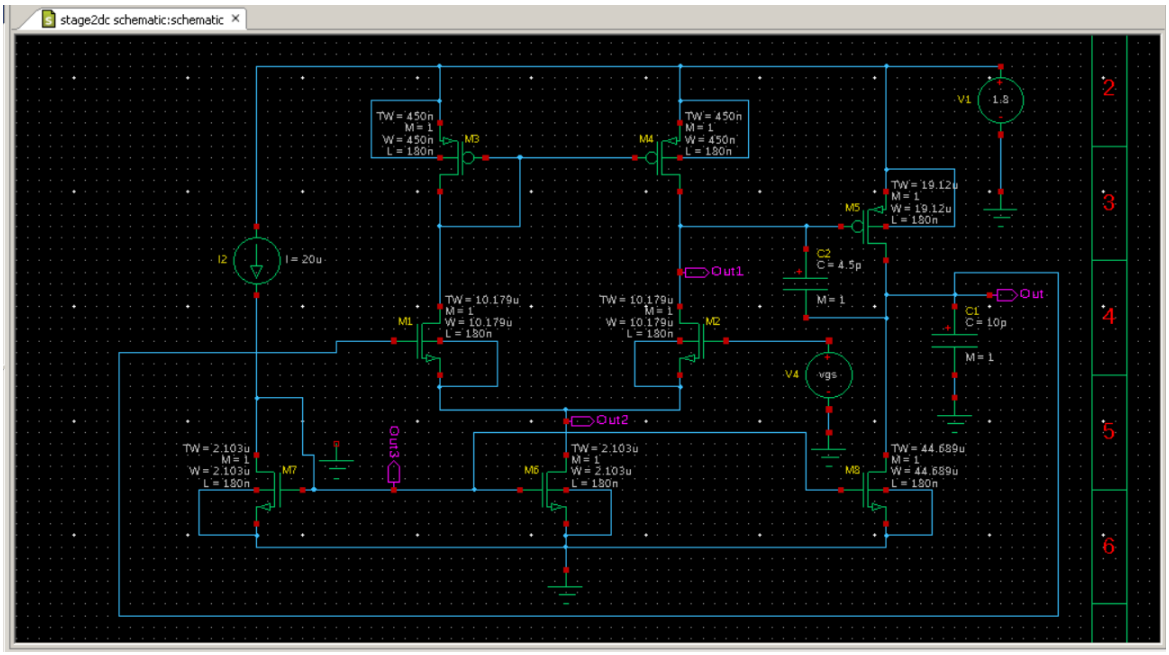

Figure 12: schematic for ICMR/OCMR

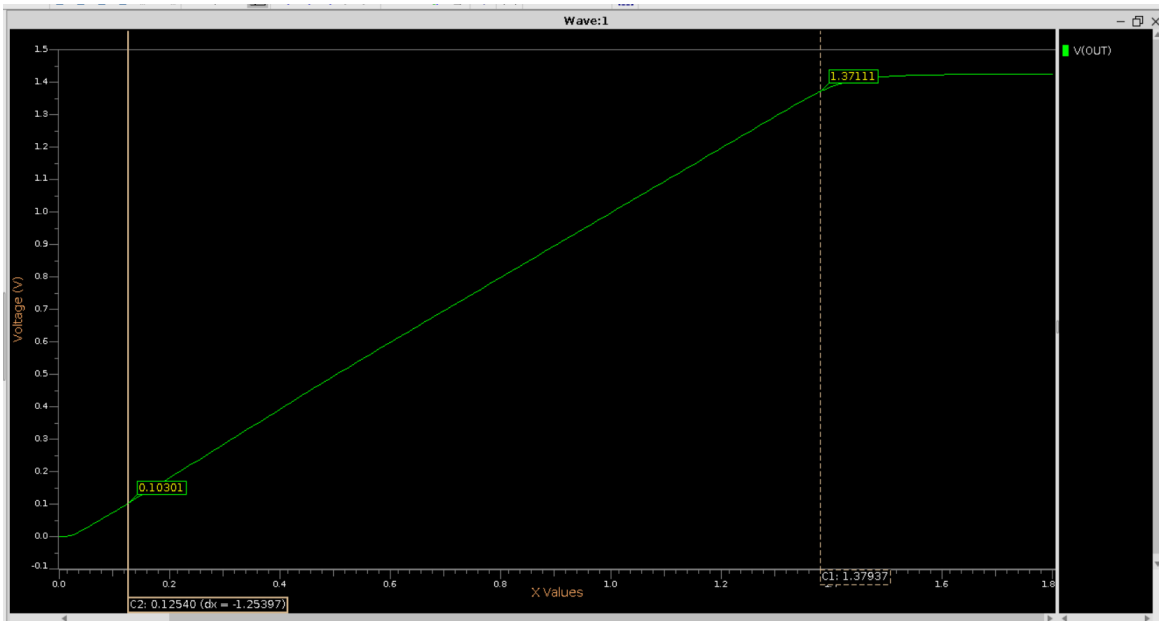

Figure 13: ICMR/OCMR

8 RESULTS

8.1 (W/l) of all transistors

Transistor	aspect ratio	width	length
M1	56.55	10.179 um	180 nm
M2	56.55	10.179um	180 nm
M3	2.5	450 nm	180 nm
M4	2.5	450 nm	180 nm
M5	11.689	2.103 um	180 nm
M6	106.22	19.12 um	180 nm
M7	248.27	44.68 um	180 nm
M8	11.689	2.103 um	180 nm

8.2 CAPACITOR VALUE

capacitor	value
C_c	4.5pf
C_L	10pf

8.3 AC Results

variable	value
Gain	53.29dB
3dB-Bandwidth	0.0284Mhz
GBW	12.65Mhz
PM	62.86
CMRR	56.55dB
PSRR	-1.877db

8.4 Transient analysis

	theoretical value	practical value
Slew rate	1	1.79
ICMR max	-	1.379
ICMR min	-	0.125
OCMR max	-	1.371
OCMR min	-	0.103

9 CONCLUSION

- A two-stage operational amplifier (op-amp) with low area can be designed using techniques like technology selection, trade-off analysis, compact transistor sizing, cascode configuration, common-mode feedback (CMFB), layout optimization, and the selective use of passive components. The needed performance can be attained while lowering silicon footprint by carefully taking these aspects into account.
- From this traditional 2-stage op amp design we can achieve high gain,high swing,medium power dissipation,and low noise.
- Power dissipated in this 2-stage op amp is 0.42mW.
- It has poor negative supply PSRR at higher frequency
- Phase margin assumption and practical value which is 60 degrees satisfied.