EE-518 Digital IC LAB

[Experiment 3]

Design 6T-SRAM and 1T-DRAM

Submitted by,

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Contents

1 AIM

1. Design a 6T-SRAM to perform a write operation and apply modifications on the same circuit to perform the read operation, using appropriate capacitances.
2. Design a 1T-DRAM to perform a write operation.
3. Compare the performance between SRAM and DRAM

2 OBJECTIVE

a) Design a 6T-SRAM by appropriate sizing of the transistors, "write" a data into 6T-SRAM using the write enable signal and check its functionality. Use additional circuitry in the 6T-SRAM so that we can "read" the data written in 6T-SRAM using read enable signal. Ensure that both read and write signal should not be active at the same time while checking the functionality of SRAM. Use 180nm technology node for the simulation.

b) Design a 1T-DRAM and check its functionality.

3 THEORY

3.1 SRAM Write Operation

A low power SRAM cell may be designed by using cross-coupled CMOS inverters. The most important advantage of this circuit topology is that the static power dissipation is very small; essentially, it is limited by small leakage current. Other advantages of this design are high noise immunity due to larger noise margins, and the ability to operate at lower power supply voltage. The major disadvantage of this topology is larger cell size. The circuit structure of the full CMOS static RAM cell is shown below. The memory cell consists of simple CMOS inverters connected back to back, and two access transistors. The access transistors are turned on whenever a word line is activated for read or write operation, connecting the cell to the complementary bit line columns.

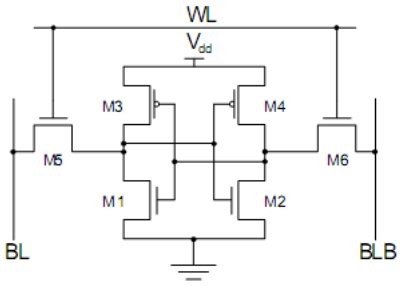

Figure 1: Circuit For SRAM Write Operation

Write Operation:- Consider the write '0' operation assuming that logic '1' is stored in the S-RAM cell initially.So node A is logic '1'.M4 is on and node B is logic'0'.Now we made Node B logic '1' by providing bit line bar logic '1'.Which on my M3 and M6 MOS and gives logic '0' at node A.

3.2 SRAM Read Operation

Consider a data read operation,Both capacitors are precharged.Assuming that logic '0' is stored in the cell. The transistors M2 and M5 are turned off, while the transistors M1 and M6 operate in linear mode. Thus internal node voltages are V1 = 0 and V2 = VDD before the cell access transistors are turned on. The active transistors at the beginning of data read operation are shown in Figure below. After the pass transistors M3 and M4 are turned on by the row selection circuitry,Capacitor Cc in left hand side of circuit will start discharging through M1 and M3.As capacitance adjacent to bit line discharges logic '0' read.

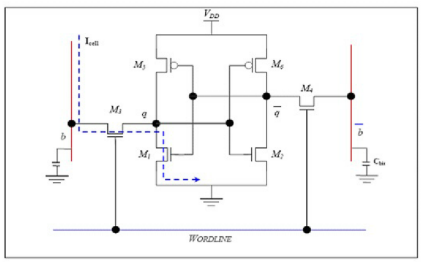

Figure 2: Circuit For SRAM Read Operation

3.3 Cell Ratio

Cell Ratio of 6T SRAM is Define by ratio of **size ratio of NMOS** to the **size ratio of excess transistors**. The cell ratio must be grater than 1.2 for large memory arrays, it is desirable to keep the cell size minimal while maintaining read stability. If transistor M1 is minimum sized, the access pass transistor M5 has to be made weaker by increasing it's length which is not desirable.Solution is to minimize the size of pass transistor and increase the width of NMOS pull down M5 to meet stability. Pull-Up Ratio define by the Size Ratio between pull up PMOS transistor and pull down NMOS transistor.

3.4 1T DRAM

Dynamic random-access memory (dynamic RAM or DRAM) is a type of random-access semiconductor memory that stores each bit of data in a memory cell, usually consisting of a tiny capacitor and a transistor, both typically based on metal-oxide-semiconductor (MOS) technology. While most DRAM memory cell designs use a capacitor and transistor, some only use two transistors. In the designs where a capacitor is used, the capacitor can either be charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1.

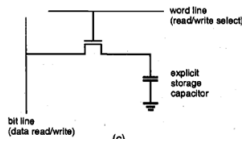

Figure 3: Circuit For DRAM Operation

4 Circuit Diagrams

4.1 6TSRAM Write Operation

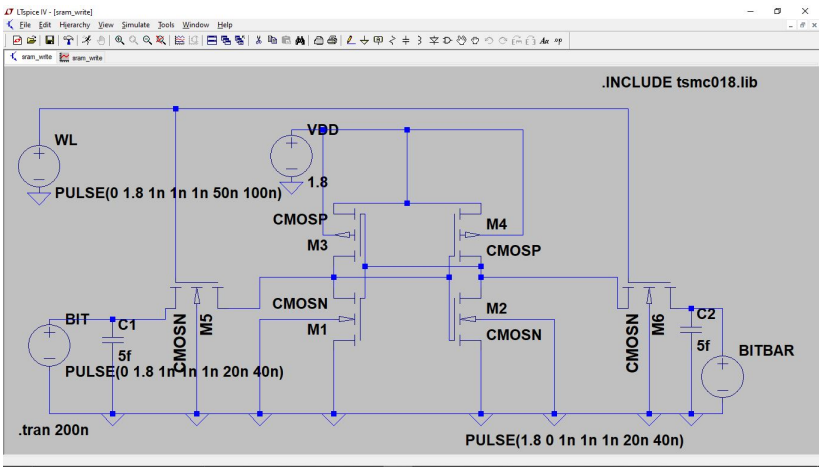

Figure 4: Circuit schematic for 6T SRAM Write Operation

4.2 6TSRAM Read Write Operation Simultaneously

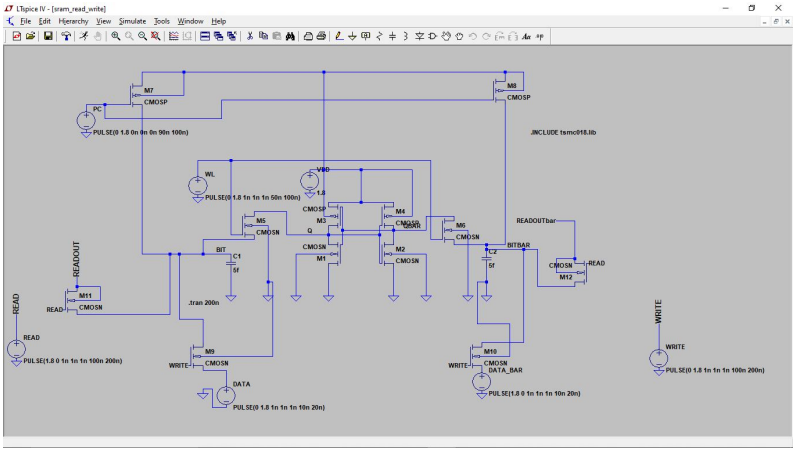

Figure 5: 6T SRAM Read Write schematic

4.3 1TDRAM Write Operation

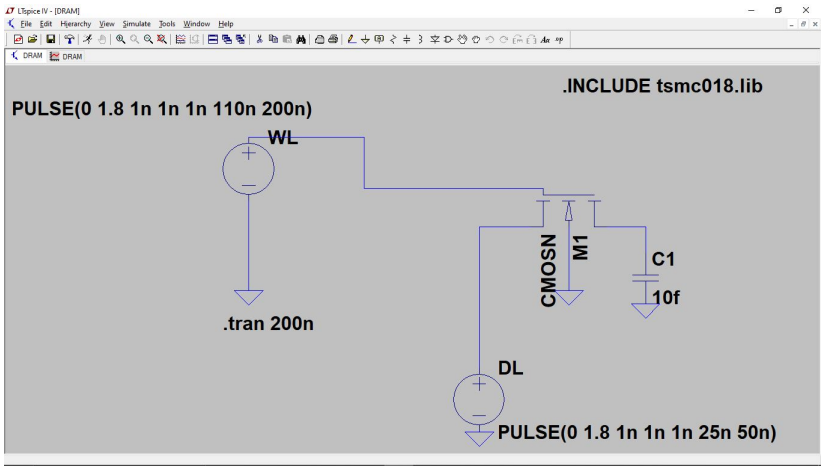

Figure 6: 1T RAM Write schematic

5 Procedure and Graphs

5.1 6TSRAM Write

1) We make the suitable circuit in the LTSpice.

2) We made Cell Ratio = 1.2 and Pull Ratio = 1.7 and done Transistor Accordingly.For the CMOS inverter circuit NMOS have L=180nm and W=468nm which are M1 and M2 and for PMOS L=180nm and W=612nm which are M3 and M4.We make W=180nm and L=360nm for Access Transistor which are M4 and M6.Load capacitance have the value of 5femtofarade.

3) We give the Pulse with value 0 and maximum value 1.8 volt as it is 180nm technology. For the Input Pulse has Delay of 0second, Rise time of 100picosecond, Fall time of 10picosecond, On time of 10nanosecond and Time period of 20nanosecond.For the Word Line Pulse has Delay of 0second, Rise time of 100picosecond, Fall time of 100picosecond, On time of 1nanosecond and Time period of 2nanosecond.

4) After Transient Simulation of 40nanosecond as shown in circuit [Fig3] we get response as given below

5) As We can see when Word Line is remain HIGH,input is get stored in transistor when Word Line is LOW transistor is doing no Operation.

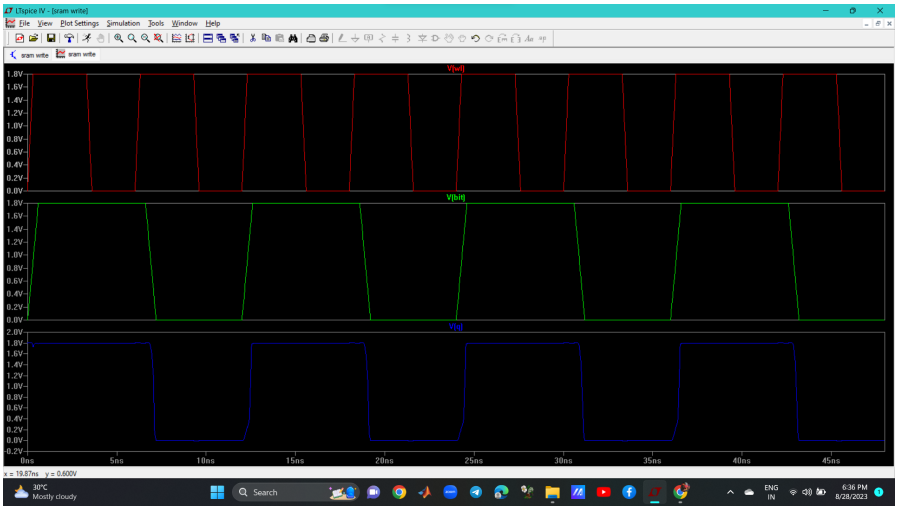

Figure 7: Transient Response of 6T SRAM write operation

5.1.1 Delay for 6TSRAM Write Operation

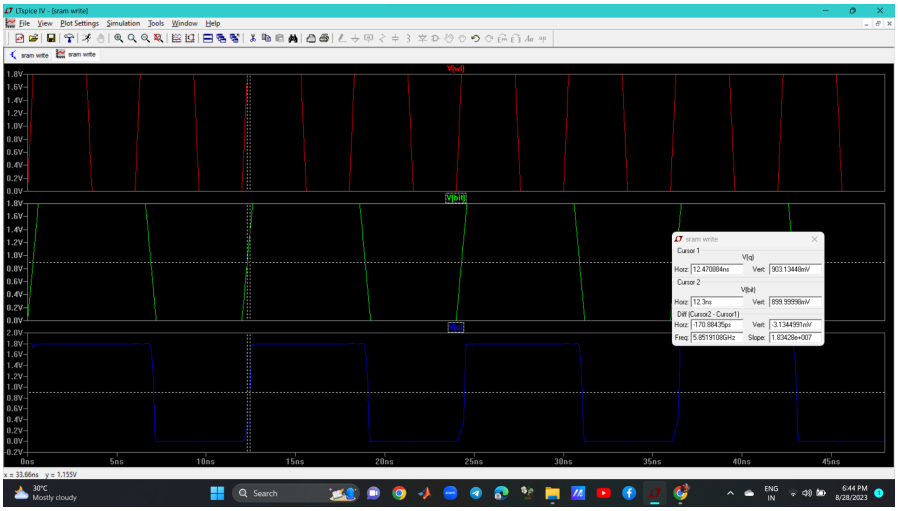

Figure 8: t_{PLH}

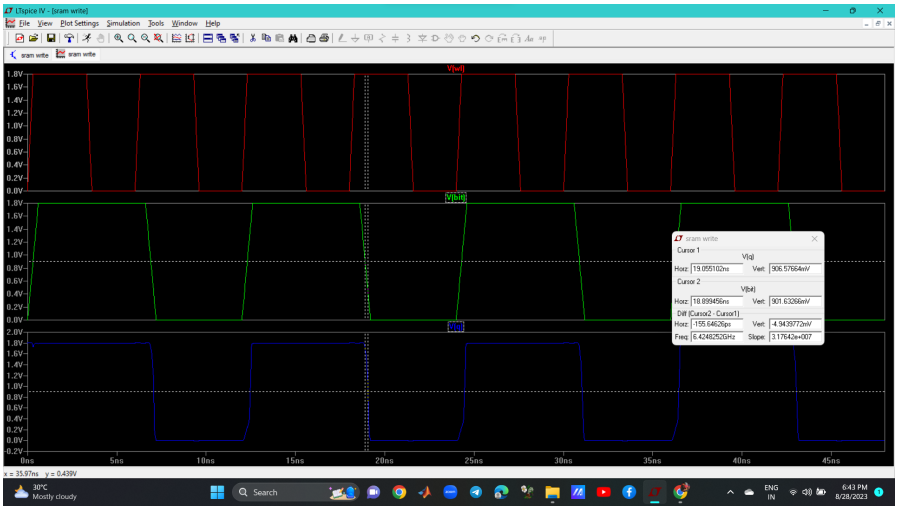

Figure 9: t_{PHL}

5.1.2 Functionality Verification

1) For the functionality verifcation We give the Pulse with value 0 and maximum value 1.8 volt as it is 180nm technology.

2) For the Word line Pulse has Delay of 0second, Rise time of 0 second, Fall time of 0 second, On time of 10nanosecond and Time period of 20nanosecond.For the Input Pulse has Delay of 0second, Rise time of 0 second, Fall time of 0 second, ON time of 1nanosecond and Time Period of 2nanosecond.

3) After Transient Simulation of 40nanosecond as shown in circuit we get response as given below

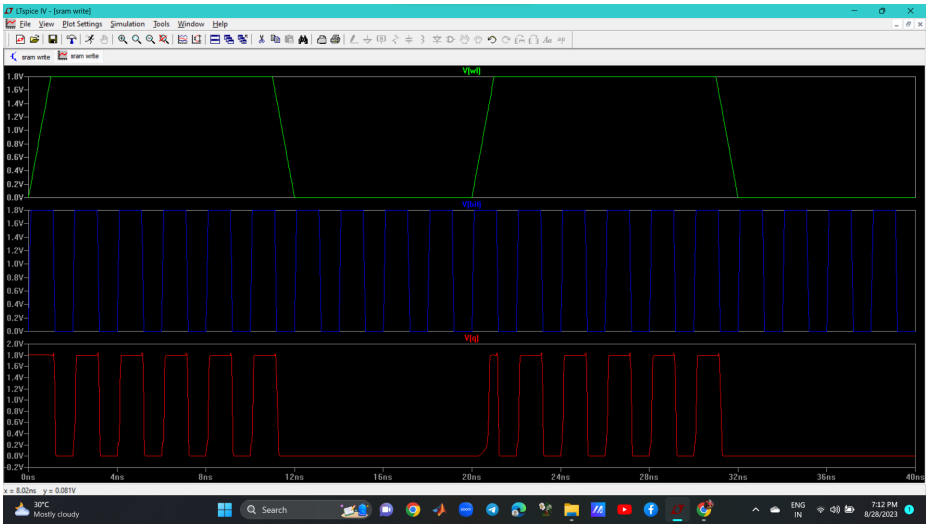

Figure 10: Verification

4) As We can see when Word Line is remain HIGH,input is get stored in transistor when Word Line is LOW transistor is doing no Operation.Which Verified our Write Operation for 6TSRAM.

5.2 SRAM Read Write Operation

1) We made Cell Ratio = 1.2 and Pull Ratio = 1.7 and done Transistor Accordingly.For the CMOS inverter circuit NMOS have L=180nm and W=432nm which are M1 and M2 and for PMOS L=180nm and W=612nm which are M3 and M4.We make W=180nm and L=360nm for Access Transistor which are M4 and M6.Load capacitance have the value of 5 femto farade.

2) We are Precharging the capacitor through PMOS which has L=180nm W=612nm which are M8 and M7.NMOS has the L=180nm and W=360nm which M9,M10,M11,M12.

3) We give the Pulse with value 0 and maximum value 1.8 volt as it is 180nm technology.For Read the data we need to Write some Data into transistor so we can read it later.

3) Precharge need to go LOW when Data signal is go from HIGH to LOW.So we give Precharge pulse and Data pulse Accordinlgy as Delay of 0.1nanosecond, Rise time of 0second, Fall time of 0second, On time of 1.9nanosecond and Time period of 2nanosecond and Delay of 0second, Rise time of 0second,Fall time of 0second, On time of 2nanosecond and Time period of 4nanosecond.

4) And We get Transient Response of 6TSRAM Read Operation as given in next page which include Precharge,Word Line, Data, Write Signal, Written Data (Q), Read Signal, Read Out Data.

Figure 11: Write and Read Operation simeultaneously

5.2.1 Functionality Verification

For the Verification we just Exchange the Pulse for Write and Read signal which are working as Enable signal as shown in [Fig6].And we get Transient response as below

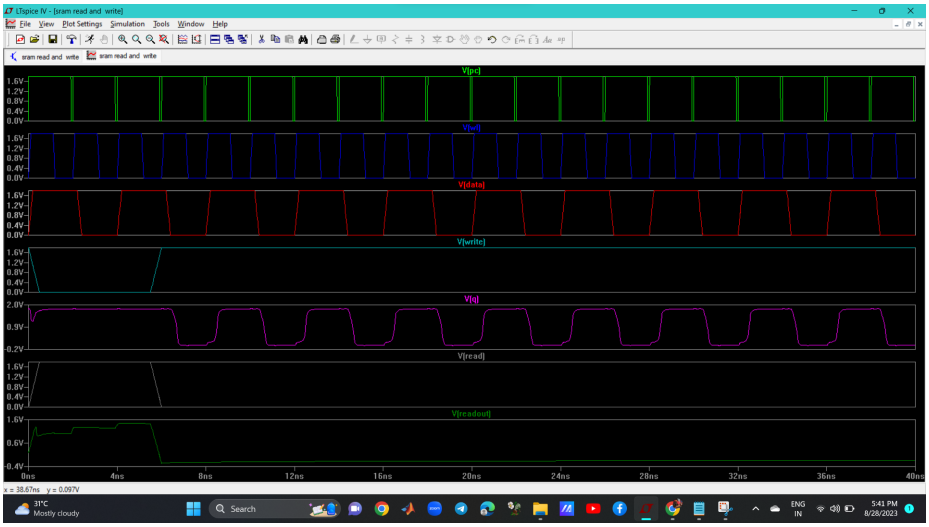

Figure 12: verification

5.3 1T DRAM Write

1) We make the suitable circuit in the LTSpice.

2) NMOS have L=180nm and W=180nm which is M1 and load capacitance have the value of 5femtofarade.

3) We give the Pulse with value 0 and maximum value 1.8 volt as it is 180nm technology. For the Word Line Pulse has Delay of 0second, Rise time of 0second, Fall time of 0second, On time of 2nanosecond and Time period of 4nanosecond.For the Input which is Bit Line Pulse has Delay of 0second, Rise time of 0second, Fall time of 0second, On time of 1nanosecond and Time period of 2nanosecond.

4) After Transient Simulation of 40nanosecond as shown in circuit [Fig7] we get response as given below

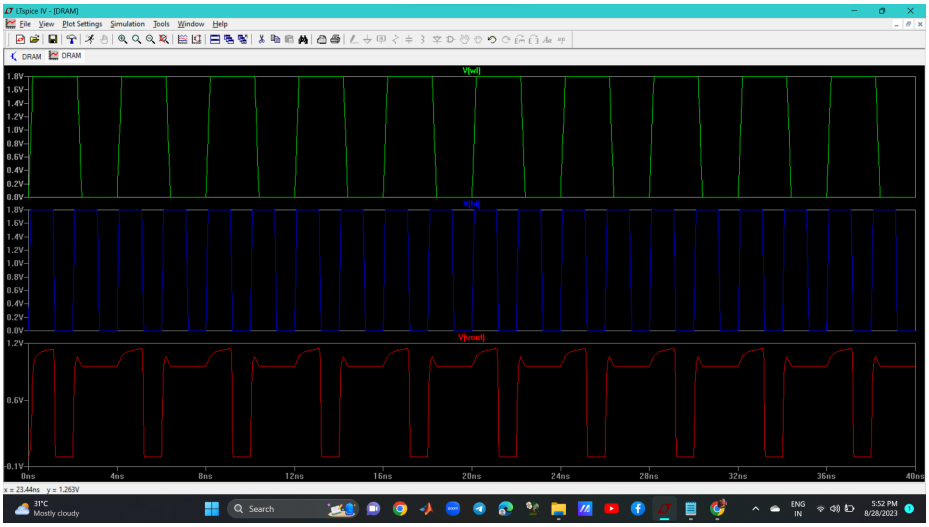

Figure 13: Transient Response of 1TDRAM Write Operation

5) As We can see when Word Line is remain HIGH,input is get stored in transistor when Word Line is LOW transistor is doing no Operation.

5.3.1 Delay for 1TDRAM Write Operation

Figure 14: t_{PLH}

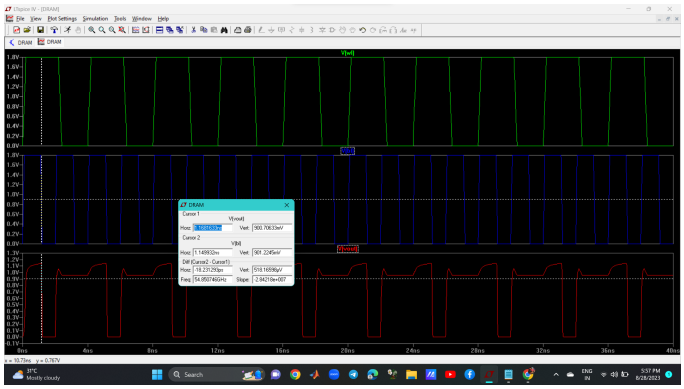

Figure 15: t_{PHL}

5.3.2 Functionality Verification

1) For the functionality verifcation We give the Pulse with value 0 and maximum value 1.8 volt as it is 180nm technology.

2) We give the Pulse with value 0 and maximum value 1.8 volt as it is 180nm technology. For the Input which is Bit Line Pulse has Delay of 0second, Rise time of 0second, Fall time of 0second, On time of 2nanosecond and Time period of 4nanosecond.For the Word Line Pulse has Delay of 0second, Rise time of 0second, Fall time of 0second, On time of 1nanosecond and Time period of 2nanosecond.

3) After Transient Simulation of 40nanosecond as shown in circuit we get response as given below

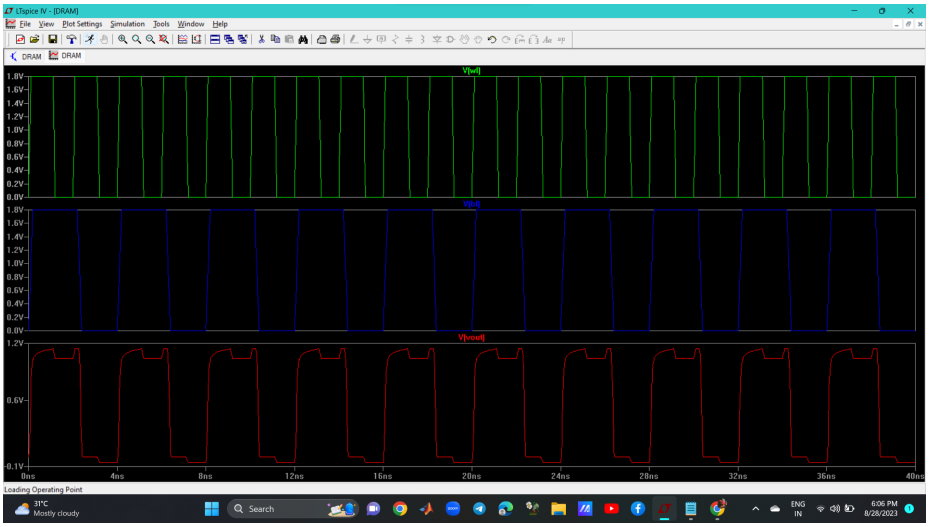

Figure 16: Verification

4) As We can see when Word Line is remain HIGH,input is get stored in transistor when Word Line is LOW transistor is doing no Operation.Which Verified our Write Operation for 1TDRAM.

6 Result

6.1 Transistor sizing:

Parameter	Value
Pull-up ratio	1.7
Cell ratio	1.2

6.2 Ratio value for SRAM transistors

	Access transistor	NMOS transistor	PMOS transistor	Precharge transistor (for read operation)
W/L	2	2.4	3.4	3.4

6.3 Performance Comparison

	Vpeak(V)	Power(uw)	t_{PLH}(ps)	t_{PHL}(ps)	t_p(ps)
SRAM	1.8	13.30	170.88	155.64	163.262
DRAM	1.22	0.793	33.29	18.23	25.76

7 OBSERVATIONS AND CONCLUSIONS

a) CMOS SRAM Cell is design with appropriate transistor sizing and its functionality is verified using transient analysis.
b) The cell ratio obtained is 1.2 and pull up ratio 1.7.
c) DRAM is slower than SRAM.
d)DRAM peak voltage is less.SRAM is more robust.