Pushpkant Yadav

System Architect - Embedded Systems & Digital Twin Platforms

pushpkantyadav@gmail.com | +91-9950238365 | LinkedIn | GitHub

Architecting digital twins of complex avionics LRUs for early hardware–software co-design and system bring-up.

Professional Summary

System Architect with 13+ years of experience designing and validating complex embedded systems, with a strong focus on digital twins and virtual platforms for avionics LRUs. Experienced in architecting QEMU-based MPSoC system models to support early software development, driver validation, and system bring-up ahead of hardware availability. Strong background in Embedded Linux, Zynq UltraScale+ MPSoC architecture, hardware–software co-design, and system-level debugging. Drives architectural proof-of-concepts, resolves high-impact technical risks, and mentors engineers across disciplines.

Core Skills

System Architecture, Digital Twin & Leadership

Embedded systems architecture, digital twin & virtual platforms, avionics LRU systems, hardware–software co-design, architectural definition & design reviews, proof-of-concepts, technical risk assessment, cross-functional technical mentoring.

Simulation & Modeling

QEMU (board & peripheral modeling), virtual prototyping, system-level modeling (UML), pre-silicon / pre-hardware validation, SystemC (TLM 2.0 – working knowledge), transaction-level modeling (conceptual).

Platforms, Processors & Software

Zynq UltraScale+ MPSoC (Cortex-A53 / R5 / PL), ARM Cortex-A/R/M, RISC-V (bare-metal & RTOS), Embedded Linux, Yocto (PetaLinux, Processor SDK Linux), BSP & boot flow bring-up, Linux device drivers, memory map, interrupts & DMA, system debugging & root-cause analysis.

FPGA, Interfaces & Timing

Vivado Design Suite, AXI bus architecture, custom PL IP integration, Verilog (design review & debug level), SPI, I2C, UART, PCIe, USB, Ethernet, IEEE-1588 PTP, NTP, GPS.

Work Experience

Honeywell Technology Solution

System Architect - Embedded Systems & Digital Twin Platforms
Sep 2024 - Present

- Architecting QEMU-based digital twins of aerospace avionics LRUs built on Zynq UltraScale+ MPSoC platforms to enable early hardware–software co-design and system-level validation.
- Defined system architecture and abstraction strategies for modeling MPSoC processing systems, programmable logic interfaces, and multiple COTS peripherals within the virtual platform.
- Enabled Embedded Linux boot, driver validation, and application bring-up on virtual platforms ahead of physical hardware availability, significantly reducing dependency on additional hardware for development and validation.
- Led architectural proof-of-concepts and resolved complex system-level issues spanning simulation models, boot flows, and low-level software interactions.
- Developed an architectural proof-of-concept simulating MPSoC RPU execution in QEMU with

selected PL peripherals modeled in SystemC, including functional synchronization between QEMU and SystemC for system-level digital twin validation.
- Architected a Linux-based, multi-tenant simulation platform enabling thousands of users to execute virtual system simulations remotely, providing a scalable alternative to physical hardware test benches.
- Extended the simulation platform to support remote debugging workflows, enabling users to attach local debuggers to virtual targets and use the simulator as a functional replacement for physical test benches in VectorCast-driven execution environments.
- Designed and validated scalable simulation capacity, supporting approximately 500–600 concurrent virtual instances for lightweight systems and 100–150 instances for hardware-intensive configurations per server.
- Collaborated with and mentored FPGA, hardware, and software teams on MPSoC architecture, virtual platform workflows, and system-level debugging.

Logic Fruit Technologies

Project Lead – Embedded Systems
Sep 2021 – Sep 2024

- Led system architecture and Embedded Linux platform development for complex telecom and defense-grade embedded systems.
- Designed and integrated MPSoC- and FPGA-based platforms, including device drivers, BSP bring-up, and high-speed interface integration.
- Architected and implemented IEEE 1588 Precision Time Protocol (PTP) solutions for timing-critical systems, including PHC clock integration and driver support.
- Mentored engineers across software, FPGA, and hardware domains, driving architectural reviews and technical decision-making.

Noble Labs

Embedded Systems Consultant / Projects Leader (Owned Firm)
Feb 2018 – Sep 2021

- Architected and delivered end-to-end embedded systems spanning hardware, firmware, and Embedded Linux platforms.
- Led system bring-up, validation, and customer-facing technical engagements across multiple embedded product domains.

NeuroEquilibrium Diagnostic Systems Pvt. Ltd.

R&D Manager / Senior Embedded Engineer
Jun 2015 – Feb 2018

- Designed and validated real-time embedded systems for medical diagnostic devices, integrating sensors, control systems, and signal processing pipelines.
- Led architecture definition and system-level debugging for safety- and reliability-critical embedded products.

CadBridge Semiconductor Pvt. Ltd.

Junior Embedded Systems Engineer
Feb 2013 – May 2015

- Developed low-level firmware and hardware interface code for embedded platforms, building a strong foundation in system bring-up and debugging.

Education

M.Tech – Embedded Systems, BITS Pilani (WILP), 2025
B.Tech – Electronics & Communication Engineering, RTU, 2011