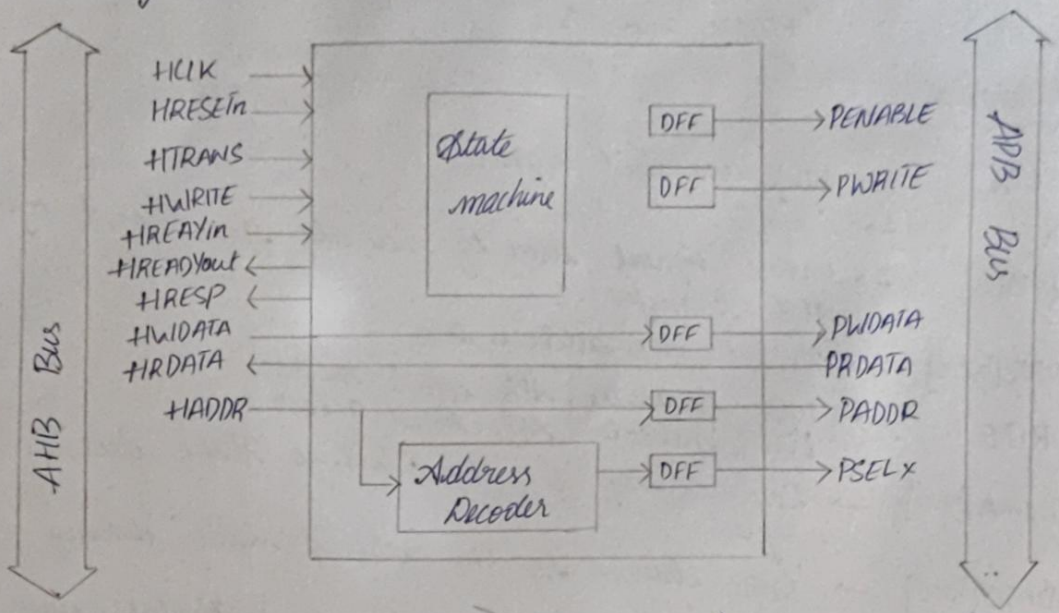
AHB to APB BRIDGE

PVM VAMSI
RN110

Block Diagram



The AHB to APB bridge is an AHB slave, providing an interface between the high speed AHB and low power APB. Read and write transfers on the AHB are converted into equivalent transfers on APB.

AHB signals

		Source
HCLK	→ This clock times all bus transfers	→ Clock source
HRESETn	→ A active low reset signal	→ Reset controller
HADDR[31:0]	→ 32-bit system address bus	→ Master
HTRANS[1:0]	→ Indicate current transfer 0 → IDLE 1 → BUSY 2 → NON SEQUENTIAL 3 → SEQUENTIAL	→ Master
HWRITE	→ HIGH for write transfer LOW for read transfer	→ Master
HSIZE[3:0]	→ Indicates the size of transfer	→ Master
HBURST[2:0]	→ Indicates type of burst and no of beats	→ Master
HWDATA[31:0]	→ The write data	→ Master

HRDATA [31:0] → Read bus data → slave
HREADYout → HIGH indicates a transfer has finished → slave
HRESP [1:0] → Information on status of transfer OKAY, ERROR, RETRY and SPLIT → slave

APB signals

PRESETn → Active low reset signal
PCLK → Clock
PENABLE → Enable signal used to indicate the second cycle of APB transfer
PADDR [31:0] → 32 bit APB address bus
PWRITE → HIGH indicates APB write access
LOW indicates APB read access
PRDATA [31:0] → Data driven by the selected slave during read cycles.
PWDATA [31:0] → Data driven to the selected slave during write cycles.
PSELx → Signal to indicate that a particular slave is activated.

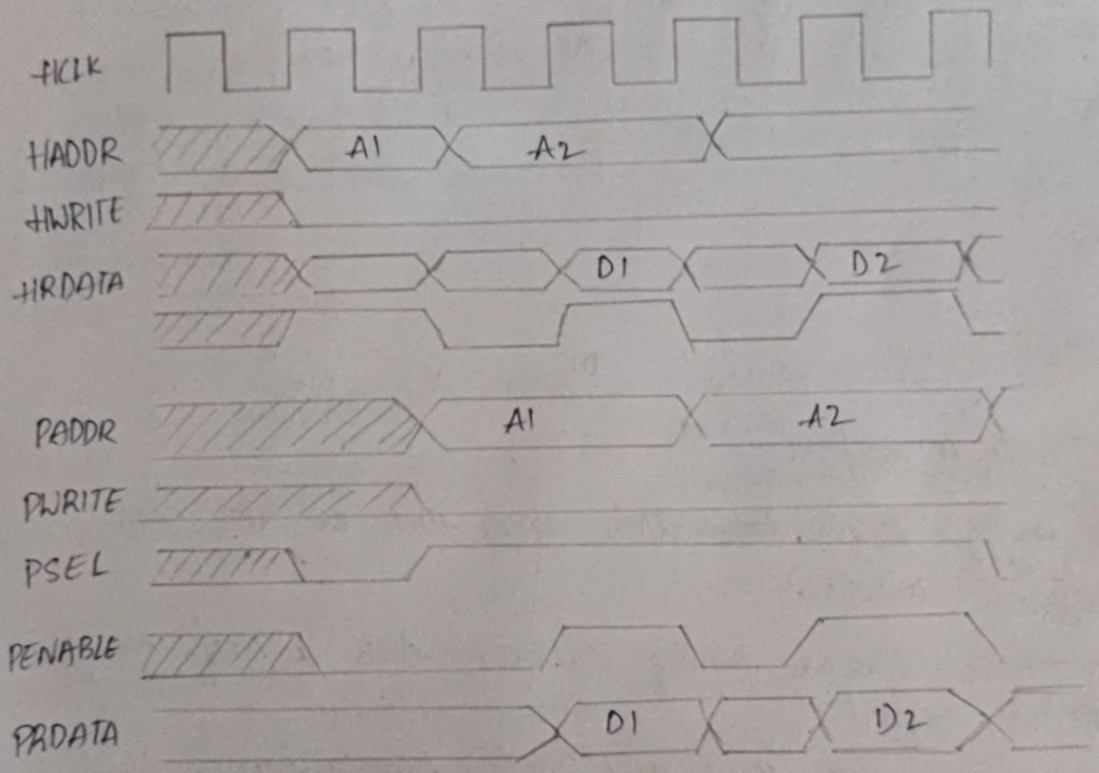
AHB bus protocol is designed to be used with a central multiplexor interconnection scheme. AHB transfer consists of an address and control cycle and one or more cycles of data. The address cannot be extended and therefore all slaves must sample the address during this time. The data, however can be extended using HREADY. HSIZE determines the size of each transfer that can be 1, 2, ..., 128 bytes. The type of transfer and number of transfer is determined by HBURST signal.

HBURST	
000	→ single transfer
001	→ Increment undefined length
010	→ WRAP 4
011	→ INCR4
100	→ WRAP 8
101	→ INCR 8
110	→ WRAP 16
111	→ INCR 16

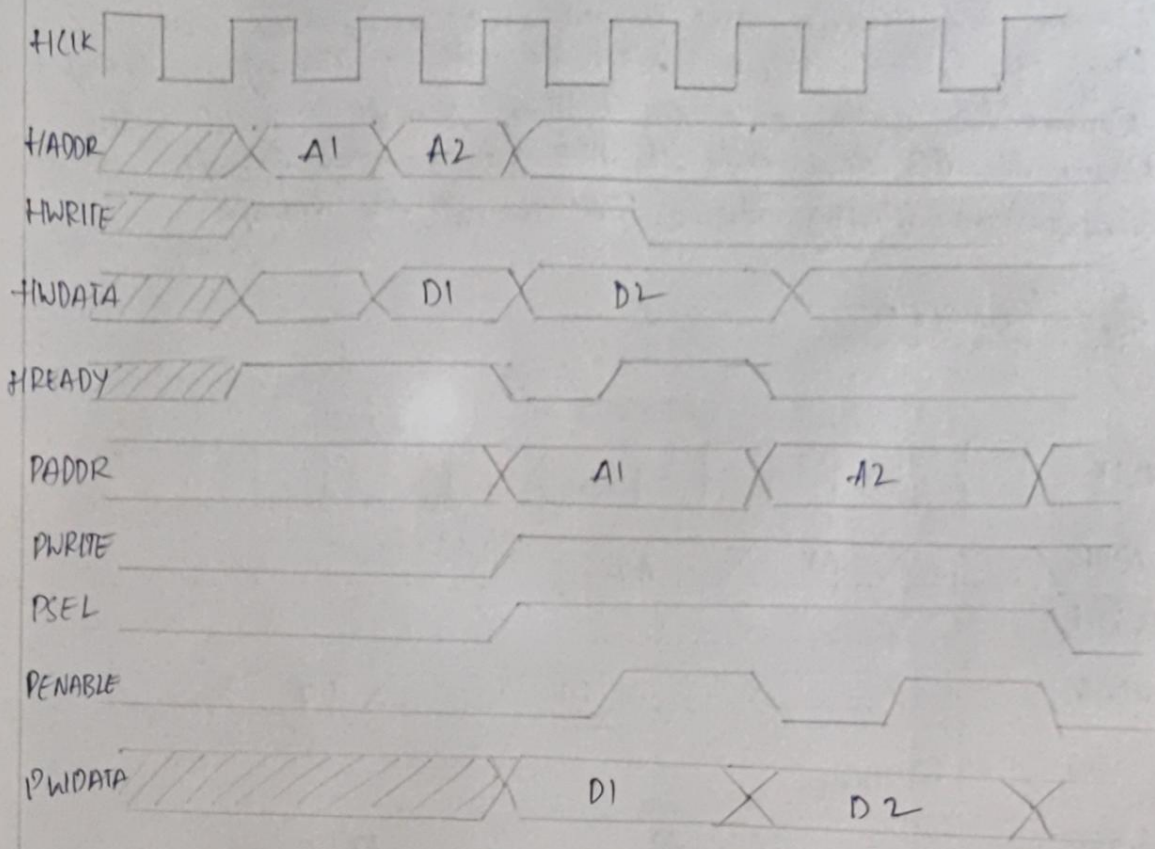
The bridge unit converts system bus transfer into APB transfers and performs the following functions.

- Latches the address and holds it valid throughout the transfer.
- Decodes the address and generates a peripheral select, PSELx. Only one select signal can be active during a transfer.
- Drives the data onto the system bus for a read transfer.
- Drives the APB data onto the APB for a write transfer.
- Generates a timing strobe, PENABLE for the transfer.

READ TRANSFER



WRITE TRANSFER



Features to be verified

1. To verify proper transaction from AHB to APB for different bursts.
2. To ensure proper timing between AHB & APB using HREADY signal.
3. To verify both Read and write transcations.
4. To verify that protocol is followed such as pipelining on AHB side and assertion of PSELx and PENABLE signal for read and write operation on APB side.

Transaction

- HADDR inside [32'h8000_0000 : 32'h8000_03FF]
  [32'h8400_0000 : 32'h8400_03FF]
  [32'h8800_0000 : 32'h8800_03FF]
  [32'h8C00_0000 : 32'h8C00_03FF]
- HSIZE inside {0, 1, 2} as APB can't handle more byte length.
- The maximum bound limit is 1024 bytes.

Coverage

- HSIZE → bins {[0:2]}
- HTRANS → bins {[2:3]}
- HWRITE → bin {0,1}
- HADDR
- Cross HSIZE, HWRITE, HADDR, HTRANS;
- PSELx → bin {1,2,4,8}
- Cross PWRITE, PSEL;

Comparison

When HWRITE = 1.

HSIZE = 0

HADDR[1:0] - 2'b00 → compare HWDATA[7:0] with PWDATA

HADDR[1:0] - 2'b01 → HWDATA[15:8] with PWDATA

- 2'b10 → HWDATA[23:16] with PWDATA

- 2'b11 → HWDATA[31:24] with PWDATA

HSIZE = 1

2'b00 → Compare HWDATA[15:0] with PWDATA.

2'b10 → Compare HWDATA[31:16] with PWDATA.

HSIZE = 2 compare HWDATA with PWDATA.

When HWRITE = 0

Same as above but instead of slicing HWDATA the slicing happens in PWDATA

TB Architecture