Indian Institute Of Technology, Bhubaneswar

Industrial Training Defence (EE4T001) Presentation

Design and Development of a Planar Flyback Transformer for Isolated Power Supply Applications

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Abstract

- **Limitations of conventional wire-wound transformers**
- Bulky and heavy
- Poor high-frequency performance
- Higher copper and core losses
- Limited power density
- **Benefits of planar transformers:**
- Compact and low-profile
- High-frequency operation
- Better thermal management
- Higher power density & efficiency

- **Objective: 2.5W flyback converter with planar transformer**
- **Tools used: Ansys PEmag, KiCad, Q3D, Maxwell 3D,Icepak, Simplorer, FreeCAD.**

TABLE I: Design Specifications of The Flyback Converter

Parameters	**Symbols**	**Values**
Input Voltage	V_i	8 - 12 V
Output Voltage	V_o	24 V
Output Power	P_o	2 - 2.5 W
Switching Frequency	f_s	250 - 350 KHz

$$V_o = \frac{N_s}{N_p}\frac{D}{(1-D)}V_i \tag{1}$$

$$D = \frac{V_{or}}{V_i + V_{or}} \tag{2}$$

The flyback converter was designed by using Equations 1 &2. The reflected voltage, Vor was adjusted to 8V so that the duty cycle, D is 0.5. The primary to secondary turns ratio, Np/ Ns is found to be 0.32 from below equation.

$$V_{or} = V_o\frac{N_p}{N_s}$$

Design Equations & Core Geometry & Material Selection

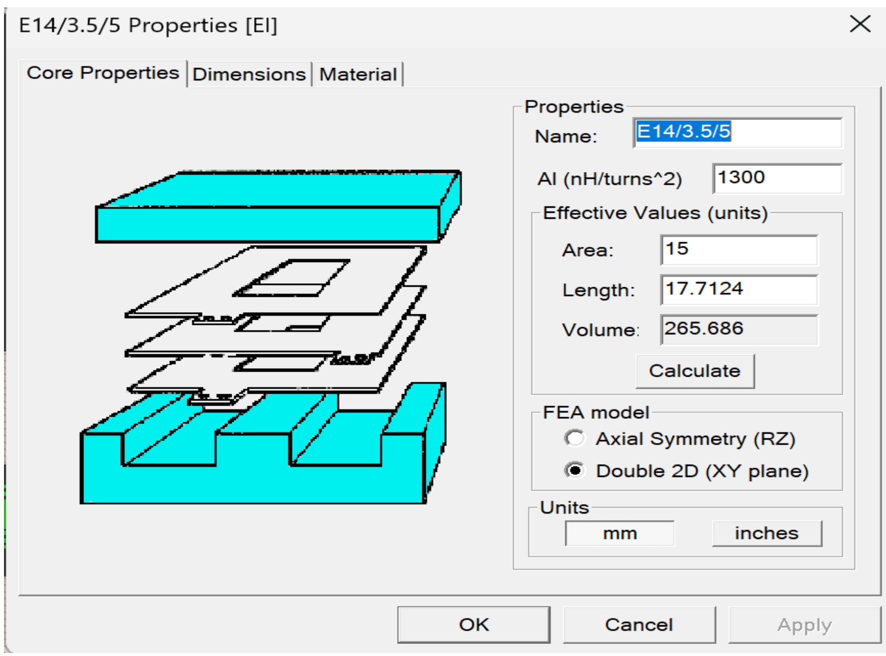
- BCM critical factor: $K_{crit} = (1 - D)^2 = (2L_s)/(R*T_s)$
- Required secondary inductance : $L_s = R_o \cdot K_{crit} / (2 \cdot f_s)$
- $L_s = 74.40\ \mu H$.
- Primary inductance from turns: $L_p = (N_p / N_s)^2 \cdot L_s$
- $\rightarrow L_p = 7.619\ \mu H$.

- **Why This Core Was Chosen**
- **Material: Ferrite 3F3**
  - Low core loss at high frequency (200–500 kHz).
  - Suitable for SMPS applications.
- **Core Shape: Planar E14/3.5/5**
  - Optimized for planar windings (flat copper traces).
  - Compact size, low profile — good for PCB integration.
- **Magnetic Properties**
  - High permeability for efficient flux linkage.
  - Bmax ~0.3 T ensures safe operation without saturation.
- **Thermal Advantage**
  - Large surface area → better heat dissipation compared to wound cores.

- Use A_L (inductance factor): A_L = L / N^2 to find N
- Decide turns: N_p = 3, N_s = 9 (from A_L and required ratio).
- The maximum possible width of the PCB track

Is calculated from below equation.

$$T_w = \frac{W - (N-1)S}{N}$$



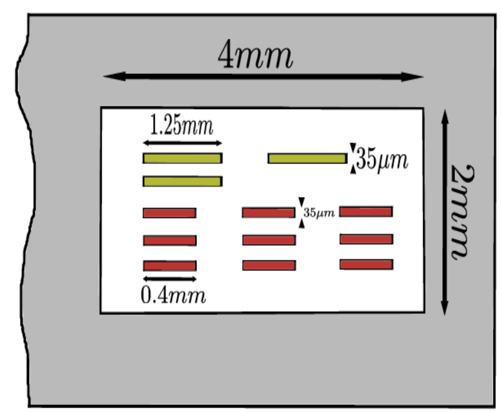
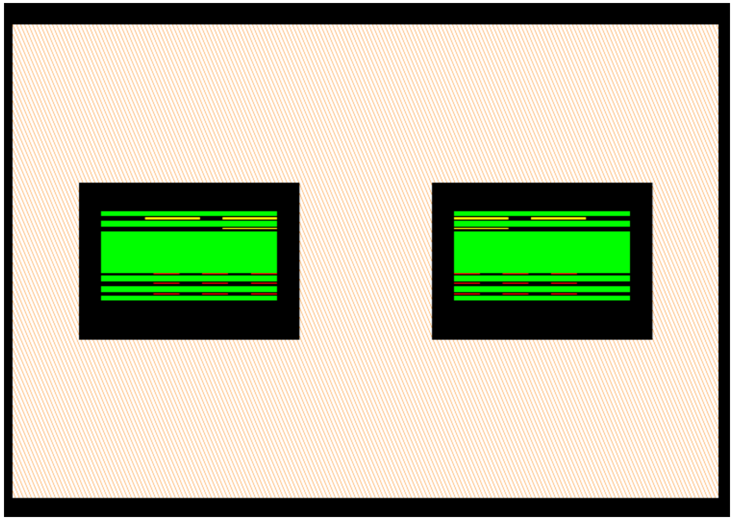


Fig. 1: Window Utilization of The Planar Transformer.

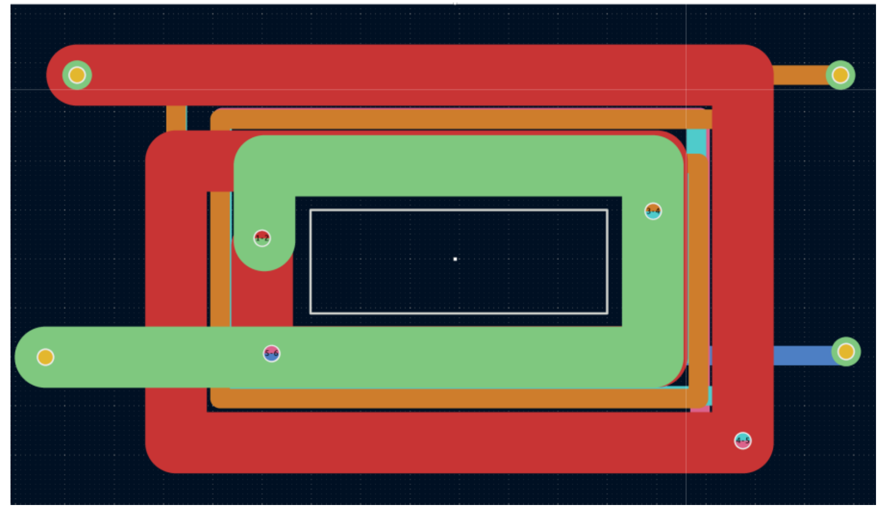
Planar Transformer Modelling

TABLE III: PCB Stacking of Primary & Secondary Windings.-

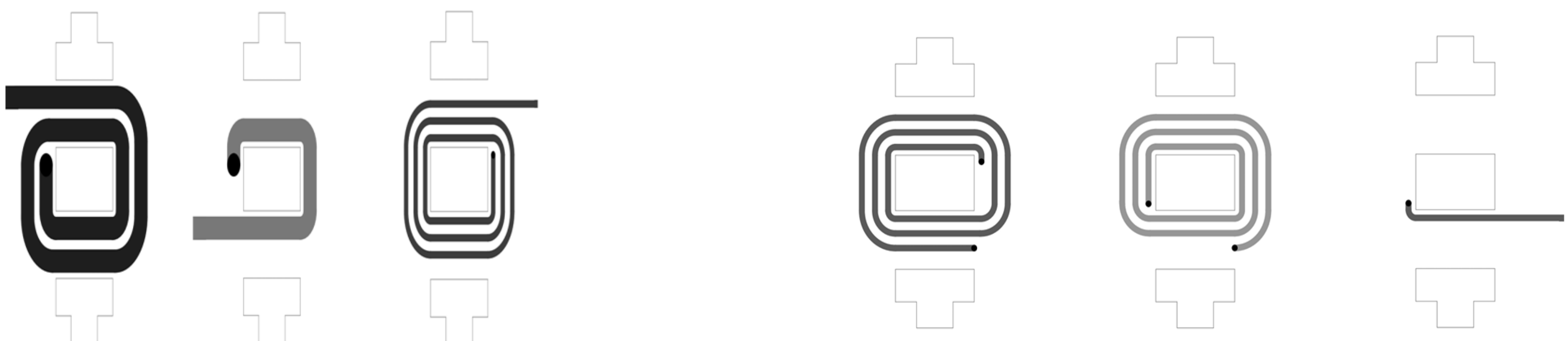
Primary winding	
Number of turns	3
Max turns per layer	2
Number of layers	2
Copper track thickness	35 μm
Copper track width	1.25 mm
Spacing between tracks	0.5 mm
Insulation between layers	60 μm
Insulation between primary & secondary	0.4 mm
Secondary winding	
Number of turns	9
Max turns per layer	3
Number of layers	3
Copper track thickness	35 μm
Copper track width	0.4 mm
Spacing between tracks	0.5 mm
Insulation between layers	60 μm



Planar Transformer 2D Model - Ansys PEmag.



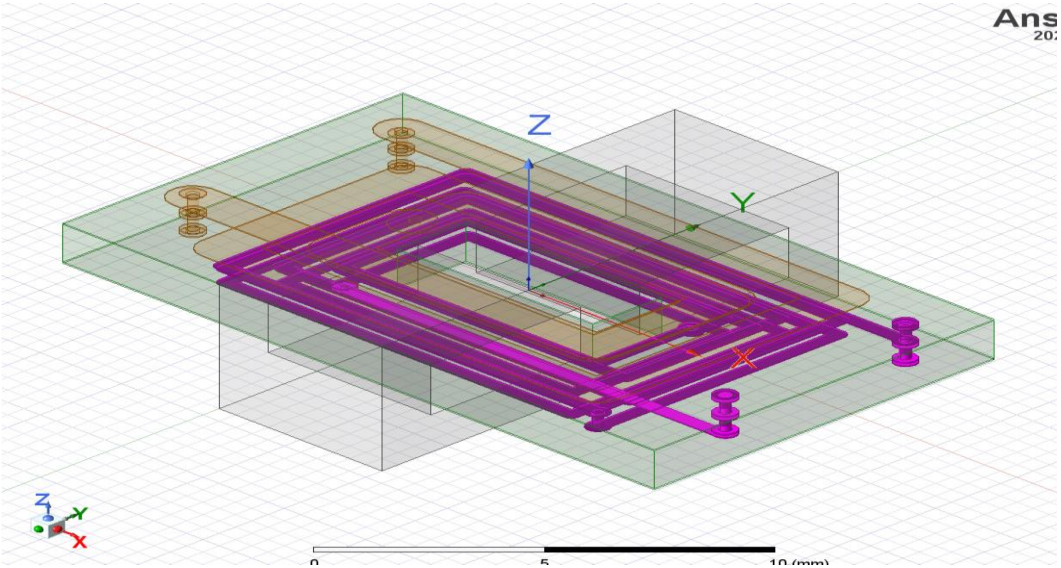
Kicad design of planar transformer PCB.

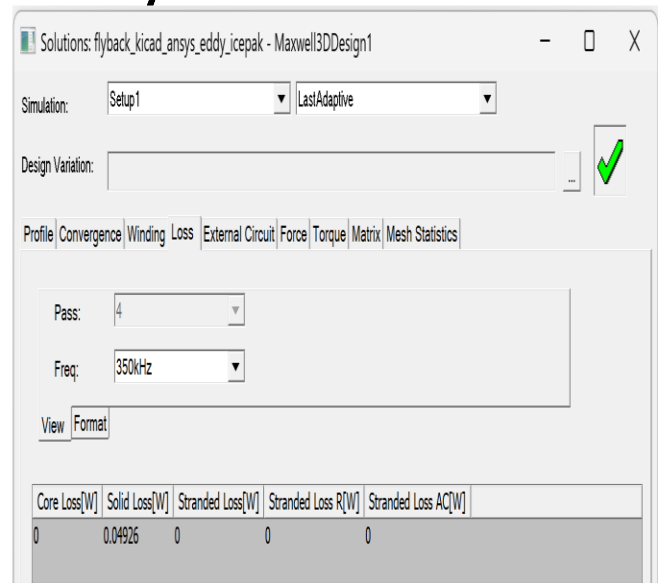


(a) Top Layer - Primary (b) Layer 2 - Primary (c) Layer 3 - Secondary (d) Layer 4 - Secondary (e) Layer 5 - Secondary (f) Bottom Layer - Secondary

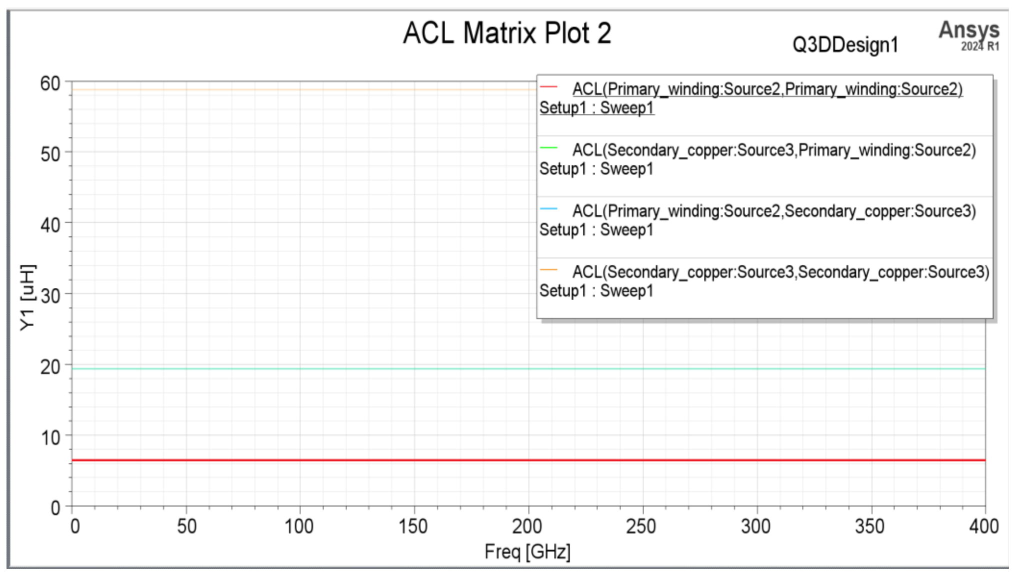
Layers of planar transformer PCB.

3D FEA Simulation Q3D and Eddy Current





Planar Transformer 3DModel-Ansy Q3D Extractor.



ACL Matrix Plot

Lp, Ls, Leakage, Mutual, Inductance & Coupling Coffecient.

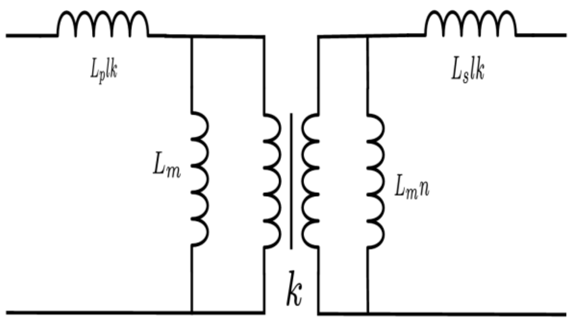


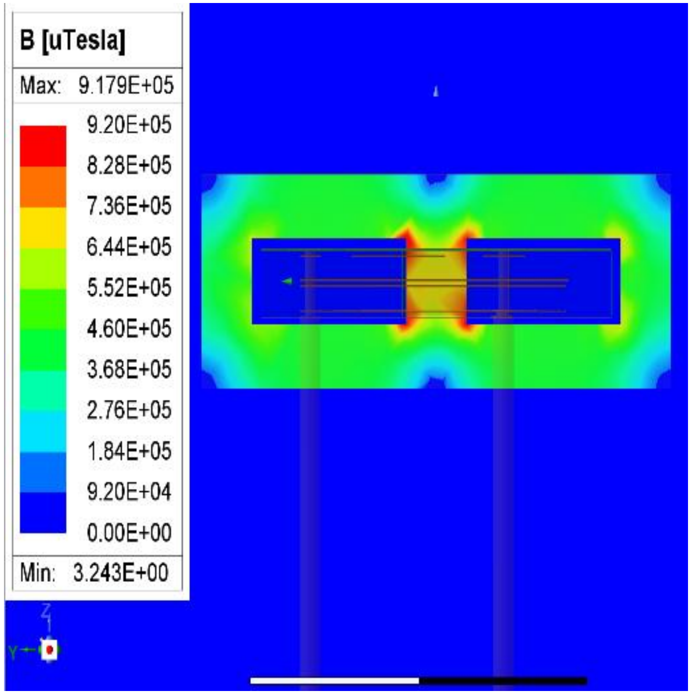
Fig. 6: Equivalent Model of a Transformer.

- Primary leakage: L_plk = L_p · (1 - k)
- Secondary leakage: L_slk = L_s · (1 - k)
- Coupling coefficient: k = M / sqrt(L_p.L_s)

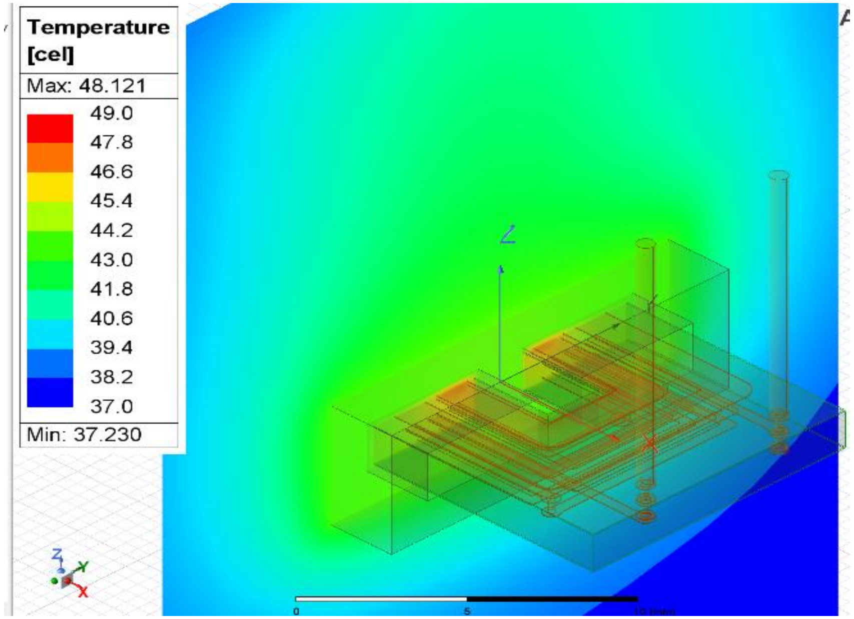
L_{plk}	L_{slk}	M	K	L_p	L_s
35 nH	0.3 nH	19.44 μH	0.9946	6.5 μH	58.77 μH

Simulated Parameters of the planar flyback transformer

3D FEA Simulation Maxwell and Icepak



3D FEA Analysis of the planar transformer



Thermal Distribution of the Designed Planar Transformer .

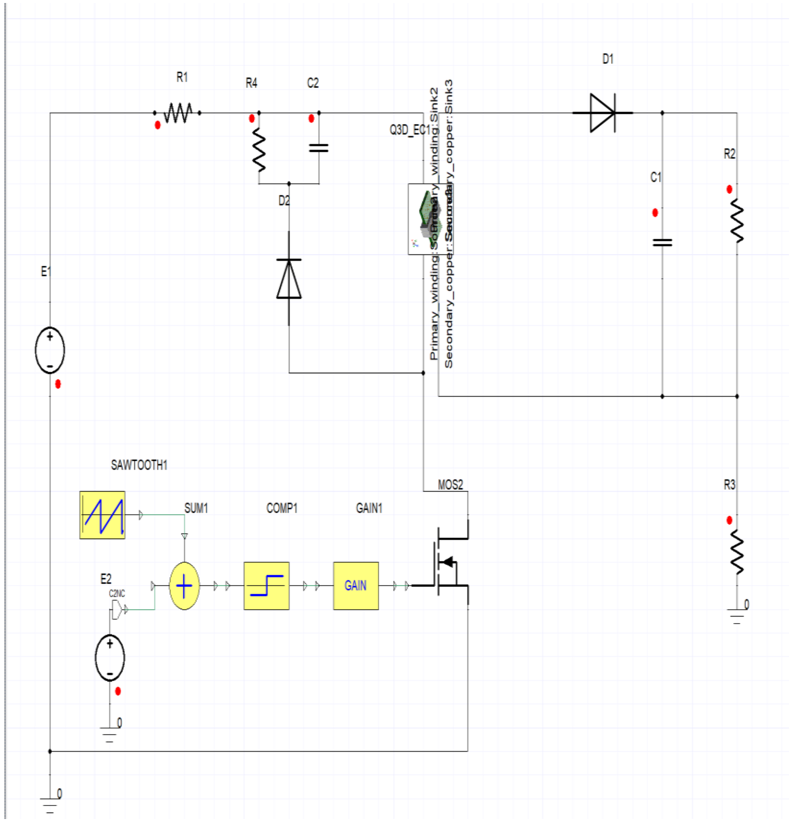
RCD Snubber Circuit & Simplorer Simulation

For the designed flyback converter circuit, 20V is considered to be the maximum Vds. So, Vsn=Vds−Vi=12V.

$$R_{sn} = \frac{V_{sn}(V_{sn} - V_{or})}{\frac{1}{2} I_{p_{peak}}^{2} L_{lk} f_s}$$

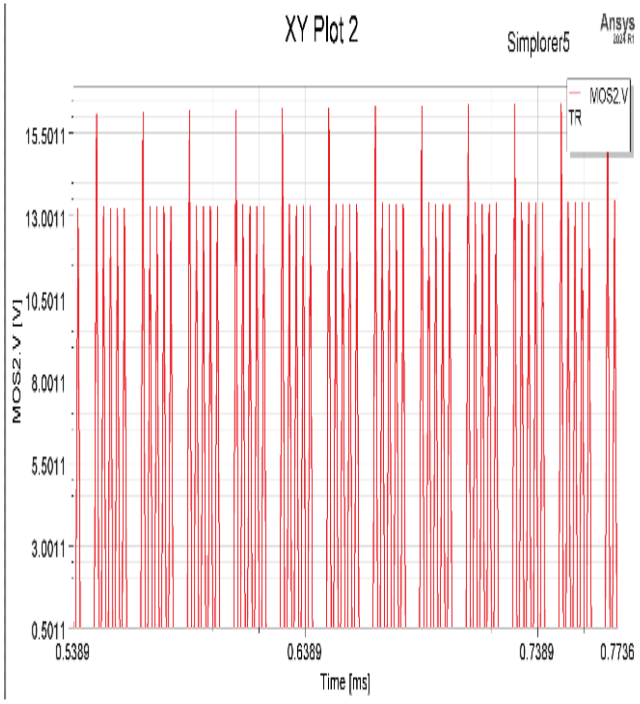
$$C_{sn} = \frac{V_{sn}}{\Delta V_{sn} R_{sn} f_s}$$

$$V_D = V_{out} + \frac{V_{in}(max)}{N_{ps}} + (20\%\ safety\ factor)$$

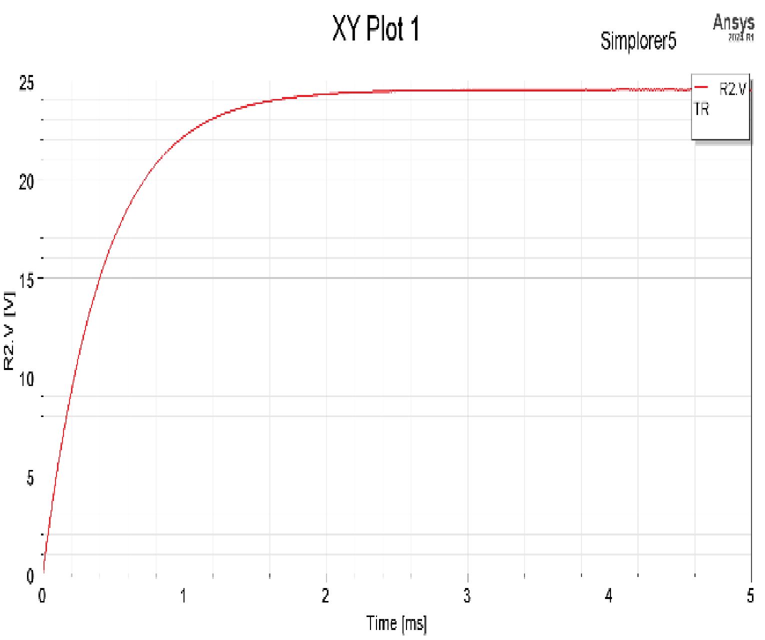


Ansys Simplorer Simulation Model.

Simplorer Simulation



(a) Drain to Source voltage, Vds of the MOSFET (V= 2.5/Div; Time = 0.1ms/Div).



b) Output voltage accross the load resistor (V =5V/Div; Time = 1mS/Div).

Conclusion

- Successfully designed and analyzed a **planar flyback transformer**.
- Covered complete workflow: **Core design → PEmag → PCB → Q3D → Eddy current → Maxwell → Icepak→ Simplorer**.
- Achieved:
  - Compact and low-profile design.
  - Reduced leakage inductance through interleaving.
  - Safe thermal and electromagnetic performance.
- Validated performance with **multiphysics simulations**.
- Confirms planar magnetics as an **efficient and reliable solution** for high-frequency converters.