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Design and Development of a Planar Flyback Transformer for Isolated Power Supply Applications

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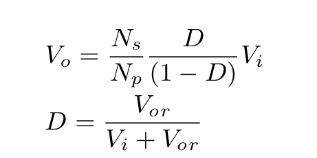
*Abstract*—The conventional wire wound magnetic components have exposed several limitations in terms of high power density, high operating frequency, and low profile in DC-DC power converters. The planar magnetic has eliminated the limitations of conventional transformers. Planar transformers are perfect for limited space applications since they are often smaller and flatter than wire-wound transformers where wire wound transformers are bulky. **In my summer internship I have simulated coupled of examples starting from simple coil , then two, four layer inductor ,two and four layer transformer , Em brake use in cars and planes doors . Here I am taking one project that I have followed from research papers.** This project involved a reduction in height of 50% from a conventional wire-wound transformer while achieving comparable electrical performance. In low-power DC- DC converter applications, flyback topology is often used as it is simple in structure and provides better isolation. In this project, a 2.5W flyback converter is designed with a planar transformer. The design of the planar transformer was accomplished by using Ansys PEmag. According to the PEmag simulation design, the PCB was designed in Kicad Designer. Then, it was exported to a finite element analysis-based software, Ansys Maxwell 3D, for further analysis including leakage inductance & coupling coefficient. A multi-physics circuit simulator, Ansys Simplorer, was also introduced in this project to observe the overall performance of the flyback converter with the designed planar transformer.

1. Key Design Parameters
2. *Inductance*

A planar flyback transformer was designed for this applica- tion as it provides galvanic isolation between the primary and secondary sides. The specifications of the flyback converter is given in Table 1

TABLE I: Design Specifications of The Flyback Converter

|  |  |  |
| --- | --- | --- |
| **Parameters** | **Symbols** | **Values** |
| Input Voltage | *Vi* | 8 - 12 V |
| Output Voltage | *Vo* | 24 V |
| Output Power | *Po* | 2 - 2.5 W |
| Switching Frequency | *fs* | 250 - 350 KHz |

The *E*14*/*3*.*5*/*5 has been chosen it has has a window height of 2*mm* where the PCB will be around 1.6mm in thickness. A proper core material was selected for the planar core, which is appropriate for the desired switching frequency range. The desired switching frequency was around 0.2-0.35 MHz. So, 3F3 ferrite material was chosen as it operates in 0.2 - 0.5 MHz . In the datasheet of the selected core, it is mentioned that the maximum inductance factor for the ungapped core is 1300*nH* for 3F3 material.

For the design requirement, primary inductance was calculated

7.619*µH*. Thus, the required turns for primary and secondary winding were calculated using Equation 8 and found to be 3 and 9, respectively.

Inductance factor or AL value*, AL* = *L*

*N* 2

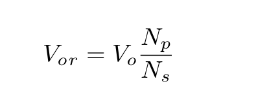
(8)

(1)

(2)

While designing the planar transformer, the PCB traces have to be stacked in the available window area and layers. The maximum possible width of the PCB track and the number of turns per layer was calculated by using Equation 9 [11].

The flyback converter was designed by using Equations 1 & 2. The reflected voltage, *Vor* was adjusted to 8V so that the duty cycle, D is 0.5.

*Tw* =

*W −* (*N −* 1)*S* (9)

*N*

The primary to secondary turns ratio, *Np*

is found to be 0.32

Here, *N* is the number of turns per layer, *W* is the winding

from Equation 3.

*Ns*

(3)

width, *S* is the spacing between traces.

Window utilization factor, *kw* is the percentage of the core window area that is filled with copper tracks [12]. The window utilization for this planar transformer is illustrated in Figure 1.

The converter was designed to be operated in BCM (Border Conduction Mode) mode under specified input voltage and full load condition. The critical point has been calculated for this condition using Equation 5 [7].

*Kcrit* = (1 *− D*)2 (4)

Using Equation 10, the *kw* of this transformer was calculated and found to be around 0.032.

*Aw.Kw* = *acp.Np* + *acs.Ns* (10)

Where, *K*

*crit*

2*Ls*

=

*RTs*

(5)

The required secondary inductance, *Ls* was calculated by using Equation 6.

*L* = *RoKcrit s* 2*fs*

(6)

= 74*.*40*µH* (7)

and the primary inductace, *Lp* = ( *Np* )2*Ls* = 7*.*619*µH*.

*Ns*

1. *Selection of Core Geometry and Core Material*

The design of the planar transformer starts with the selection of the core. The selection of a core is an iterative process with trade-offs between different core properties like core shape, size, and material. Selecting a core shape is vital as different core shapes have different window areas. For

Fig. 1: Window Utilization of The Planar Transformer.



Here, *Aw* is the available core window area, *kw* is the window utilization factor, *acp* & *acn* is the cross-sectional area of the primary and secondary traces and *Np* & *Ns* is the primary and secondary number of turns.

1*oz* copper was used in the PCB tracks of both primary and secondary. The current density, *J* of the tracks was calculated using Equation 11.

the flyback converter, selecting a core with more window area is suggested, which minimizes the leakage inductances and provides adequate winding isolation for maintaining the

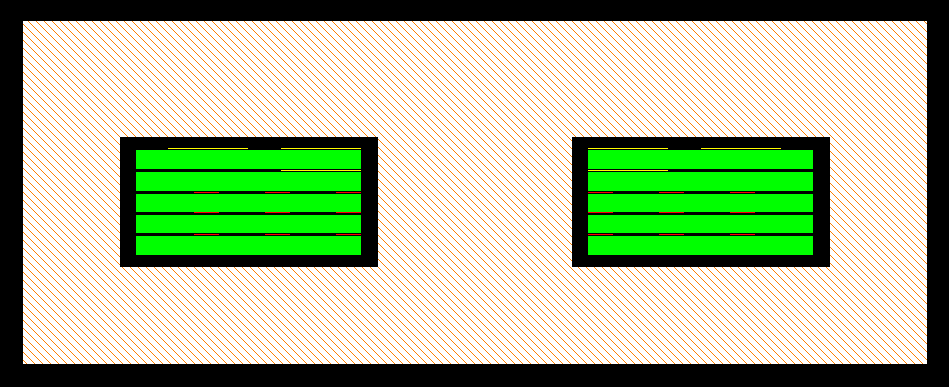
*J* = *IP RMS*

*ac*

Here, *IP RMS* is the primary RMS current.

(11)

required creepage distance. For the chosen core, the specified maximum flux density, *Bm*

is around 0.4 *T* . It can be seen from the core’s core loss vs flux density plot that core loss rises as operational flux density rises [10]. So, the maximum flux density was considered to be around 0.3 *T* for this operation.

The selection of core geometry was validated by calculating the relationship between area product (*Ac.Aw*) of the core and energy handling capacity of the inductor. [13].

*Ac.Aw*

*≥ Lp × IP peak × IT RMS*

*B × J × Kw*

(12)

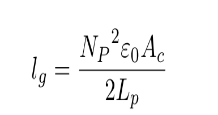
Fig. 2: Planar Transformer 2D Model - Ansys PEmag.

*Ac* is the effective area of the selected core. Area product is

TABLE III: PCB Stacking of Primary & Secondary Windings.-

found to be 112 *mm*4 and the selected core has area product

of 113.6 *mm*4.



(13)

**Primary winding**

Number of turns 3

Max turns per layer 2

Number of layers 2

Copper track thickness 35 *µm*

Copper track width 1.25 mm

The required air-gap was calculated using Equation 13 and air-gap is found around 10*µm* and air-gap per core leg comes out to be 3*.*34*µm*. Air-gap was provided by placing insulating tap between the cores.

1. Planar Transformer Modelling

The required parameters to design planar transformer has been calculated using the design Equations discussed in sec- tion 2. The specifications for planar transformer modelling is given in Table 2.

TABLE II: Design Specifications Of The Flyback Converter.

|  |  |
| --- | --- |
| **Parameters** | **Values** |
| Primary Winding | 3 Turns |
| Secondary Winding | 9 Turns |
| Primary Inductance | 7.619 *µH* |
| Secondary Inductance | 74.40 *µH* |
| Primary Current | 1.5 *A* |
| Total RMS Current | 1.225 *A* |
| Maximum Flux Density | 0.3 *T* |
| Core Type | *E*14*/*3*.*5*/*5 & *PLT* 14*/*5*/*1*.*5 |
| Fill Factor | 0.032 |
| Core Material | 3*F* 3 |
| Switching Frequency | 350 kHz |
| Air-gap Per Leg | 3*.*34*µm* |

1. *Planar Transformer Design in Ansys PEmag*

The preliminary planar transformer design with the ap- propriate winding strategy given in Table 3 was simulated in Ansys PEmag to calculate the self-inductances of the primary and secondary windings. In PEmag, the winding type, required insulation and the operating frequency was defined accordingly. Ansys PEmag design of the planar transformer was illustrated in Figure 2.

1. *PCB Design and 3D FEA Simulation*

The proposed planar transformers PCB has been designed in Kicad PCB designer with the properties of Table 3. After completing the design in Kicad, the model was exported to ANSYS Maxwell 3D as a step file for further 3D

Spacing between tracks 0.5 mm

Insulation between layers 60 *µm*

Insulation between primary & secondary 0.4 mm

**Secondary winding**

Number of turns 9

Max turns per layer 3

Number of layers 3

Copper track thickness 35 *µm*

Copper track width 0.4 mm

Spacing between tracks 0.5 mm

Insulation between layers 60 *µm*

FEA analysis. Figure 3 & 4 shows the top view and the different layers of the designed planar transformer PCB.

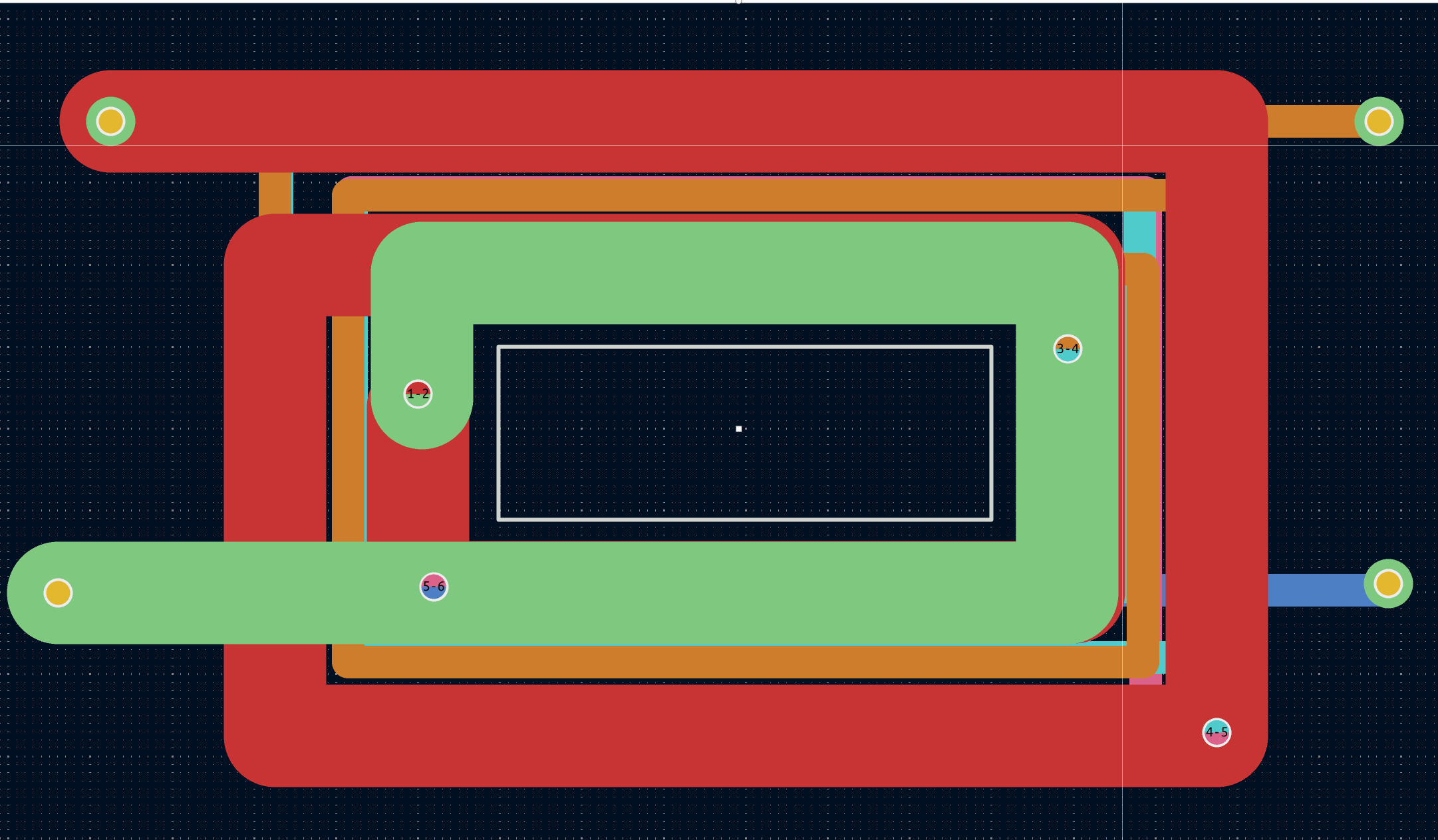


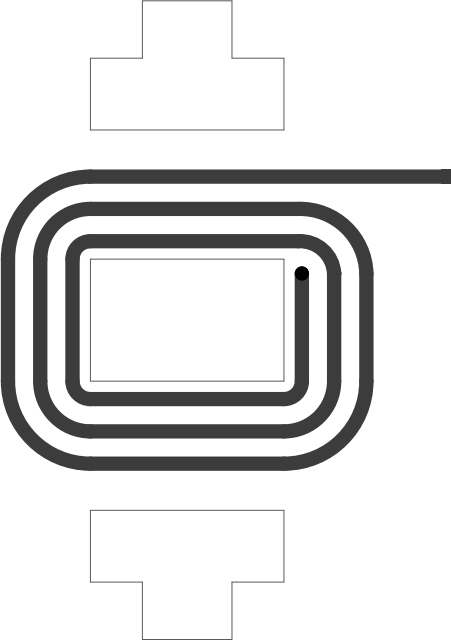
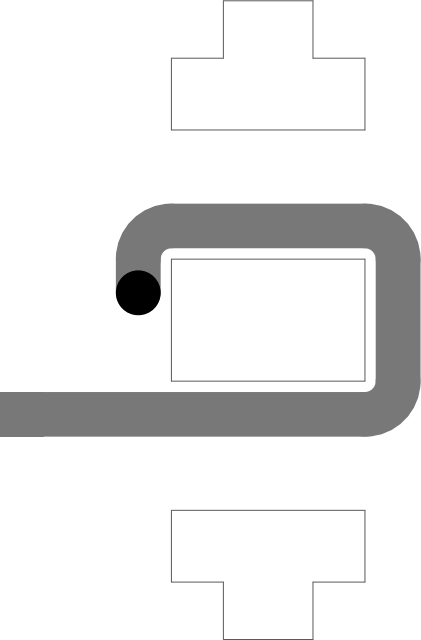
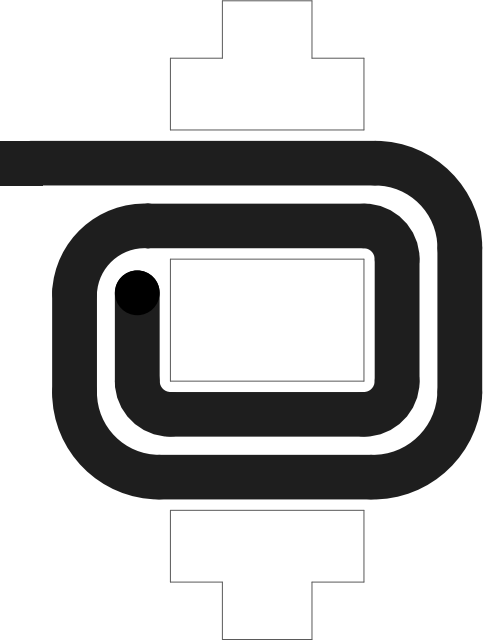
Fig. 3: Kicad design of planar transformer PCB.

In ANSYS Maxwell 3D, the core was designed using the geometry in the datasheet, and 3F3 material properties were assigned to the core. The whole model was enclosed in a region of air which acts as a boundary.

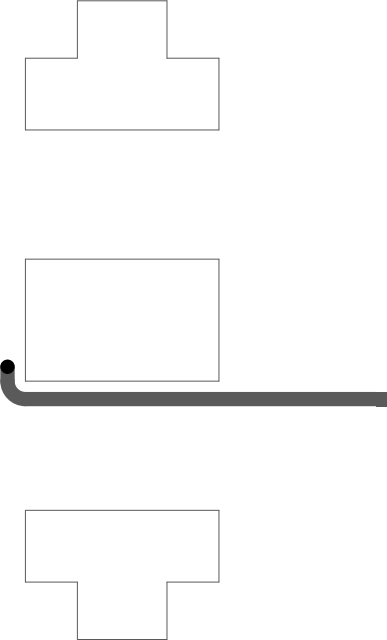
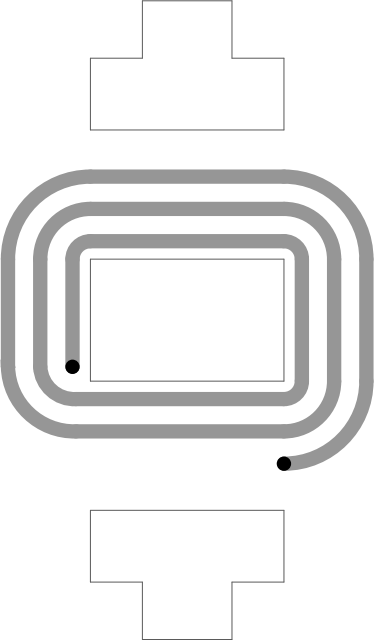
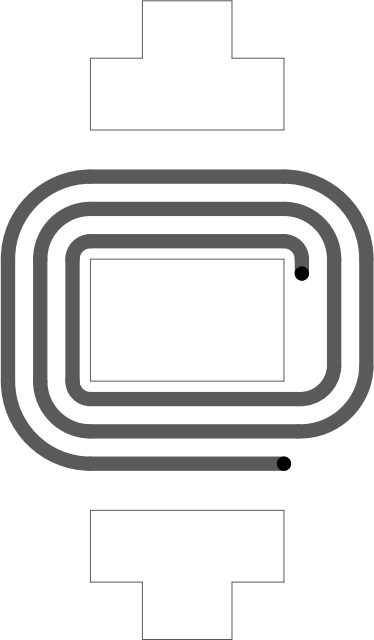
Figure 5(a) shows the complete design of the planar trans- former in Ansys Maxwell 3D. After assigning the excitations properly, the simulation was performed using eddy current solver. The primary and the secondary inductance from the simulation result were 6.5*µH* and 58.77*µH*, respectively.

In figure 5(b), It was observed that the peak operating flux density

a voltage spike.

The primary (*Lplk*) and secondary (*Lslk*) leakage inductance of this planar transformer is calculated using Equation 14 & 15.

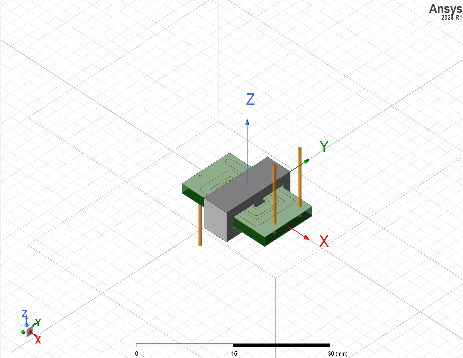
(a) Top Layer - Primary (b) Layer 2 - Primary (c) Layer 3 - Secondary

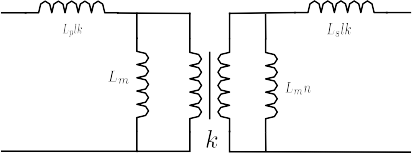


1. Layer 4 - Secondary (e) Layer 5 - Secondary (f) Bottom Layer - Sec-

ondary

Fig. 4: Layers of planar transformer PCB.



Fig. 6: Equivalent Model of a Transformer.

*Lp* = *Lm* + *Lplk* (14)

*Lm* = *Lp.k* (15)

From equation 14 & 15, primary leakage inductance is -

*Lplk* = *Lp*(1 *− k*) (16) Similarly, for secondary leakage inductance is -

*Lslk* = *Ls*(1 *− k*) (17)

Here, *Lp* and *Ls* is the primary and secondary self inductance and *K* is the coupling coefficient. Coupling coefficient *K*, is be found by Equation 18.

*M*

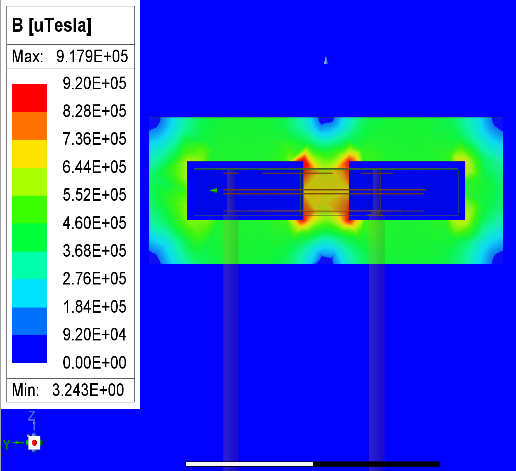
*k* = √*L L*

*p*

*s*

(18)

* 1. Planar Transformer 3D Model - Ansys Maxwell 3D.



* 1. Peak Flux Density of the planar transformer.

Fig. 5: 3D FEA Analysis of the planar transformer

of the core is 0.917T.

As Leakage inductance has some negative impact on the

here, *M* is the mutual inductance. The *Lp*, *Ls* and *M* can be determined by 3D FEA simulation in ANSYS Maxwell 3D.

TABLE IV: Simulated Parameters of the planar flyback trans- former

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| *Lplk* | *Lslk* | *M* | *K* | *Lp* | *Ls* |
| 35 *nH* | 0.3 *nH* | 19.44 *µH* | 0.9946 | 6.5 *µH* | 58.77 *µH* |

A RCD Snubber circuit was designed for the flyback converter circuit. When the switch turns off, a high voltage spike appears on the switch due to the presence of the leakage inductance in the windings.

This high voltage spike may damage the MOSFET therefore a RCD snubber circuit is required to clamp the voltage.

The selected controller IC has an integrated MOSFET switch that has a maximum 65V drain to source voltage, *Vds*. So, the maximum *Vds* when the MOSFET is off should be less than 65V. For the designed flyback converter circuit, 20V is considered to be the maximum *Vds*. So, *Vsn* = *Vds − Vi* = 12V.

Both *Rsn* & *Csn* is determined by using Equation 19 & 20 -

switching device. During ON time leakage inductance stores

*sn*

*Ip*

*R* = *Vsn*(*Vsn − Vor*)

(19)

some energy that does not transfer to the secondary side. In OFF time this stored energy of the leakage inductance is dis-

1 2

2 *peak*

*Llkfs*

sipated either in the RCD clamping circuit or TVS(Transient Voltage Suppressor) diode to save the switching device from

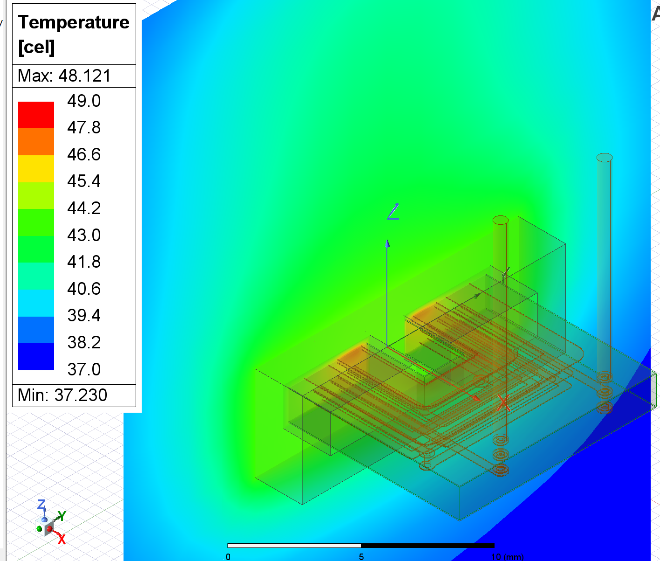
*Csn*

*Vsn*

=

∆*VsnRsnfs*

(20)

For this designed flyback planar transformer *Rsn* and *Csn* is determined to be around 4*k*Ω and 13*nF* .

A diode that is fast and has sufficient reverse voltage break- down has been chosen for this circuit. The main criterion for choosing the output diode is a reverse-voltage rating that the diode can withstand while operating. The rating of the diode has been selected by using below Equation 21.

*VD* = *V*

*out*

+ *Vin*(*max*) + (20% *safety factor*) (21)

*Nps*

1. Close View of the Planar Trans- former.

An ANSYS Simplorer simulation was performed where elec- tromagnetic component and power electronic circuits were coupled together to determine the designed planar transformers performance. Figure 7 & 8 shows the simplorer simulation model and simulation results.

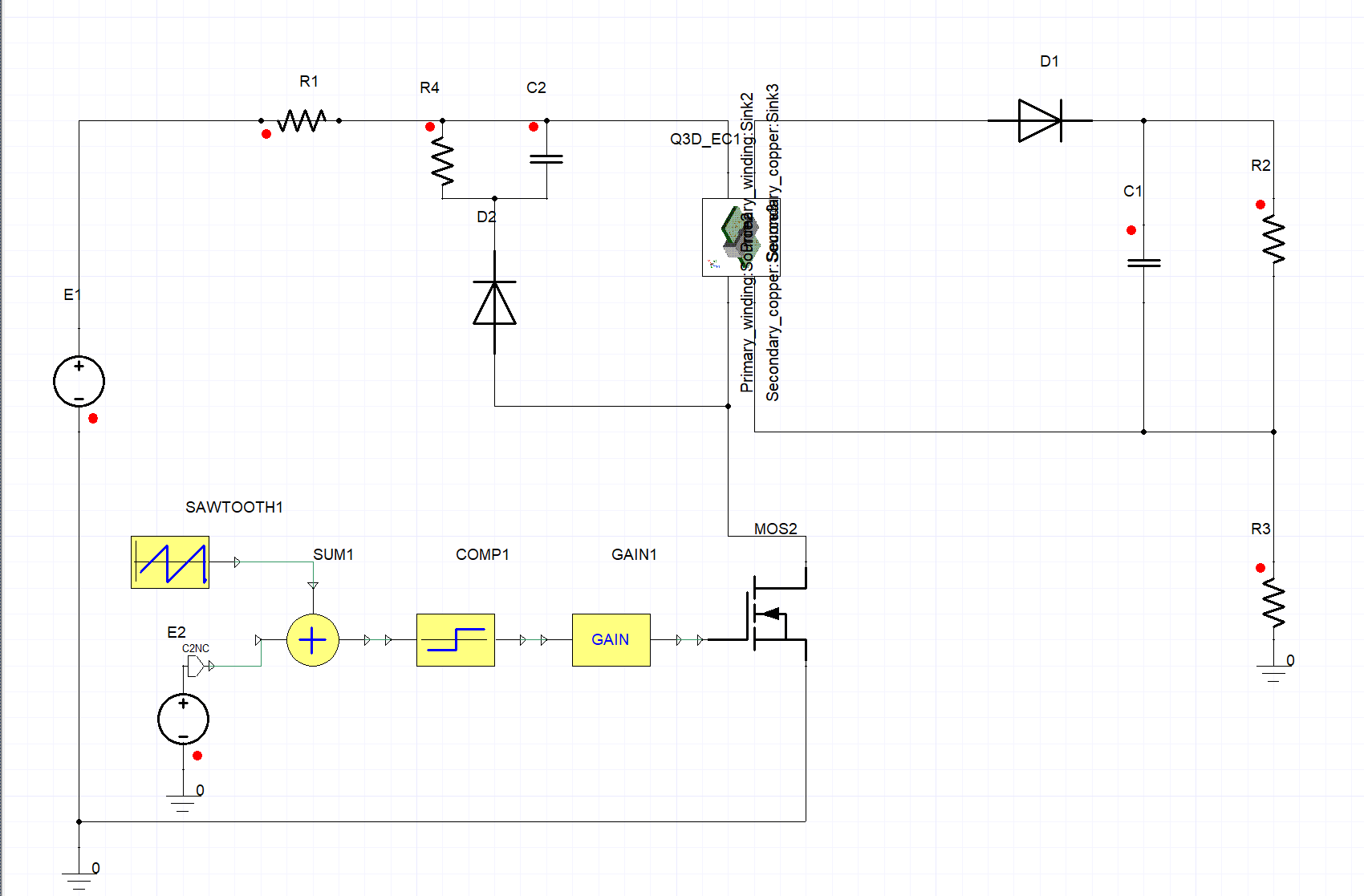
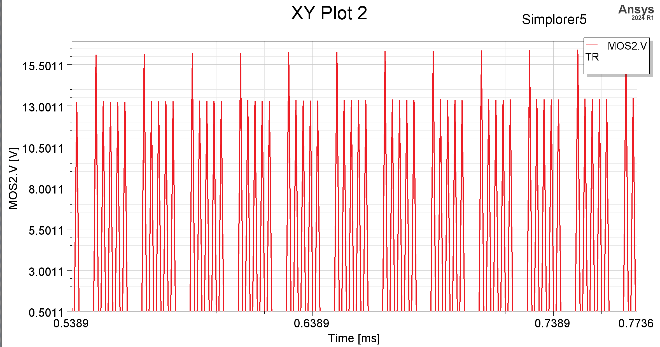
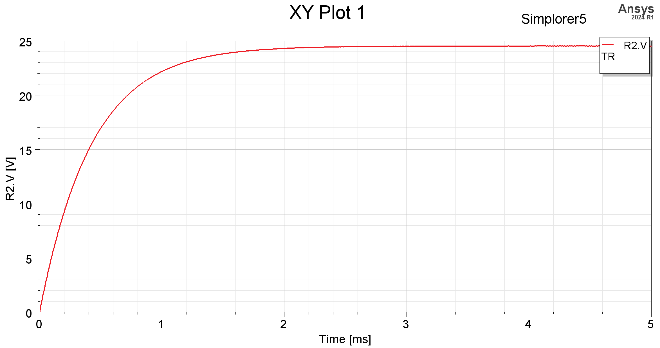


Fig. 7: Ansys Simplorer Simulation Model.



1. Drain to Source voltage, Vds of the MOSFET (V= 2.5/Div; Time = 0.1ms/Div).



(b) Output voltage accross the load resistor (V =5V/Div; Time = 1mS/Div).

Fig. 12: Thermal Distribution of the Designed Planar Trans- former (3D FEM Simulation).

A two-way coupled simulation was performed using ANSYS Maxwell and ANSYS Icepak to evaluate the thermal performance of the planar transformer .The result are shown in fig 12.

V. Conlcusion

This paper has presented a comprehensive design study and development of a 350kHz PCB integrated flyback planar transformer. Through this project, various aspects of planar transformers have been explored, including their design prin- ciples, winding patterns and manufacturing techniques. The research findings suggest that planar transformers offer a com- pelling solution for compact power electronics applications, including renewable energy systems, electric vehicles, and aerospace. However, further research is necessary to optimize planar transformer design and manufacturing processes to enhance their performance and reduce their production cost. One of the disadvantages of the planar transformer is inter- winding capacitances. These inter-winding capacitances must be integrated into the converter design or minimized through improved winding layout design. Potential future research scope involves exploring an analytical approach to precisely simulate the planar inductor, considering skin, proximity, and parasitic effects. Overall, this paper highlights the potential of planar transformers in the power electronics industry and sustainable energy system

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1. Drain to Source voltage, Vds of the MOSFET (V= 2.5/Div; Time = 0.1ms/Div).

Fig. 8: ANSYS Simplorer Simulation Results.

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