74AHC08; 74AHCT08

Quad 2-input AND gate Rev. 03 — 14 November 2007

Product data sheet

General description 1.

The 74AHC08; 74AHCT08 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard JESD7-A.

The 74AHC08; 74AHCT08 provides the quad 2-input AND function.

2. **Features**

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than V_{CC}
- For 74AHC08 only: operates with CMOS input levels
- For 74AHCT08 only: operates with TTL input levels
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

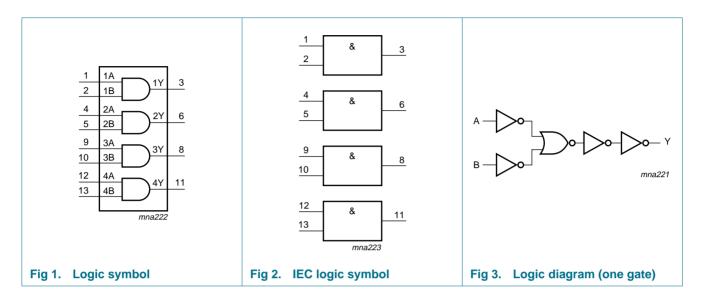
Ordering information 3.

Table 1. **Ordering information**

Type number	Package								
	Temperature range	Name	Description	Version					
74AHC08D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1					
74AHCT08D			body width 3.9 mm						
74AHC08PW	-40 °C to +125 °C TSSOP14		plastic thin shrink small outline package; 14 leads;	SOT402-1					
74AHCT08PW			body width 4.4 mm						
74AHC08BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very	SOT762-1					
74AHCT08BQ			thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm						

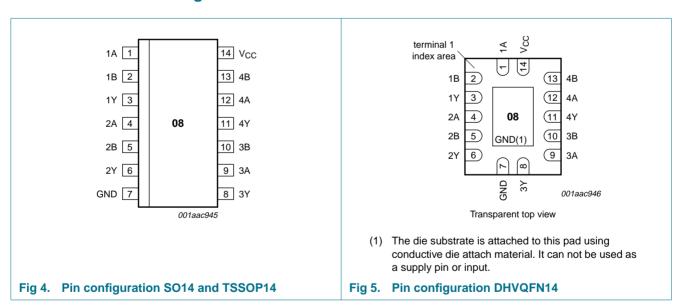


4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1B	2	data input
1Y	3	data output
2A	4	data input
2B	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3B	10	data input
4Y	11	data output
4A	12	data input
4B	13	data input
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection[1]

Input	Output	
nA	nB	nY
L	X	L
X	L	L
Н	Н	Н

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_1 < -0.5 \text{ V}$	<u>[1]</u> –20	-	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> _	±20	mA
I _O	output current	$V_O = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±25	mA
I _{CC}	supply current		-	75	mA
I_{GND}	ground current		–75	-	mA
T _{stg}	storage temperature		-65	+150	°C

4 of 14

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$			
	SO14 package		[2] -	500	mW
	TSSOP14 package		<u>[3]</u> -	500	mW
	DHVQFN14 package		<u>[4]</u> _	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] Ptot derates linearly with 8 mW/K above 70 °C.
- [3] Ptot derates linearly with 5.5 mW/K above 60 °C.
- [4] Ptot derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter		74AH0	74AHC08			74AHCT08		
			Min	Тур	Max	Min	Тур	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_{I}	input voltage		0	-	5.5	0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.3 V \pm 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
For type	74AHC08	'								
V_{IH}	HIGH-level	$V_{CC} = 2.0 \text{ V}$	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = -50 \mu A; V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu A; V_{CC} = 3.0 \text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.4	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.8	-	3.7	-	V

Product data sheet

Quad 2-input AND gate

5 of 14

Table 6. Static characteristics ... continued

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}				'	'			
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
C _I	input capacitance		-	3.0	10	-	10	-	10	pF
For type	74AHCT08									
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	8.0	-	0.8	-	0.8	V
V_{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_O = -50 \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -8.0 \text{ mA}$	3.94	-	-	3.8	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
II	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
ΔI_{CC}	additional supply current	per input pin; $V_{I} = V_{CC} - 2.1 \text{ V}; I_{O} = 0 \text{ A};$ other pins at V_{CC} or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	3.0	10	-	10	-	10	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics *GND = 0 V; For test circuit see Figure 7.*

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C t	to +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
For type	74AHC08						•				
t _{pd}	propagation	nA, nB to nY; see Figure 6	[2]								
	delay	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$									
		C _L = 15 pF		-	4.0	8.8	1.0	10.5	1.0	11.0	ns
		$C_L = 50 pF$		-	5.6	12.3	1.0	14	1.0	15.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C _L = 15 pF		-	3.0	5.9	1.0	7.0	1.0	7.5	ns
		$C_L = 50 pF$			4.2	7.9	1.0	9.0	1.0	10.0	ns
C _{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[3]	-	10.0	-	-	-	-	-	pF
For type	74AHCT08										
t _{pd}	propagation	nA, nB to nY; see Figure 6	[2]								
	delay	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C _L = 15 pF		-	3.2	6.9	1.0	8.0	1.0	9.0	ns
		$C_L = 50 pF$		-	4.2	7.9	1.0	9.0	1.0	10.0	ns
C _{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[3]	-	12.0	-	-	-	-	-	pF

^[1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 5.0 \text{ V}$).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz, f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

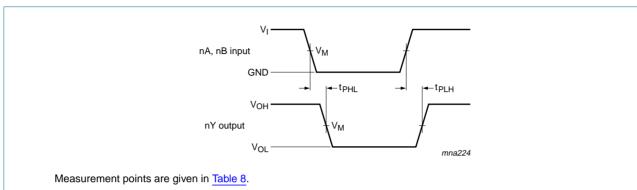
 $\Sigma(C_L\times V_{CC}{}^2\times f_o)$ = sum of the outputs.

^[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

^[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

7 of 14

11. Waveforms



 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

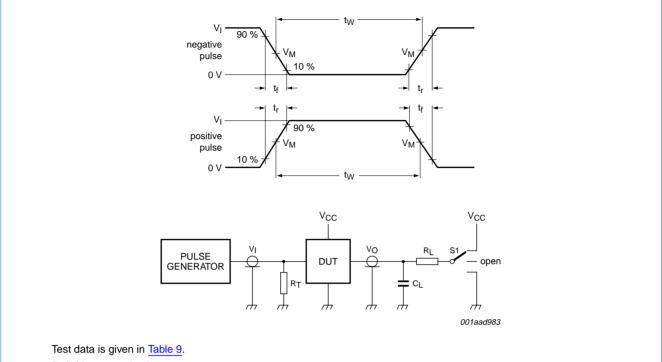
Fig 6. The input (nA, nB) to output (nY) propagation delays

Table 8. **Measurement points**

Product data sheet

Туре	Input	Output
	V _M	V _M
74AHC08	0.5V _{CC}	0.5V _{CC}
74AHCT08	1.5 V	0.5V _{CC}

8 of 14



Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 7. Load circuit for switching times

Table 9. **Test data**

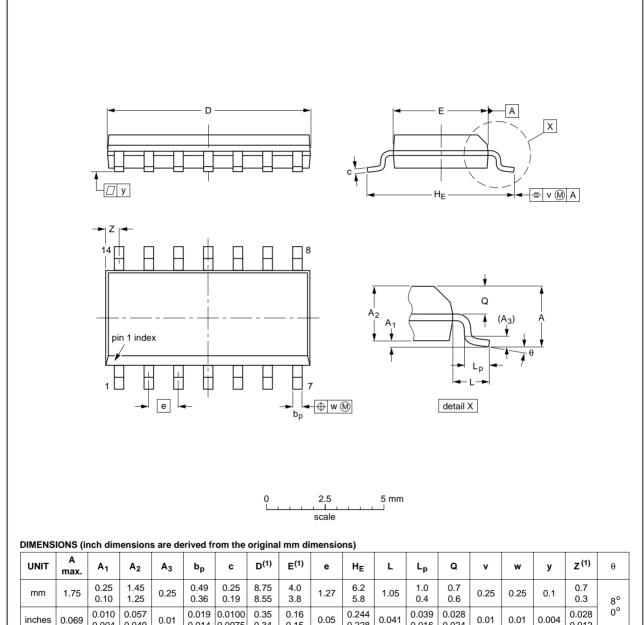
Product data sheet

Туре	Input	Load		S1 position			
	VI	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
74AHC08	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}
74AHCT08	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



inches

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014

0.0075

0.34

0.15

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

0.228

0.016

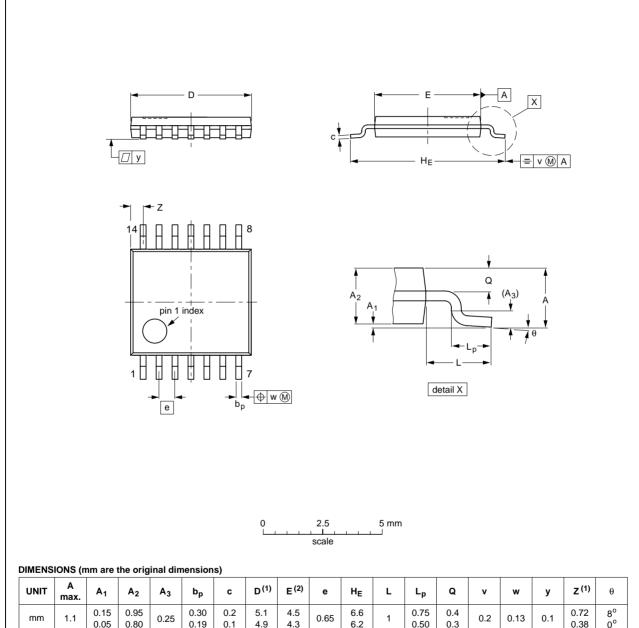
Fig 8. Package outline SOT108-1 (SO14)

0.004

74AHC_AHCT08_3 © NXP B.V. 2007. All rights reserved.

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT402-1		MO-153				99-12-27 03-02-18	

Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

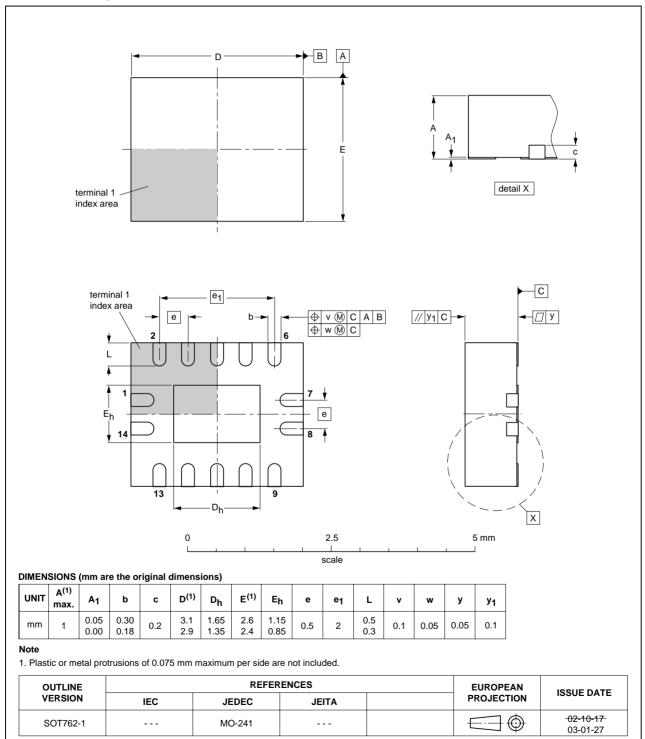


Fig 10. Package outline SOT762-1 (DHVQFN14)

74AHC_AHCT08_3 © NXP B.V. 2007. All rights reserved.

12 of 14

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Product data sheet

Document ID	Release date	Data sheet status	Change notice	Supersedes					
74AHC_AHCT08_3	20071114	Product data sheet	-	74AHC_AHCT08_2					
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 								
	 Legal texts have b 	peen adapted to the new o	company name where ap	propriate.					
	 Section 3: DHVQI 	FN14 package added.							
	 Section 7: derating 	g values added for DHVQ	FN14 package.						
	 Section 12: outline 	e drawing added for DHV	QFN14 package.						
74AHC_AHCT08_2	19990924	Product specification	-	74AHC_AHCT08_1					
74AHC_AHCT08_1	19981218	Product specification	-	-					

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For additional information, please visit: http://www.nxp.com

For sales office addresses, send an email to: salesaddresses@nxp.com

17. Contents

1	General description
2	Features
3	Ordering information
4	Functional diagram 2
5	Pinning information
5.1	Pinning
5.2	Pin description
6	Functional description 3
7	Limiting values 3
8	Recommended operating conditions 4
9	Static characteristics 4
10	Dynamic characteristics 6
11	Waveforms
12	Package outline 9
13	Abbreviations
14	Revision history
15	Legal information
15.1	Data sheet status
15.2	Definitions
15.3	Disclaimers
15.4	Trademarks13
16	Contact information
17	Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



