Data620 Testing Device - Project Overview

The Data620 computer is a unique and fascinating machine built using analog electronic circuitry. It employs a versalogic signaling scheme where a logical **false** or bit value **0** is represented by **0V**, while a logical **true** or bit value **1** is represented by **-12V**. This unconventional voltage scheme sets it apart from many modern digital systems.

Constructed from basic electronic components such as resistors, capacitors, diodes, and transistors, the Data620's entire system is divided into a large number of printed circuit boards (PCBs). Each PCB contains analog circuitry, and it is known that some of these boards may include faulty or erroneous components.

Currently, there is no dedicated testing device available to verify the functionality of these PCBs. Such a device would be highly valuable to anyone restoring or working with the Data620, as it would allow for systematic troubleshooting and repair.

This project represents the first draft towards developing such a testing device. It includes preliminary hardware design concepts and the necessary SPICE simulations to understand and verify the circuitry. However, at this stage, only the hardware draft exists.

Software development for this testing device has not yet begun and will be based on reverse engineering efforts of the DATA620 PCBs currently being carried out by third parties.

Software development for this testing device is in its early stages and will proceed following the completion of a stable hardware version. It also awaits the reverse engineering efforts of the DATA620 PCBs carried out by third parties.

This project is currently an independent effort (not affiliated with Usage Electric or other existing Data620 projects). We hold great respect for the significant contributions and extensive work carried out by Usage Electric and the dedicated volunteers contributing to the Usagi Electric Data620 project. Our development is separate, however, we are more than willing to explore opportunities to collaborate and join forces in the future.

As this is an initial draft, the design undoubtedly contains errors and inaccuracies. We warmly welcome constructive feedback and suggestions from the community to improve and refine the project.

For those interested in learning more about the Data620 itself, the following discussion provides valuable insights and historical context:

- https://retrocomputingforum.com/t/data-620-transistor-minicomputer/3847
- https://github.com/Nakazoto/Data620
- https://www.youtube.com/watch?v=YR9E9ZvHkQE

Thank you to all that participate with **Usage Electric** for your interest and support in preserving this remarkable piece of computing history.

License Overview

This project contains software, hardware designs, and documentation. Each part is licensed under terms appropriate to its nature.

Hardware Designs

The schematics, PCB layouts, and other hardware design source files are licensed under the **CERN Open Hardware Licence Version 2 - Strongly Reciprocal (CERN-OHL-S v2.0)**. See CERN-OHL-S for the full text.

Software

The controller source code, build scripts, and related software files are licensed under the **MIT License**. See MIT for the full text.

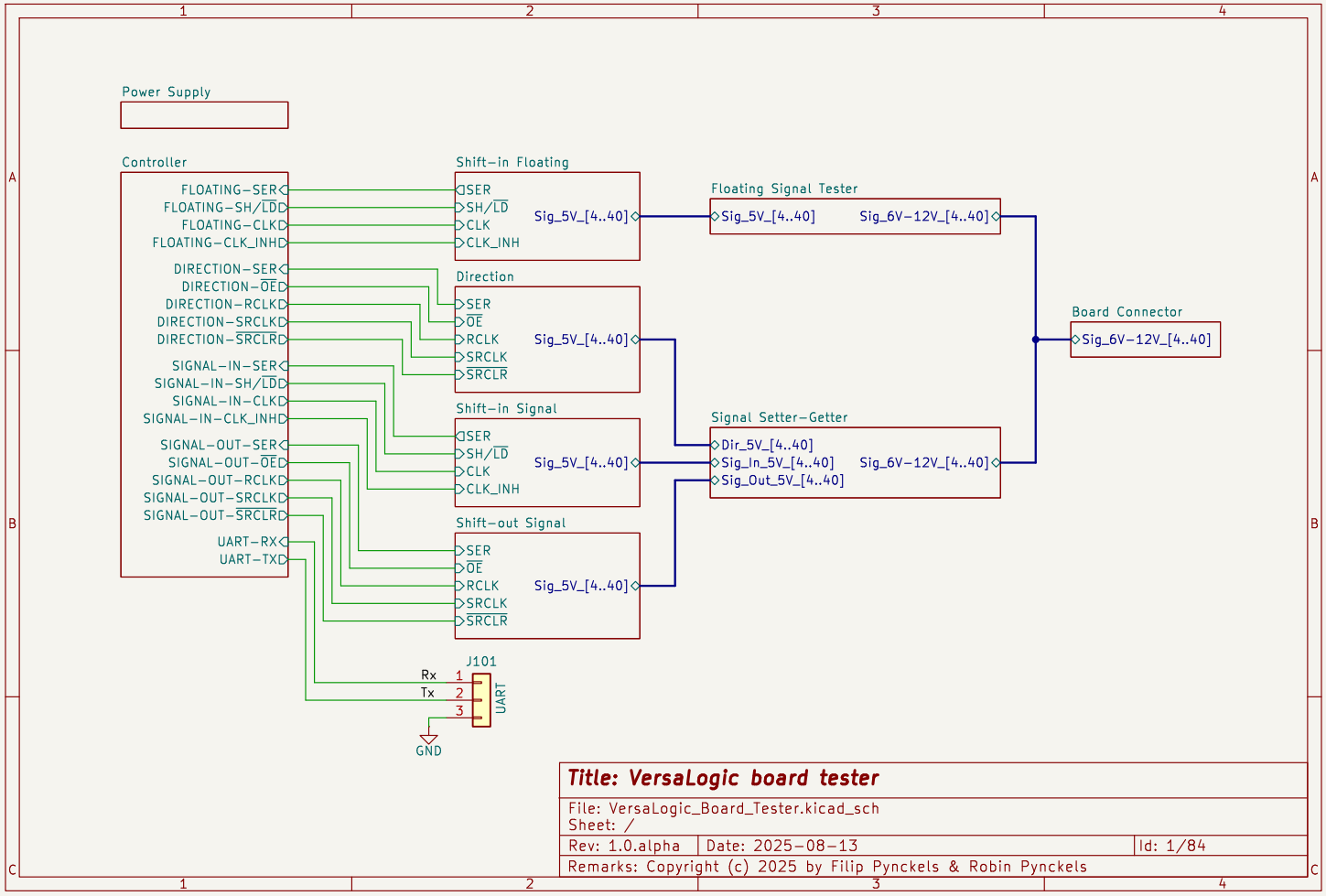
Documentation

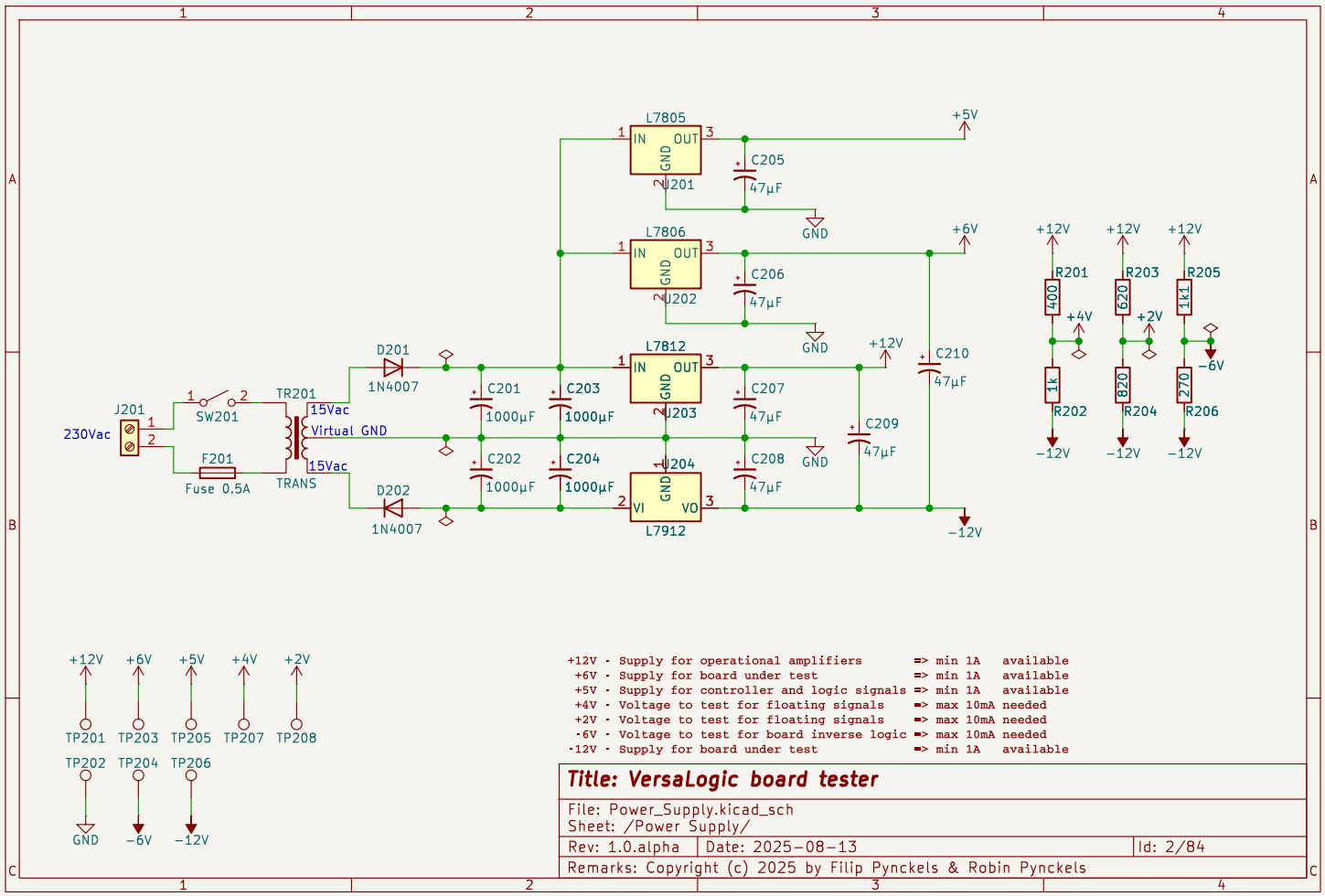
The written documentation, guides, and non-code instructional materials are licensed under the **Creative Commons Attribution Non Commercial Share Alike 4.0 International (CC-NC-SA 4.0)** license. See CC-NC-SA for the full text.

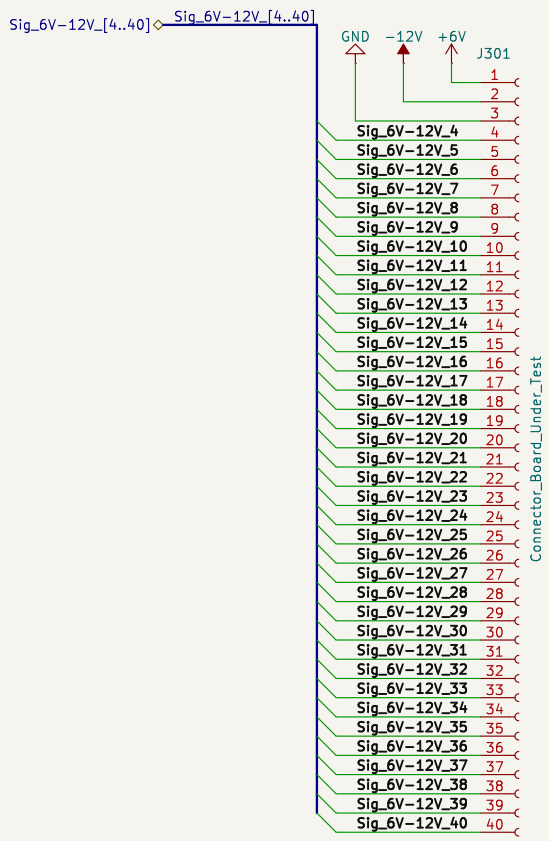
Summary

- **Software** → MIT License
- **Hardware** → CERN-OHL-S v2.0
- **Documentation** → CC-NC-SA 4.0

You are free to use, modify, and distribute each component under its respective license terms.


Power Supply
Controller
FLOATING-SER
FLOATING-SH/LD
FLOATING-CLK
FLOATING-CLK_INH
DIRECTION-SER
DIRECTION-OE
DIRECTION-RCLK
DIRECTION-SRCLK
DIRECTION-SRCLR
SIGNAL-IN-SER
SIGNAL-IN-SH/LD
SIGNAL-IN-CLK
SIGNAL-IN-CLK_INH
SIGNAL-OUT-SER
SIGNAL-OUT-OE
SIGNAL-OUT-RCLK
SIGNAL-OUT-SRCLK
SIGNAL-OUT-SRCLR
UART-RX
UART-TX
Shift-in Floating
SER
SH/LD
CLK
CLK_INH
Sig_5V_[4..40]
Direction
OE
RCLK
SRCLK
SRCLR
Shift-in Signal
Shift-out Signal
Floating Signal Tester
Sig_6V-12V_[4..40]
Board Connector
Signal Setter-Getter
Dir_5V_[4..40]
Sig_In_5V_[4..40]
Sig_Out_5V_[4..40]
J101
Rx
Tx
UART
GND
Title: VersaLogic board tester
File: VersaLogic_Board_Tester.kicad_sch
Sheet: /
Rev: 1.0.alpha
Date: 2025-08-13
Id: 1/84
Remarks: Copyright (c) 2025 by Filip Pynckels & Robin Pynckels

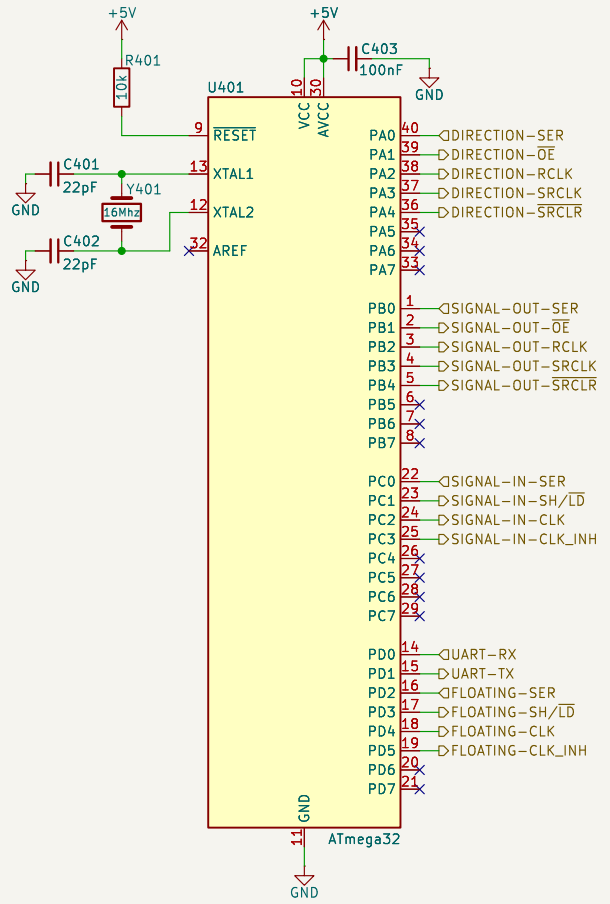

L7805
L7806
L7812
L7912
U201
U202
U203
U204
IN
OUT
GND
VI
VO
+5V
+6V
+12V
-12V
C205
C206
C207
C208
C209
C210
47µF
C201
C202
C203
C204
1000µF
D201
D202
1N4007
J201
230Vac
SW201
F201
Fuse 0.5A
TR201
TRANS
15Vac
Virtual GND
R201
R202
R203
R204
R205
R206
400
1k
620
820
1k1
270
+4V
+2V
-6V
TP201
TP203
TP205
TP207
TP208
TP202
TP204
TP206
+12V - Supply for operational amplifiers => min 1A available
+6V - Supply for board under test => min 1A available
+5V - Supply for controller and logic signals => min 1A available
+4V - Voltage to test for floating signals => max 10mA needed
+2V - Voltage to test for floating signals => max 10mA needed
-6V - Voltage to test for board inverse logic => max 10mA needed
-12V - Supply for board under test => min 1A available
Title: VersaLogic board tester
File: Power_Supply.kicad_sch
Sheet: /Power Supply/
Rev: 1.0.alpha
Date: 2025-08-13
Id: 2/84
Remarks: Copyright (c) 2025 by Filip Pynckels & Robin Pynckels



Title: VersaLogic board tester

File: Board_Connector.kicad_sch
Sheet: /Board Connector/

Rev: 1.0.alpha | Date: 2025-08-13 | Id: 3/84



All control signals for the shift buffers are available for the controller
to give the program maximal options to alter the functioning of the hardware.

The program logic can be as follows:

1. Shift in the floating pins (bit 4..40). See "Floating Signal Tester" schematic
   for description of the bit values.

2. Use winner takes all algorithm to decide which board type is inserted in
   the board connector.

3. Set direction of the board pins conform to the board that is plugged in.

3. Loop through test scenarios: per scenario:
   - Set output pin values (TTL logic)
   - Read and verify input pin values (TTL logic)

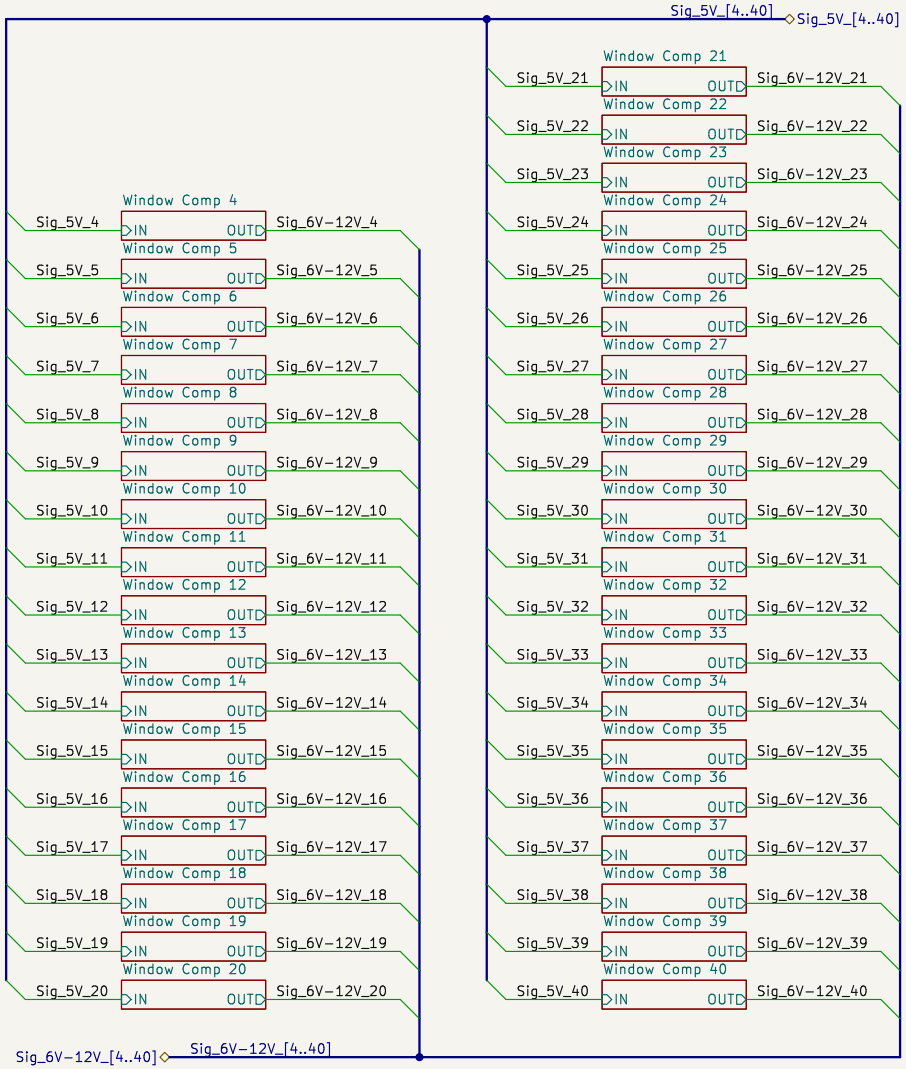
If the controller has to be reprogrammed frequently, it is advisable to use
a ZIF socket.

The UART pins use TTL logic (5V, 0V).

Title: VersaLogic board tester

File: Controller.kicad_sch
Sheet: /Controller/

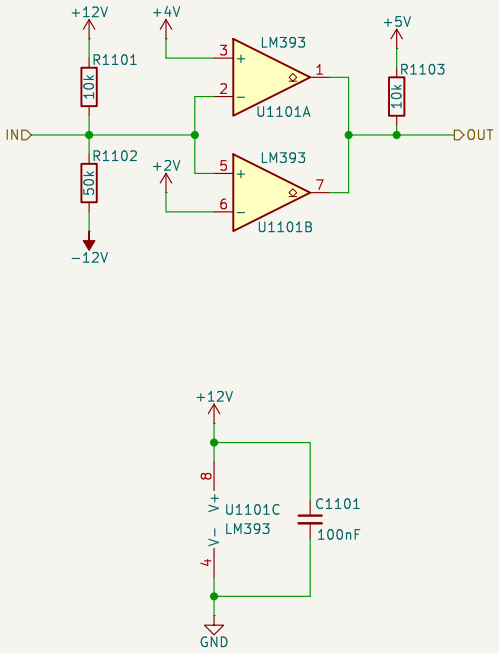
Rev: 1.0.alpha | Date: 2025-08-13 | Id: 4/84



Input - Tri-state bus (0V, -12V, floating)
Can be pulled up to +6V when short circuit on board under test

Output - Digital bus (TTL logic): 5V (true) in case input is floating
GND (false) in case output is not floating

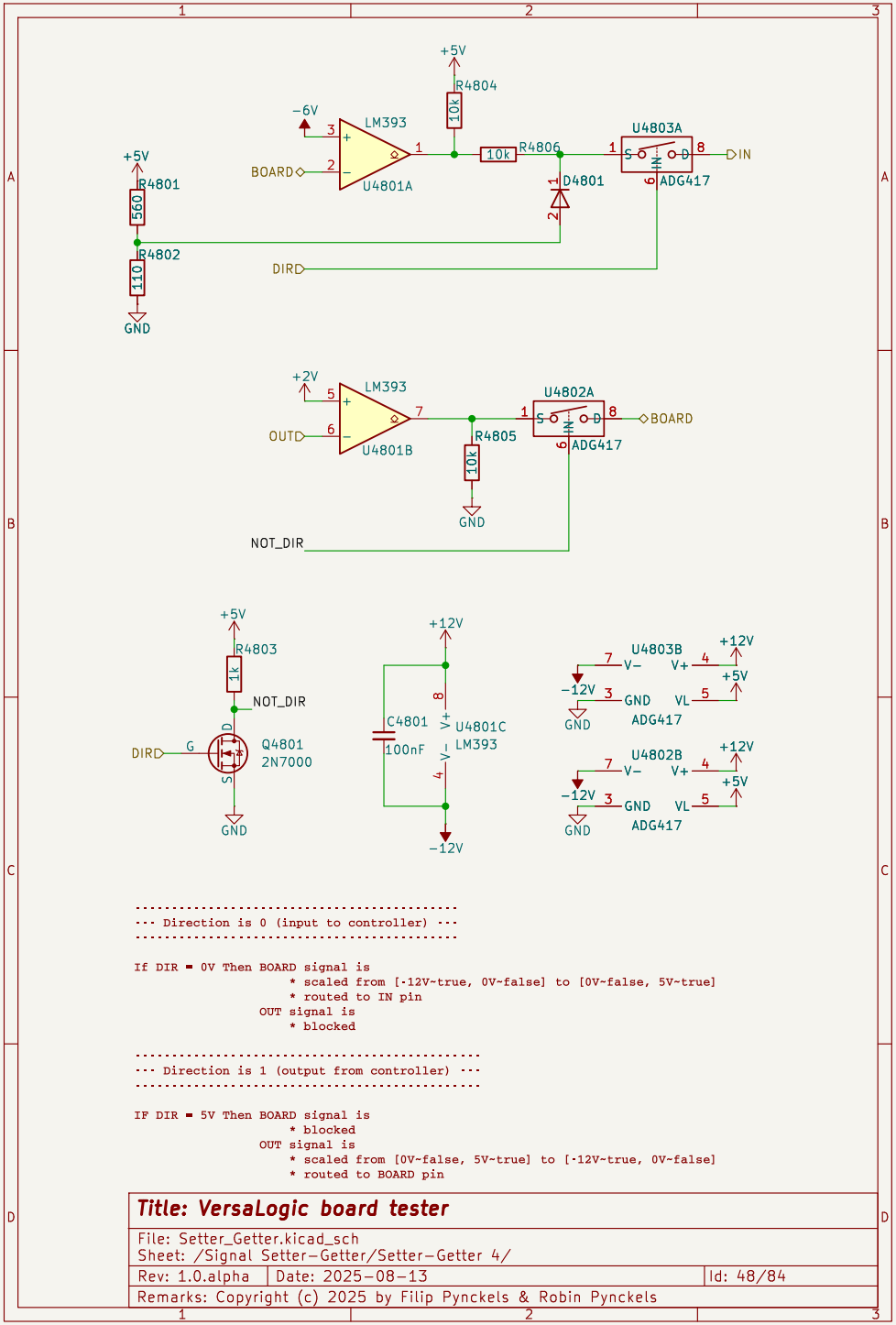
Title: VersaLogic board tester		
File: Floating_Signal_Tester.kicad_sch Sheet: /Floating Signal Tester/		
Rev: 1.0.alpha	Date: 2025-08-13	Id: 9/84
Remarks: Copyright (c) 2025 by Filip Pynckels & Robin Pynckels		



Input - Tri-state (0V, -12V, floating)
Can be pulled up to +6V when short circuit on board under test

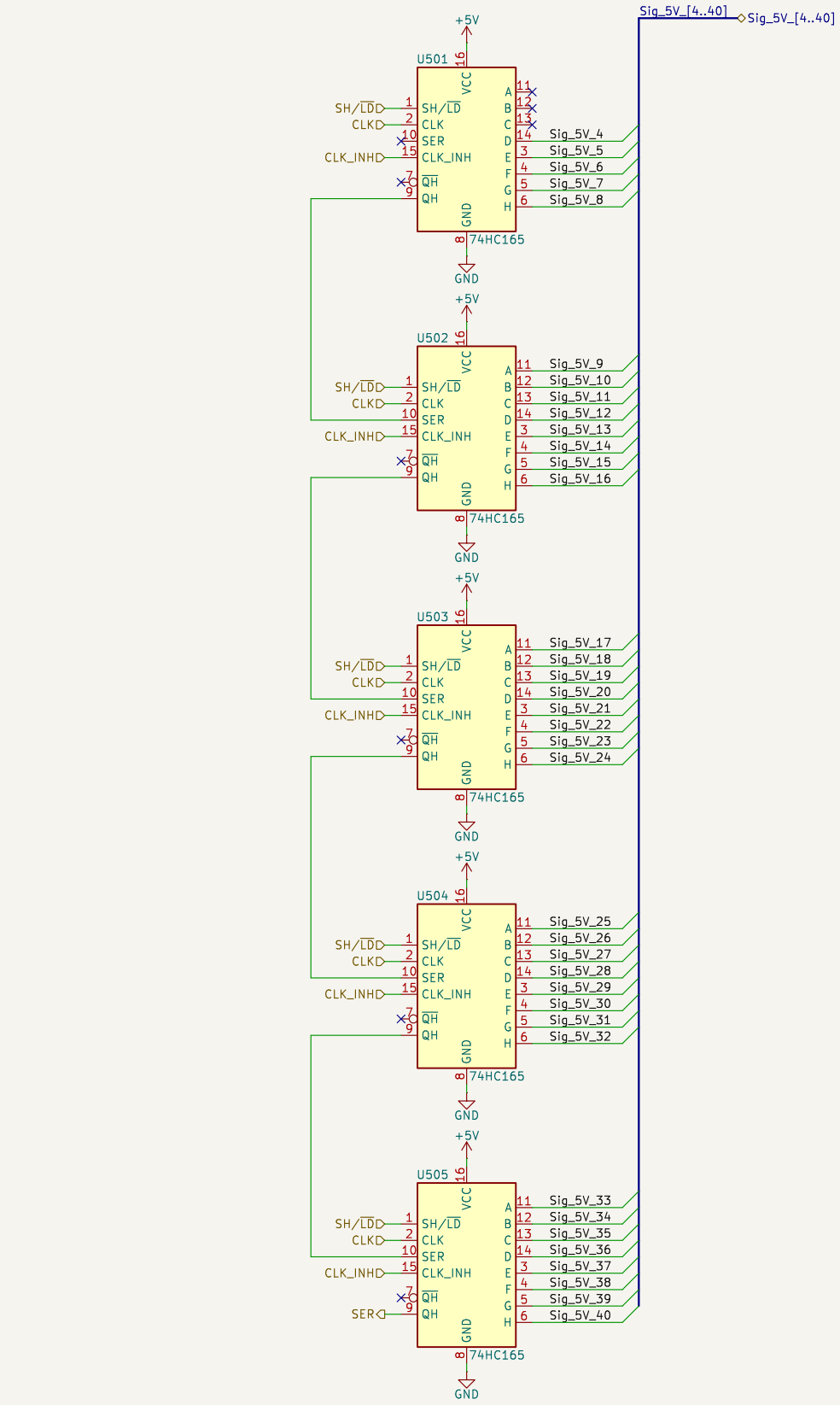
Output - 5V in case input is floating (due to open collector comparator and pull-up resistor)
GND in case input is not floating (due to current limited clamping diode)

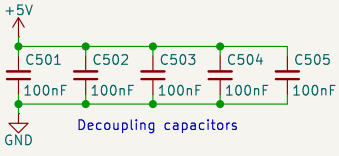
Title: VersaLogic board tester		
File: Window_Comparator.kicad_sch Sheet: /Floating Signal Tester/Window Comp 4/		
Rev: 1.0.alpha	Date: 2025-08-13	Id: 11/84
Remarks: Copyright (c) 2025 by Filip Pynckels & Robin Pynckels		




```
-------------------------------------------
--- Direction is 0 (input to controller) ---
-------------------------------------------

If DIR = 0V Then BOARD signal is
                    * scaled from [-12V~true, 0V~false] to [0V~false, 5V~true]
                    * routed to IN pin
                OUT signal is
                    * blocked

-----------------------------------------------
--- Direction is 1 (output from controller) ---
-----------------------------------------------

IF DIR = 5V Then BOARD signal is
                    * blocked
                OUT signal is
                    * scaled from [0V~false, 5V~true] to [-12V~true, 0V~false]
                    * routed to BOARD pin
```

Title: VersaLogic board tester		
File: Setter_Getter.kicad_sch Sheet: /Signal Setter-Getter/Setter-Getter 4/		
Rev: 1.0.alpha	Date: 2025-08-13	Id: 48/84
Remarks: Copyright (c) 2025 by Filip Pynckels & Robin Pynckels		





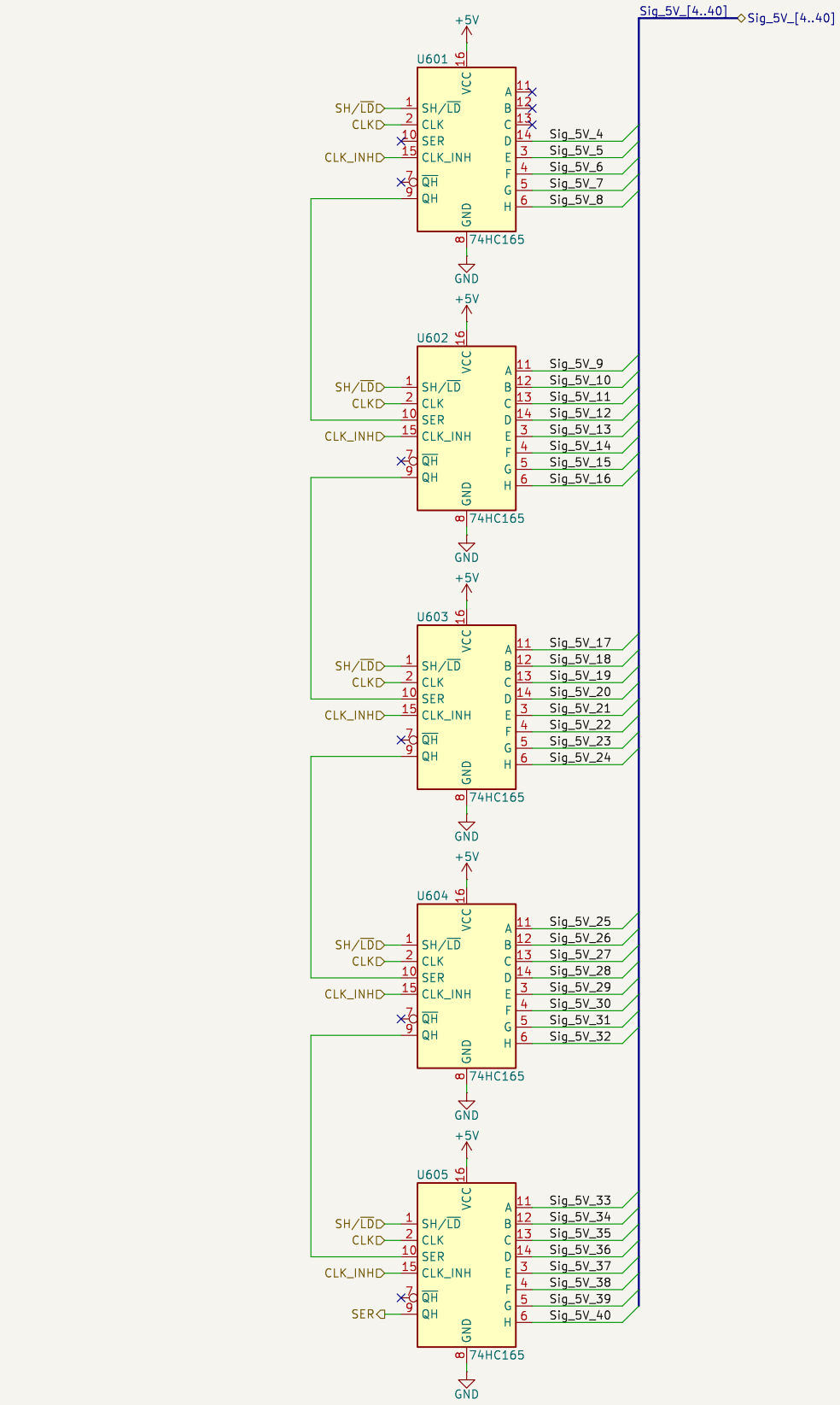
Input - Parallel input (TTL logic) on digital bus (5V, 0V)
Output - Serial output to controller

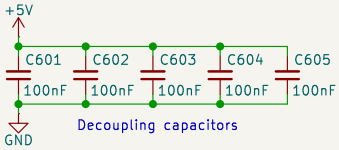
All control signals are broken out to the controller to give the program maximal options to alter the functioning of the hardware.

Title: VersaLogic board tester

File: Shift_In.kicad_sch
Sheet: /Shift-in Floating/

Rev: 1.0.alpha | Date: 2025-08-13 | Id: 5/84





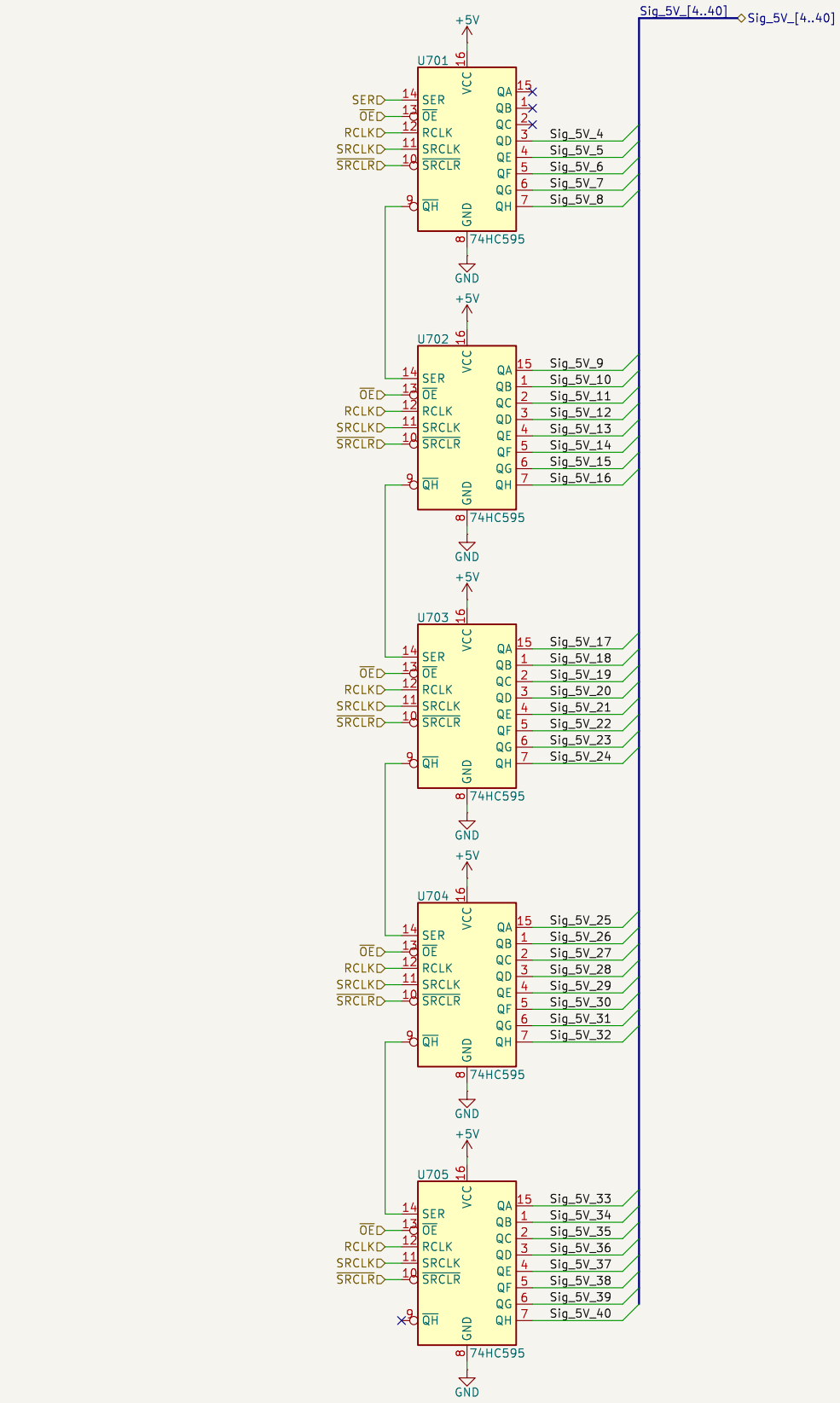
Input - Parallel input (TTL logic) on digital bus (5V, 0V)
Output - Serial output to controller

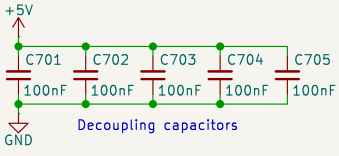
All control signals are broken out to the controller to give the program maximal options to alter the functioning of the hardware.

Title: VersaLogic board tester

File: Shift_In.kicad_sch
Sheet: /Shift-in Signal/

Rev: 1.0.alpha | Date: 2025-08-13 | Id: 6/84





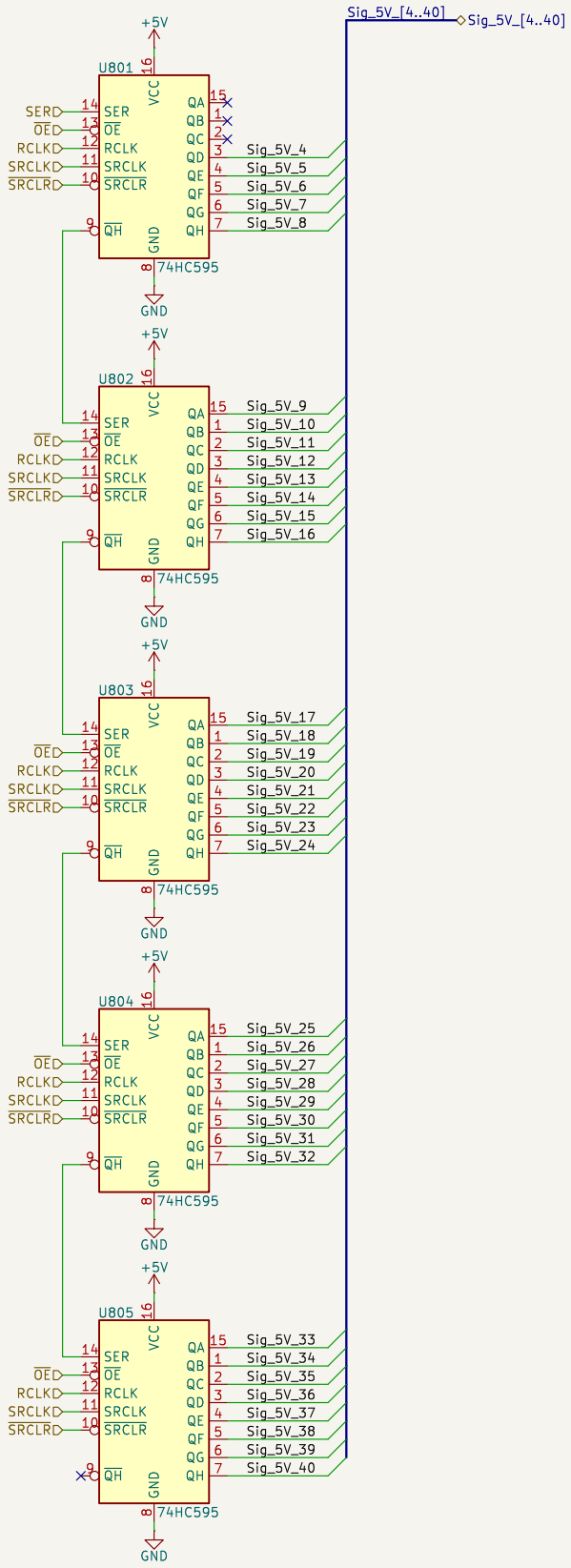
Input - Serial input from controller
Output - Parallel output (TTL logic) on digital bus (5V, 0V)

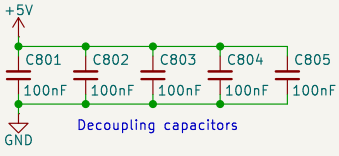
All control signals are broken out to the controller to give the program maximal options to alter the functioning of the hardware.

Title: VersaLogic board tester

File: Shift_Out.kicad_sch
Sheet: /Direction/

Rev: 1.0.alpha | Date: 2025-08-13 | Id: 7/84





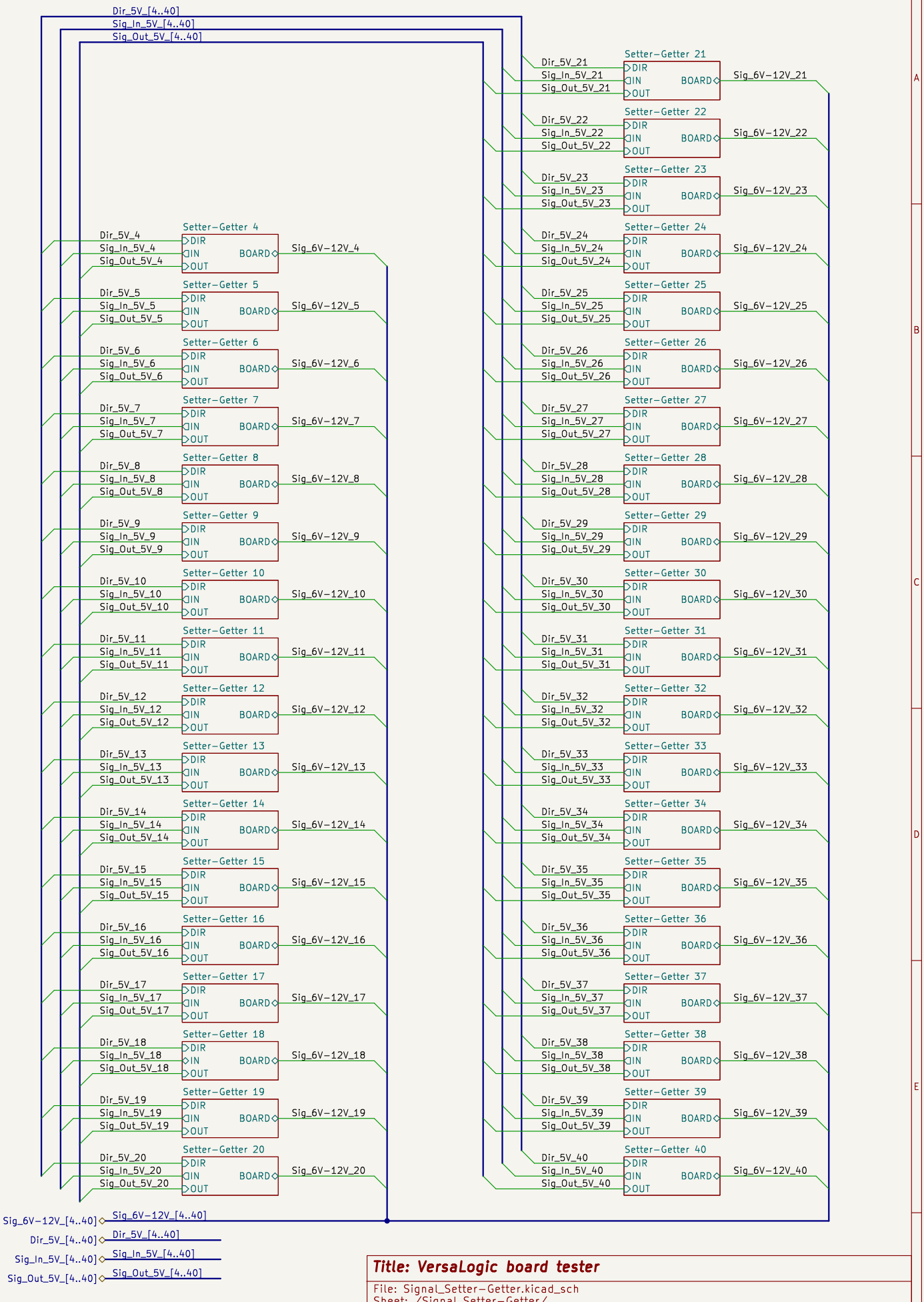
Input - Serial input from controller
Output - Parallel output (TTL logic) on digital bus (5V, 0V)

All control signals are broken out to the controller to give the program maximal options to alter the functioning of the hardware.

Title: VersaLogic board tester

File: Shift_Out.kicad_sch
Sheet: /Shift-out Signal/

Rev: 1.0.alpha | Date: 2025-08-13 | Id: 8/84



Title: VersaLogic board tester

File: Signal_Setter-Getter.kicad_sch
Sheet: /Signal Setter-Getter/

Rev: 1.0.alpha | Date: 2025-08-13 | Id: 10/84