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LIST OF PARTS

Inputs

- Clock – 1 bit, the clock feeds into the clock inputs for our adder/subtractor.
- Input – 32 bits, binary integer for A input.
- Input – 32 bits, binary integer for B input.
- OpCode – 4 bits, binary code to indicate operation.
- Carry-In – 1 bit, binary integer for our adder/subtractor.

Outputs

- Error – 1 bit, true if an error state has occurred.
- Carry-Out – 1 bit, binary integer which conveys the carry result from the adder/subtractor.
- Value – 32 bits, the current output of the ALU.

Interfaces

- ACC.D, 32-bits, the next value into the register.
- ACC.Q, 32-bits, the current value from the register.
- FullAdder.A, 32-bits, takes its value of Input A.
- FullAdder.B, 32-bits, takes in the value of the Input B.
- FullAdder.Cin, 32 bits, the last carry, used for the Error Check.
- FullAdder.Cout, 32 bits, the last carry, used for the Error Check.
- FullAdder.Sum, 32 bits, the actual sum, feeds into CH6 for addition and CH8 for subtraction.
- Greater_Than,32 bits take the value of Input A & B
- Less_Than,32 bits take the value of Input A & B
- Equal,32 bits take the value of Input A & B
- Multiplexer.b, 32 bits, output of the multiplexer into ACC.
- Multiplexer.Ch0, 32 bits, feedback for the current value of ACC into multiplexer
- Multiplexer.Ch1, 32 bits, feedback for the current value of ACC into Reset
- Multiplexer.Ch3, 32 bits, results of OR into the multiplexer.
- Multiplexer.Ch5, 32 bits, results of AND into the multiplexer.
- Multiplexer.Ch12, 32 bits, results of Greater_Than into the multiplexer.
- Multiplexer.Ch13, 32 bits, results of Equal into the multiplexer.
- Multiplexer.Ch14, 32 bits, results of Less_Than into the multiplexer**.**
- Multiplexer.Ch15, 32 bits, results of Error check into the multiplexer.
- Multiplexer.Ch2, Ch4 Ch7, Ch9, Ch10 Ch11-32bit channels, unused.
- Multiplexer.S, 4-bits, the one-hot control into the multiplexer (opcodes)

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Gates

- AND gate, 32-bits, both channels are used for the inputs A and B
- OR gate, 32-bits, both channels are used for the inputs A and B
- XOR gate, 1 bit, one channel is the carry-in for our adder/subtractor, the other is the carry-out. Used to display the overflow.

Combinational Logic Components

- Multiplexer, 16 channel, 32-bit multiplexer for result operation
- Adder/Subtractor, 32-bit, performs add or subtract operation on inputs A and B.
- Comparator, 32-bit, performs less than, equals, and greater than operations on inputs A and B

Sequential Logic Components

- ACC, 32-bit register that contains the current result

Modules

- Test Bench – Main module, runs clock and stimulus. (not shown)
- Alu_32_bit – Module that combines the components for the ALU
- MUX_16_1_ V2 – Module that creates the 16 to 1 mux
- HA – half adder component for adder/subtractor
- FA – Full adder component for add/subtractor
- Adder_subtractor – module that puts together components for adder/subtractor
- AND_32b – module that creates the 32-bit AND gate
- OR_32b – module that creates the 32-bit OR gate
- EQ – module component for Equals module
- Equals – main module that performs equal to operation on two 32-bit inputs
- GT – module component for greaterthan module
- Greater_than – main module that performs greater_than operation on two 32-bit inputs
- GT 2x1 – 2 bit greater than module
- GT 4x1 – 4 bit greater than module
- LT_32B – main module that performs less than operation on two 32-bit inputs
- LT – module component for main Less than module
- LT_2b – 2 bit less than module
- Acc – module that creates the 32-bit register and decides when it is reset
- And_32x1 – helper modules for modules using 32-bit AND gates
- And_16x1 – 16 bit module component for and_32x1 module
- And_8x1 – 8 bit module component for and_32x1 module
- And_4x1 – 4 bit module component for and_32x1 module
- Or_32x1 – helper module for modules using 32-bit OR gates
- or_16x1 – 16 bit module component for or_32x1 module
- or_8x1 – 8 bit module component for or_32x1 module
- or_4x1 – 4 bit module component for or_32x1 module

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Op-Code Table

Command	Opcode	Description
No Operation	0000	System is idle, stays in ready state.
Add	0110	Perform an ADD operation (A + B)
Subtract	1000	Perform a Subtraction operation (A – B)
AND	0101	Perform an AND operation
OR	0011	Perform an OR operation
Less Than	1110	If (A < B) then return true otherwise False
Greater Than	1101	If (A > B) then return true otherwise False
Equal	1100	If (A = B) then return true otherwise False
Reset	1111	Overflow, Null, Invalid_Input

Modes of Operation

Mode	Opcode	Description
Ready	0000	System is idle
AND	0001	Performing an ADD operation
OR	0011	Performing an OR operation
ADD	0010	Performing an ADD operation
SUB	1000	Performing an SUB operation
ERR	1111	An error has occurred, and will not return to ready until reset

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State Table

Current State	Command	Next state
ADD	No-Op, Reset	Ready
AND	No-Op, Reset	Ready
OR	Reset	Ready
Greater_Than	Reset	Ready
Less_Than	Reset	Ready
Equal	Reset	Ready
SUB	No-Op, Reset	Ready
Error	Reset	Ready
Ready	And	AND
Ready	Subtract	SUB
Ready	Add	ADD

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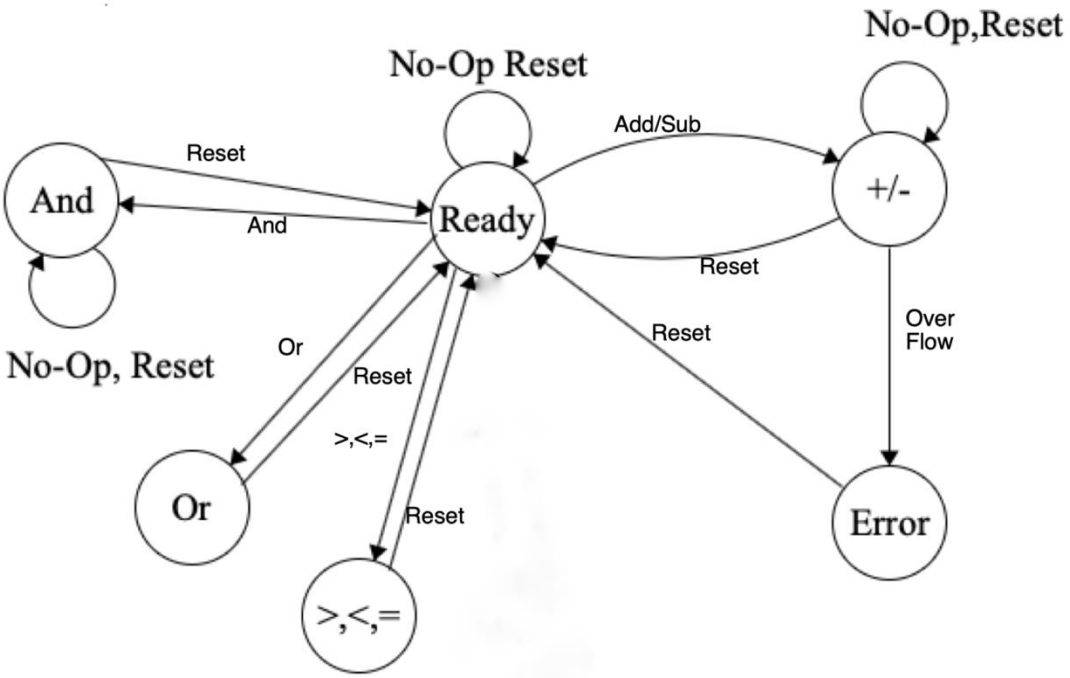
State Machine



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Circuit Diagram