TESS Focal Plane Electronics Manual

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Very Preliminary Edition

Commit 00a421e
Tag FPE-6.1-RR1

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The TESS Focal Plane Electronics (FPE) serve as the intermediary between the CCD sensors on a focal plane and the Data Handling Unit (DHU).

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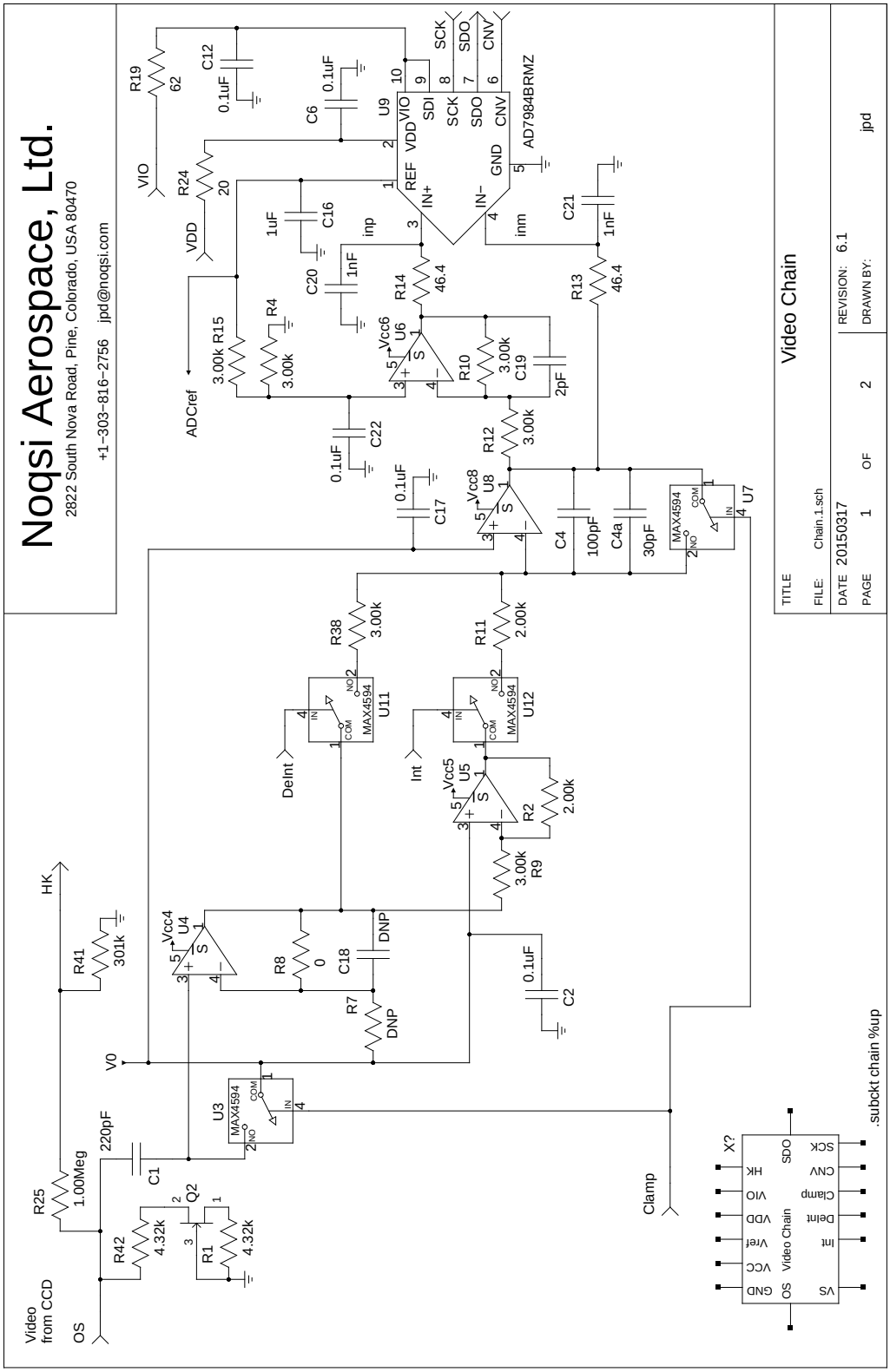

Figure 1: Chain.1

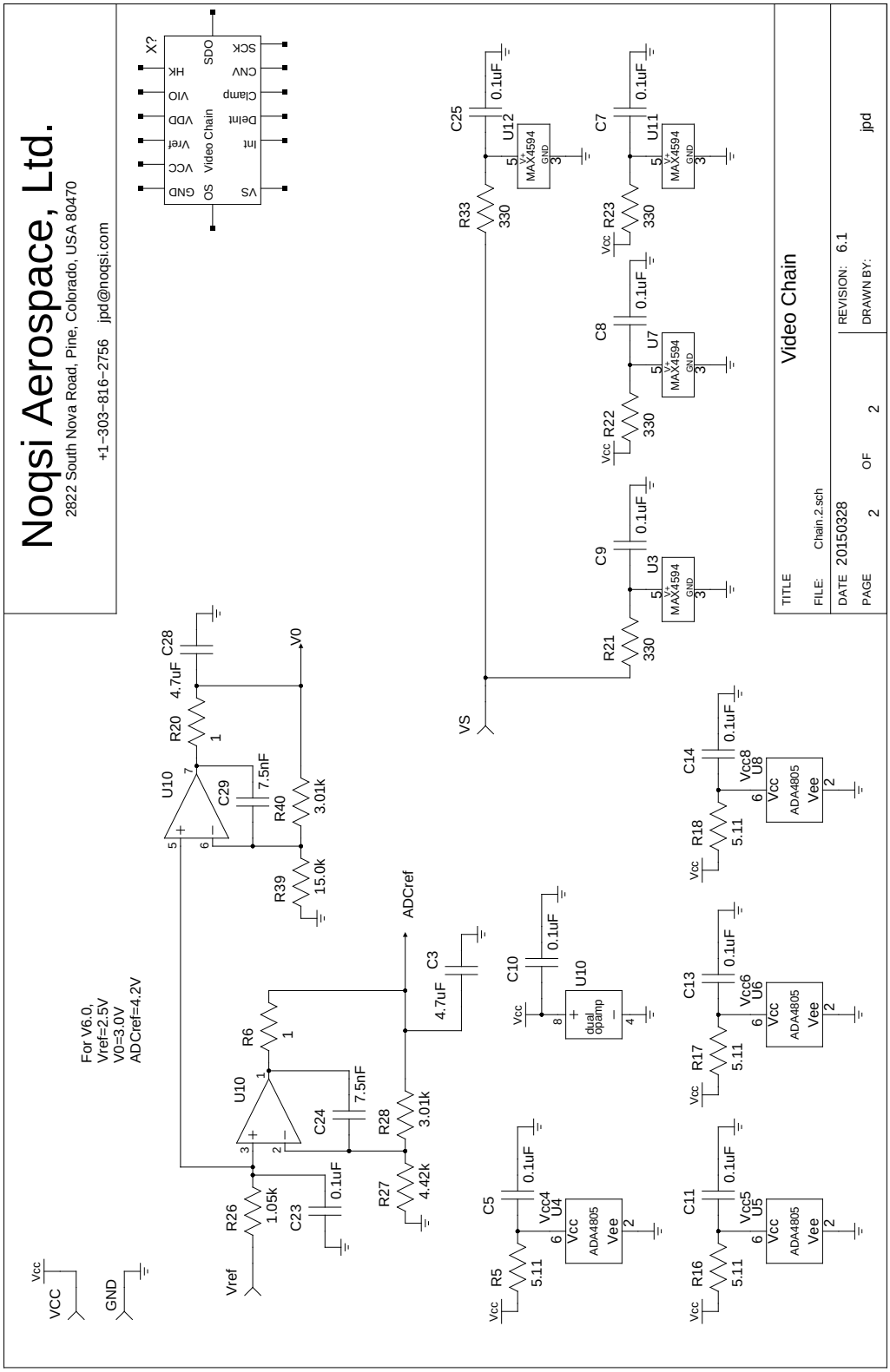

Figure 2: Chain.2

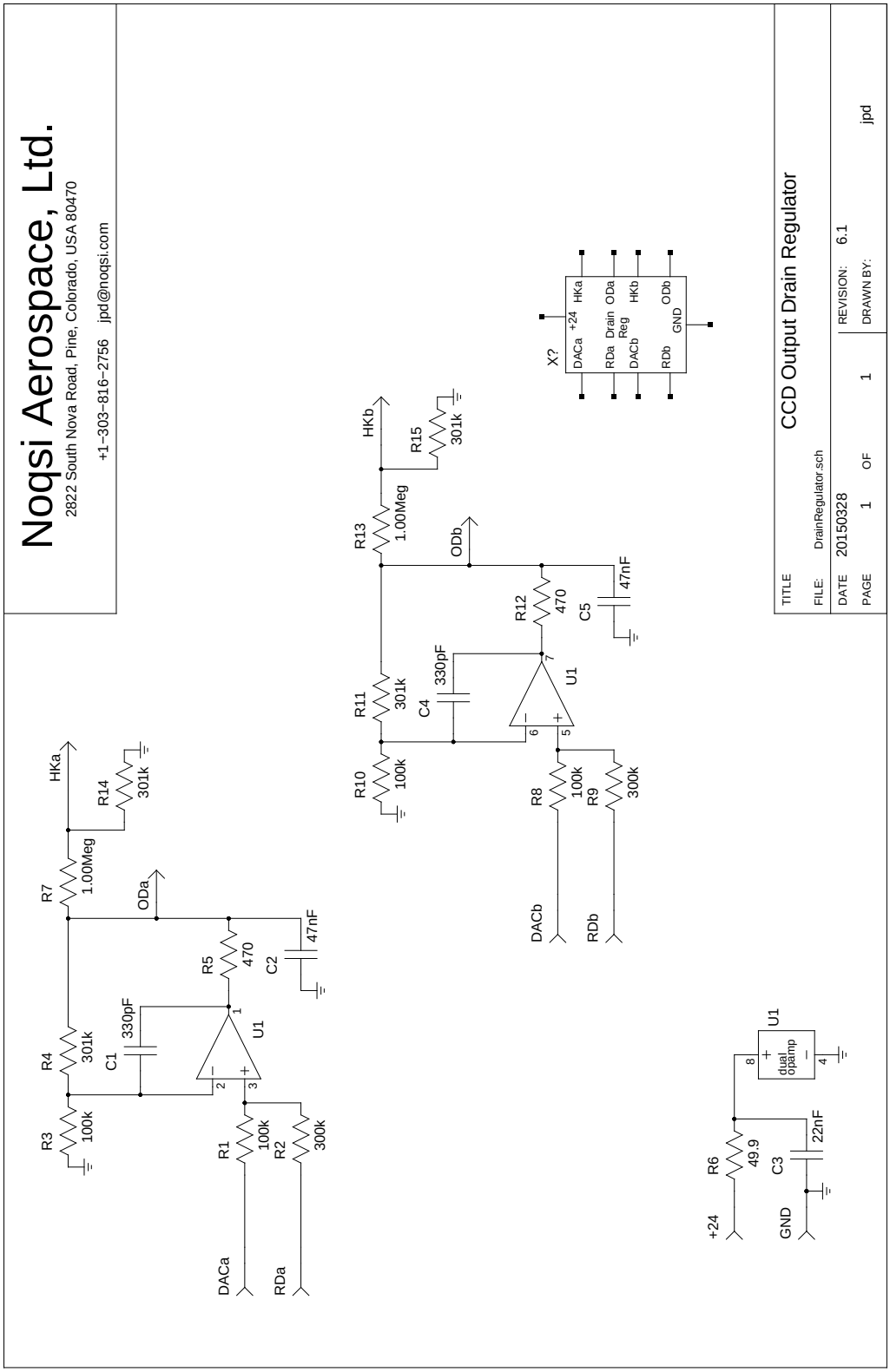

Figure 3: DrainRegulator

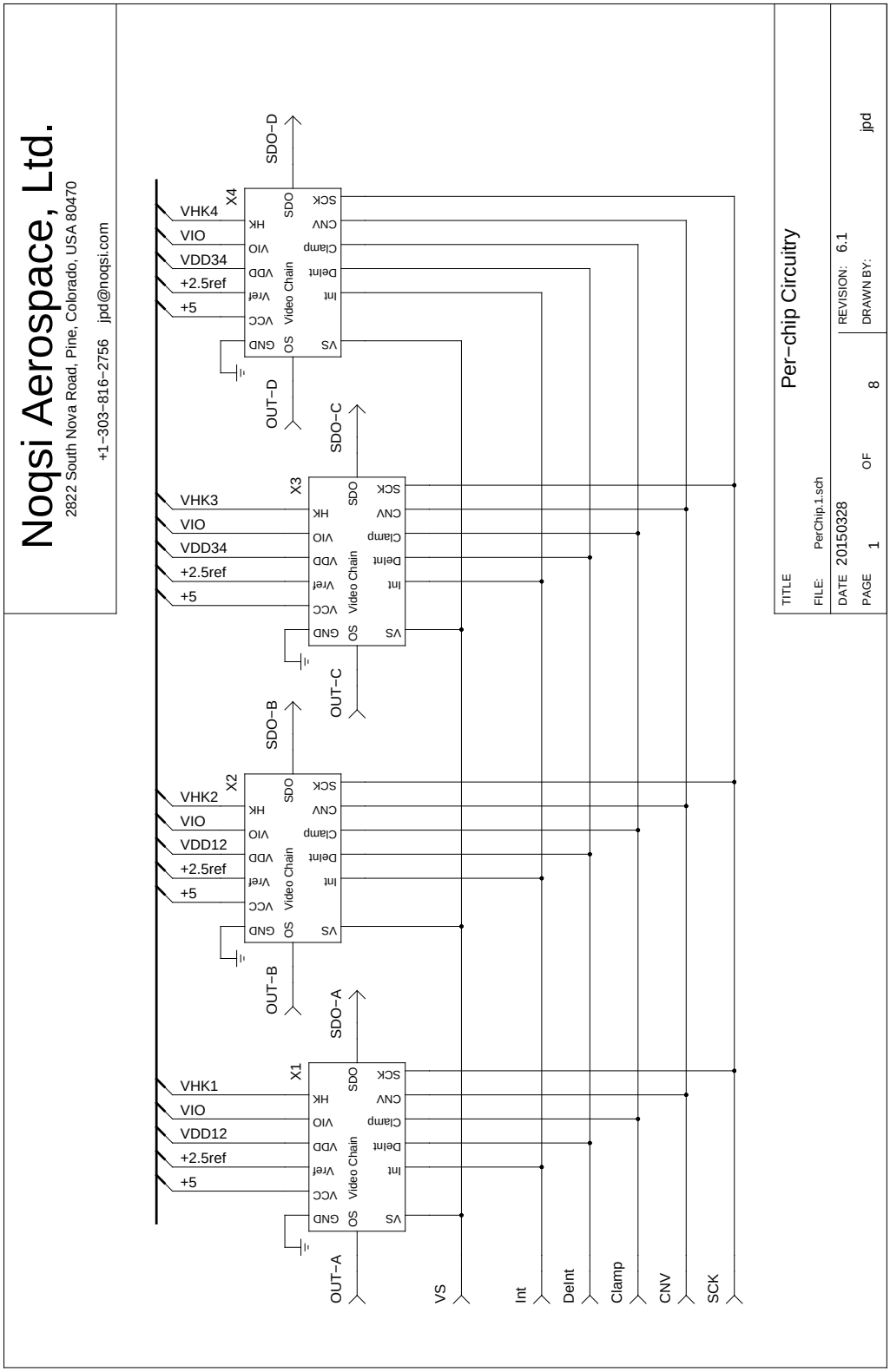

Figure 4: PerChip.1

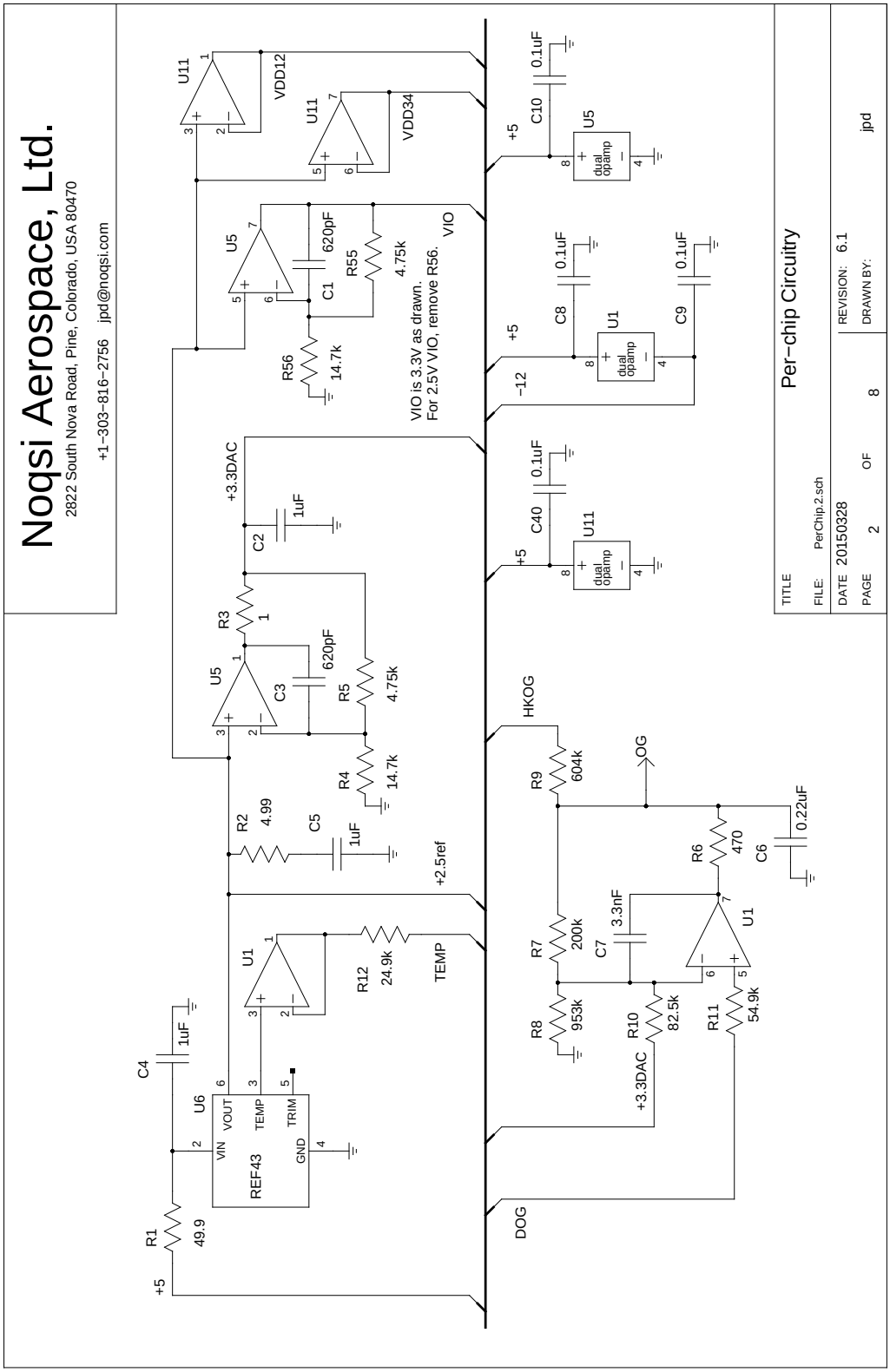

Figure 5: PerChip.2

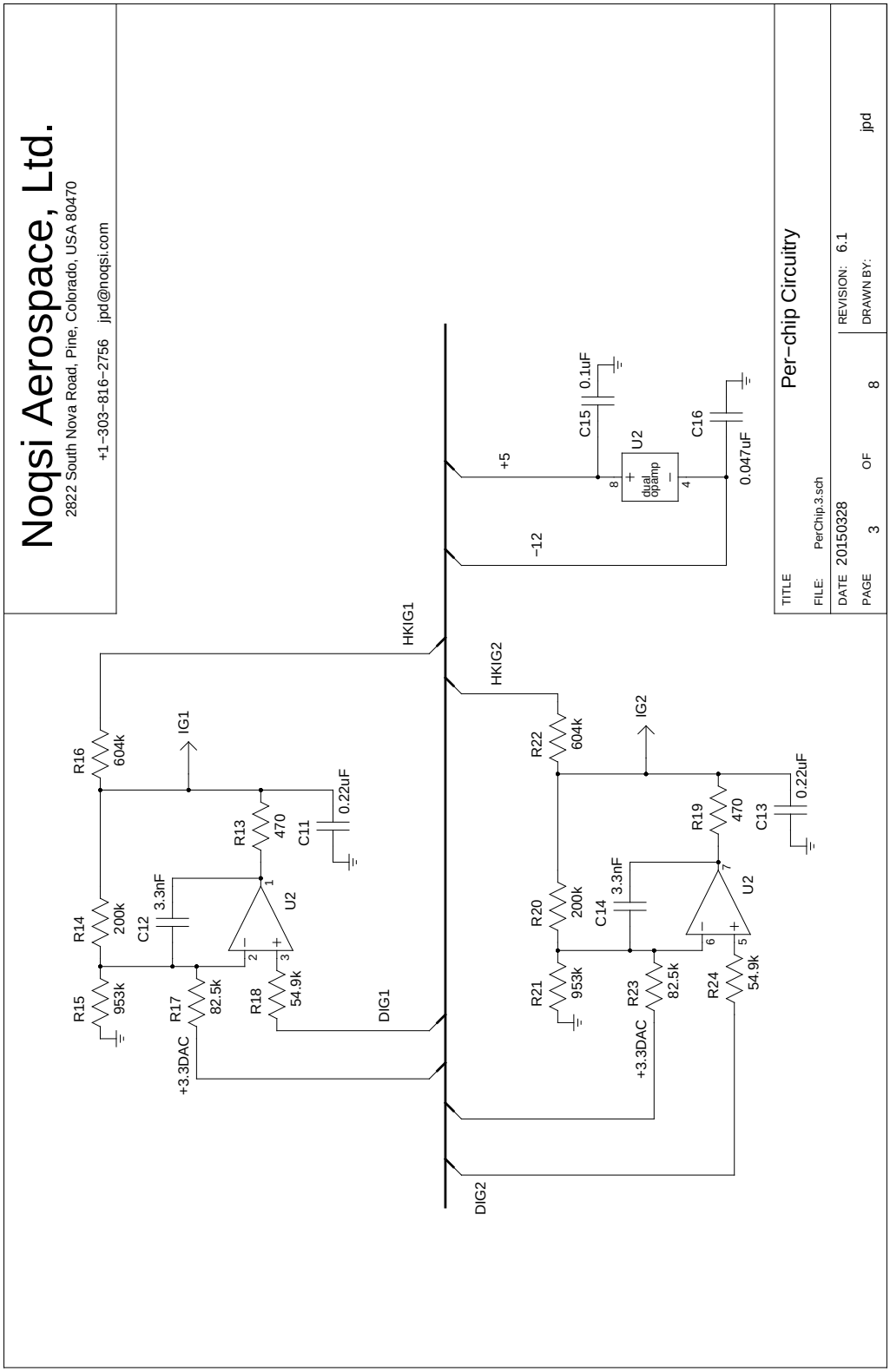

Figure 6: PerChip.3

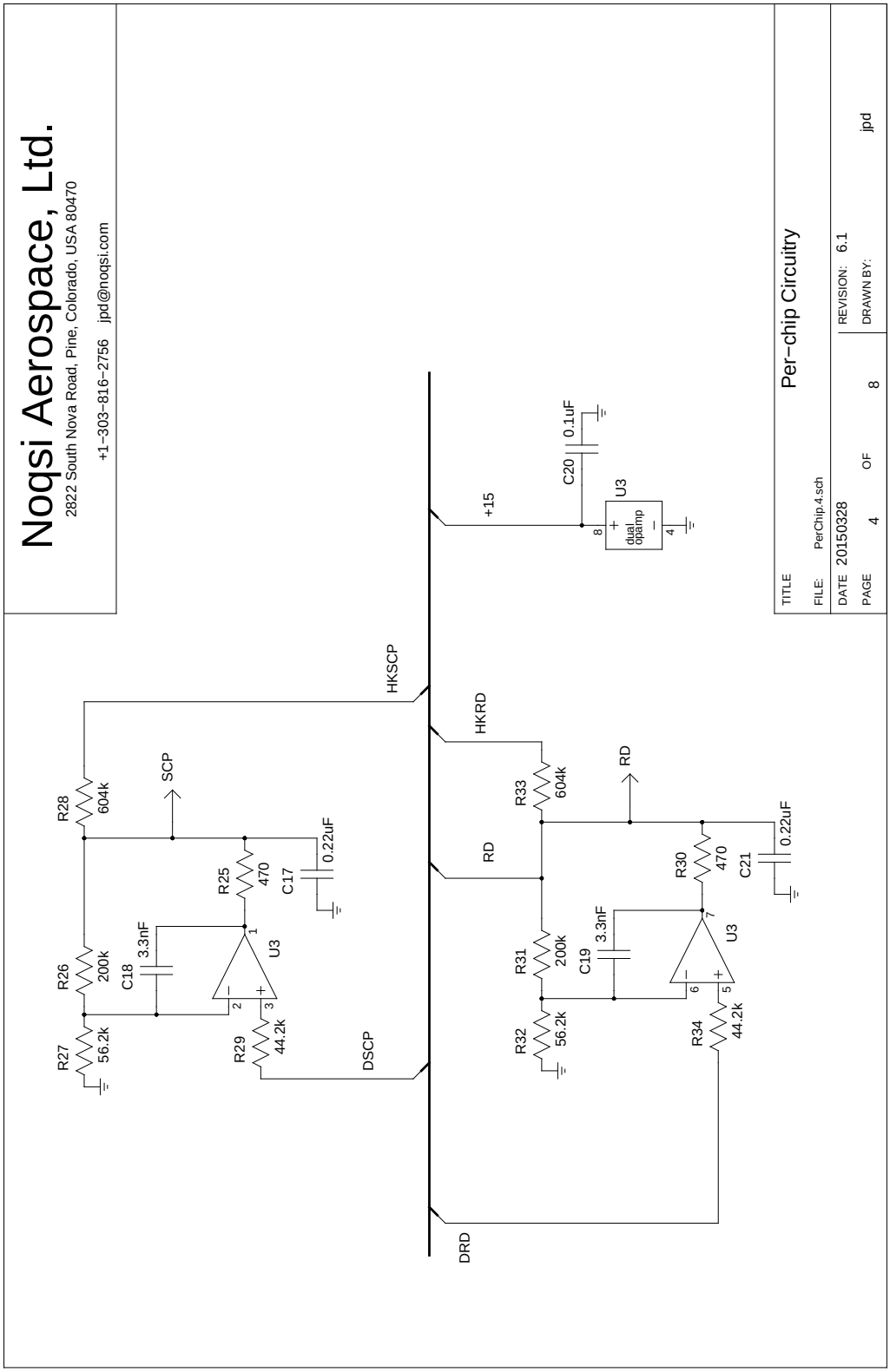

Figure 7: PerChip.4

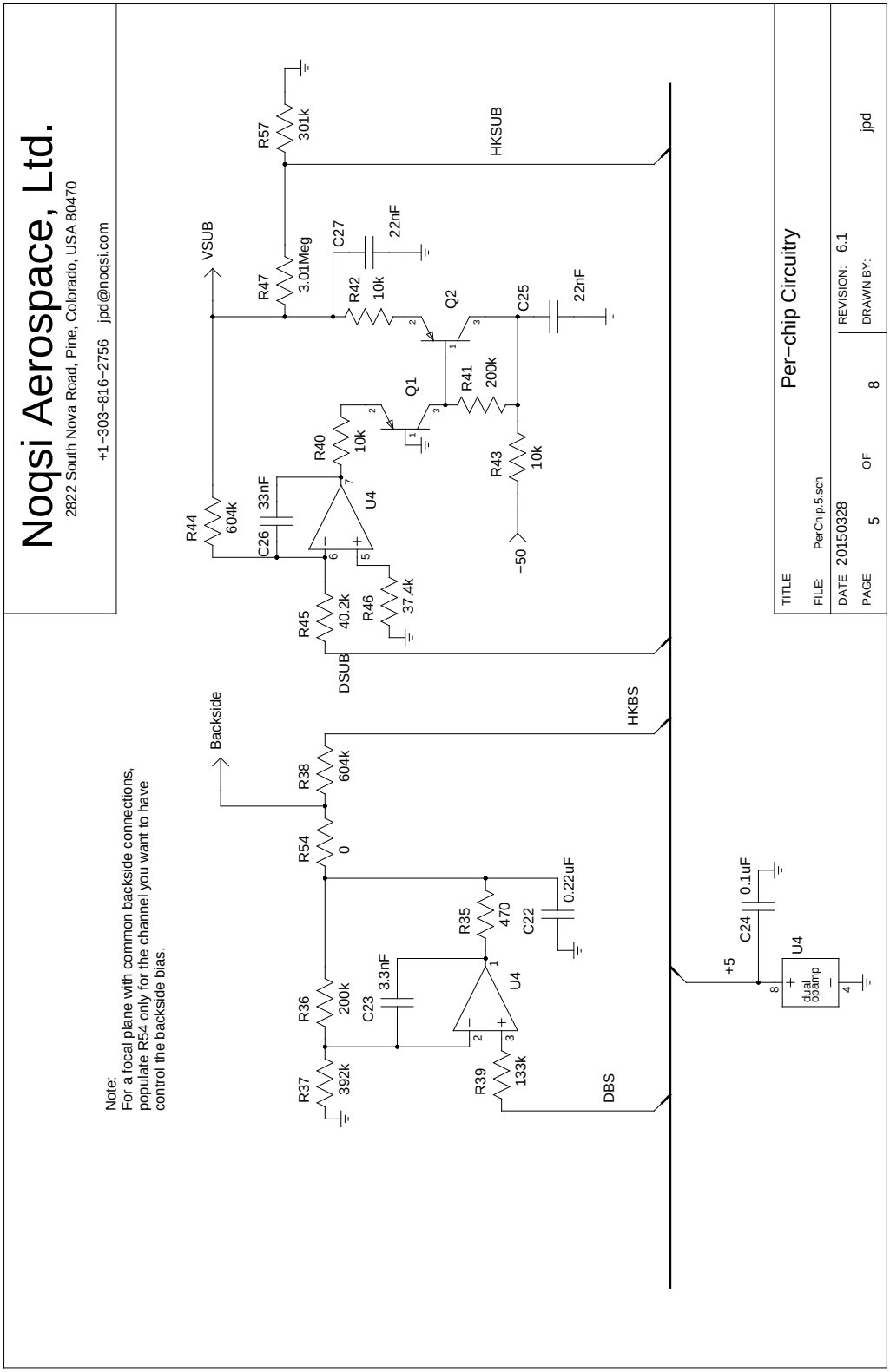

Figure 8: PerChip.5

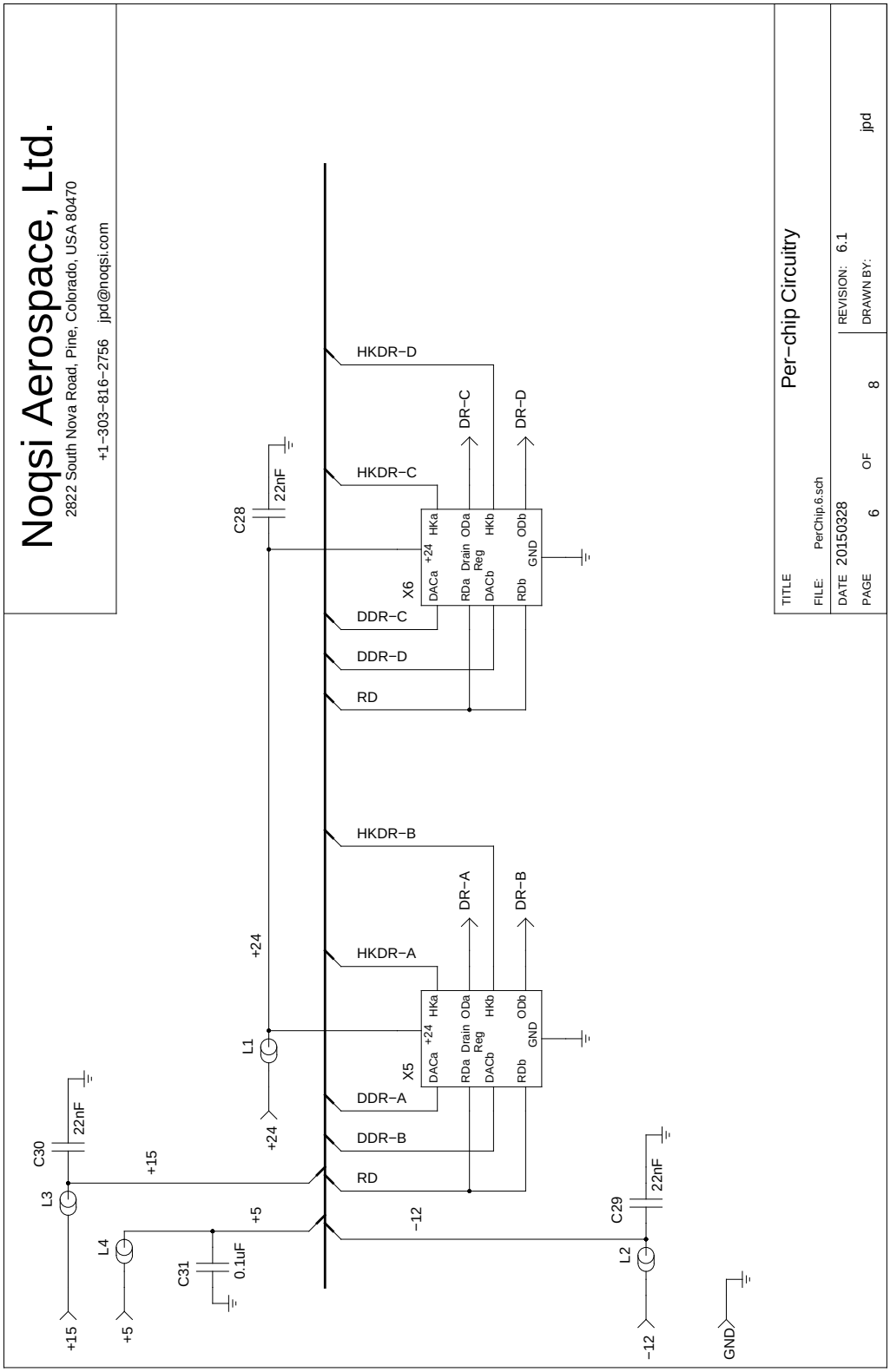

Figure 9: PerChip.6

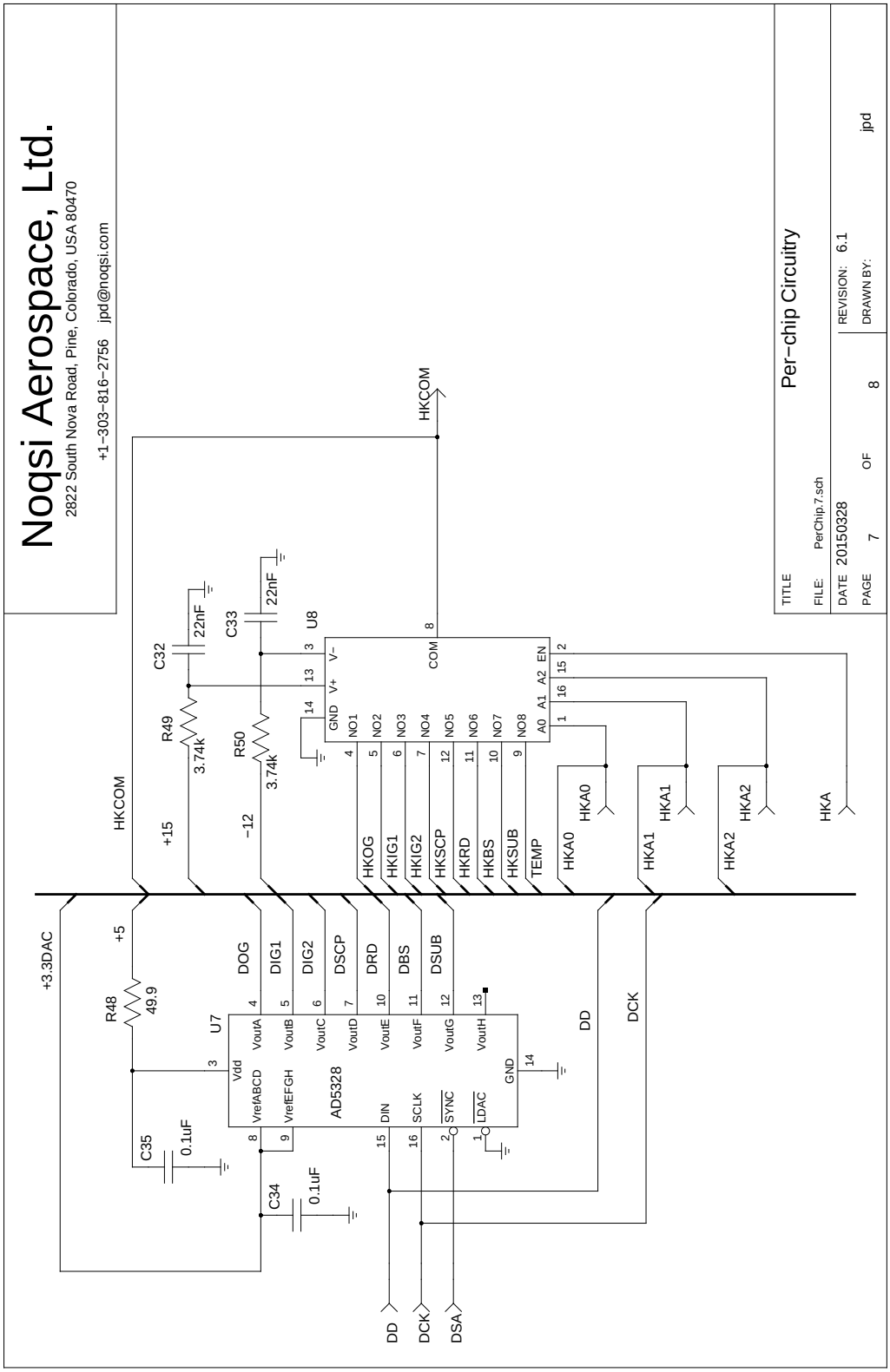

Figure 10: PerChip.7

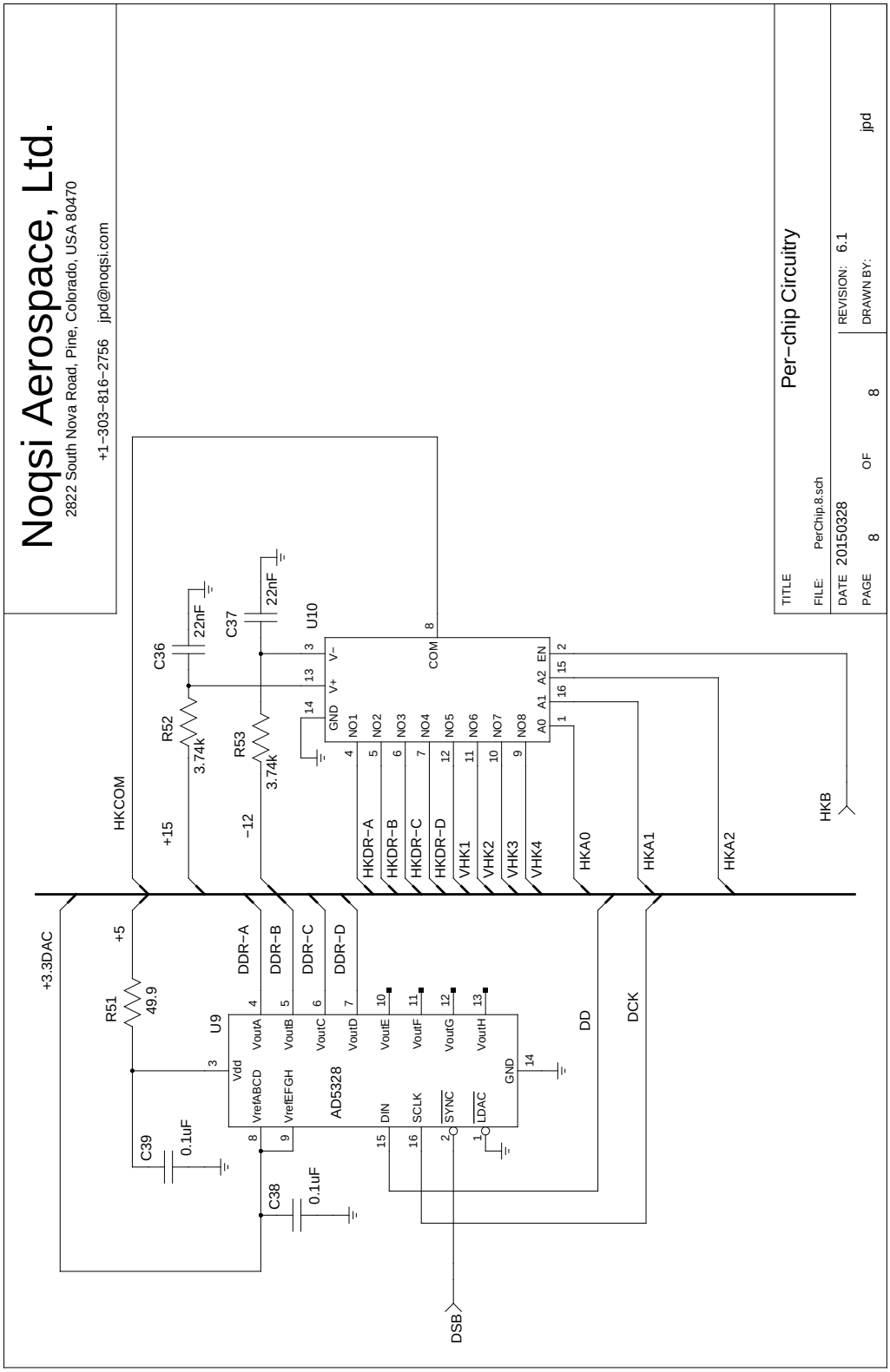

Figure 11: PerChip.8

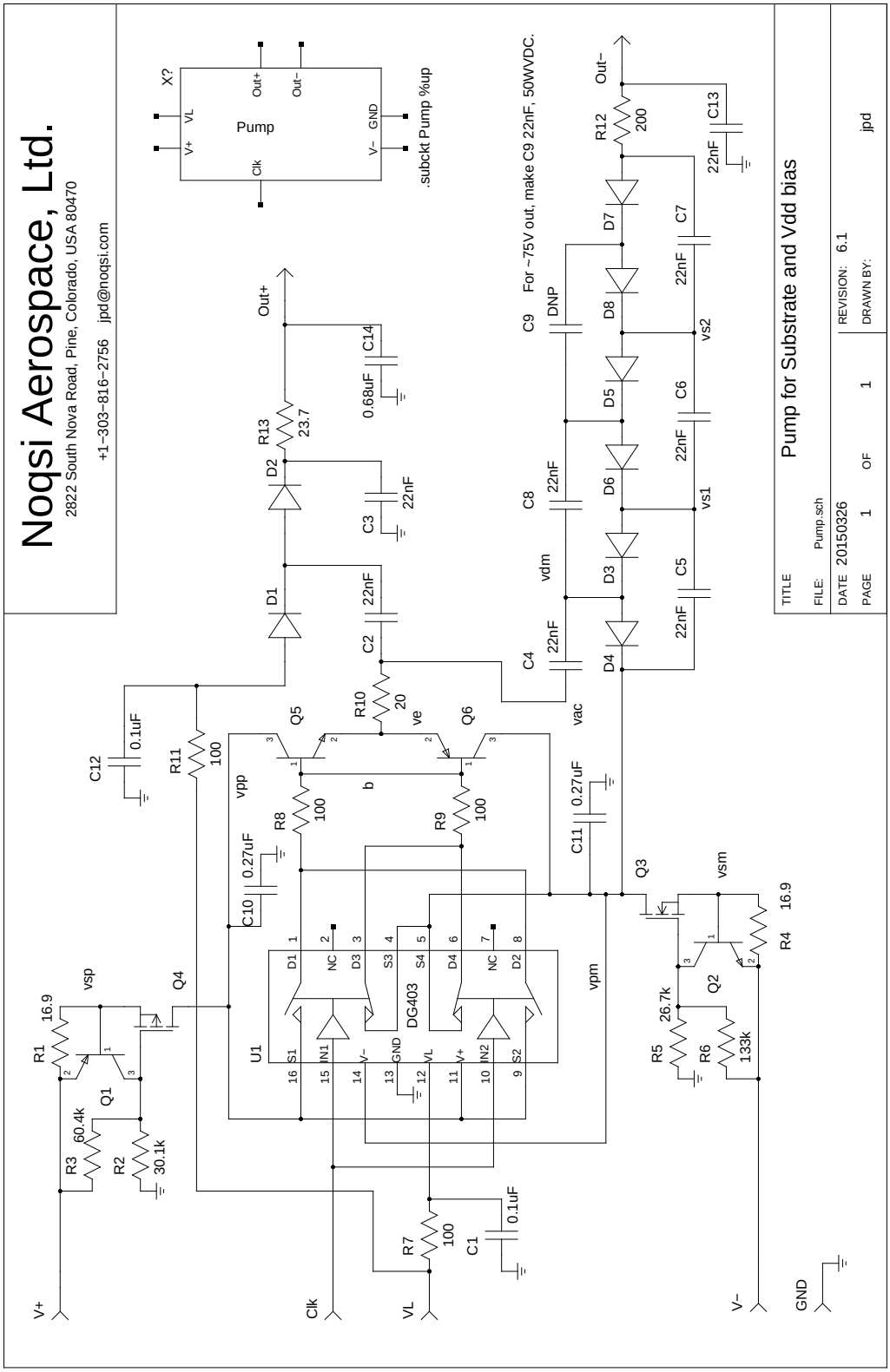

Figure 12: Pump

2.2 Video Board Top Level

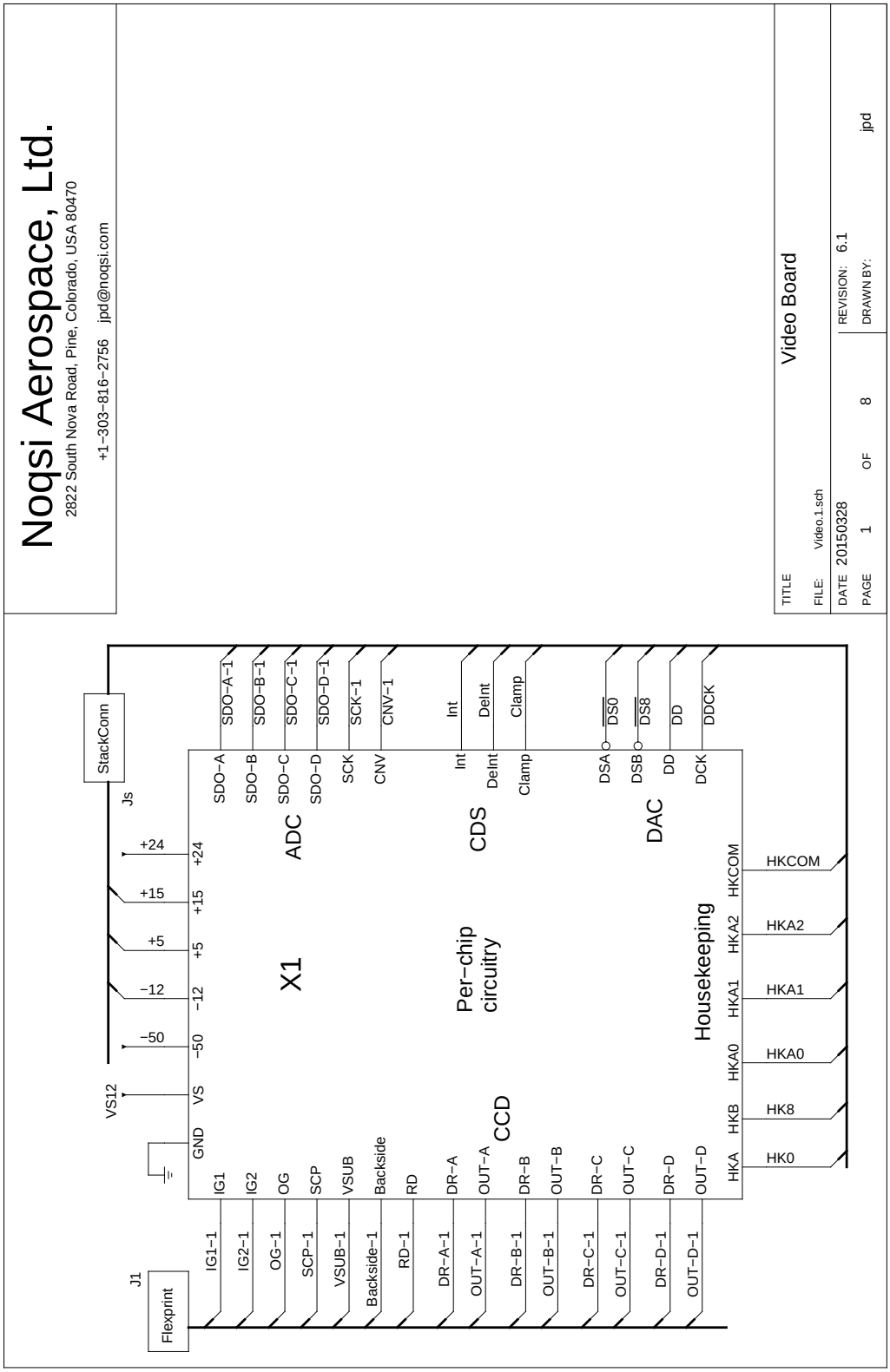

Figure 13: Video.1

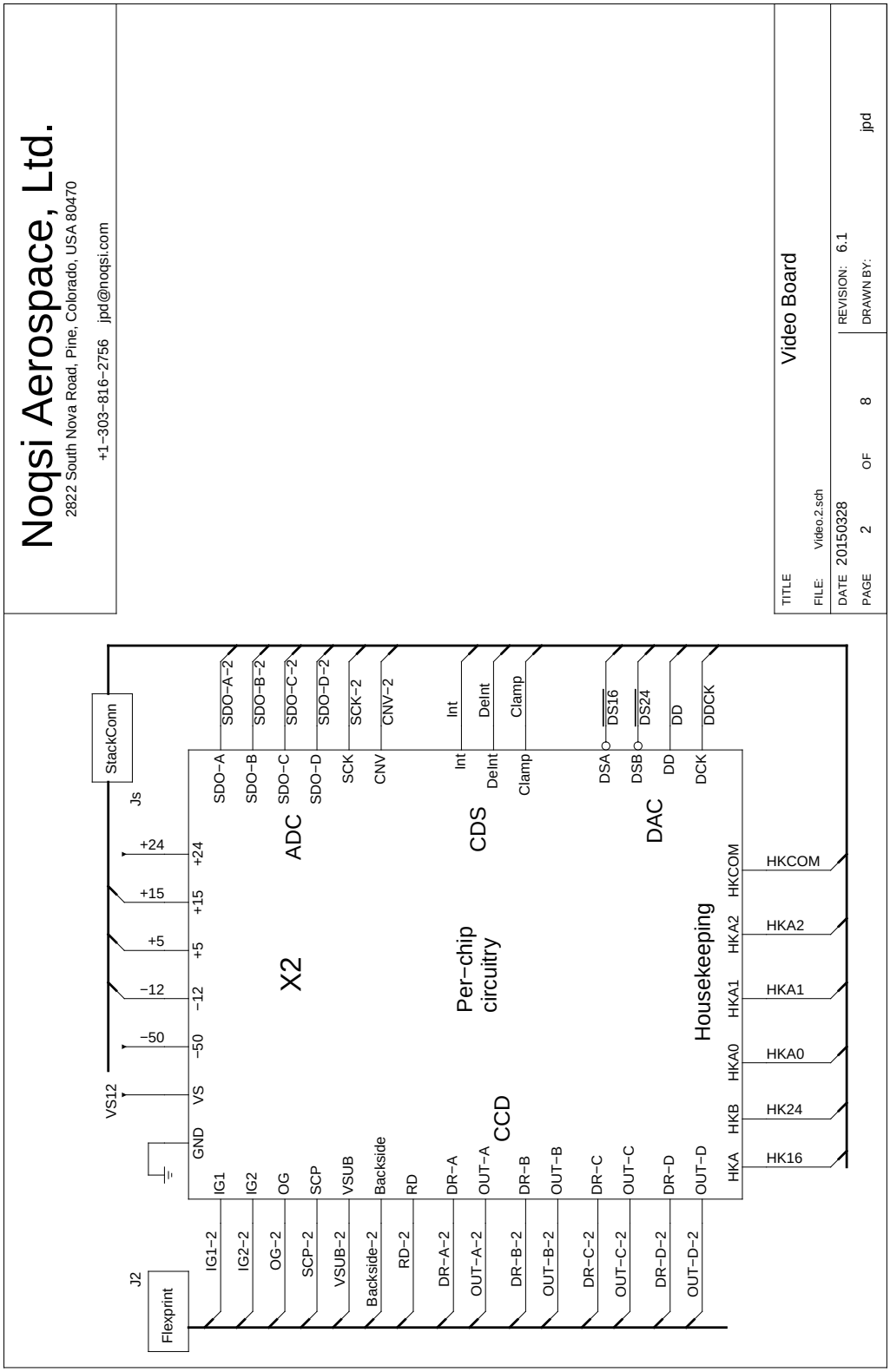

Figure 14: Video.2

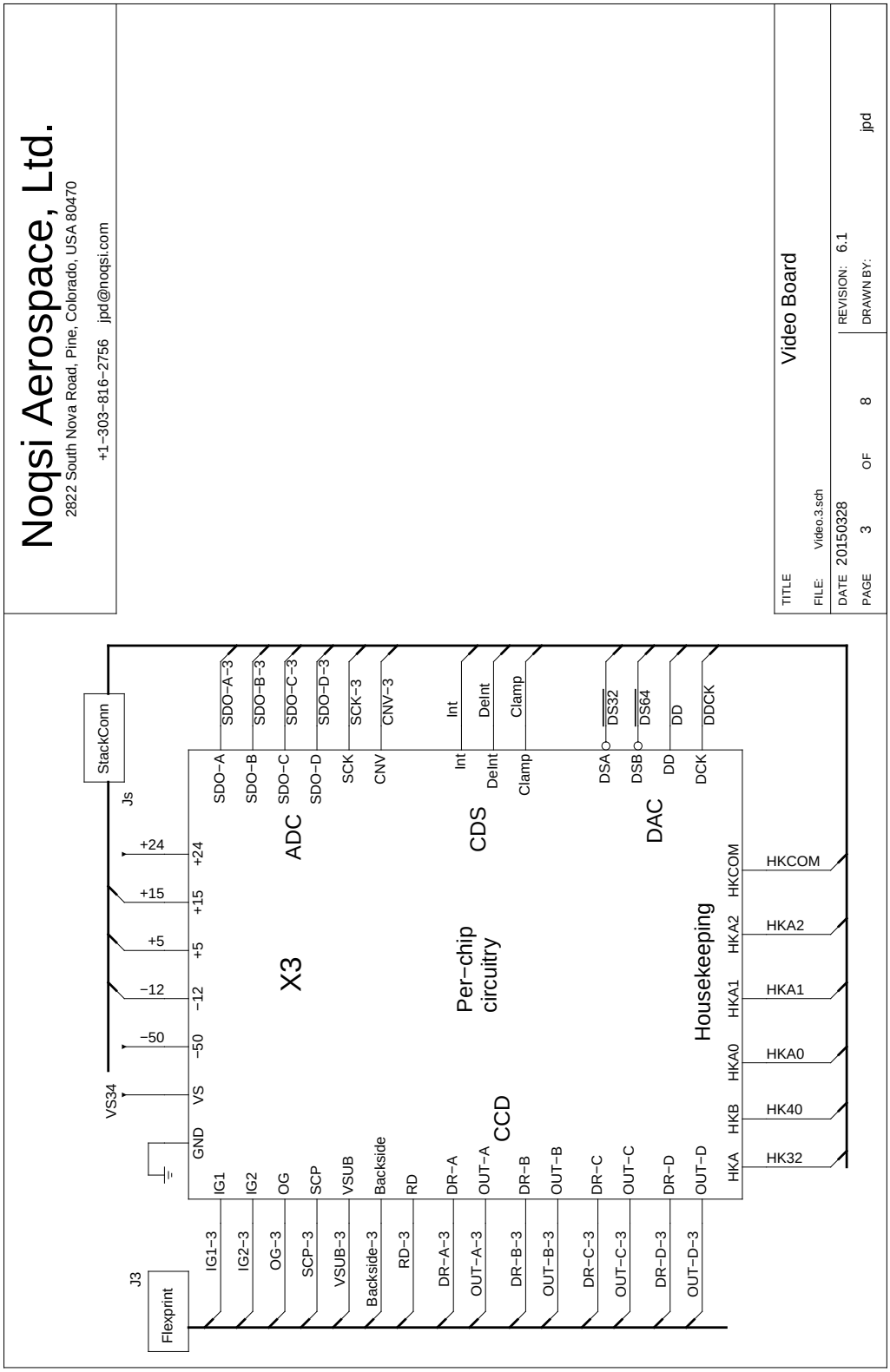

Figure 15: Video.3

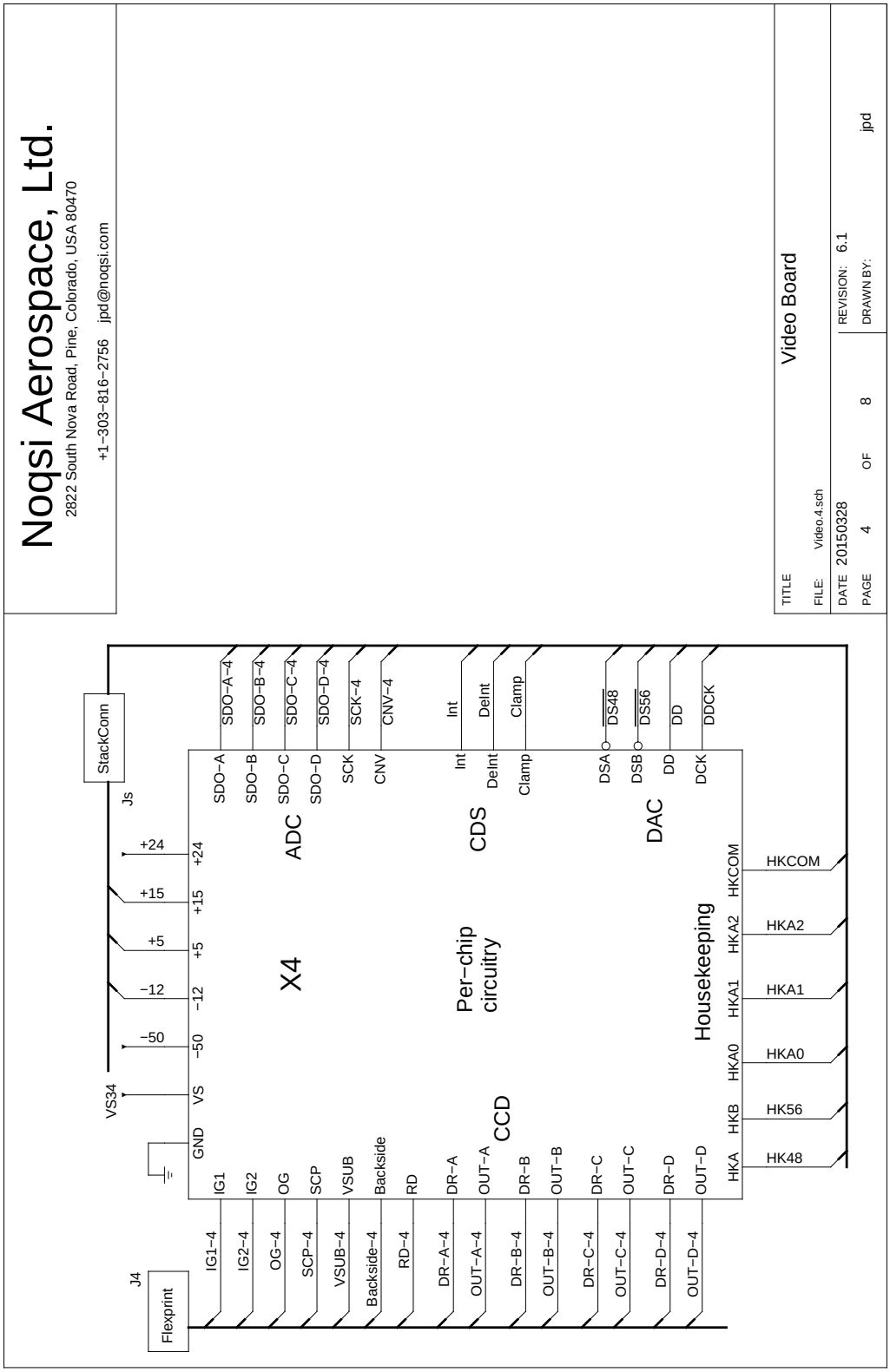

Figure 16: Video.4

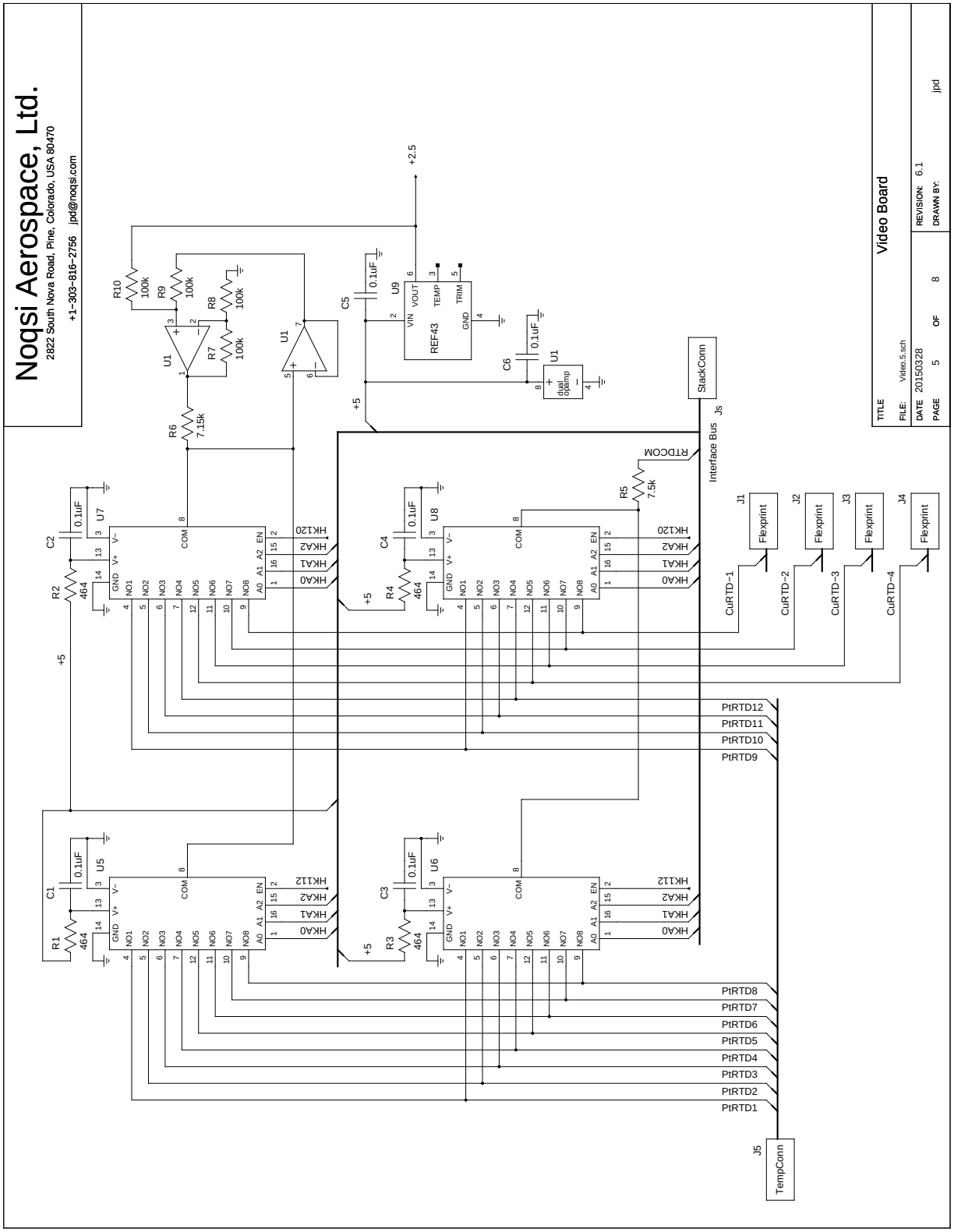

Figure 17: Video.5

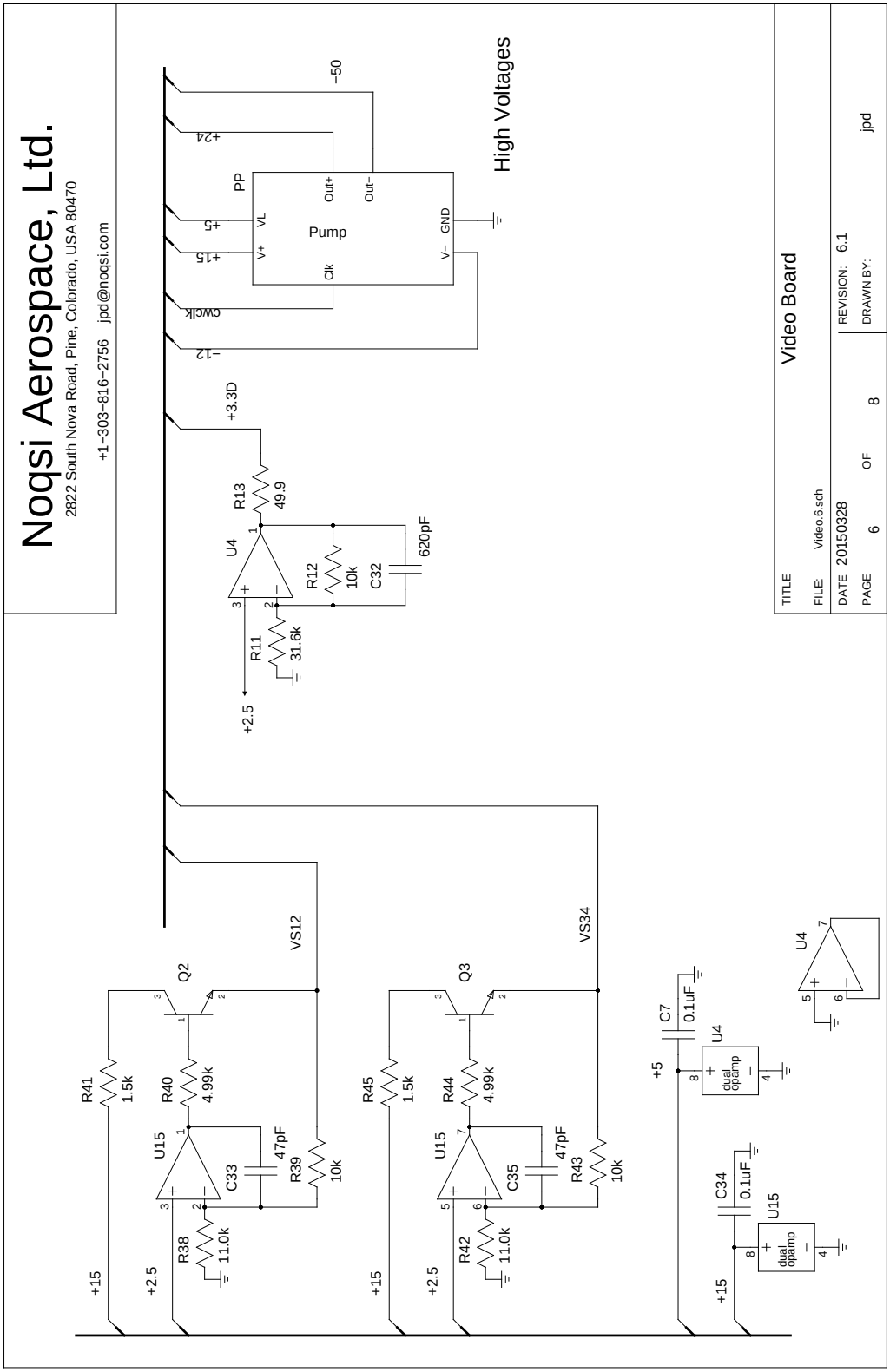

Figure 18: Video.6

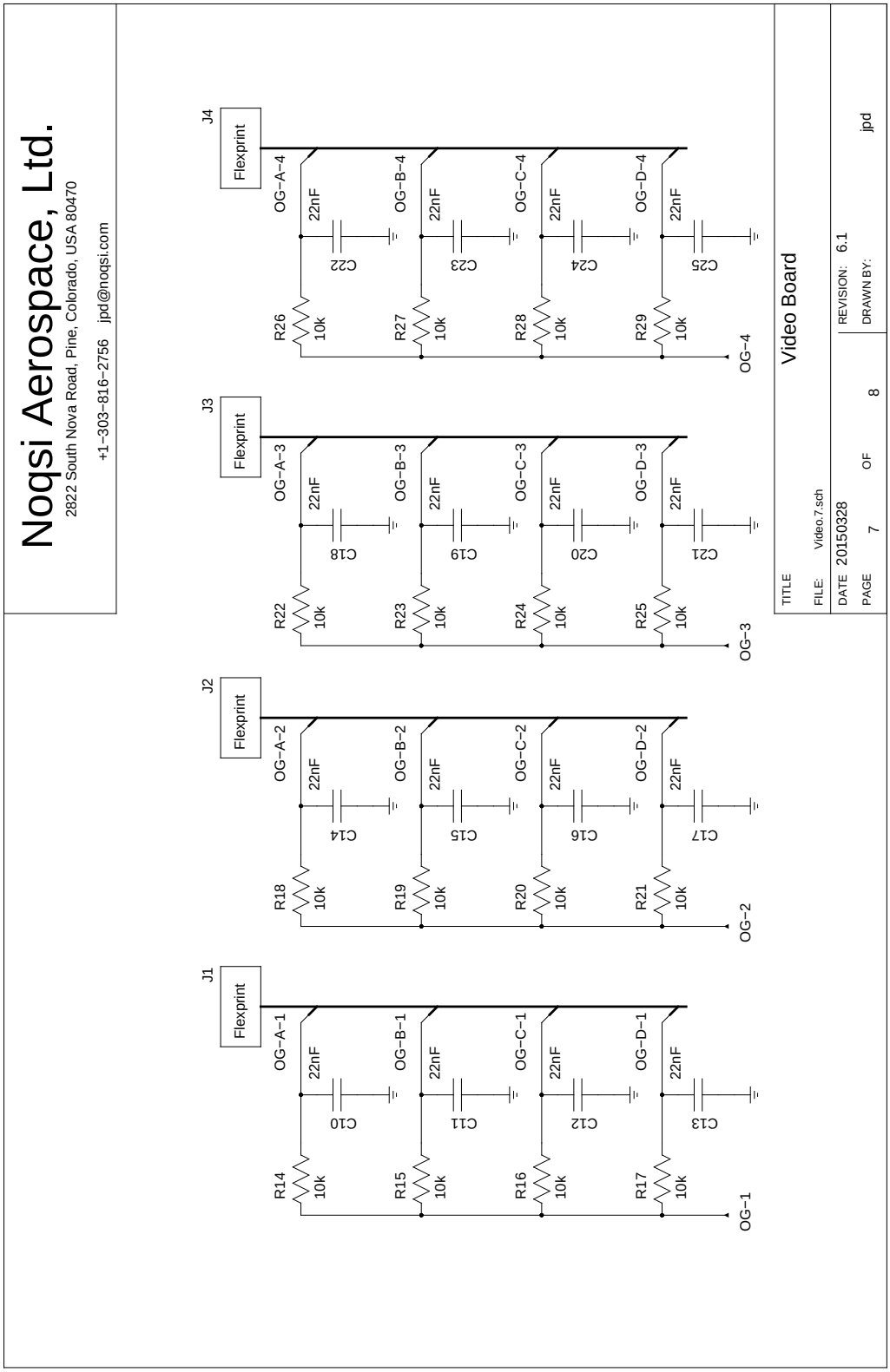

Figure 19: Video.7

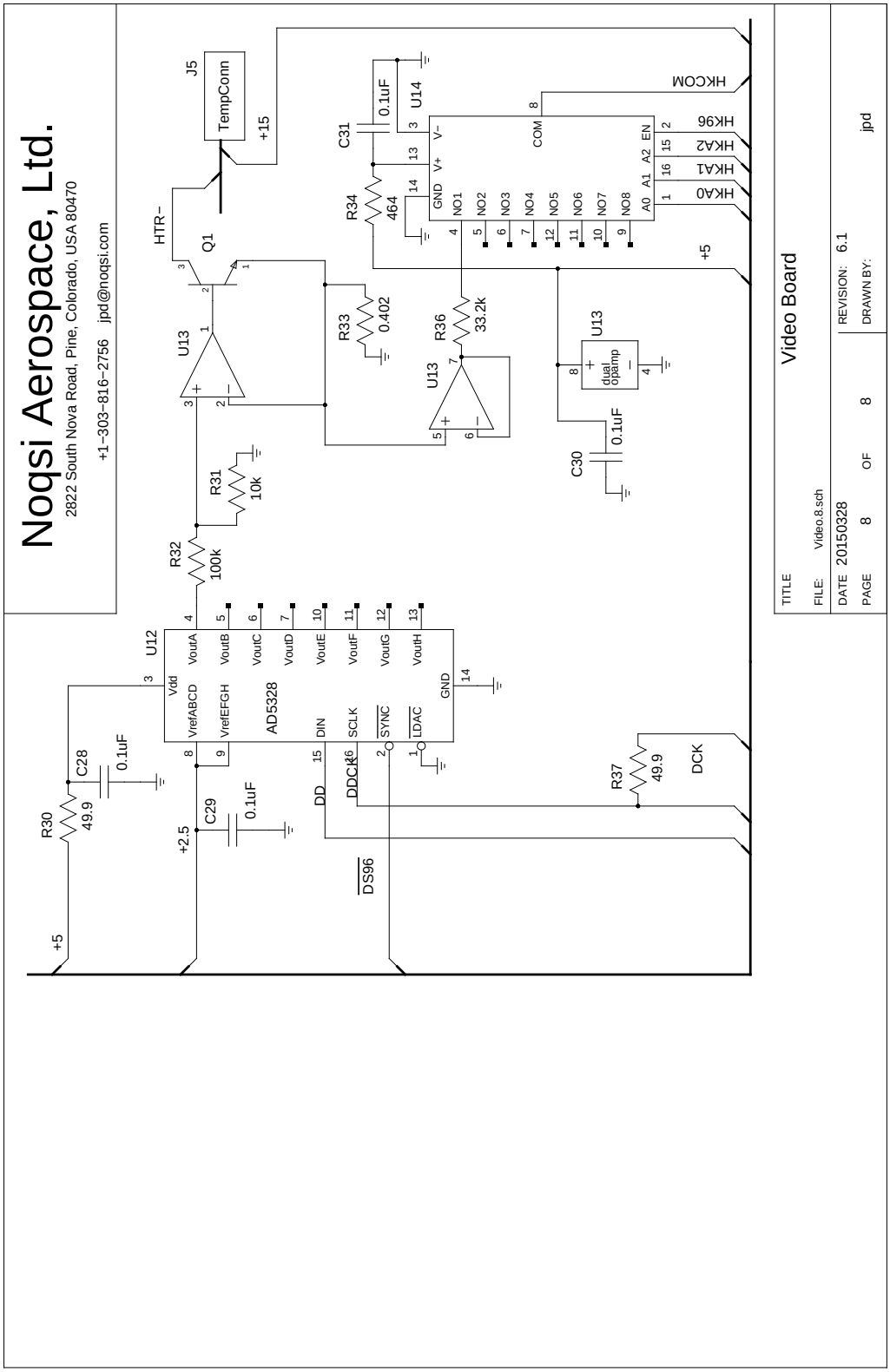

Figure 20: Video.8

2.3 Video Board Connectors

J1, J2, J3, and J4 connect to the flexprint cables from CCD1, CCD2, CCD3, and CCD4. Table 1 shows the pinout of J1. The -1 at the end of most net names indicates that the net serves CCD1. For J2, the corresponding net names end in -2, etc. Table 2 shows the pinout for J5, which serves the external temperature sensors and heater. Table 5 covers Js, the board stack connector.

Table 1: Flexprint Connector

Connector	Pin	Net	Signal
J1	1	Backside-1	case
J1	2	IG1-1	IG1
J1	3	IG2-1	IG2
J1	4	P1-OR-1	S1CD
J1	5	P2-OR-1	S2CD
J1	6	P3-OR-1	S3CD
J1	7	P1-U-1	S1U
J1	8	P2-U-1	S2U
J1	9	P3-U-1	S3U
J1	13	P3-IA-1	IA3
J1	14	P2-IA-1	IA2
J1	15	P1-IA-1	IA1
J1	19	GND	CS
J1	20	P3-OR-1	S3AB
J1	21	P2-OR-1	S2AB
J1	22	P1-OR-1	S1AB
J1	23	P3-FS-1	FS3
J1	24	P2-FS-1	FS2
J1	25	P1-FS-1	FS1
J1	26	VSUB-1	SUB
J1	27	ID-1	ID
J1	28	GND	RETD
J1	29	OG-D-1	OGD
J1	30	DR-D-1	DRD
J1	31	OUT-D-1	OSD
J1	32	GND	RTD78
J1	33	CuS-1	RTD56
J1	34	RD-1	RD
J1	35	OUT-C-1	OSC
J1	36	DR-C-1	DRC
J1	37	OG-C-1	OGC
J1	38	GND	RETC
J1	39	SCP-1	SCP
J1	40	GND	RETB

Table 1: Flexprint Connector (continued)

Connector	Pin	Net	Signal
J1	41	OG-B-1	OGB
J1	42	DR-B-1	DRB
J1	43	OUT-B-1	OSB
J1	44	RG-1	RG
J1	45	CuS-1	RTD34
J1	46	CuRTD-1	RTD12
J1	47	OUT-A-1	OSA
J1	48	DR-A-1	DRA
J1	49	OG-A-1	OGA
J1	50	GND	RETA
J1	51	SCP-1	USD

Table 2: Temperature Connector

Connector	Pin	Net
J5	1	GND
J5	2	GND
J5	3	GND
J5	4	GND
J5	5	GND
J5	6	GND
J5	7	GND
J5	8	GND
J5	9	GND
J5	10	GND
J5	11	GND
J5	12	GND
J5	17	PtRTD0
J5	18	PtRTD1
J5	19	PtRTD2
J5	20	PtRTD3
J5	21	PtRTD4
J5	22	PtRTD5
J5	23	PtRTD6
J5	24	PtRTD7
J5	25	PtRTD8
J5	26	PtRTD9
J5	27	PtRTD10
J5	28	PtRTD11
J5	16	+15
J5	31	HTR-

3 Interface Board

3.1 Building blocks

3.1.1 Drivers for high capacitance (parallel) clocks

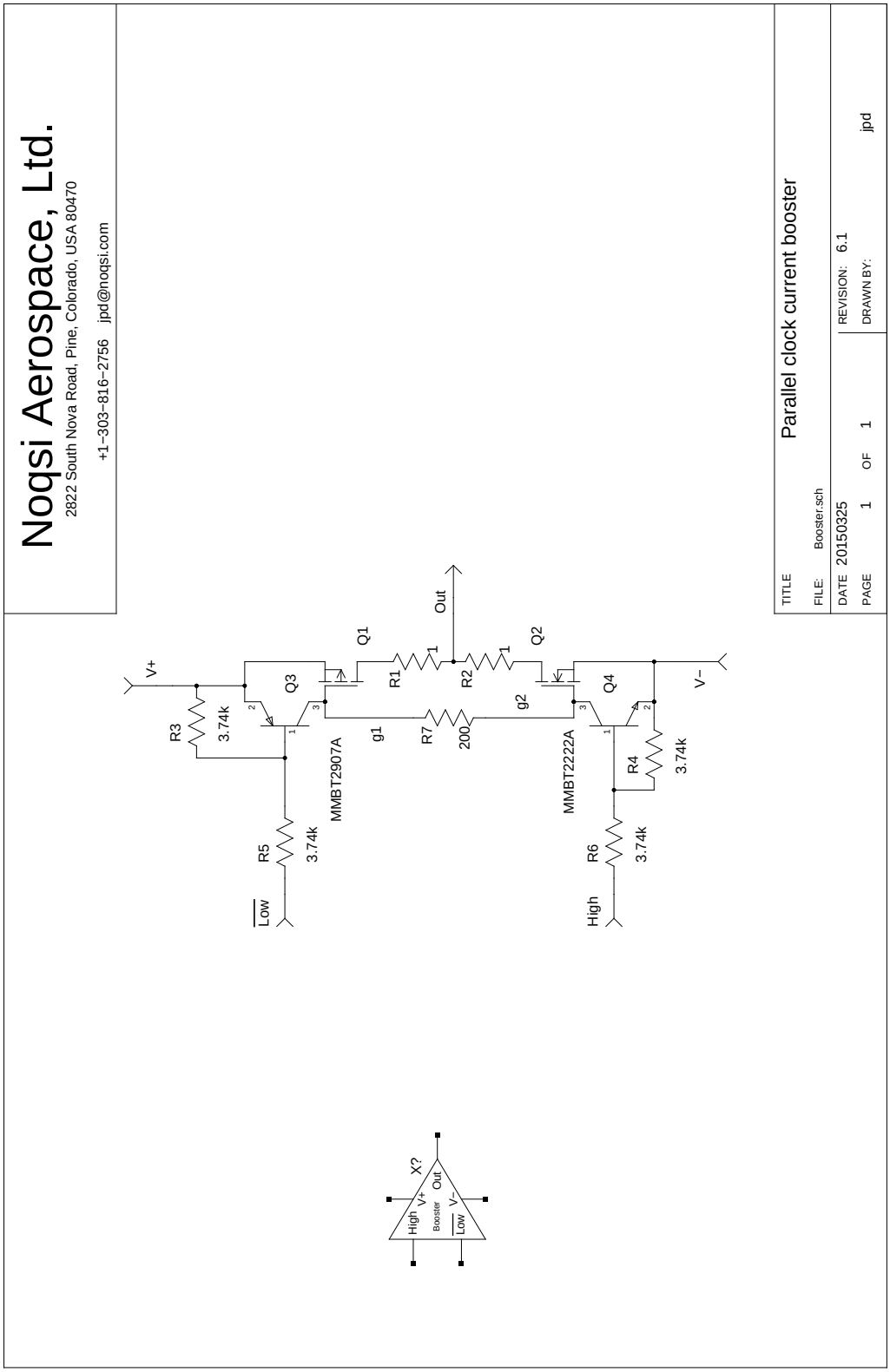

Figure 21: Booster

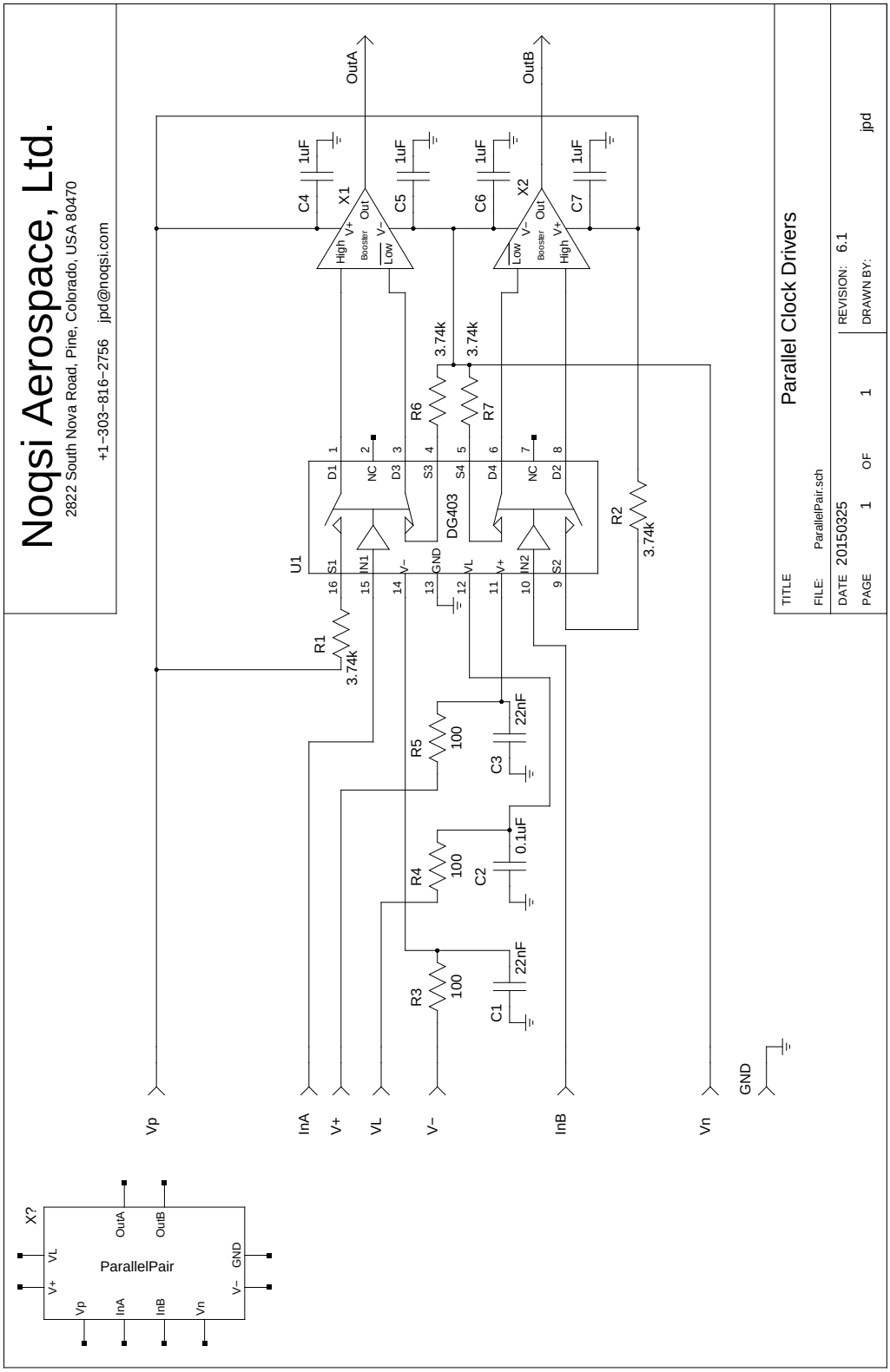

Figure 22: ParallelPair

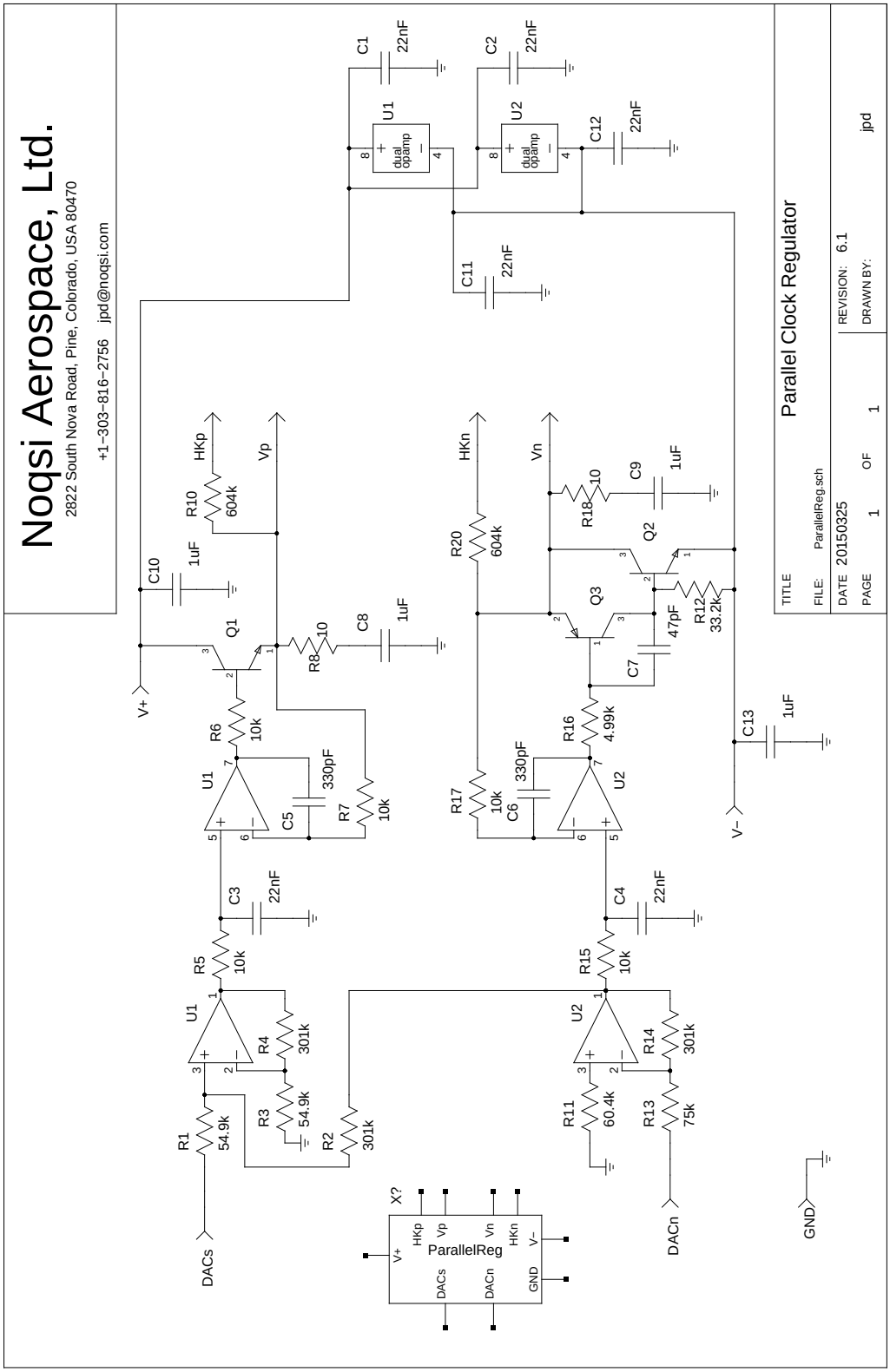

Figure 23: ParallelReg

3.1.2 Drivers for low capacitance clocks

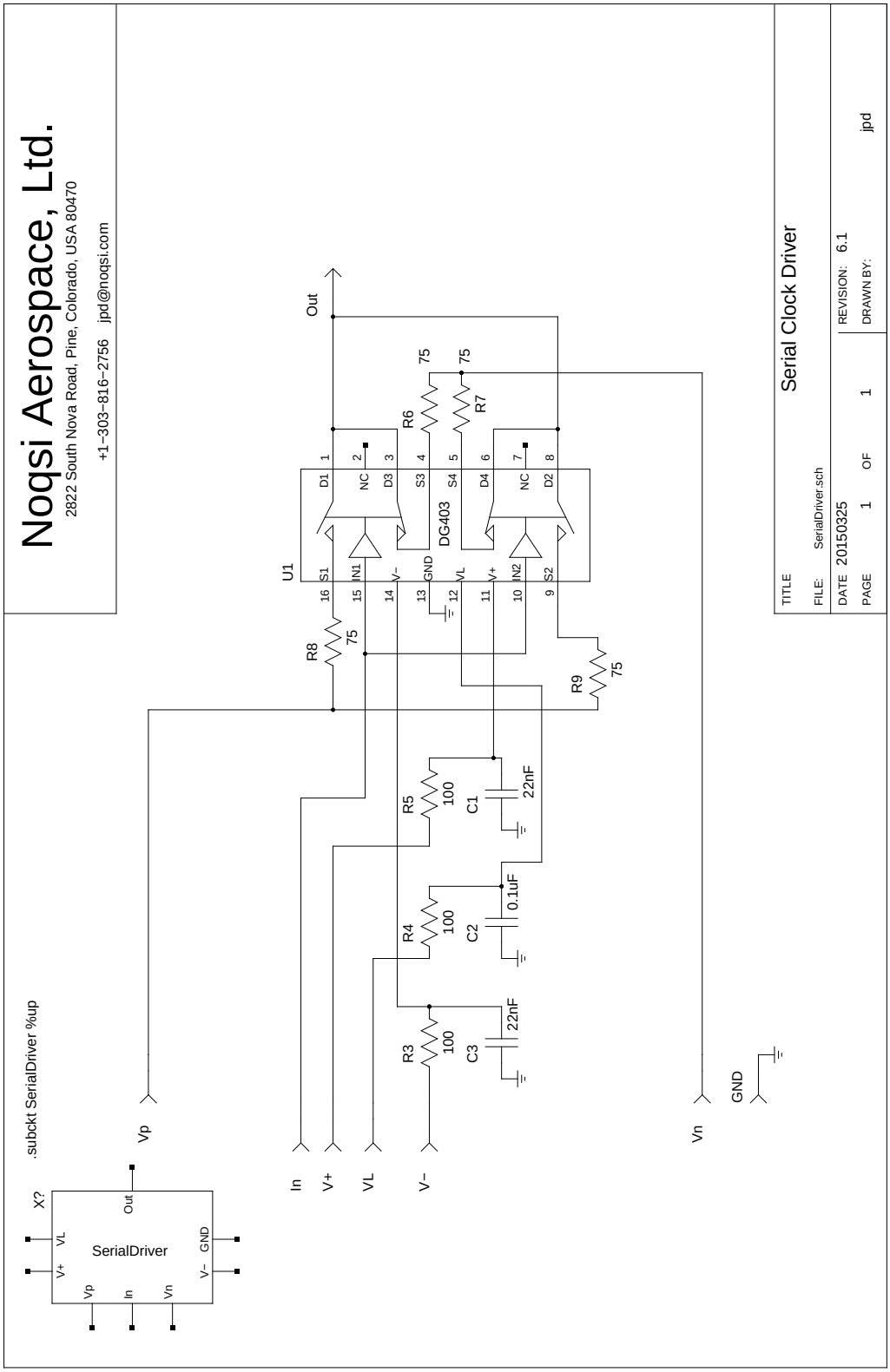

Figure 24: SerialDriver

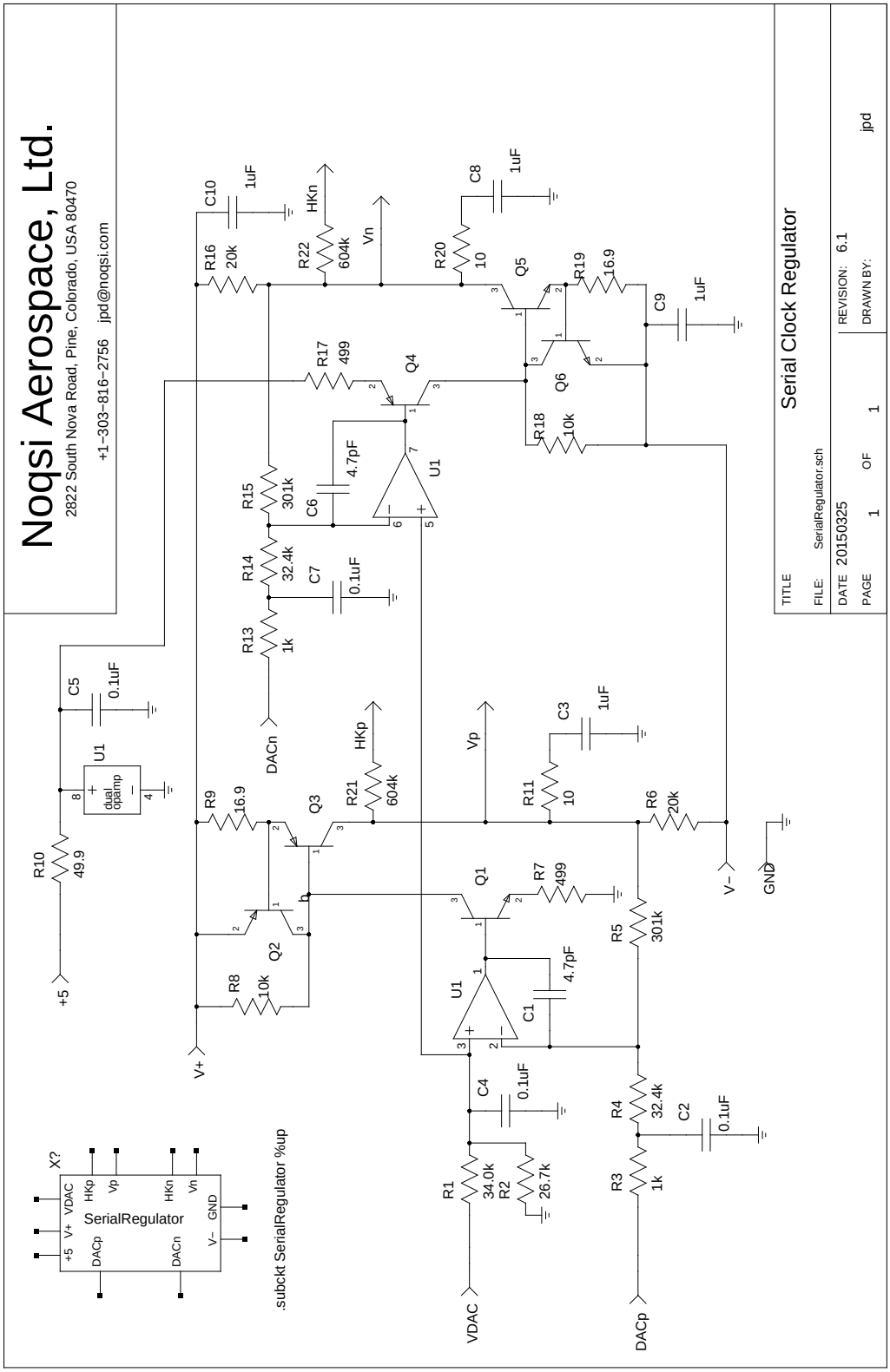

Figure 25: SerialRegulator

3.1.3 Clock drivers for one CCD

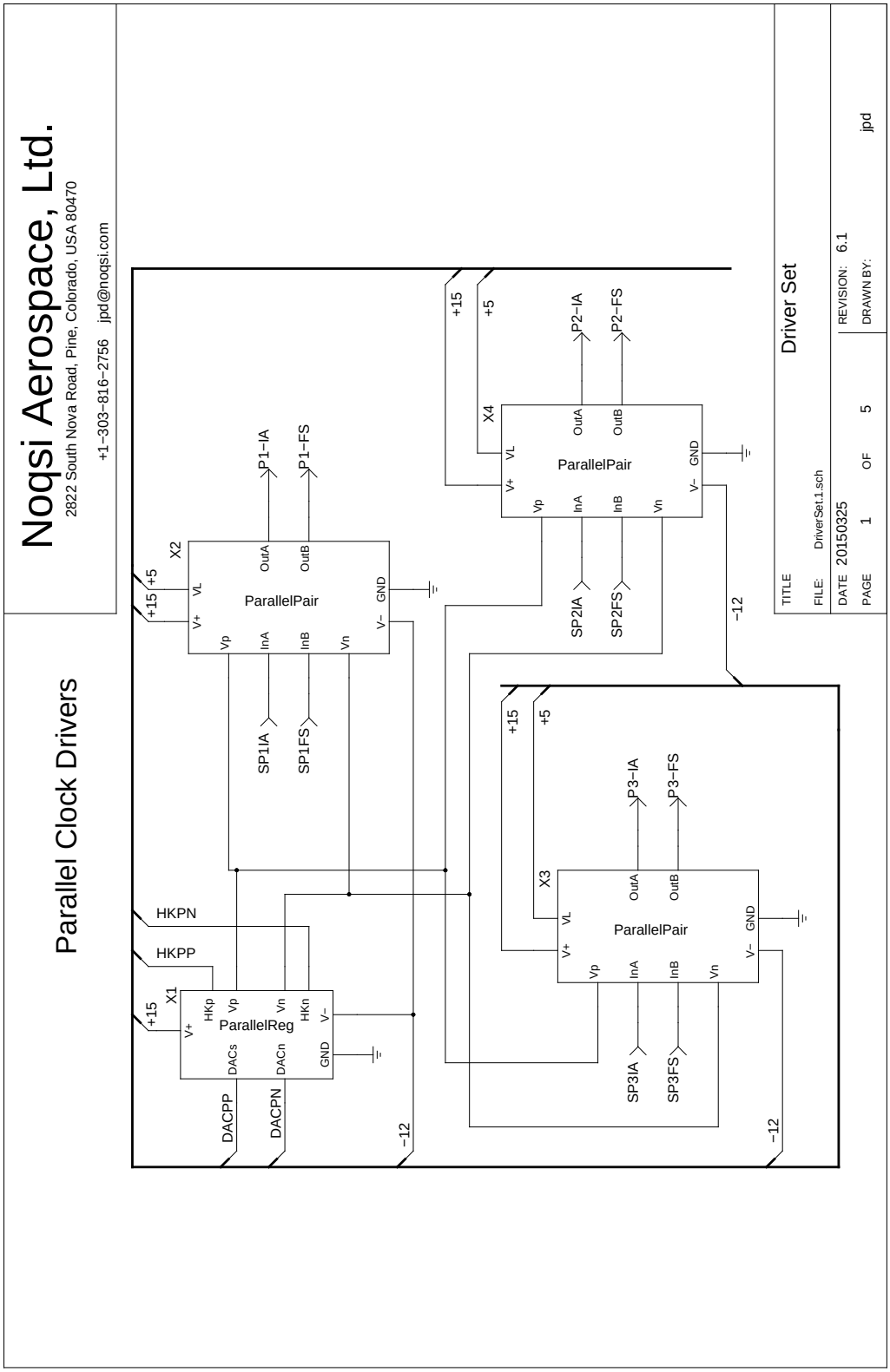

Figure 26: DriverSet.1

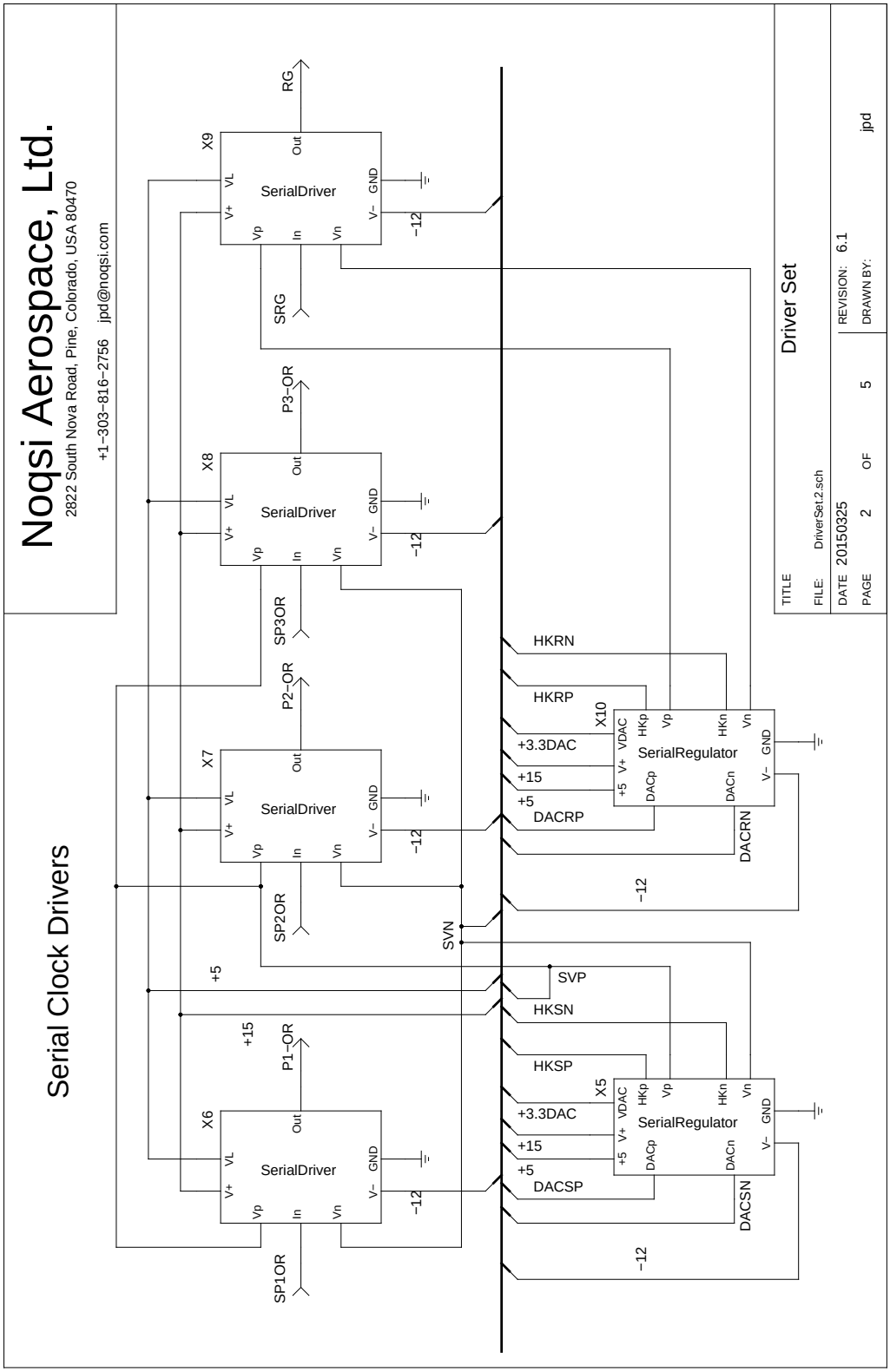

Figure 27: DriverSet.2

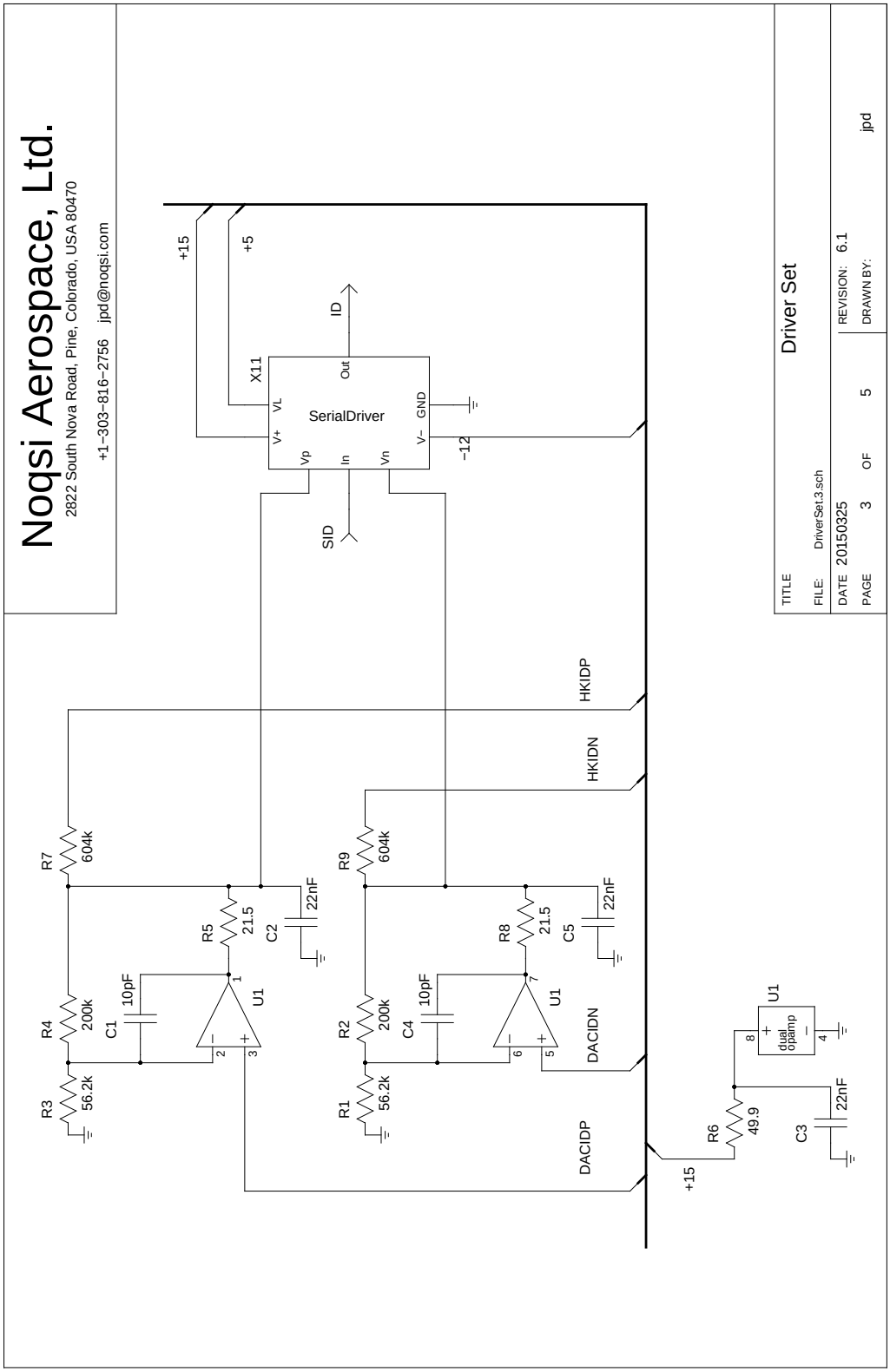

Figure 28: DriverSet.3

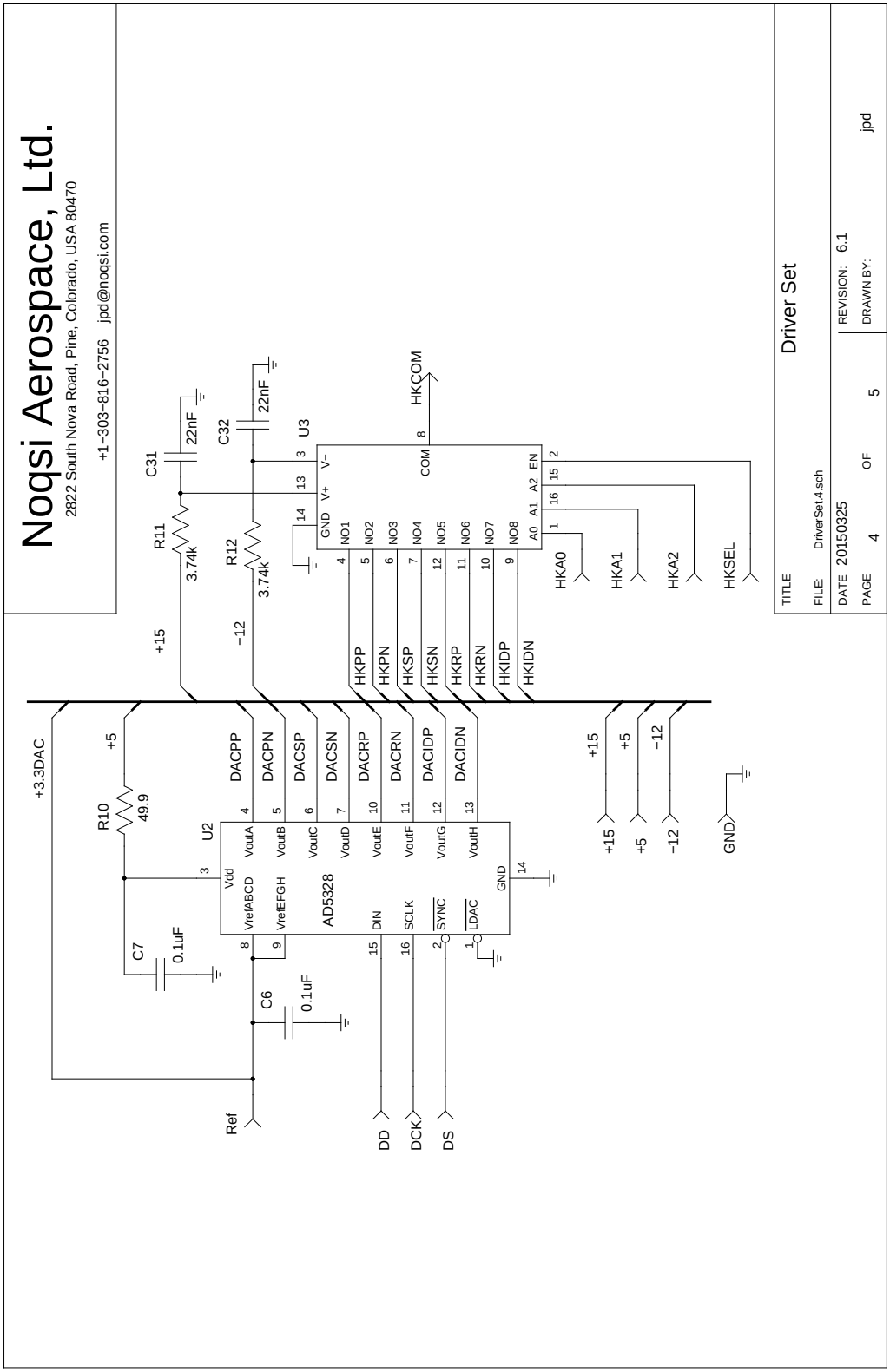

Figure 29: DriverSet.4

3.1.4 Power conditioning

Figure 30 shows the power regulators for the Artix FPGA. An RC filter on the reference insures that the 1.8V AUX power rises more slowly than the 1V core power. The 2.5V and 3.3V IO power follow the 1.8V AUX power with additional delays. This insures proper initialization. Q5 pulls down the 3.3V IO power if the 1.8V level is low, insuring that the rated maximum 2.625V difference cannot be exceeded for more than the allowed time (see Xilinx data sheet DS181). The resistors on the collectors of the pass transistors limit the surge current, and are rated to handle the fault current if the FPGA should latch up.

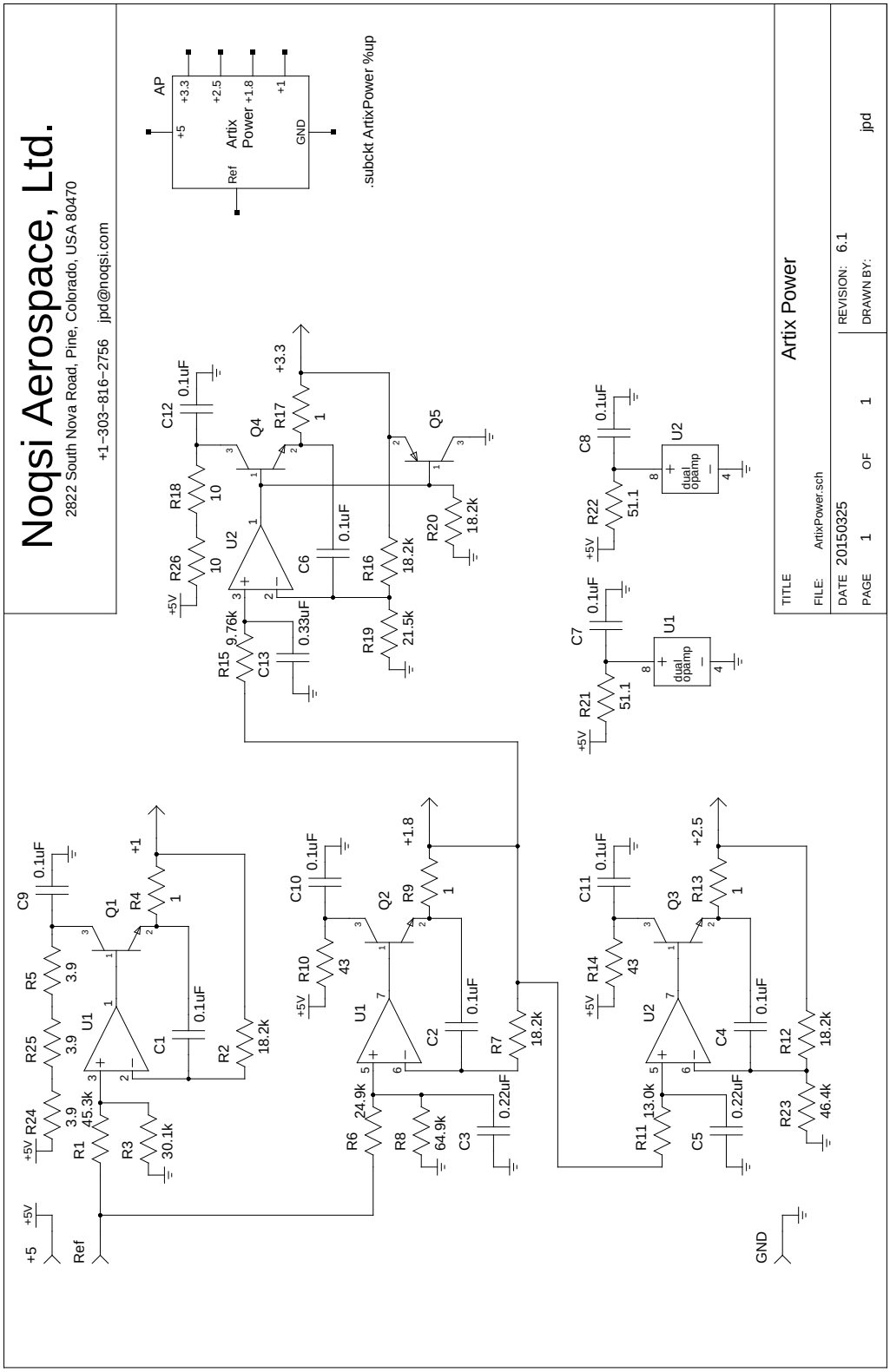

Figure 30: ArtixPower

3.2 Interface Board Top Level

Figure 31 shows the Artix FPGA (U4). Its pin connections are too complex to draw: Table 4 shows them. J9 is the JTAG header for FPGA debugging. J6 is the data connector to the DHU. J8 is test signals and configuration jumpers for the FPGA. Table 3 shows its pinout. For the pinouts of Js, the stacking connector, see Table 5.

Table 3: FPGA Test Header

Connector	Pin	Net
J8	1	GND
J8	2	TestMode-1
J8	3	GND
J8	4	TestMode-0
J8	5	GND
J8	6	DONE_0
J8	7	GND
J8	8	M0_0
J8	9	GND
J8	10	M1_0
J8	11	GND
J8	12	M2_0
J8	13	GND
J8	14	$\overline{\text{INIT}}$
J8	15	GND
J8	16	$\overline{\text{PROGRAM}}$

Table 4: Artix FPGA Connections

Pin	Net	Signal
U18	SP1-IA-4	CCD_IA1_pin[3]
W17	SP1-IA-3	CCD_IA1_pin[2]
V22	SP1-IA-2	CCD_IA1_pin[1]
AA19	SP1-IA-1	CCD_IA1_pin[0]
R14	SP2-IA-4	CCD_IA2_pin[3]
AB18	SP2-IA-3	CCD_IA2_pin[2]
AB20	SP2-IA-2	CCD_IA2_pin[1]
P14	SP2-IA-1	CCD_IA2_pin[0]
P19	SP3-IA-4	CCD_IA3_pin[3]
N17	SP3-IA-3	CCD_IA3_pin[2]
T18	SP3-IA-2	CCD_IA3_pin[1]
R16	SP3-IA-1	CCD_IA3_pin[0]
U22	SP1-FS-4	CCD_FS1_pin[3]
P20	SP1-FS-3	CCD_FS1_pin[2]
R21	SP1-FS-2	CCD_FS1_pin[1]

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
T21	SP1-FS-1	CCD_FS1_pin[0]
V17	SP2-FS-4	CCD_FS2_pin[3]
U17	SP2-FS-3	CCD_FS2_pin[2]
AA18	SP2-FS-2	CCD_FS2_pin[1]
R18	SP2-FS-1	CCD_FS2_pin[0]
P21	SP3-FS-4	CCD_FS3_pin[3]
P22	SP3-FS-3	CCD_FS3_pin[2]
P17	SP3-FS-2	CCD_FS3_pin[1]
U21	SP3-FS-1	CCD_FS3_pin[0]
K21	SDO-D-4	CCD_ADC_Sdi_pin[15]
H15	SDO-C-4	CCD_ADC_Sdi_pin[14]
G18	SDO-B-4	CCD_ADC_Sdi_pin[13]
H22	SDO-A-4	CCD_ADC_Sdi_pin[12]
K22	SDO-D-3	CCD_ADC_Sdi_pin[11]
H18	SDO-C-3	CCD_ADC_Sdi_pin[10]
H14	SDO-B-3	CCD_ADC_Sdi_pin[9]
H17	SDO-A-3	CCD_ADC_Sdi_pin[8]
J14	SDO-D-2	CCD_ADC_Sdi_pin[7]
M21	SDO-C-2	CCD_ADC_Sdi_pin[6]
H20	SDO-B-2	CCD_ADC_Sdi_pin[5]
J15	SDO-A-2	CCD_ADC_Sdi_pin[4]
L21	SDO-D-1	CCD_ADC_Sdi_pin[3]
J22	SDO-C-1	CCD_ADC_Sdi_pin[2]
G20	SDO-B-1	CCD_ADC_Sdi_pin[1]
G17	SDO-A-1	CCD_ADC_Sdi_pin[0]
T19	HKA6	HSK_ADC_Sel_pin[6]
R19	HKA5	HSK_ADC_Sel_pin[5]
AA21	HKA4	HSK_ADC_Sel_pin[4]
T20	HKA3	HSK_ADC_Sel_pin[3]
W22	HKA2	HSK_ADC_Sel_pin[2]
W21	HKA1	HSK_ADC_Sel_pin[1]
AA20	HKA0	HSK_ADC_Sel_pin[0]
M18	$\overline{\text{DS88}}$	CLC_DCS_pin[3]
N22	$\overline{\text{DS80}}$	CLC_DCS_pin[2]
L18	$\overline{\text{DS72}}$	CLC_DCS_pin[1]
K18	$\overline{\text{DS64}}$	CLC_DCS_pin[0]
M22	DCS3	CLC_CS8_11_pin[3]
L20	DCS2	CLC_CS8_11_pin[2]
L19	DCS1	CLC_CS8_11_pin[1]
N19	DCS0	CLC_CS8_11_pin[0]
M15	TestMode-1	TestMode_pins[1]
K17	TestMode-0	TestMode_pins[0]

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
N18	$\overline{\text{RED}}$	DebugStatus_pins[5]
M13	$\overline{\text{ORANGE}}$	DebugStatus_pins[4]
J20	$\overline{\text{YELLOW}}$	DebugStatus_pins[3]
J21	$\overline{\text{GREEN}}$	DebugStatus_pins[2]
J16	$\overline{\text{BLUE}}$	DebugStatus_pins[1]
K19	$\overline{\text{WHITE}}$	DebugStatus_pins[0]
L15	Cam_ID-4	Cam_ID[4]
K13	Cam_ID-3	Cam_ID[3]
L13	Cam_ID-2	Cam_ID[2]
K14	Cam_ID-1	Cam_ID[1]
N20	Cam_ID-0	Cam_ID[0]
E19	osc_clk	osc_clk_60_pin
V18	cwclk	ChargePumpClk_pin
P16	SP1OR	CCD_S1_pin
R17	SP2OR	CCD_S2_pin
N14	SP3OR	CCD_S3_pin
N13	SRG	CCD_RstGate_pin
P15	SID	CCD_InDiode_pin
L16	Clamp	CCD_ADC_Clamp_pin
L14	DeInt	CCD_ADC_Hold_pin
M16	Int	CCD_ADC_Int_pin
K16	CNV	CCD_ADC_Cnv_pin
H19	SCK	CCD_ADC_Sck_pin
R22	D422	Cmd_DIN_pin
U20	C422	Cmd_SCK_pin
G15	DATA-A	dataA_out_pin_p
G16	$\overline{\text{DATA-A}}$	dataA_out_pin_n
H13	DATA-B	dataB_out_pin_p
G13	$\overline{\text{DATA-B}}$	dataB_out_pin_n
V19	HKC	HSK_ADC_Sck_pin
N15	HKD	HSK_ADC_Sdi_pin
Y21	$\overline{\text{HKCS}}$	HSK_ADC_Cnv_pin
Y22	HK64	HSK_ADC_64_pin
V20	HK72	HSK_ADC_72_pin
AB22	HK80	HSK_ADC_80_pin
AB21	HK88	HSK_ADC_88_pin
Y18	HK104	HSK_ADC_104_pin
M20	DD	CLC_DAC_Din_pin
J19	DCK	CLC_DAC_Sck_pin
M9	GND	VN_0
L10	GND	VP_0
G11	DONE_0	DONE_0

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
N10	GND	DXP_0
K9	GND	GNDADC_0
K10	+1.8F	VCCADC_0
M10	GND	VREFP_0
E12	GND	VCCBATT_0
V12	TCK	TCK_0
N9	GND	DXN_0
L9	GND	VREFN_0
L12	C422	CCLK_0
U11	M0_0	M0_0
U10	M1_0	M1_0
U12	$\overline{\text{INIT}}$	INIT_B_0
R13	TDI	TDI_0
U13	TDO	TDO_0
U9	M2_0	M2_0
U8	+3.3F	3.30
N12	$\overline{\text{PROGRAM}}$	PROGRAM_B_0
T13	TMS	TMS_0
F12	+3.3F	VCCO_0
T12	+3.3F	VCCO_0
AA17	GND	VCCO_13
AB14	GND	VCCO_13
V16	GND	VCCO_13
W13	GND	VCCO_13
Y10	GND	VCCO_13
M14	+3.3F	3.30
P18	+3.3F	3.30
R15	+3.3F	3.30
T22	+3.3F	3.30
U19	+3.3F	3.30
Y20	+3.3F	3.30
G19	+2.5F	2.50
H16	+2.5F	2.50
J13	+2.5F	2.50
K20	+2.5F	2.50
L17	+2.5F	2.50
N21	+2.5F	2.50
A17	+3.3F	3.30
B14	+3.3F	3.30
C21	+3.3F	3.30
D18	+3.3F	3.30
E15	+3.3F	3.30

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
F22	+3.3F	3.30
AA7	GND	VCCO_34
AB4	GND	VCCO_34
R5	GND	VCCO_34
T2	GND	VCCO_34
V6	GND	VCCO_34
W3	GND	VCCO_34
C1	GND	VCCO_35
F2	GND	VCCO_35
H6	GND	VCCO_35
J3	GND	VCCO_35
M4	GND	VCCO_35
N1	GND	VCCO_35
D11	GND	MGTPRXP1_216
B10	GND	MGTPRXP2_216
D9	GND	MGTPRXP3_216
B8	GND	MGTPRXP0_216
C11	GND	MGTPRXN1_216
A10	GND	MGTPRXN2_216
C9	GND	MGTPRXN3_216
A8	GND	MGTPRXN0_216
F8	GND	MGTRREF_216
D8	GND	GND
A2	GND	GND
A3	GND	GND
A5	GND	GND
A7	GND	GND
A9	GND	GND
A11	GND	GND
A12	GND	GND
A22	GND	GND
AA2	GND	GND
AA12	GND	GND
AA22	GND	GND
AB9	GND	GND
AB19	GND	GND
B3	GND	GND
B12	GND	GND
B19	GND	GND
C3	GND	GND
C6	GND	GND
C10	GND	GND

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
C12	GND	GND
C16	GND	GND
D3	GND	GND
D4	GND	GND
D12	GND	GND
D13	GND	GND
E4	GND	GND
E5	GND	GND
E7	GND	GND
E9	GND	GND
E11	GND	GND
E20	GND	GND
F5	GND	GND
F11	GND	GND
F17	GND	GND
G5	GND	GND
G6	GND	GND
G7	GND	GND
G8	GND	GND
G9	GND	GND
G10	GND	GND
G12	GND	GND
G14	GND	GND
H1	GND	GND
H7	GND	GND
H9	GND	GND
H11	GND	GND
H21	GND	GND
J8	GND	GND
J10	GND	GND
J12	GND	GND
J18	GND	GND
K5	GND	GND
K7	GND	GND
K11	GND	GND
K15	GND	GND
L2	GND	GND
L8	GND	GND
L22	GND	GND
M7	GND	GND
M11	GND	GND
M19	GND	GND

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
N6	GND	GND
N8	GND	GND
N16	GND	GND
P3	GND	GND
P7	GND	GND
P9	GND	GND
P11	GND	GND
P13	GND	GND
R8	GND	GND
R10	GND	GND
R12	GND	GND
R20	GND	GND
T7	GND	GND
T9	GND	GND
T11	GND	GND
T17	GND	GND
U4	GND	GND
U14	GND	GND
V1	GND	GND
V11	GND	GND
V21	GND	GND
W8	GND	GND
W18	GND	GND
Y5	GND	GND
Y15	GND	GND
H8	+1F	VCCINT
H10	+1F	VCCINT
J7	+1F	VCCINT
J9	+1F	VCCINT
K8	+1F	VCCINT
L7	+1F	VCCINT
M8	+1F	VCCINT
N7	+1F	VCCINT
P8	+1F	VCCINT
P10	+1F	VCCINT
R7	+1F	VCCINT
R9	+1F	VCCINT
T8	+1F	VCCINT
T10	+1F	VCCINT
H12	+1.8F	1.80
K12	+1.8F	1.80
M12	+1.8F	1.80

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
P12	+1.8F	1.80
R11	+1.8F	1.80
J11	+1F	VCCBRAM
L11	+1F	VCCBRAM
N11	+1F	VCCBRAM

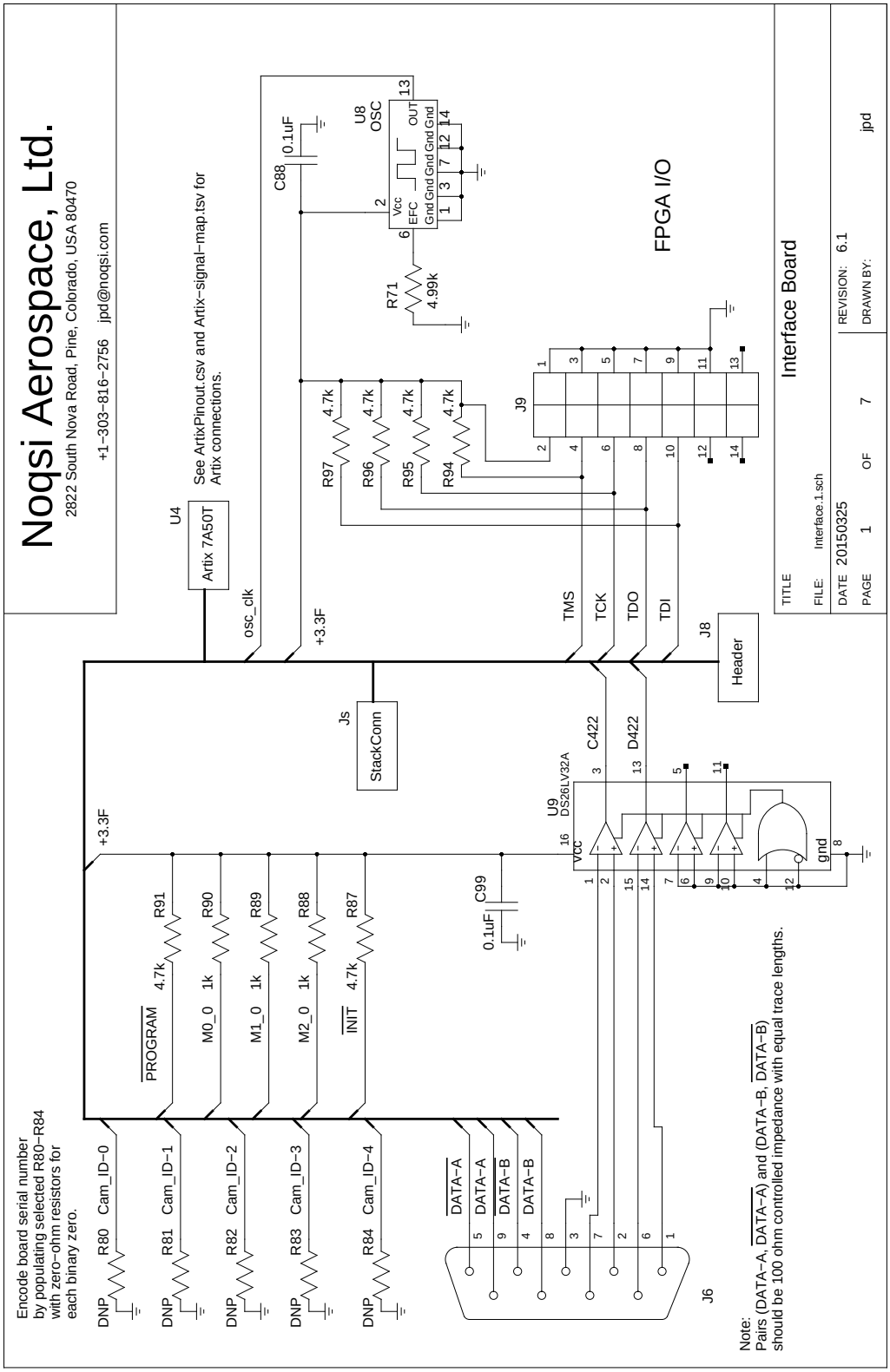

Figure 31: Interface.1

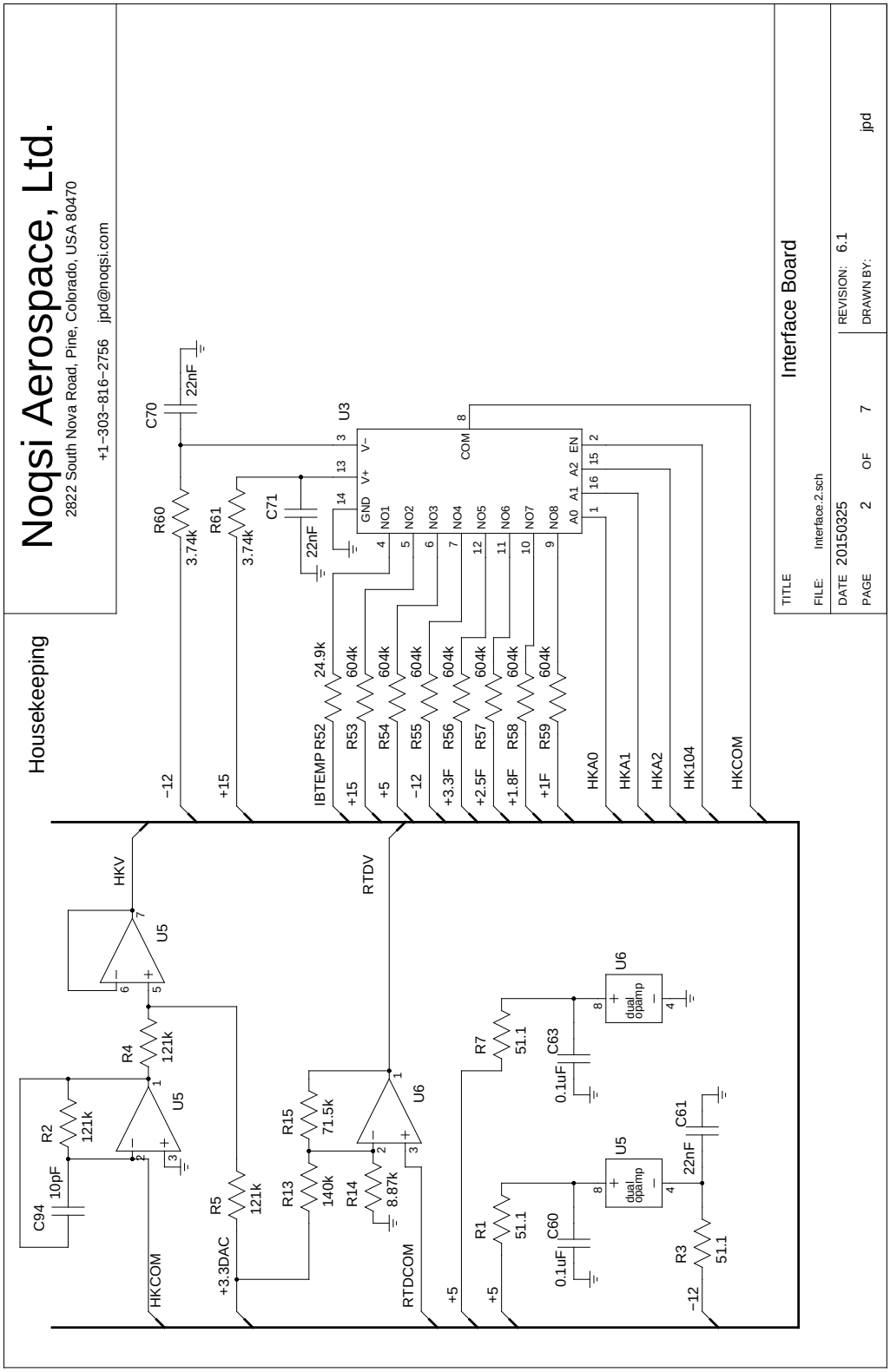

Figure 32: Interface.2

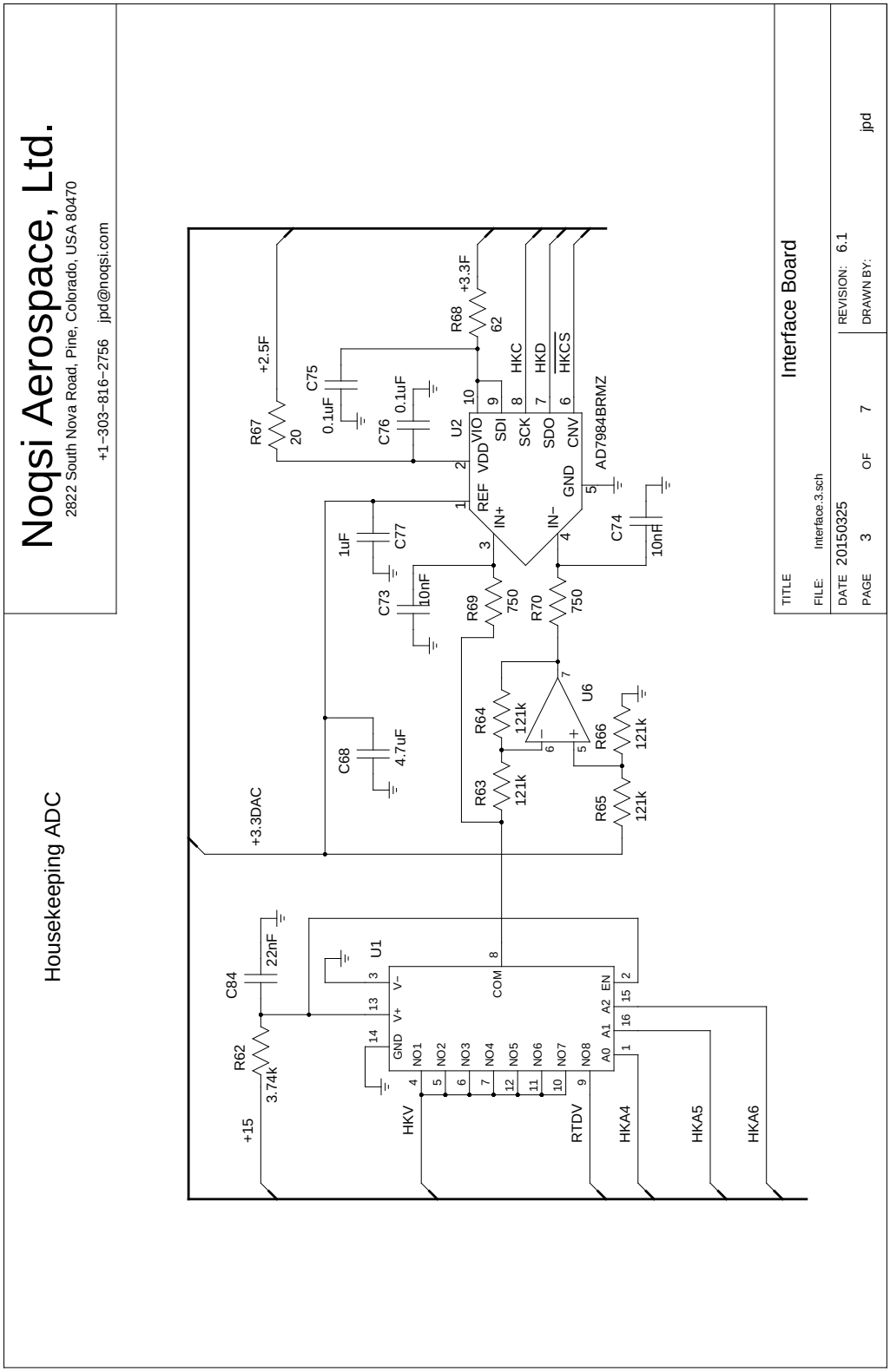

Figure 33: Interface.3

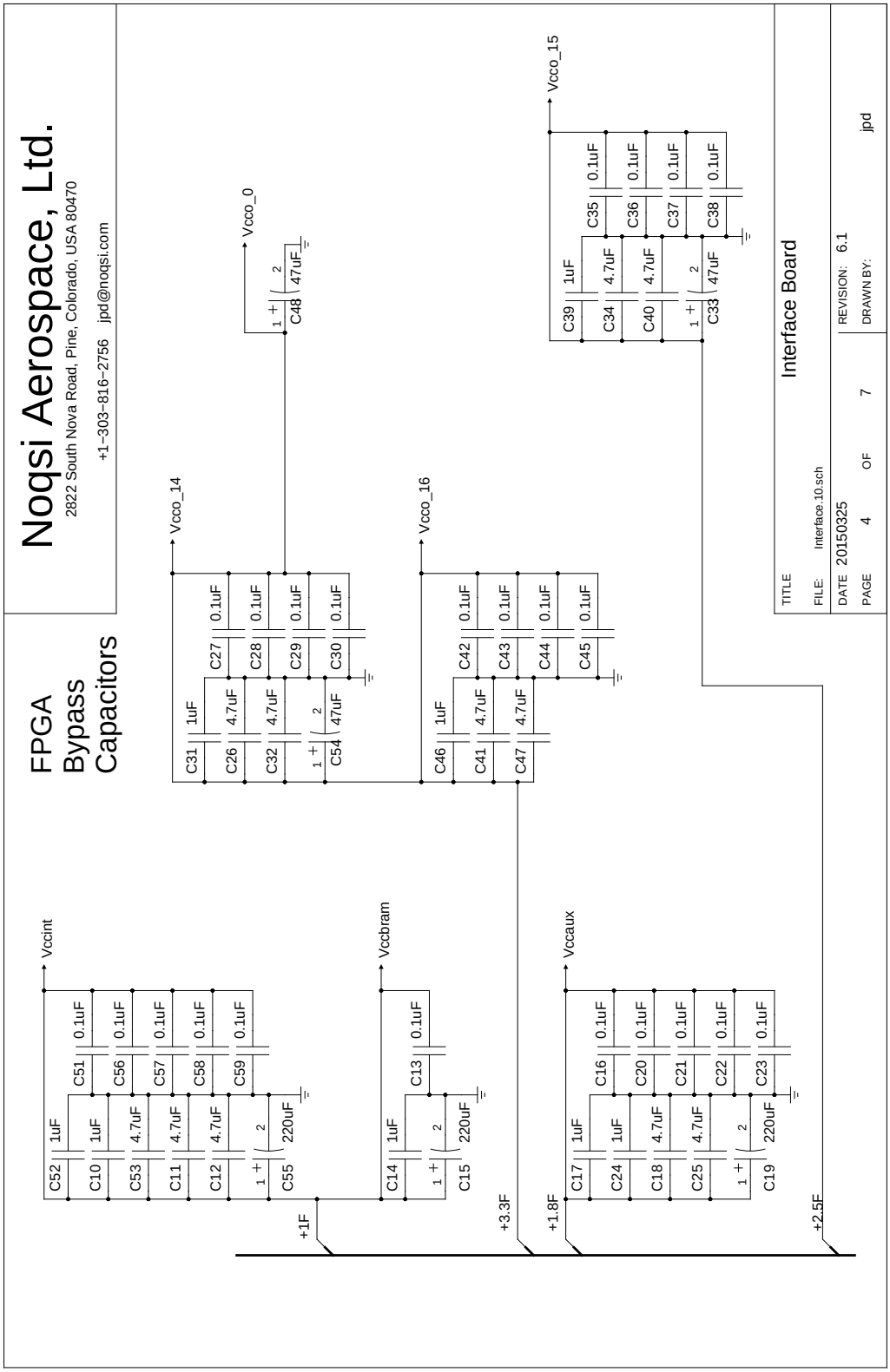

Figure 34: Interface.4

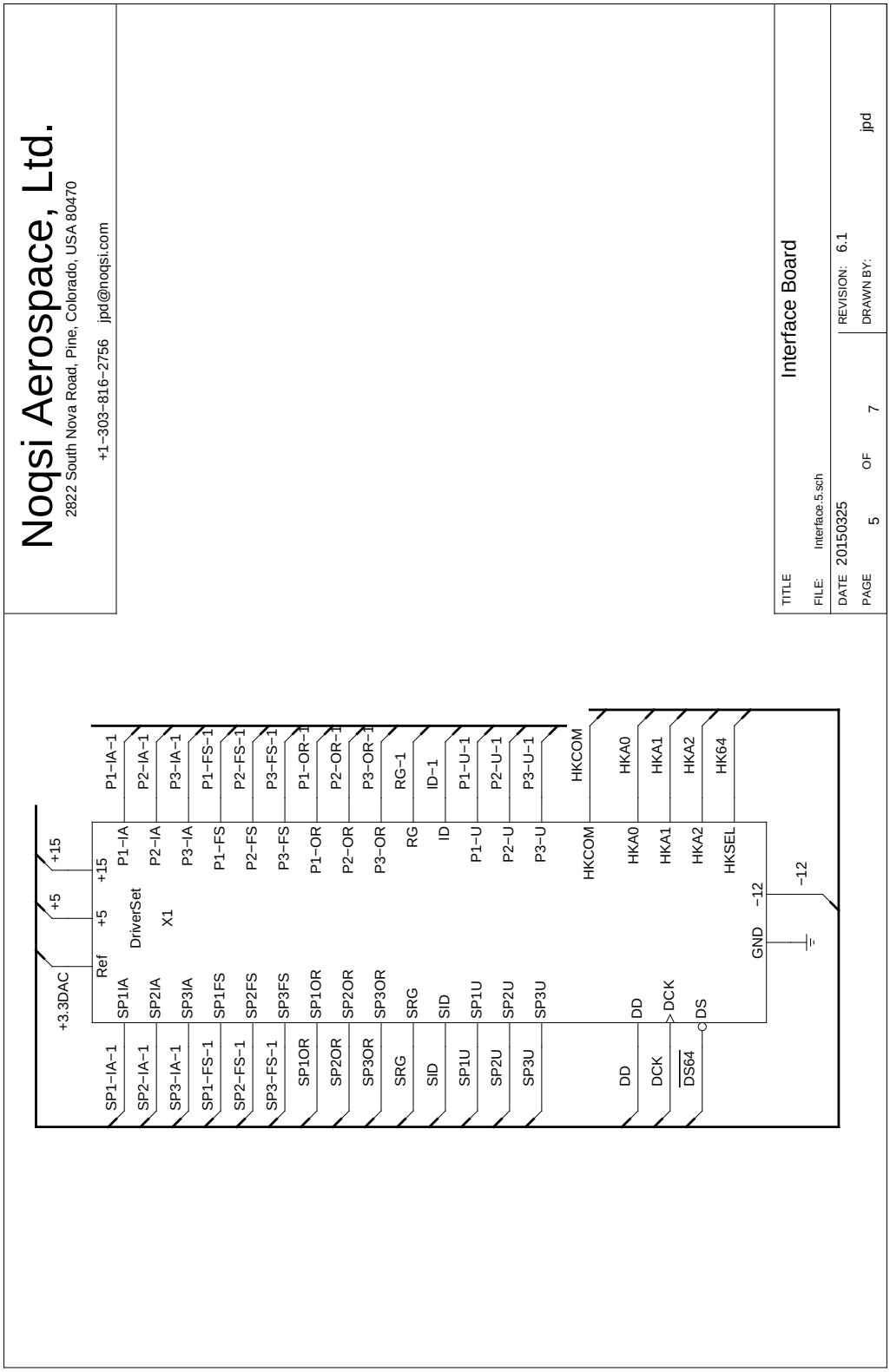

Figure 35: Interface.5

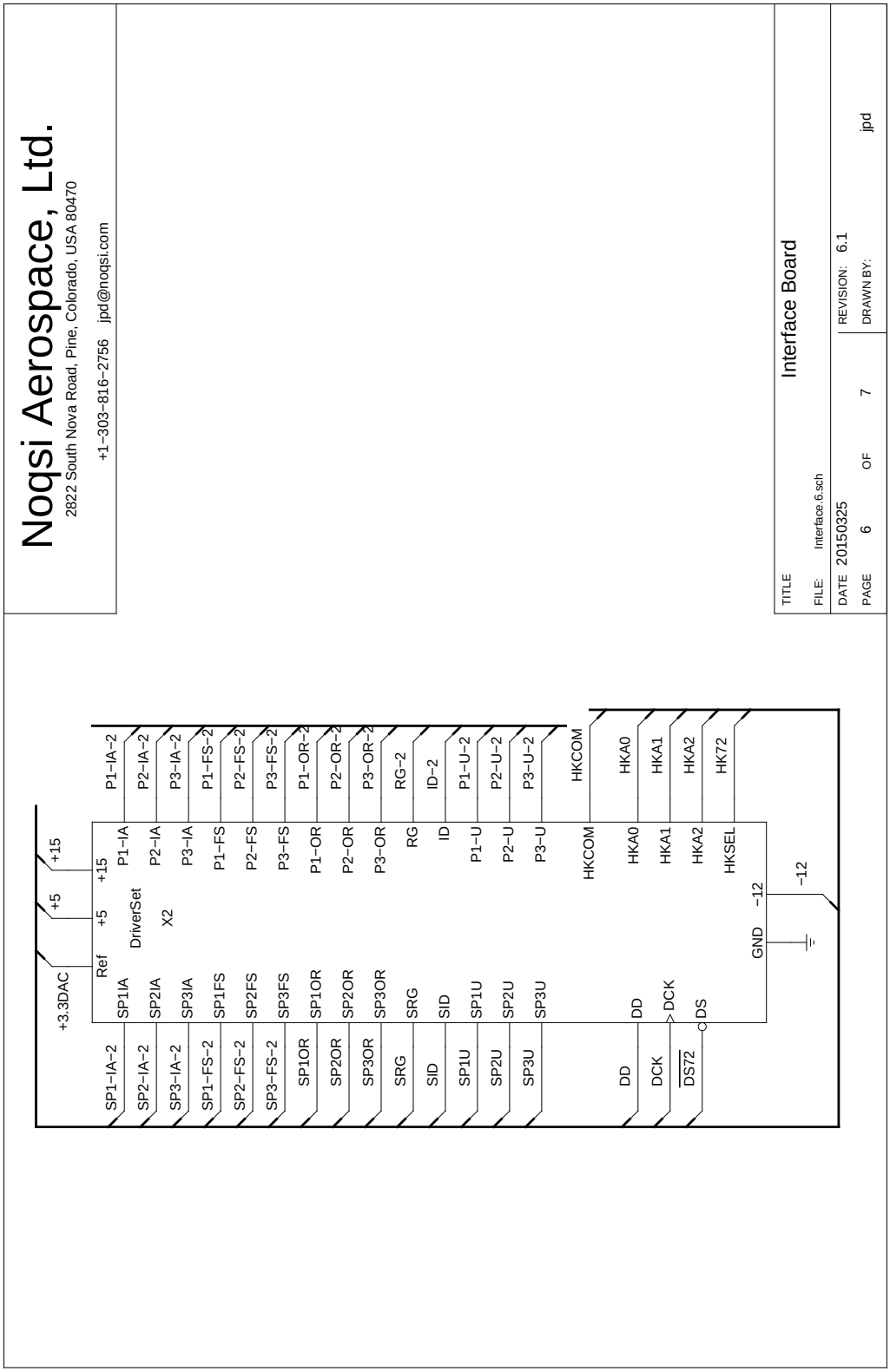

Figure 36: Interface.6

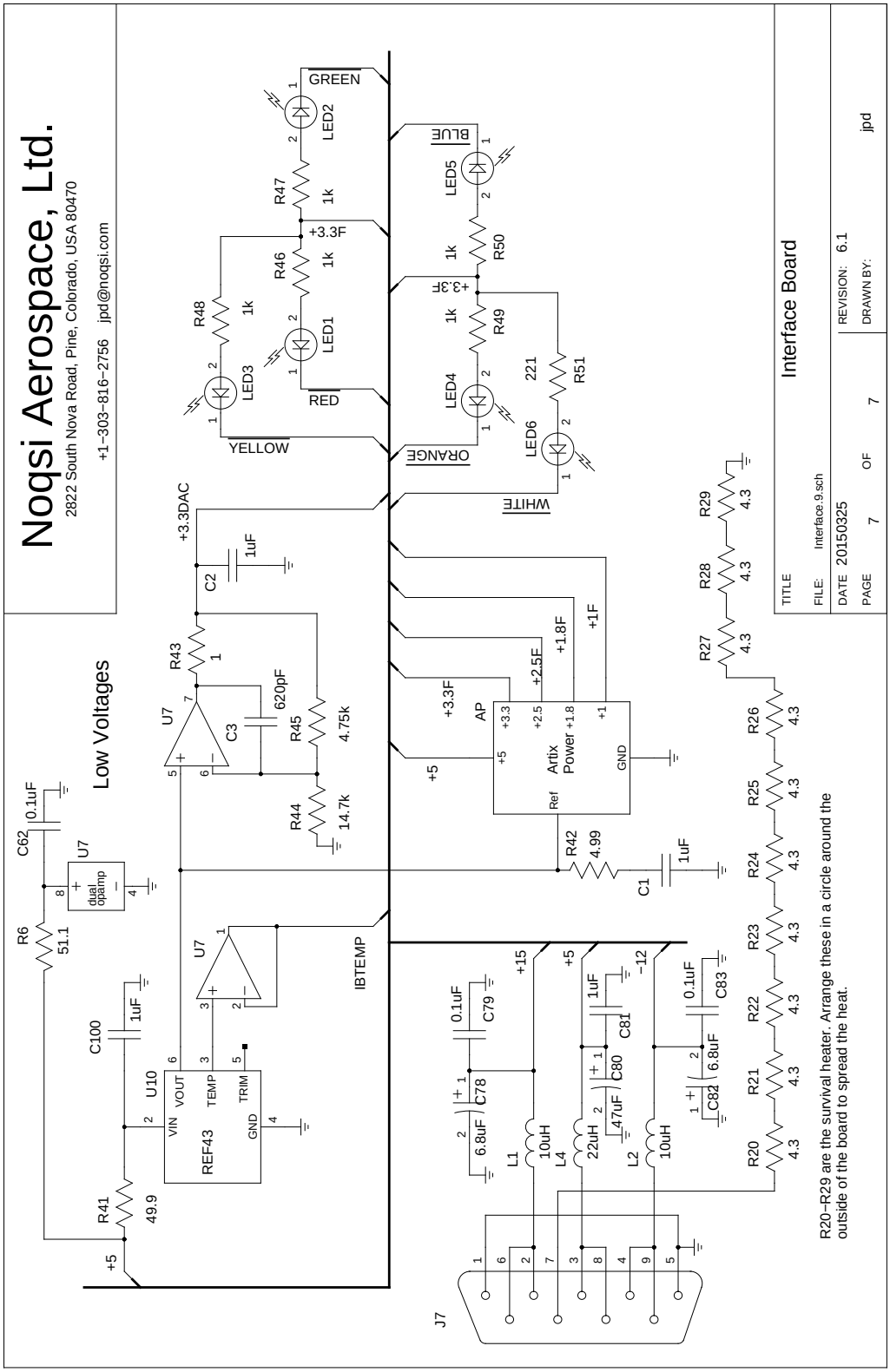

Figure 37: Interface.7

Figure 37 shows power input from the DHU (J7) and low voltage power conditioning. LEDs are for debugging: we will not install them on flight boards.

4 Driver Board

See the previous section for the DriverSet building blocks.

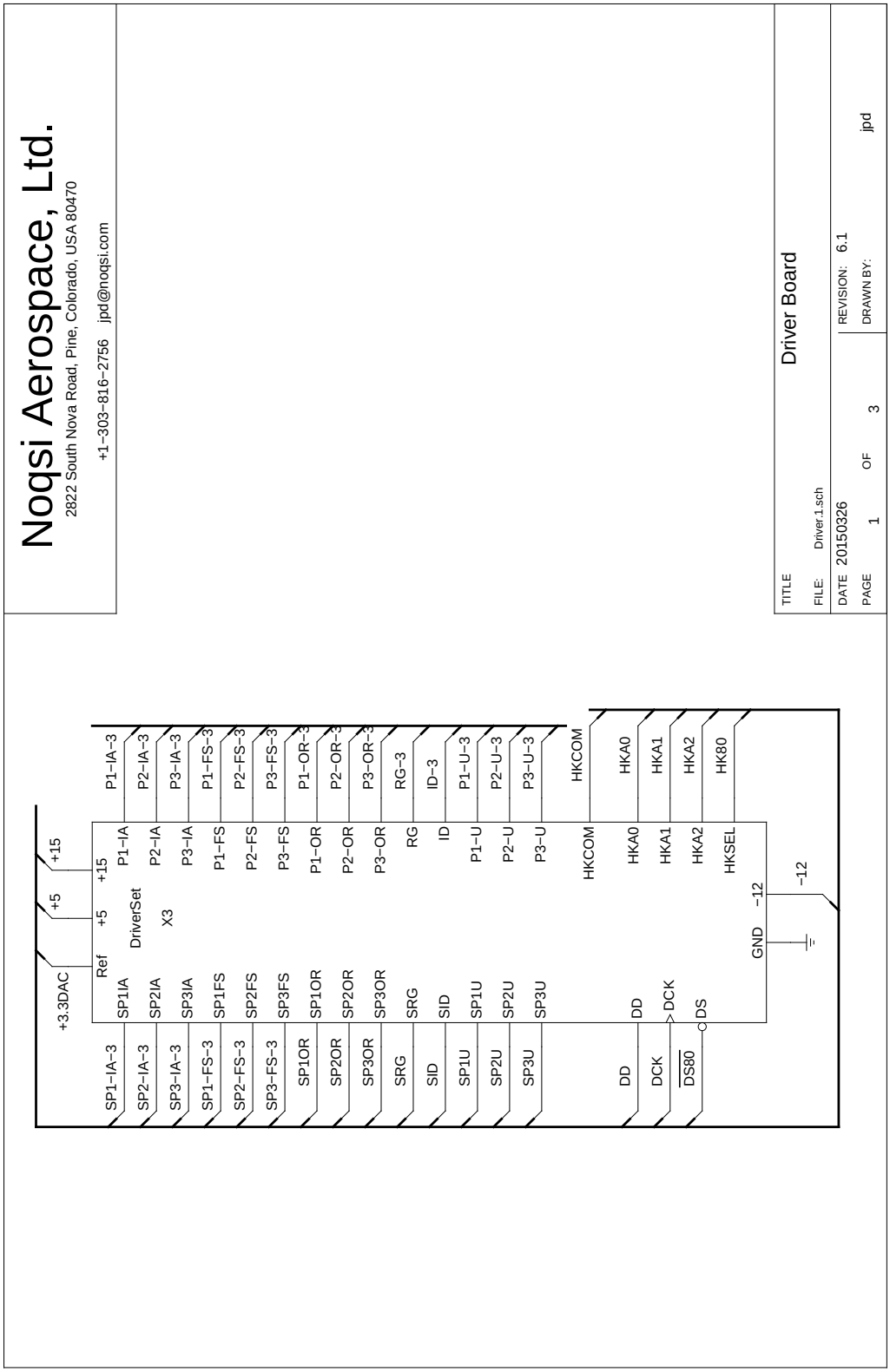

Figure 38: Driver.1

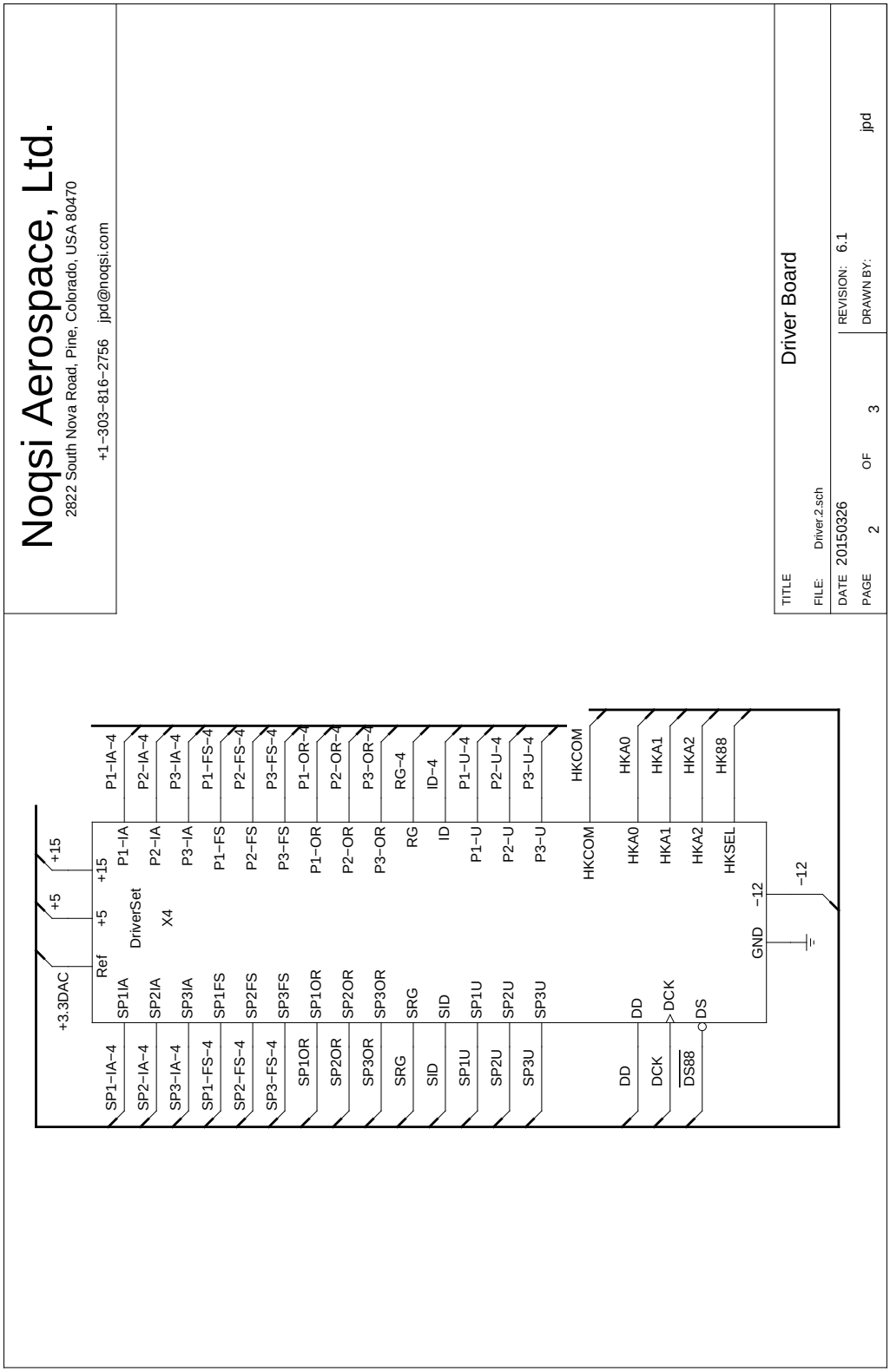

Figure 39: Driver.2

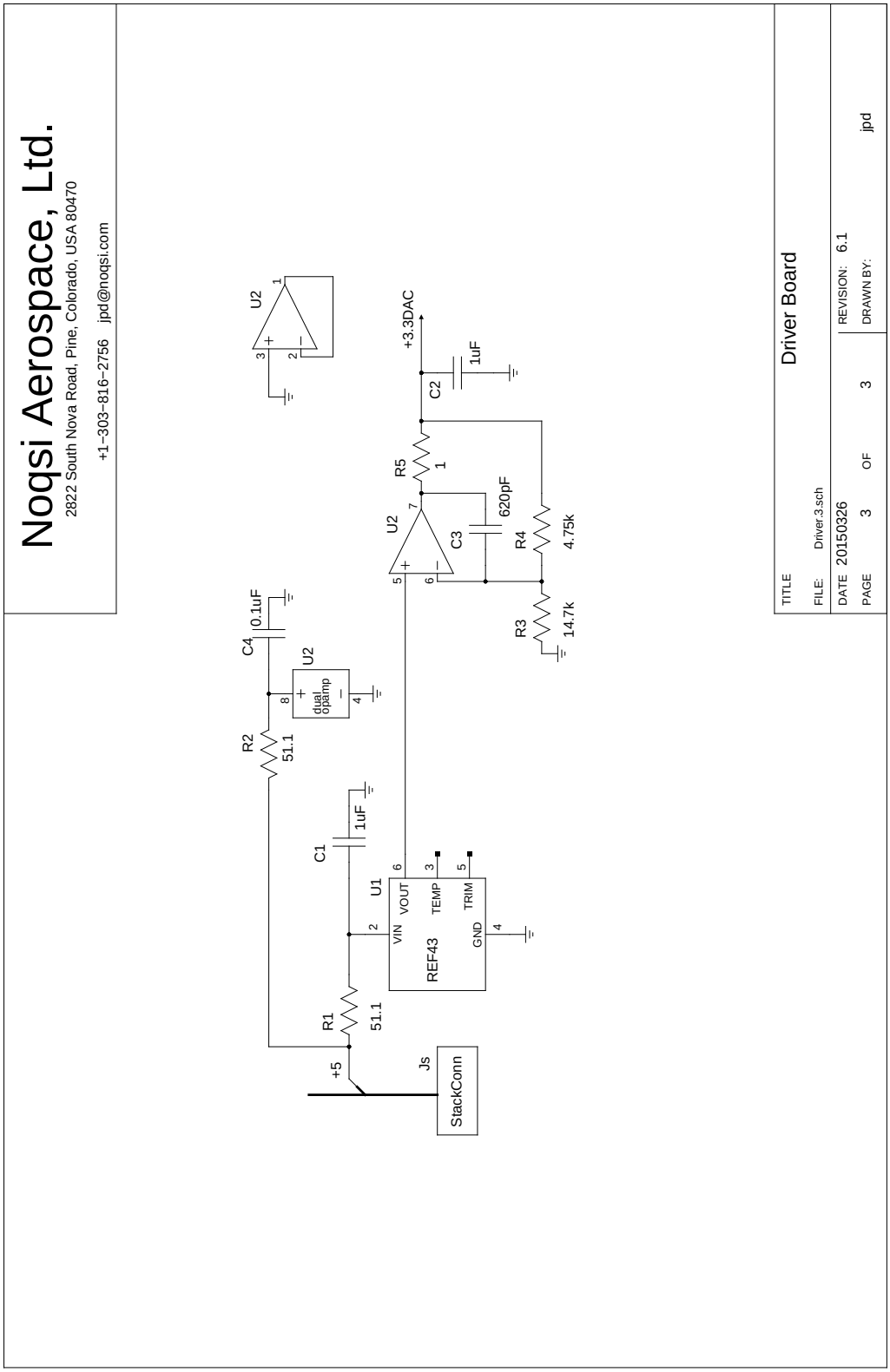

Figure 40: Driver.3

5 Stack Interconnection

Table 5: Inter-board Stack Connections

1	GND			101	ID-4		
		51	P1-FS-1			151	GND
2	SDO-A-1			102	P3-U-4		
		52	P2-FS-1			152	SDO-D-4
3	GND			103	P2-U-4		
		53	P3-FS-1			153	GND
4	SDO-B-1			104	P1-U-4		
		54	P3-OR-1			154	SDO-C-4
5	GND			105	P3-IA-4		
		55	P2-OR-1			155	GND
6	SDO-C-1			106	P2-IA-4		
		56	P1-OR-1			156	SDO-B-4
7	GND			107	P1-IA-4		
		57	RG-1			157	GND
8	SDO-D-1			108	RG-4		
		58	P1-IA-1			158	SDO-A-4
9	GND			109	P1-OR-4		
		59	P2-IA-1			159	GND
10	SCK			110	P2-OR-4		
		60	P3-IA-1			160	$\overline{\text{DS0}}$
11	GND			111	P3-OR-4		
		61	P1-U-1			161	GND
12	CNV			112	P3-FS-4		
		62	P2-U-1			162	$\overline{\text{DS8}}$
13	GND			113	P2-FS-4		
		63	P3-U-1			163	GND
14	Int			114	P1-FS-4		
		64	ID-1			164	$\overline{\text{DS16}}$
15	GND			115	SP3-FS-4		
		65	SP1-IA-1			165	GND
16	DeInt			116	SP2-FS-4		
		66	SP2-IA-1			166	$\overline{\text{DS24}}$
17	GND			117	SP1-FS-4		
		67	SP3-IA-1			167	GND
18	Clamp			118	SP3-IA-4		
		68	SP1-FS-1			168	$\overline{\text{DS32}}$
19	GND			119	SP2-IA-4		
		69	SP2-FS-1			169	GND
20	cwclk			120	SP1-IA-4		
		70	SP3-FS-1			170	$\overline{\text{DS40}}$
21	GND			121	HK80		
		71	HK0			171	GND
22	DD			122	HK88		
		72	HK8			172	SPARE
23	GND			123	HK96		
		73	HK16			173	GND
24	DCK			124	HK104		

		74	HK24			174	RTDCOM
25	GND			125	HK112		
		75	HK32			175	GND
26	SP1OR			126	HK120		
		76	HK40			176	+15
27	GND			127	HKA0		
		77	HK48			177	GND
28	SP2OR			128	HKA1		
		78	HK56			178	-12
29	GND			129	HKA2		
		79	HK64			179	GND
30	SP3OR			130	HKCOM		
		80	HK72			180	+5
31	GND			131	SP3-FS-3		
		81	SP1-IA-2			181	GND
32	SRG			132	SP2-FS-3		
		82	SP2-IA-2			182	$\overline{\text{DS48}}$
33	GND			133	SP1-FS-3		
		83	SP3-IA-2			183	GND
34	SID			134	SP3-IA-3		
		84	SP1-FS-2			184	$\overline{\text{DS56}}$
35	GND			135	SP2-IA-3		
		85	SP2-FS-2			185	GND
36	SP1U			136	SP1-IA-3		
		86	SP3-FS-2			186	$\overline{\text{DS64}}$
37	GND			137	ID-3		
		87	P1-FS-2			187	GND
38	SP2U			138	P3-U-3		
		88	P2-FS-2			188	$\overline{\text{DS72}}$
39	GND			139	P2-U-3		
		89	P3-FS-2			189	GND
40	SP3U			140	P1-U-3		
		90	P3-OR-2			190	$\overline{\text{DS80}}$
41	GND			141	P3-IA-3		
		91	P2-OR-2			191	GND
42	$\overline{\text{DS96}}$			142	P2-IA-3		
		92	P1-OR-2			192	$\overline{\text{DS88}}$
43	GND			143	P1-IA-3		
		93	RG-2			193	GND
44	SDO-A-2			144	RG-3		
		94	P1-IA-2			194	SDO-D-3
45	GND			145	P1-OR-3		
		95	P2-IA-2			195	GND
46	SDO-B-2			146	P2-OR-3		
		96	P3-IA-2			196	SDO-C-3
47	GND			147	P3-OR-3		
		97	P1-U-2			197	GND
48	SDO-C-2			148	P3-FS-3		
		98	P2-U-2			198	SDO-B-3
49	GND			149	P2-FS-3		

		99	P3-U-2			199	GND
50	SDO-D-2			150	P1-FS-3		
		100	ID-2			200	SDO-A-3

6 Operating parameters and Housekeeping Channels

While the implementation details differ, the housekeeping channels and the DAC-controlled parameters share a common addressing scheme. An address is seven bits. All seven are provided to the multiplexors and their selection logic as HKA[6:0]. The most significant four bits DCS[3:0] drive the DAC selection logic: the least significant three bits are part of the serial command that sets a DAC. In the following tables CC represents two bits selecting the CCD in offset binary (00⇒CCD1, 01⇒CCD2, 10⇒CCD3, 11⇒CCD4).

The control ranges often go outside the actual range allowed for the parameters, which depend on circuit details and power supply voltages. I will document these limits in the future. Control is sometimes relative to another parameter. If the control range is not given, the parameter is not under DAC control.

6.1 Bias Group

Table 6: Bias Group

Address 0CCXXXX			
XXXX	Housekeeping Signal	Scale	Control Range
0000	Output Gate	±16.5V	-8.0V, 4.0V
0001	Input Gate 1	±16.5V	-8.0V, 4.0V
0010	Input Gate 2	±16.5V	-8.0V, 4.0V
0011	Scupper	±16.5V	0, 15.0V
0100	Reset Drain	±16.5V	0, 15.0V
0101	Backside	±16.5V	0, 5.0V
0110	Substrate	±82V	0, -50V
0111	Board Temperature	±360K	
1000	Output Drain A	±27.3V	0, 10.0V†
1001	Output Drain B	±27.3V	0, 10.0V†
1010	Output Drain C	±27.3V	0, 10.0V†
1011	Output Drain D	±27.3V	0, 10.0V†
1100	Output Source A	±27.3V	
1100	Output Source B	±27.3V	
1100	Output Source C	±27.3V	
1100	Output Source D	±27.3V	

† Relative to Reset Drain for the specified chip

6.2 Clock Driver Group

Table 7: Clock Driver Group

Address 10CCXXX			
XXX	Housekeeping Signal	Scale	Control Range
000	Parallel High	±16.5V	0, 18.1V†
001	Parallel Low	±16.5V	0, -13.2V
010	Serial High	±16.5V	14.9V, -14.9V
011	Serial Low	±16.5V	14.9V, -14.9V
100	Reset High	±16.5V	14.9V, -14.9V
101	Reset Low	±16.5V	14.9V, -14.9V
110	Input Diode High	±16.5V	0, +15.0V
111	Input Diode Low	±16.5V	0, +15.0V

† Relative to Parallel Low for the specified chip

6.3 Heater Group

Table 8: Heater Group

Address 1100000			
XXX	Housekeeping Signal	Scale	Control Range
1100000	Heater Current	±418mA	0, 12.5V†

† Control range in mA depends on the external heater resistance

6.4 Interface Group

Table 9: Interface Group

Address 1101XXX		
XXX	Housekeeping Signal	Scale
000	Board Temperature	±360K
001	+15	±16.5V
010	+5	±16.5V
011	-12	±16.5V
100	+3.3F	±16.5V
101	+2.5F	±16.5V
110	+1.8F	±16.5V
111	+1F	±16.5V

Table 10: Thermal Group

Address 111XXXX		
XXX	Housekeeping Signal	Scale
0000	Pt1000 sensor 1	-125C, +130C
0001	Pt1000 sensor 2	-125C, +130C
0010	Pt1000 sensor 3	-125C, +130C
0011	Pt1000 sensor 4	-125C, +130C
0100	Pt1000 sensor 5	-125C, +130C
0101	Pt1000 sensor 6	-125C, +130C
0110	Pt1000 sensor 7	-125C, +130C
0111	Pt1000 sensor 8	-125C, +130C
1000	Pt1000 sensor 9	-125C, +130C
1001	Pt1000 sensor 10	-125C, +130C
1010	Pt1000 sensor 11	-125C, +130C
1011	Pt1000 sensor 12	-125C, +130C
1100	AlCu sensor CCD1	-150C, +40C
1101	AlCu sensor CCD2	-150C, +40C
1110	AlCu sensor CCD3	-150C, +40C
1111	AlCu sensor CCD4	-150C, +40C

6.5 Thermal Group

The Thermal Group (Table 10) sensors are external temperature-sensitive resistors. The nominal range for the circuitry is 500Ω to 1500Ω, which translates into the given temperature ranges. It may be useful to calibrate the board using external fixed resistors near the limits of the range.