TESS Focal Plane Electronics Manual

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Fri Sep 4 16:20:40 2015 -0400

Very Preliminary Edition

Version 6.1.12.dev9
Tag 6.1.12.dev9

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1 Introduction

The TESS Focal Plane Electronics (FPE) serve as the intermediary between the four CCD sensors on a focal plane and the Data Handling Unit (DHU). Three boards make up a full FPE assembly: Video (§2), Interface (§3), and Driver (§4). The boards are connected by a 200 pin bus implemented with stacking connectors.

Each CCD has independent clock and bias level controls. This makes the FPE robust against short-circuit failure of a CCD: in that case setting clock levels to zero will minimize fault current. Each CCD also has independent parallel clock timing to enable staggered frame store operations. This helps with the trade-off between the need to minimize the power surge due to the rapid clocking of high capacitance gates during transfer and the desire to minimize streaking by clocking as rapidly as possible. Timing of other CCD clocks is synchronous among the four CCDs.

The Driver board is not strictly necessary in a testing environment. Without the Driver board, CCD 1 and CCD 2 are fully functional. The driver board supplies clocks for CCD 3 and CCD 4. A passive jumper board that connected CCD 1 clocks to CCD 3 and CCD 2 clocks to CCD 4 would allow operation of four CCDs without a driver board, but without as much independence of clock timing and voltages.

2 Video Board

2.1 Input and Signal Processing Strategy

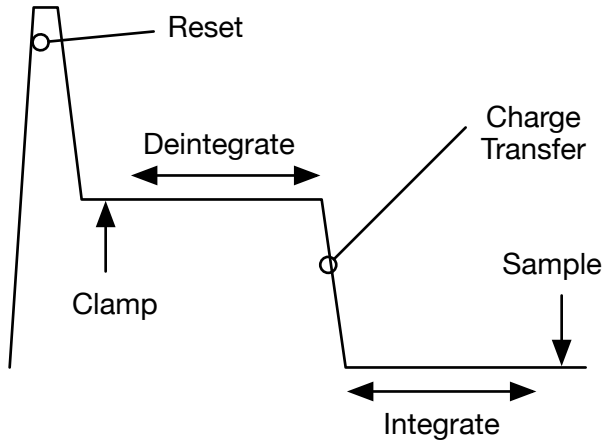

Figure 1: Video Signal From CCD

Figure 1 shows voltage versus time for a typical CCD video signal. The reset pulse resets the output node to a reference voltage that is approximately constant. However, that voltage is relatively large

(10–15V) and somewhat uncertain due to switching ("kTC") noise. Then, we transfer electrons into the output node, resulting in a negative voltage step proportional to the charge.

We measure the height of the step with a three-stage process. First, we couple the signal into our measurement chains through a capacitor. On the output side of the capacitor, we have a "clamp": a switch that forces the signal to a more reasonable level (about 3V for TESS). After we release the clamp, we "deintegrate", averaging the baseline level before charge transfer. After charge transfer, we "integrate", averaging the level after charge transfer. The difference in the averages is our best estimate the height of the step. We sample that difference and digitize it. In CCD jargon, this is "correlated double sampling". Our approach combines the common "clamp/sample" and "Dual slope" approaches.

2.2 Building blocks

2.2.1 The Video Measurement Chain

Figure 2 shows the signal path through the measurement chain. Q2 is the active current load for the CCD output. R1 controls the current. As shown, it sinks ≈ 0.5 mA.

U3 is the clamp. U4 buffers the clamped video. R7, R8, and C18 control the buffer gain: for maximum dynamic range we will use unity gain. U8 is the integrator that performs the signal averaging. U11 and U12 switch its inputs to control the sign of the the input signal for the deintegrate and integrate phases.

U5 inverts the video signal, so the input to the integrator is positive during the integrate phase. It also attenuates the signal slightly to achieve greater dynamic range. R11 is reduced relative to R38 to compensate for this attenuation, keeping the correlated double sampling balanced.

U9, the ADC, uses a differential input. U6 inverts the integrator output to provide this. Filters R14/C20 and R13/C21 provide some anti-aliasing, limiting the effect of broadband noise at the outputs of U6 and U8. The ADC does not work well for a rapidly slewing input: U11 and U12 should both be off for an adequate time to allow the ADC inputs to settle before the ADC samples.

Jerry, Joel, and I need to get together, compare sims and reality, and define what the timing diagram should really be -jpd

R25 feeds a current proportional to the CCD output voltage to the housekeeping circuitry for monitoring the DC component. R41 prevents the voltage on the line from exceeding the limit of the housekeeping multiplexor.

C4 should be a low hysteresis capacitor, not a common NP0. It's split because commercial capacitors of this type are difficult to obtain for values > 100 pF. For flight, this may be a single capacitor.

Figure 3 shows the support circuitry for the measurement chain. U10 provides local voltage regulation.

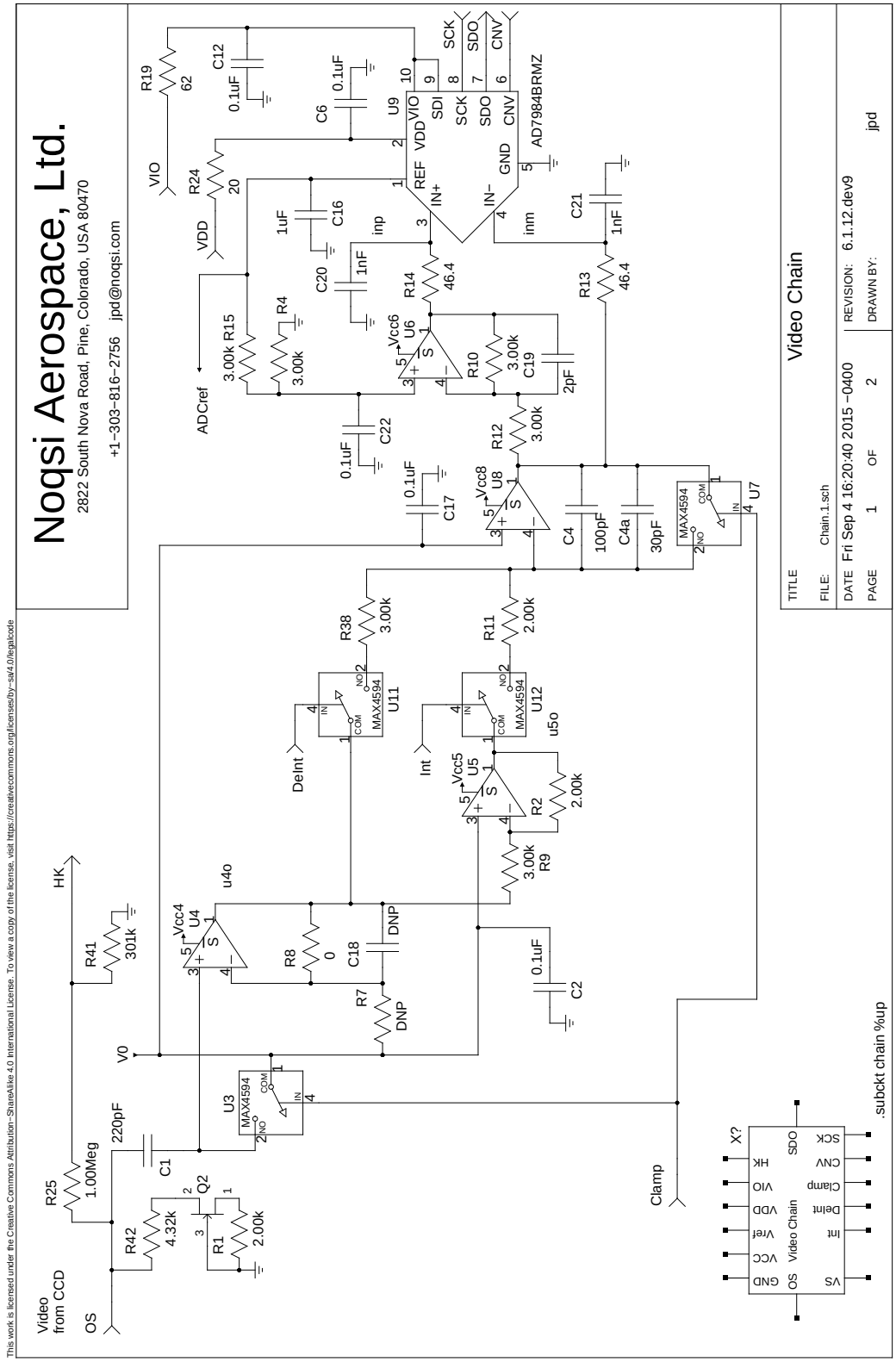

Figure 2: Chain.1

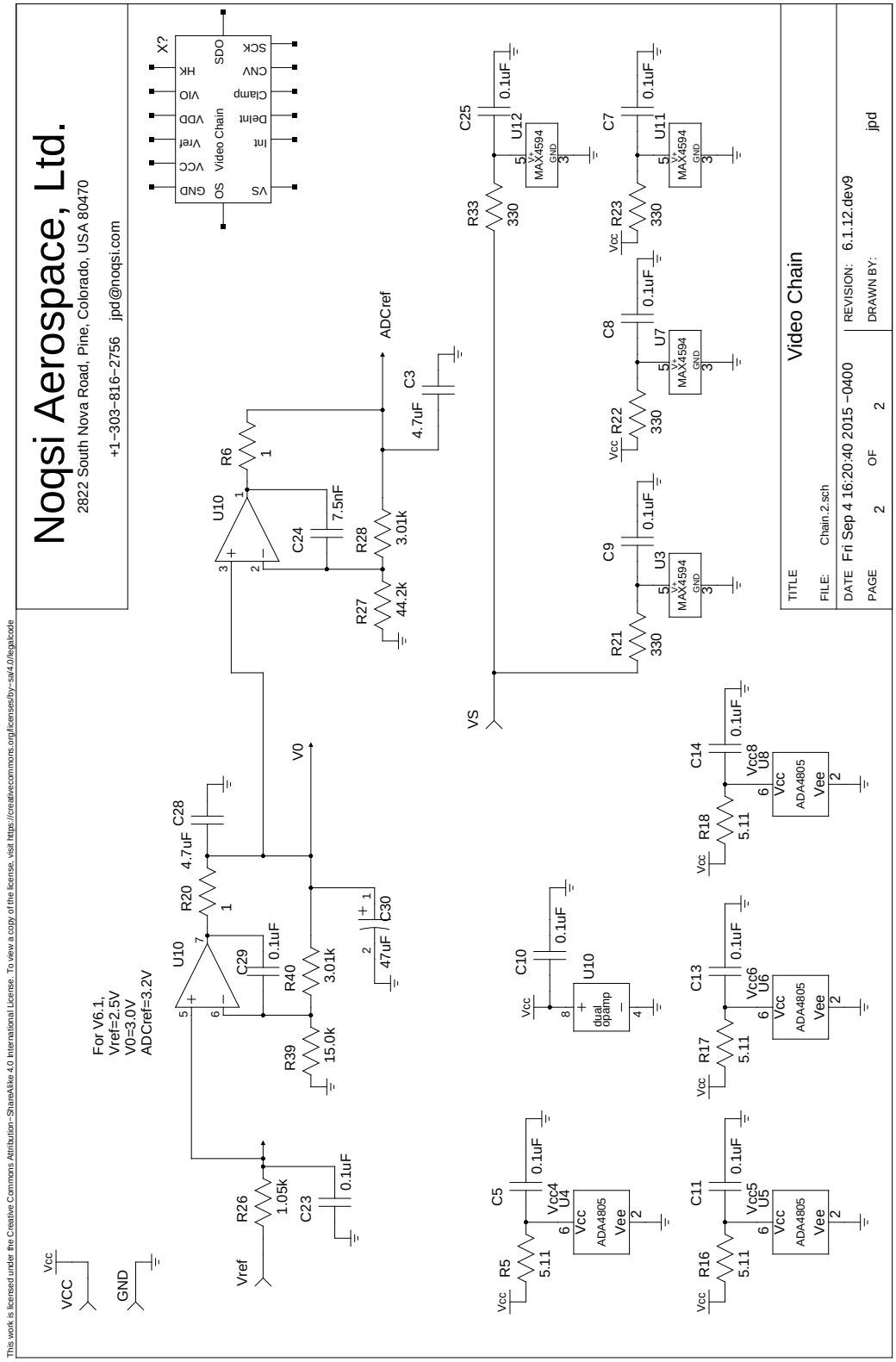

Figure 3: Chain.2

2.2.2 Drain Regulator

To protect the CCD charge sense MOSFET from overvoltage, the output drain voltage range is controlled relative to the CCD reset drain. Since the reset drain voltage controls the gate voltage on the sense MOSFET, limiting the difference to 10V limits the gate-drain voltage (see CCID80 data sheet).

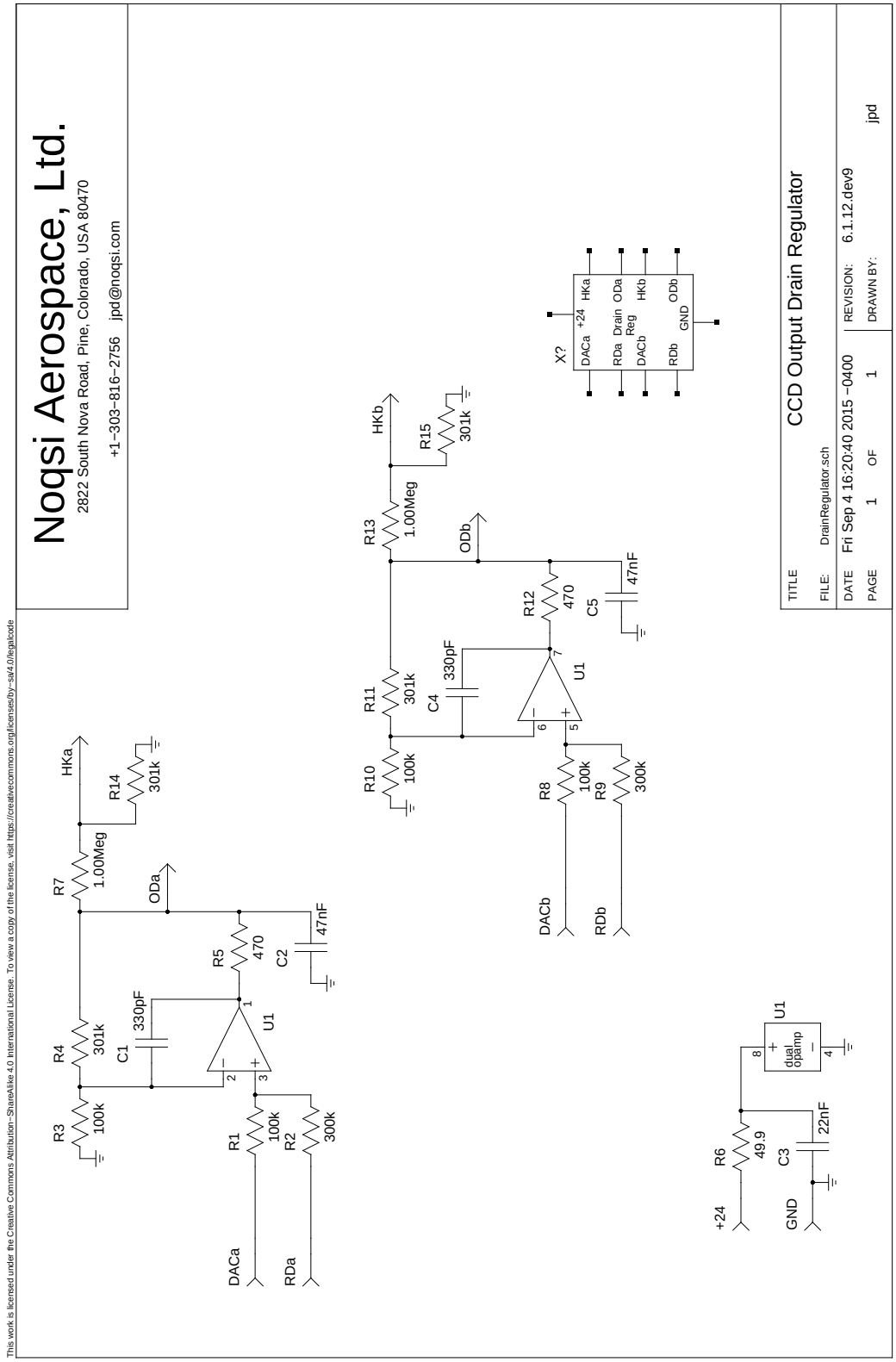

Figure 4: DrainRegulator

2.2.3 Per-Chip Circuitry

Most of the Video board is consists of four blocks devoted to per-chip video processing and operating bias generation. In each block, there is a video measurement chain for each segment (Figure 5). Figure 6 shows local fixed voltage regulation and the variable output gate regulator. Figures 7–10 show regulators for other variable CCD biases. Figures 11 and 12 show the DACs and housekeeping multiplexors that support these functions, as tabulated in Table 7 in Section 6.

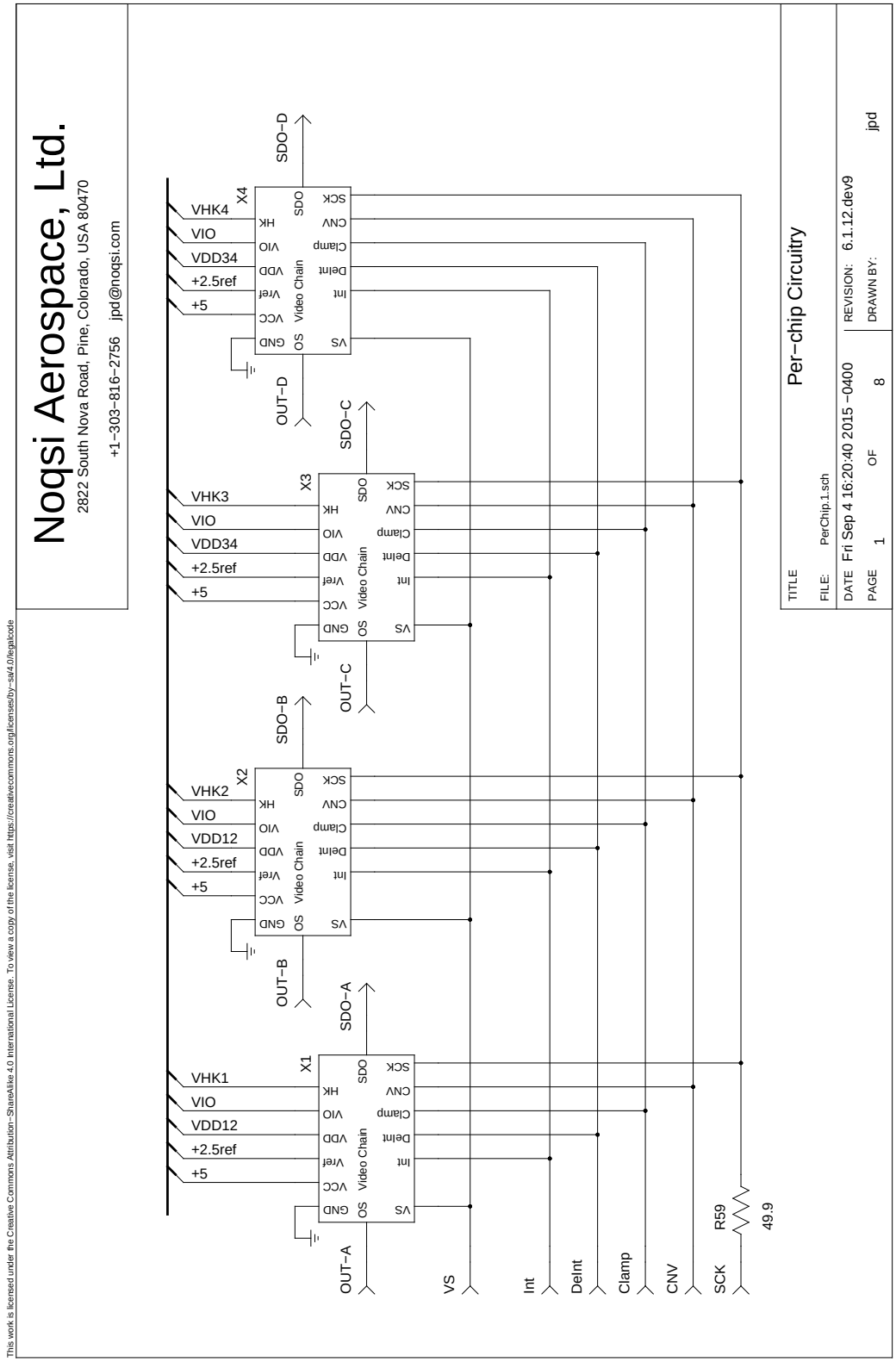

Figure 5: PerChip.1

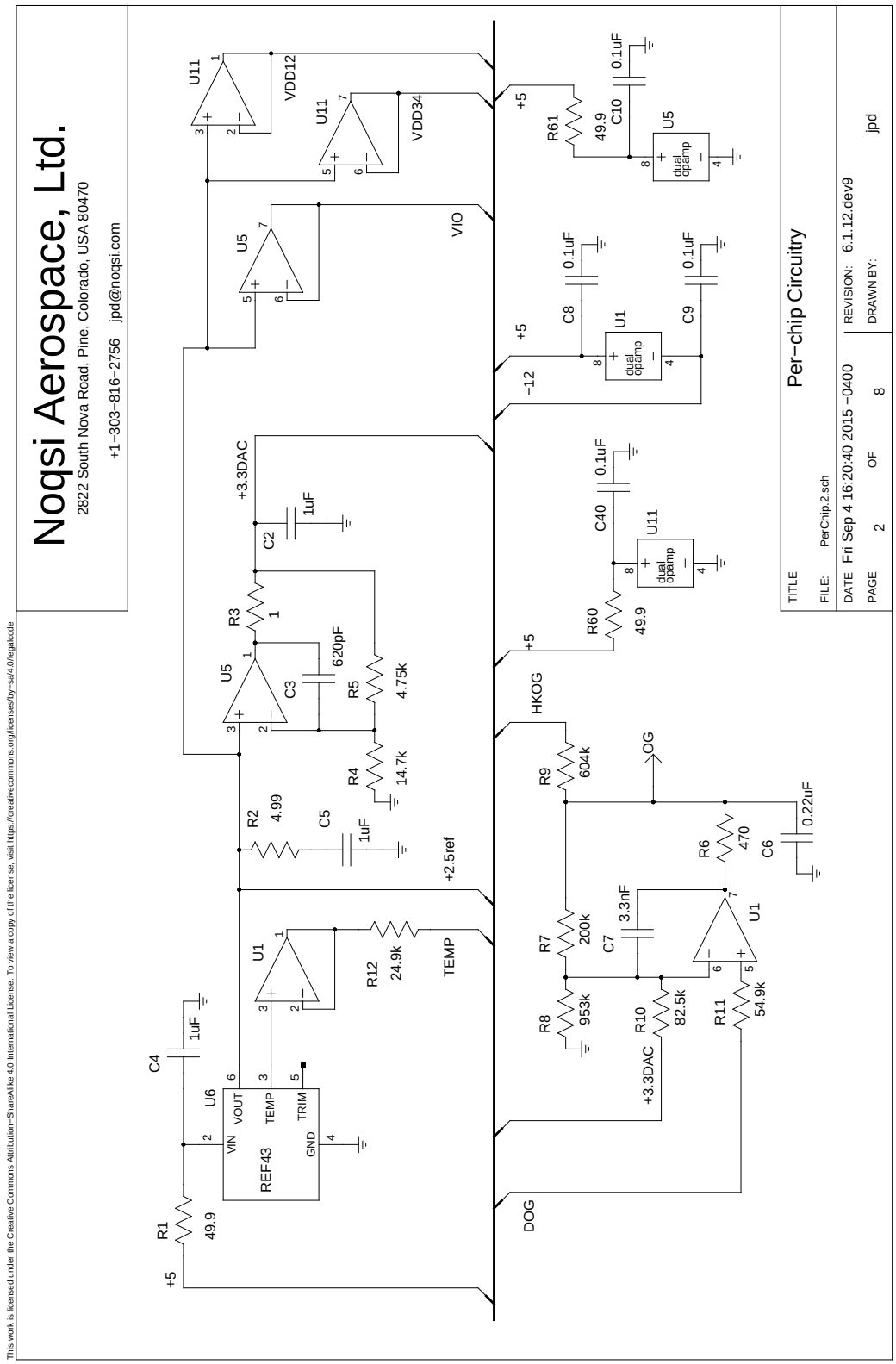

Figure 6: PerChip.2

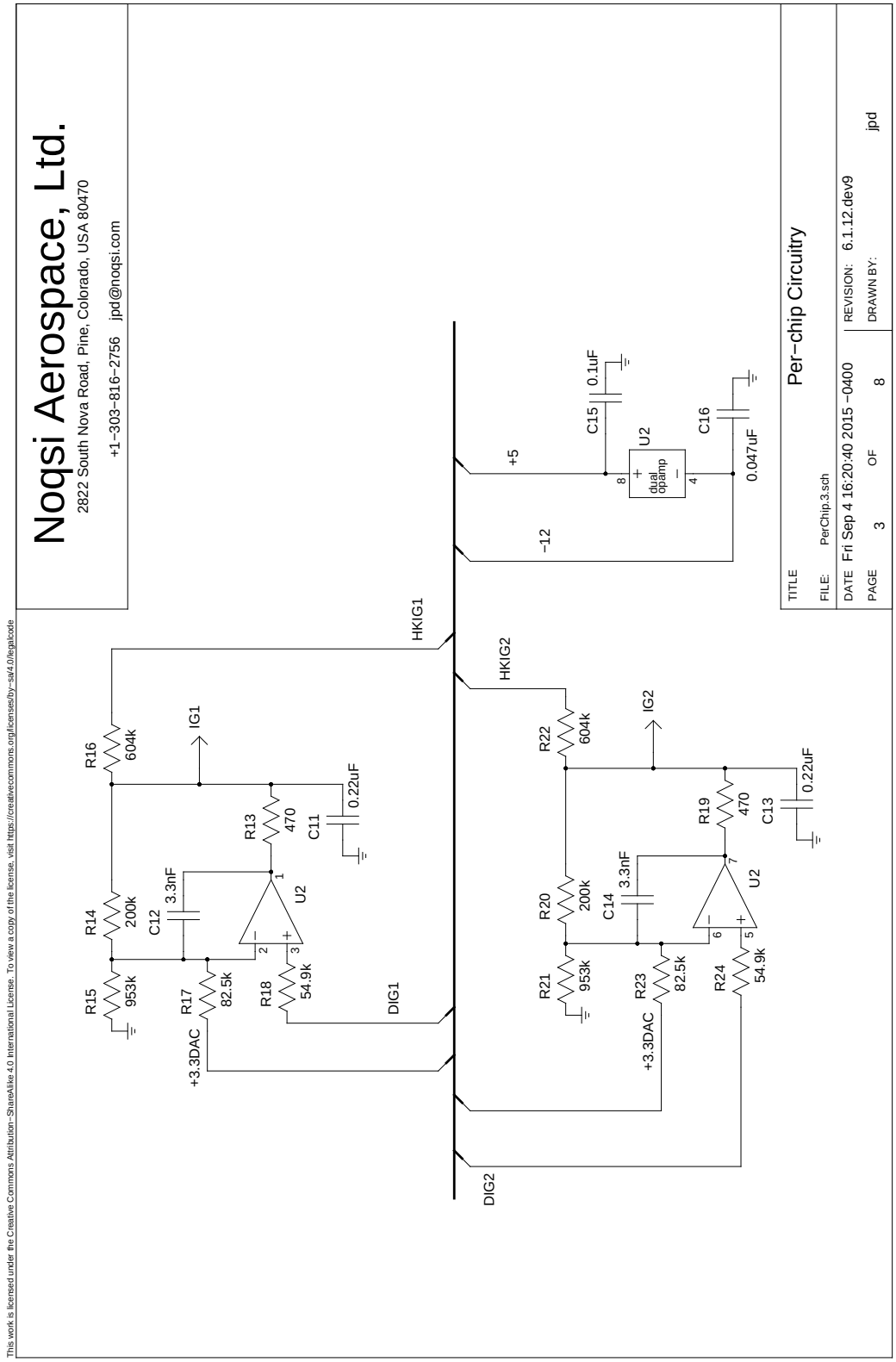

Figure 7: PerChip.3

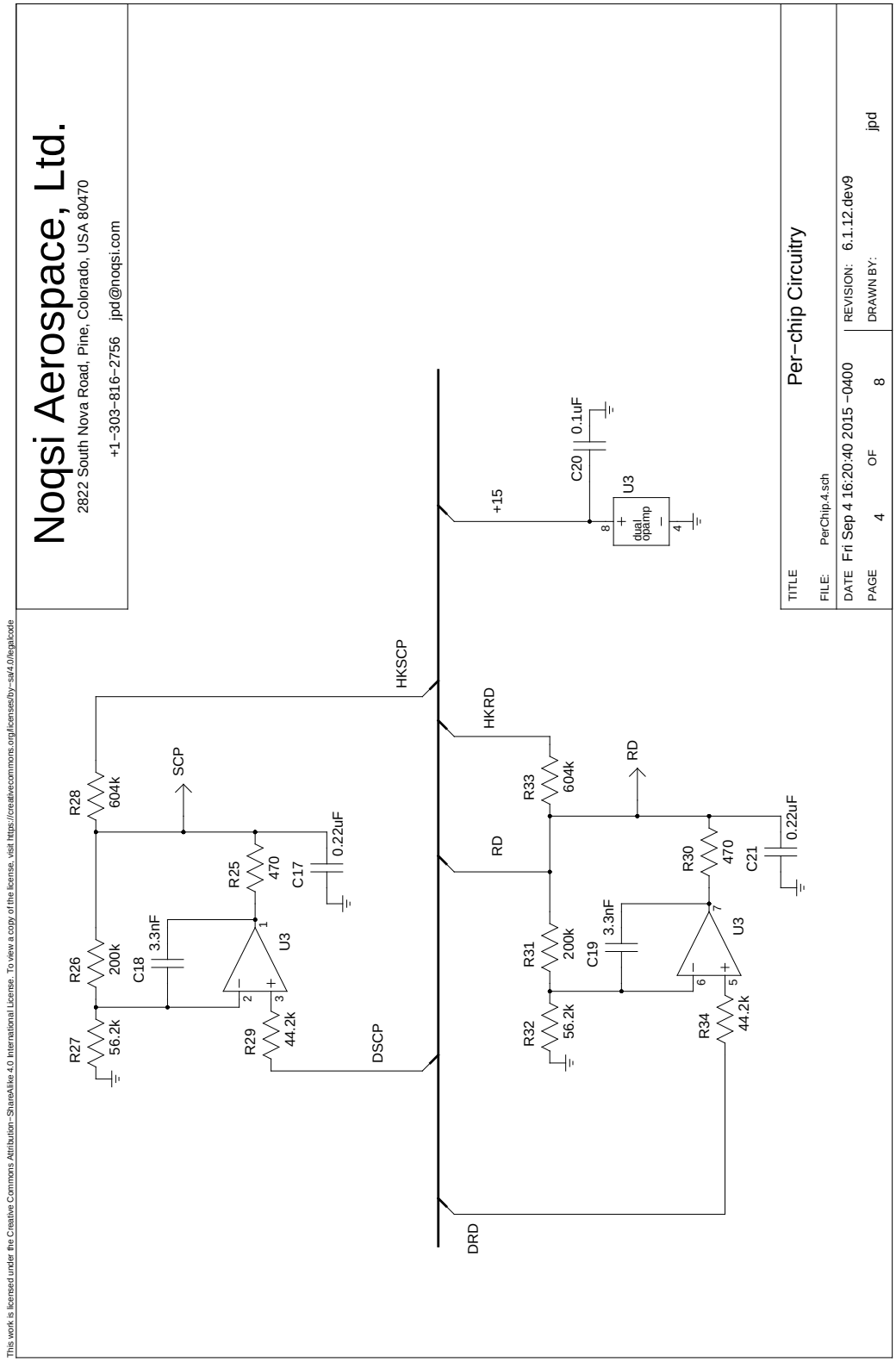

Figure 8: PerChip.4

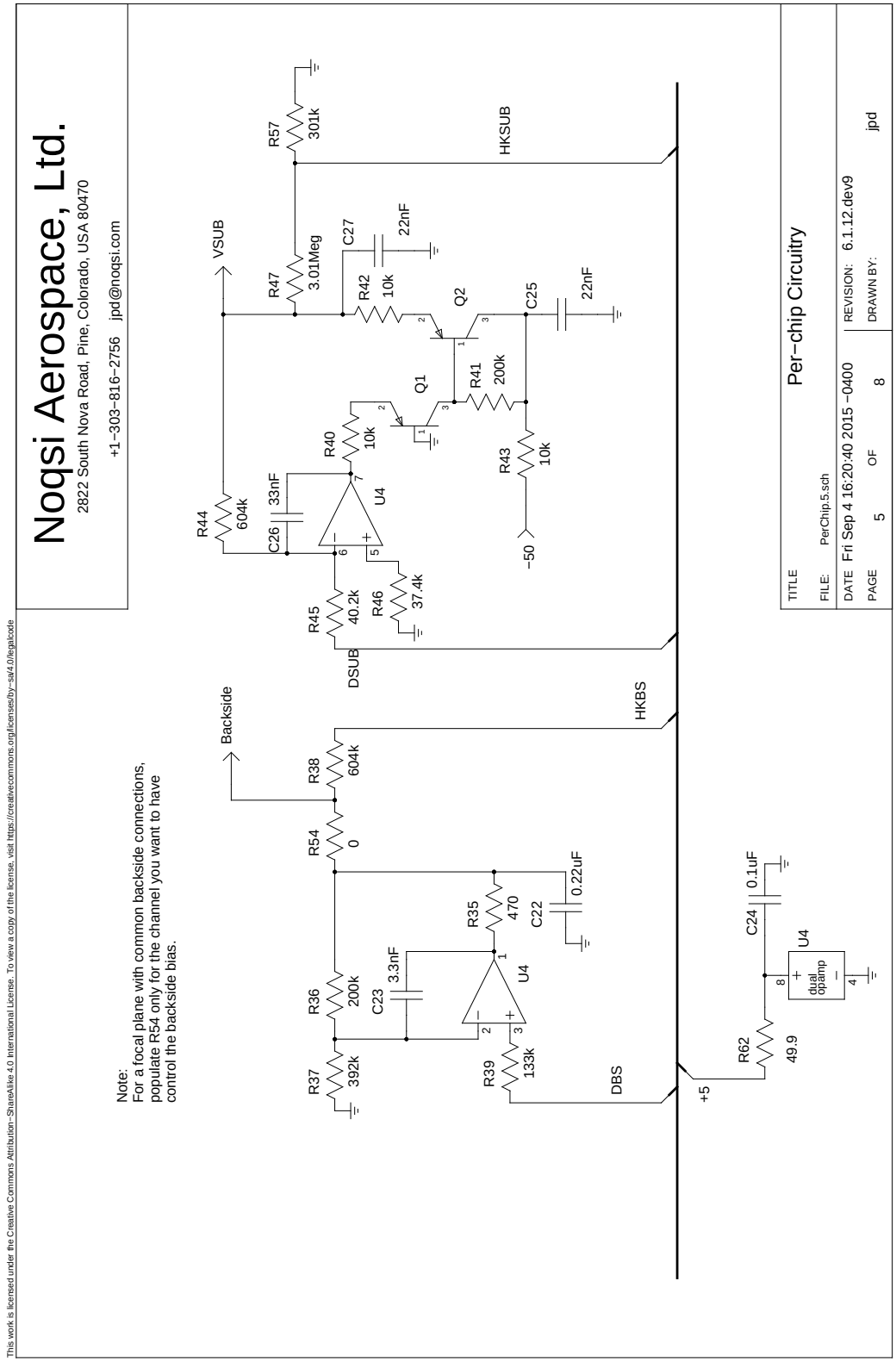

Figure 9: PerChip.5

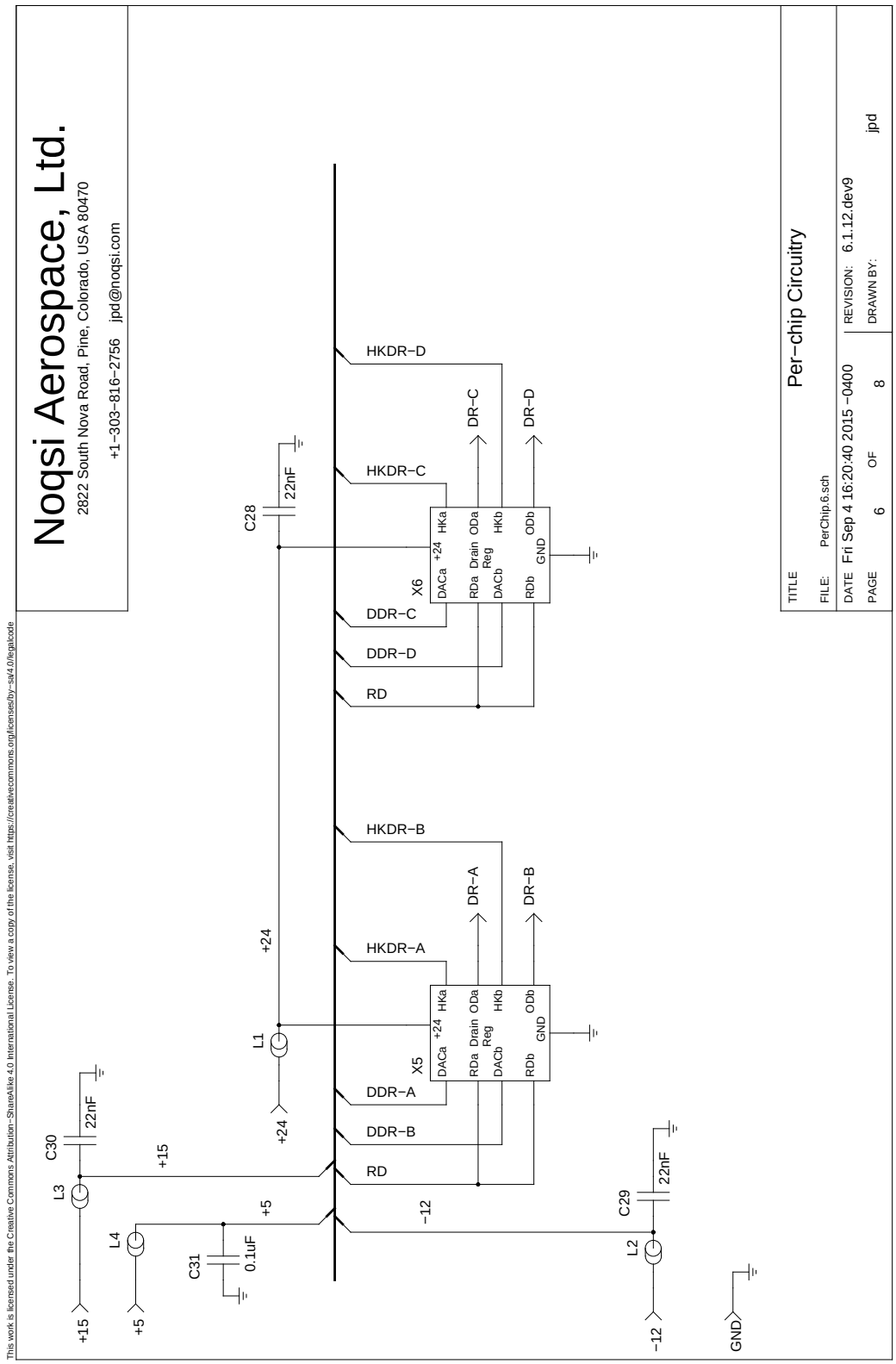

Figure 10: PerChip.6

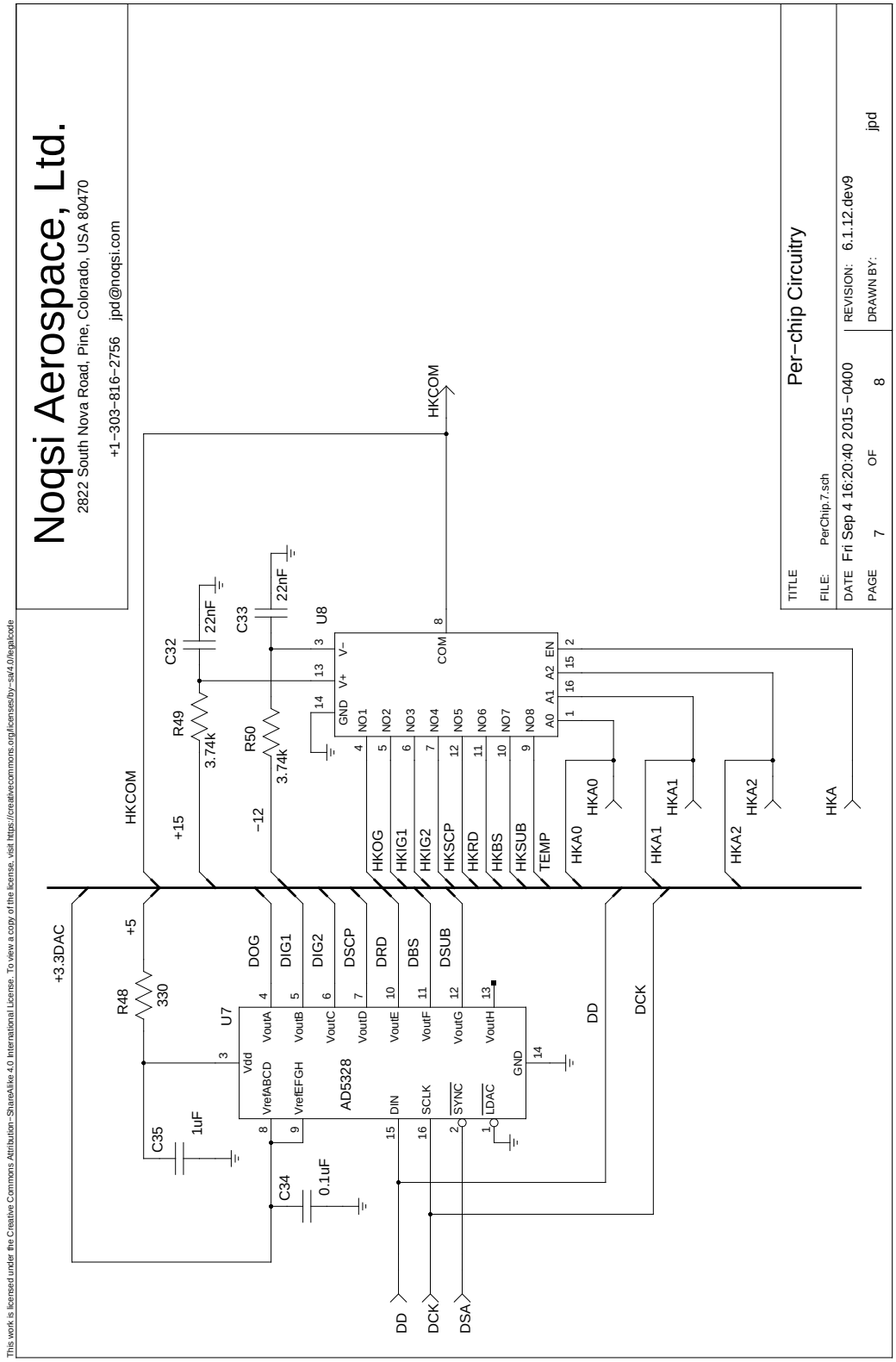

Figure 11: PerChip.7

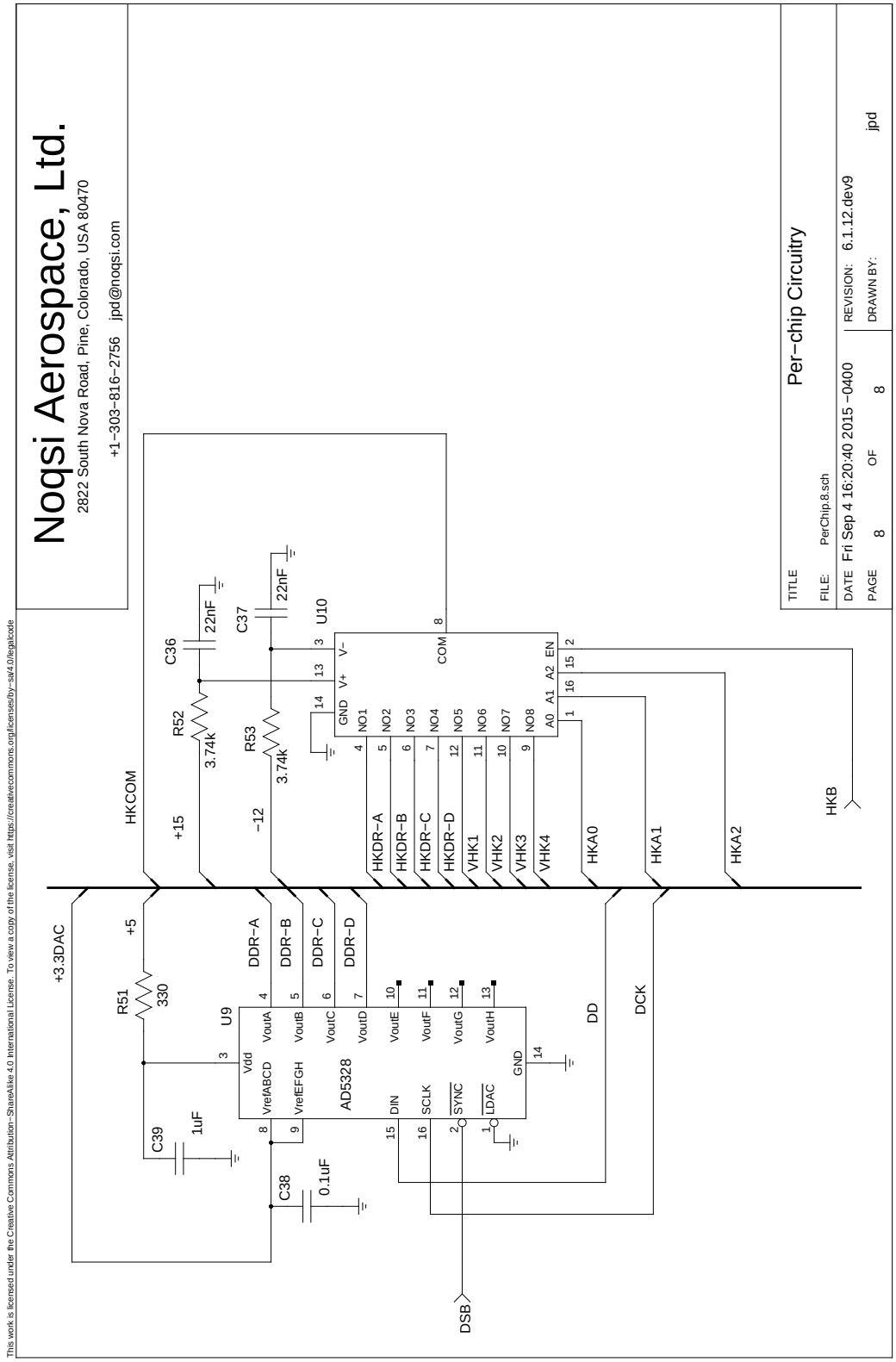

Figure 12: PerChip.8

2.2.4 Charge Pumps

The CCD output drains and substrate bias require modest currents at voltages outside the power supply rails. In Figure 13, U1, Q5, and Q6 generate a $\approx$ 25V peak-to-peak square wave. This is AC-coupled to a pair of Cockroft-Walton diode/capacitor ladders to make 24V (nominal) for the drain regulators, and -50V (nominal) for the substrate regulator.

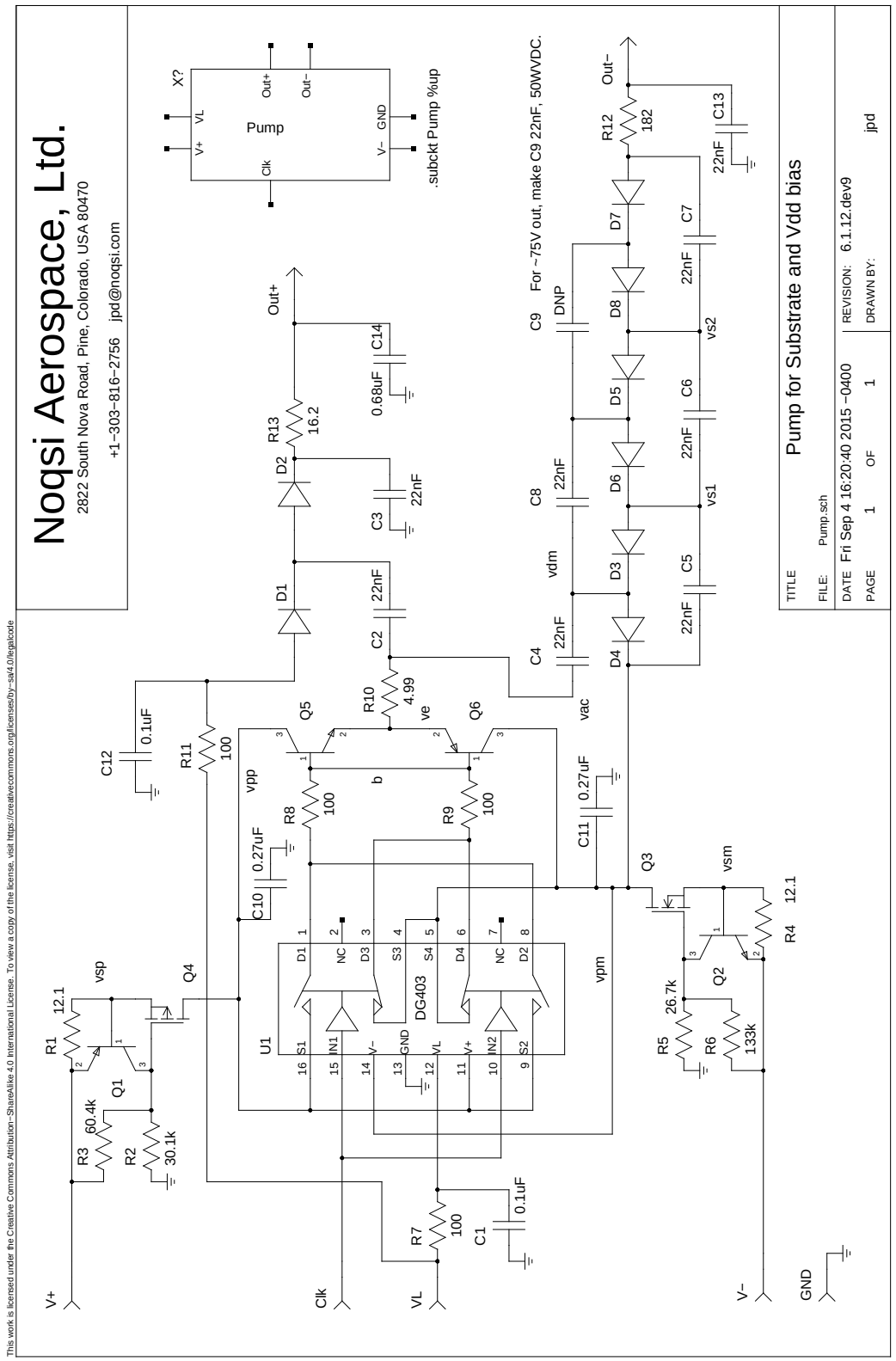

Figure 13: Pump

2.3 Video Board Top Level

Figures 14-17 show the connections to the per-chip blocks.

Figure 18 shows the readout circuitry for the resistive temperature sensors on the CCD chip and camera structure. U1 is a fixed current source. U5 and U7 steer the current to the selected sensor. U6 and U8 select the resulting voltage, transmitting it to RTDCOM on the stacking connector. This goes to the housekeeping ADC on the Interface board.

Figure 19 shows more local voltage generation and regulation. VS12 and VS34 are regulated 4.8V for the switches in the measurement chains: these need tight regulation to control charge injection.

Figure 20 shows filters on the output gates. Since the output gates are next to the charge sense node, they may be a source of noise or crosstalk.

Figure 21 shows the control circuit for the trim heater. Q1 is an LM195: an IC that behaves like a transistor except that it shuts down if it becomes too hot.

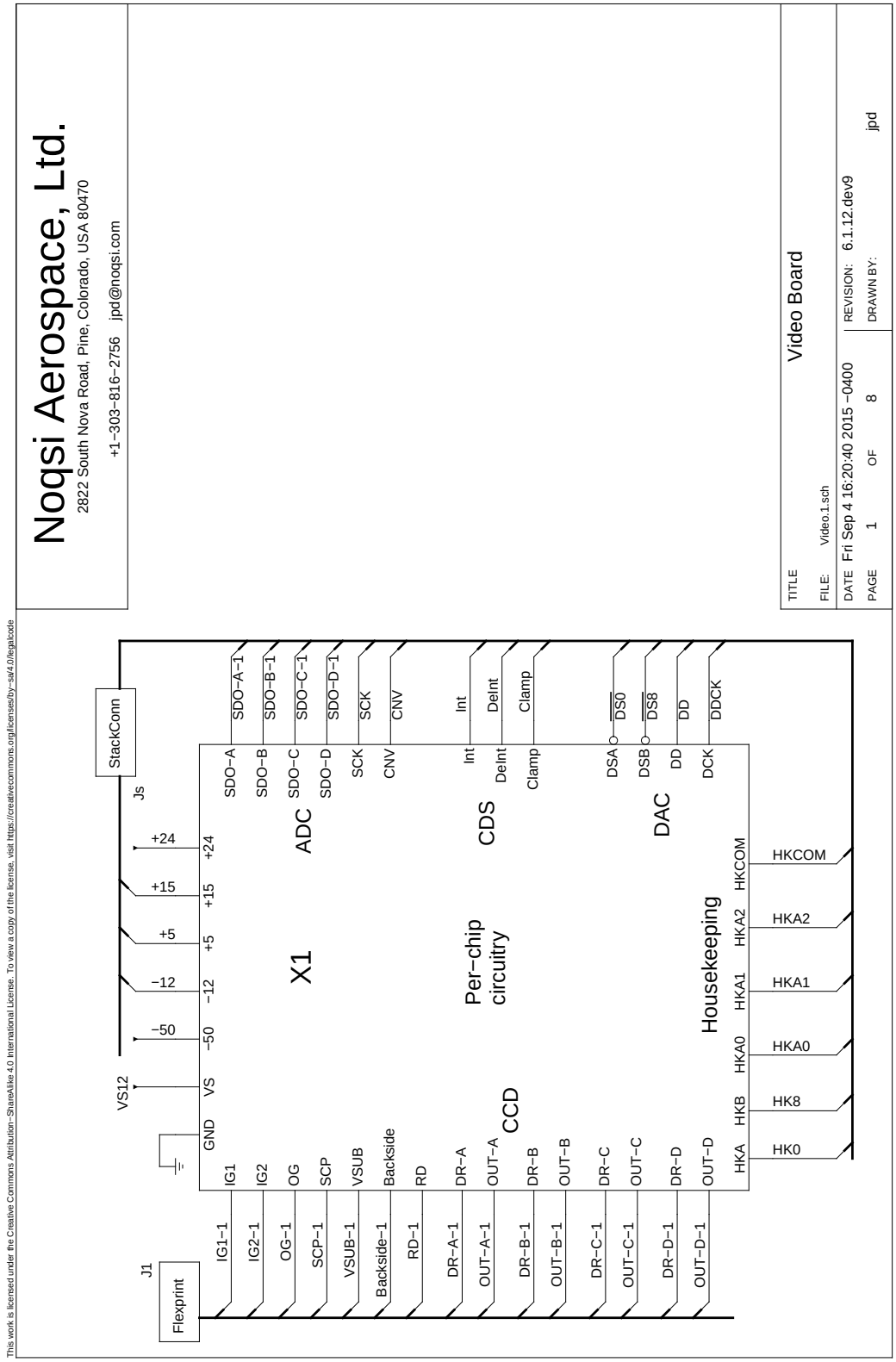

Figure 14: Video.1

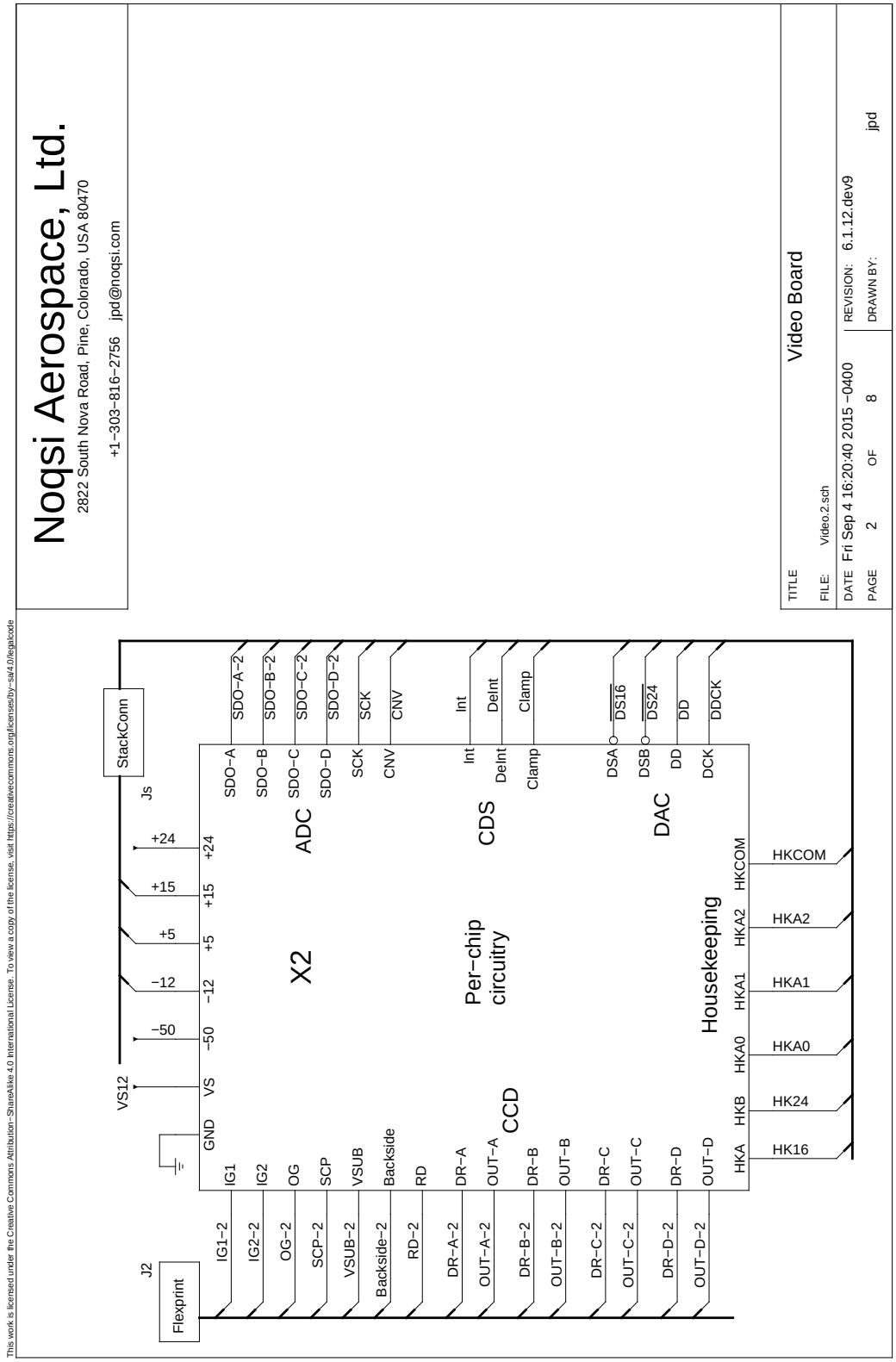

Figure 15: Video.2

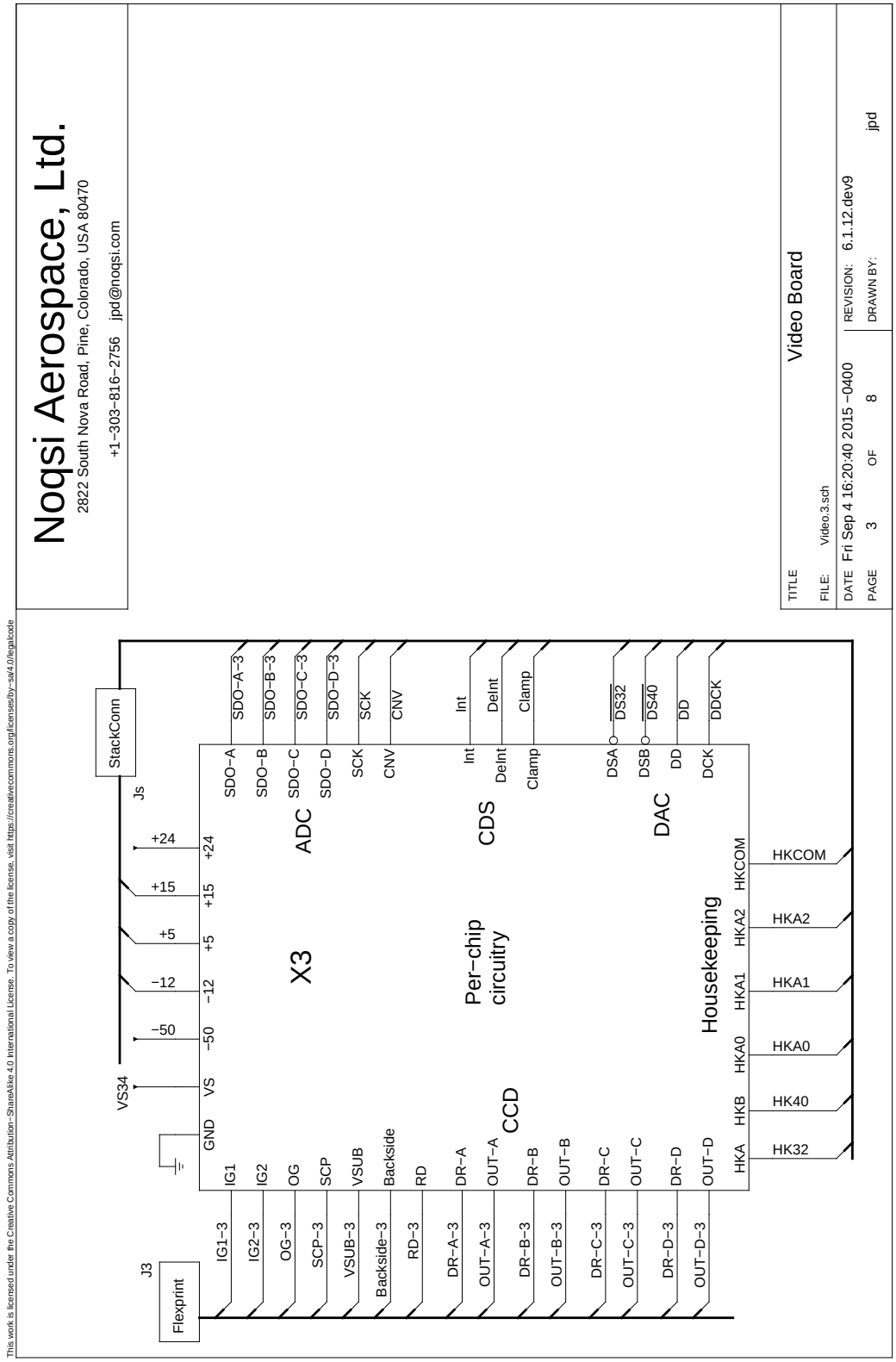

Figure 16: Video.3

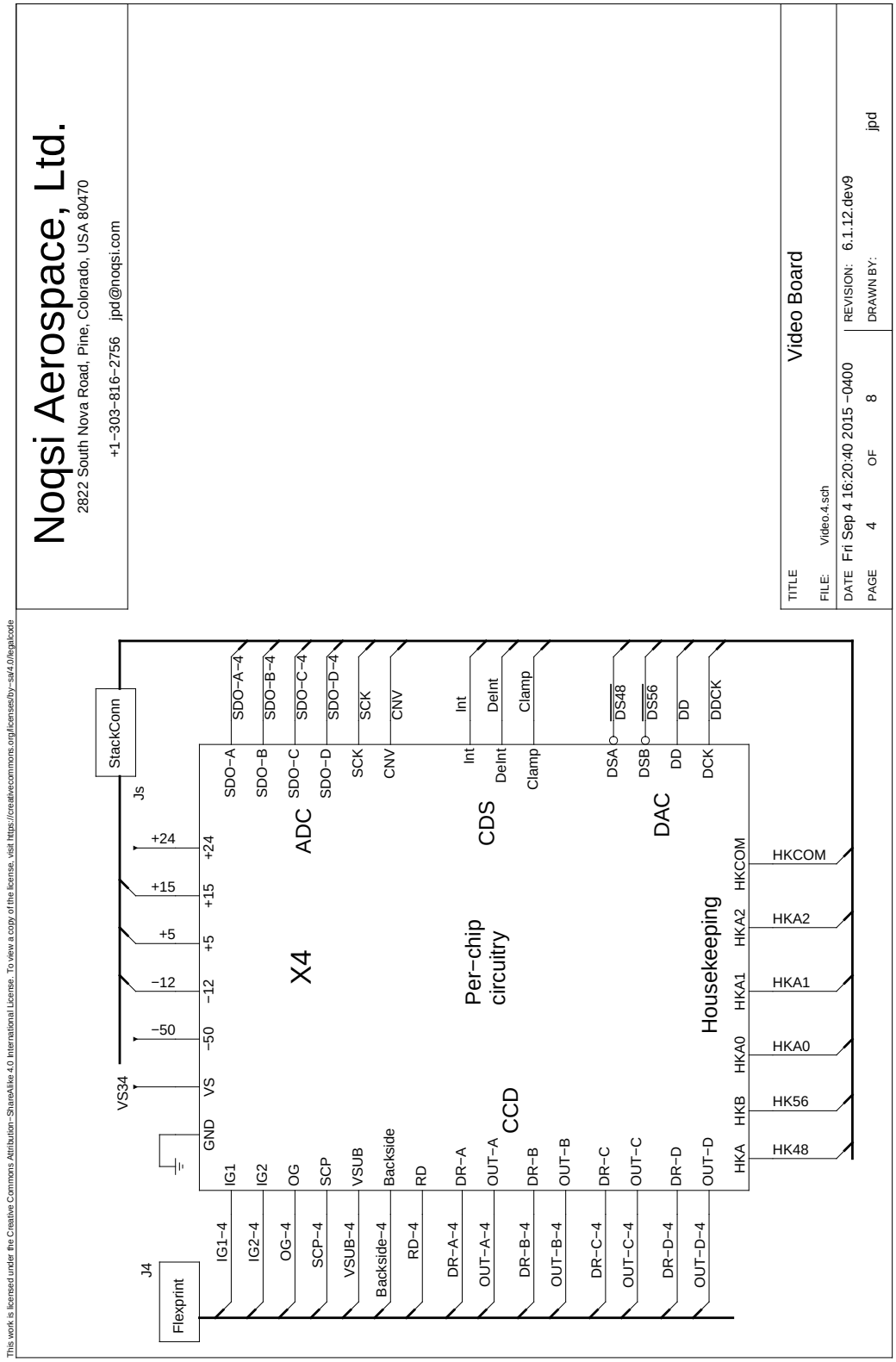

Figure 17: Video.4

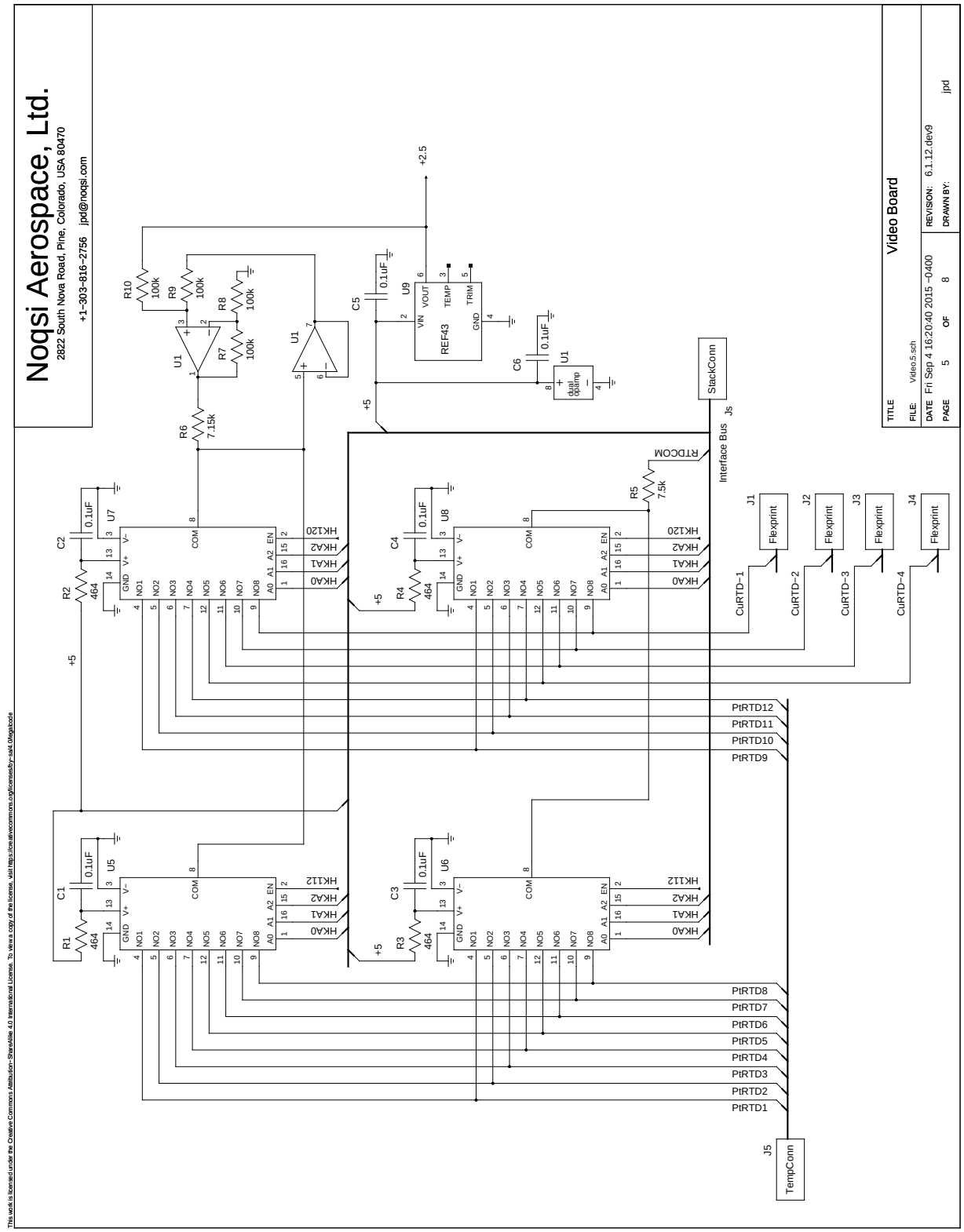

Figure 18: Video.5

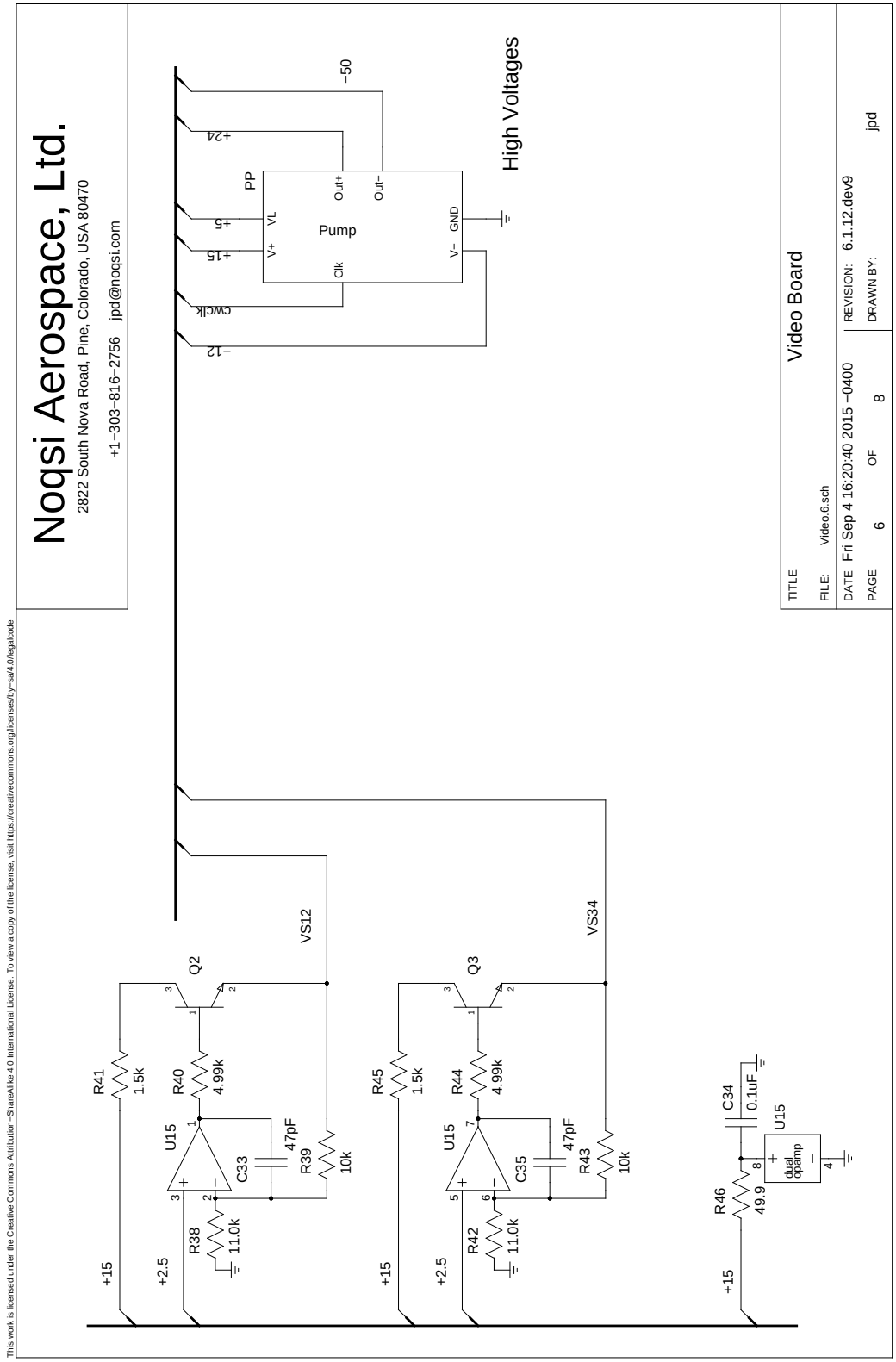

Figure 19: Video.6

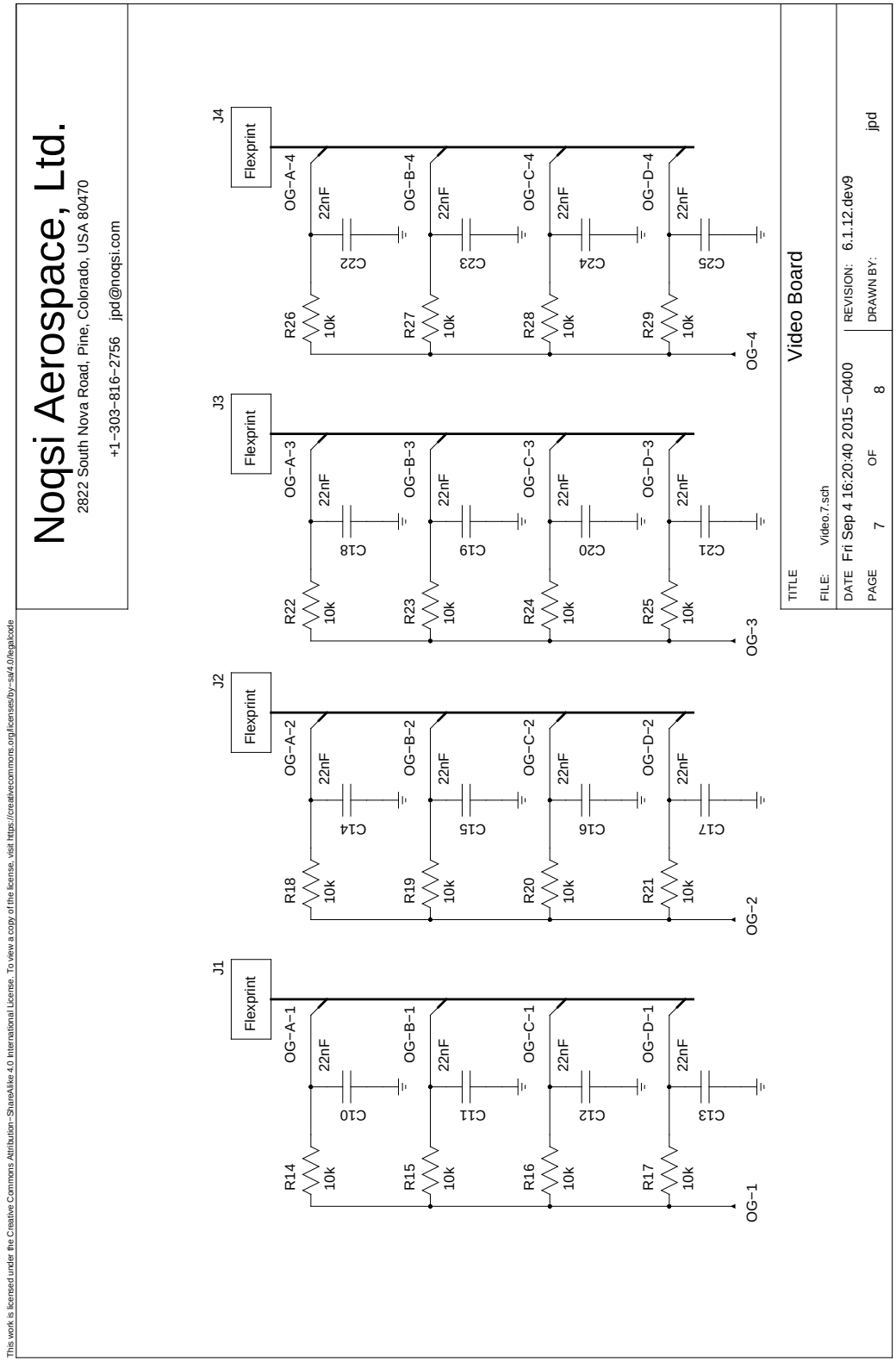

Figure 20: Video.7

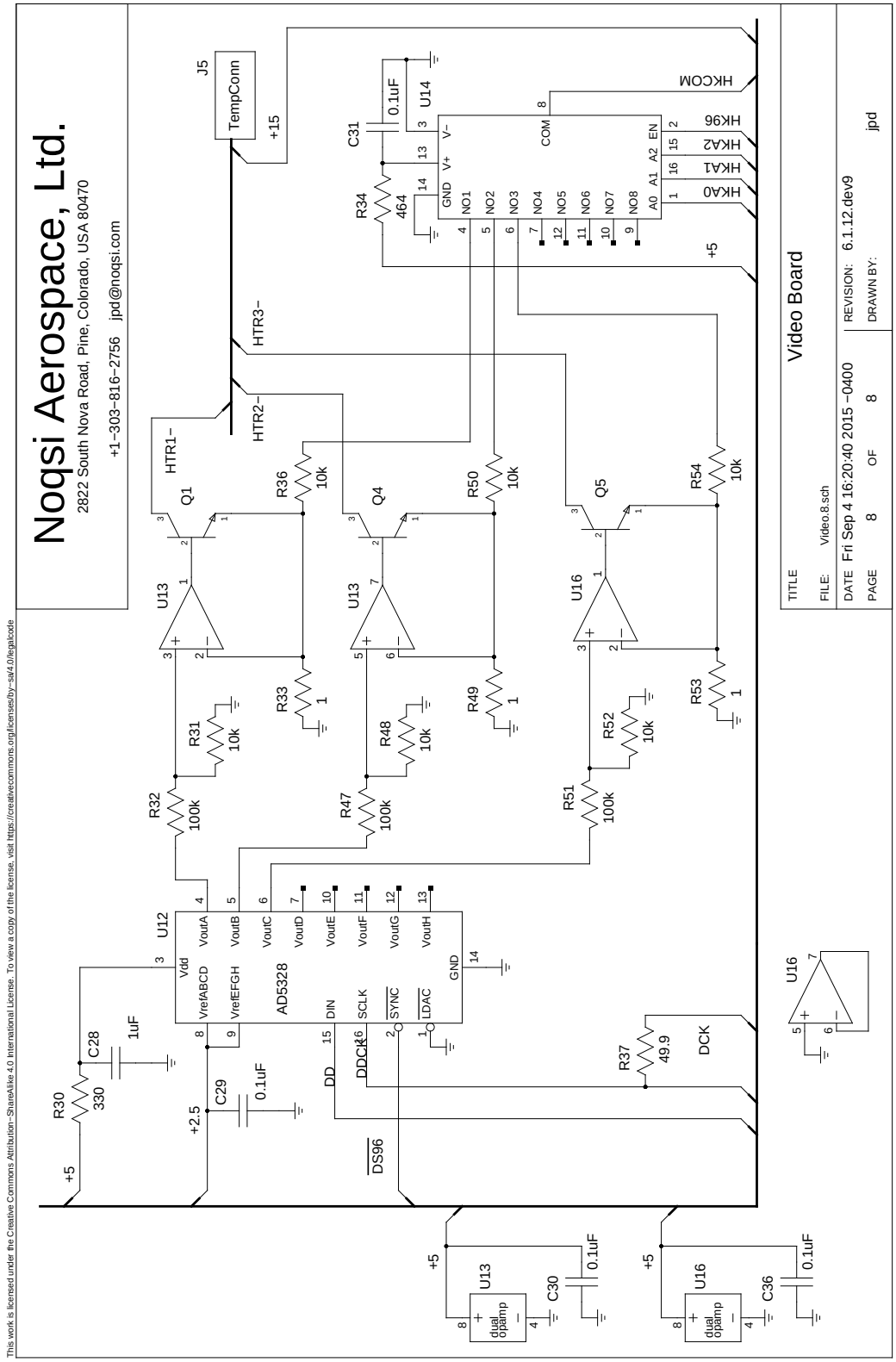

Figure 21: Video.8

2.4 Video Board Connectors

J1, J2, J3, and J4 connect to the flexprint cables from CCD1, CCD2, CCD3, and CCD4, respectively. Table 1 shows the pinout of J1. The -1 at the end of most net names indicates that the net serves CCD1. For J2, the corresponding net names end in -2, etc. Table 2 shows the pinout for J5, which serves the external temperature sensors and heater. Table 5 covers Js, the board stack connector.

Table 1: Flexprint Connector

Connector	Pin	Net	Signal
J1	1	Backside-1	case
J1	2	IG1-1	IG1
J1	3	IG2-1	IG2
J1	4	P1-OR-1	S1CD
J1	5	P2-OR-1	S2CD
J1	6	P3-OR-1	S3CD
J1	7	P1-U-1	S1U
J1	8	P2-U-1	S2U
J1	9	P3-U-1	S3U
J1	13	P3-IA-1	IA3
J1	14	P2-IA-1	IA2
J1	15	P1-IA-1	IA1
J1	19	GND	CS
J1	20	P3-OR-1	S3AB
J1	21	P2-OR-1	S2AB
J1	22	P1-OR-1	S1AB
J1	23	P3-FS-1	FS3
J1	24	P2-FS-1	FS2
J1	25	P1-FS-1	FS1
J1	26	VSUB-1	SUB
J1	27	ID-1	ID
J1	28	GND	RETD
J1	29	OG-D-1	OGD
J1	30	DR-D-1	DRD
J1	31	OUT-D-1	OSD
J1	32	GND	RTD78
J1	33	CuS-1	RTD56
J1	34	RD-1	RD
J1	35	OUT-C-1	OSC
J1	36	DR-C-1	DRC
J1	37	OG-C-1	OGC
J1	38	GND	RETC
J1	39	SCP-1	SCP

Table 1: Flexprint Connector (continued)

Connector	Pin	Net	Signal
J1	40	GND	RETB
J1	41	OG-B-1	OGB
J1	42	DR-B-1	DRB
J1	43	OUT-B-1	OSB
J1	44	RG-1	RG
J1	45	CuS-1	RTD34
J1	46	CuRTD-1	RTD12
J1	47	OUT-A-1	OSA
J1	48	DR-A-1	DRA
J1	49	OG-A-1	OGA
J1	50	GND	RETA
J1	51	SCP-1	USD

Table 2: Temperature Connector

Connector	Pin	Net	Comment
J5	1	GND	PtRTD1 return
J5	2	GND	PtRTD2 return
J5	3	GND	PtRTD3 return
J5	4	GND	PtRTD4 return
J5	5	GND	PtRTD5 return
J5	6	GND	PtRTD6 return
J5	7	GND	PtRTD7 return
J5	8	GND	PtRTD8 return
J5	9	GND	PtRTD9 return
J5	10	GND	PtRTD10 return
J5	11	GND	PtRTD11 return
J5	12	GND	PtRTD12 return
J5	17	PtRTD1	
J5	18	PtRTD2	
J5	19	PtRTD3	
J5	20	PtRTD4	
J5	21	PtRTD5	
J5	22	PtRTD6	
J5	23	PtRTD7	
J5	24	PtRTD8	
J5	25	PtRTD9	
J5	26	PtRTD10	
J5	27	PtRTD11	
J5	28	PtRTD12	
J5	14	+15	HTR1 return
J5	15	+15	HTR2 return
J5	16	+15	HTR3 return
J5	29	HTR1-	
J5	30	HTR2-	
J5	31	HTR3-	

3 Interface Board

3.1 Building blocks

3.1.1 Drivers for high capacitance (parallel) clocks

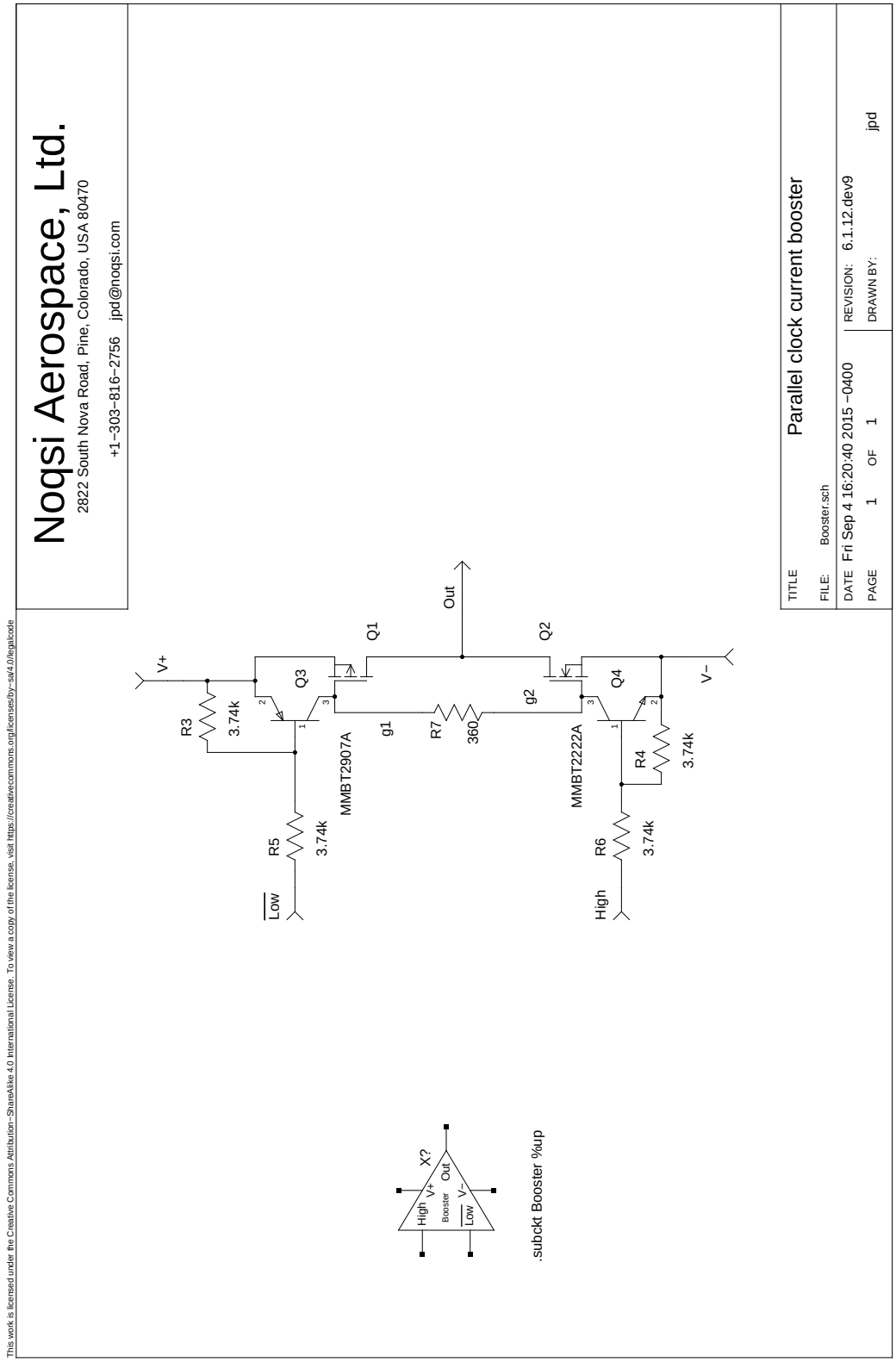

Figure 22: Booster

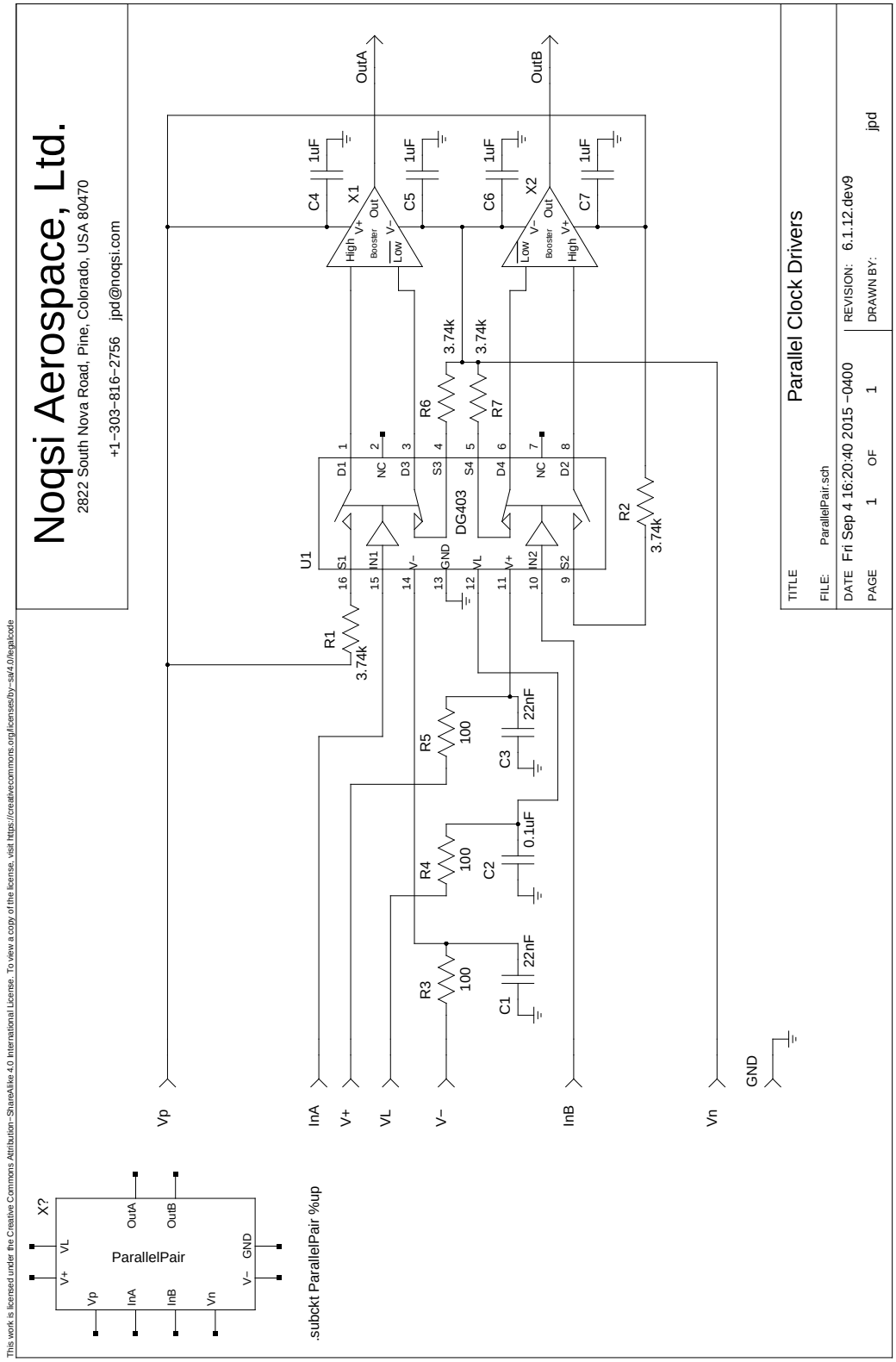

Figure 23: ParallelPair

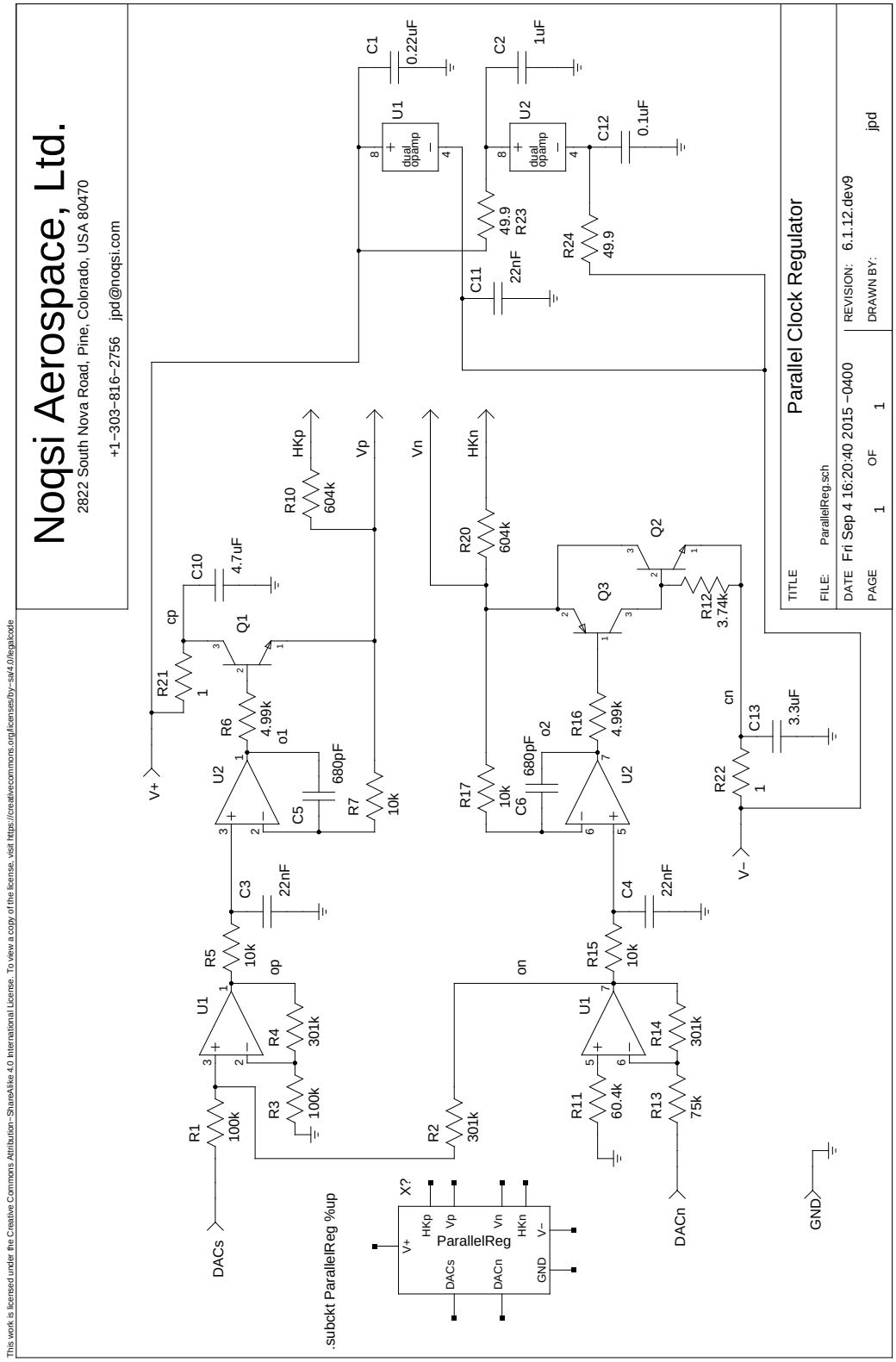

Figure 24: ParallelReg

3.1.2 Drivers for low capacitance clocks

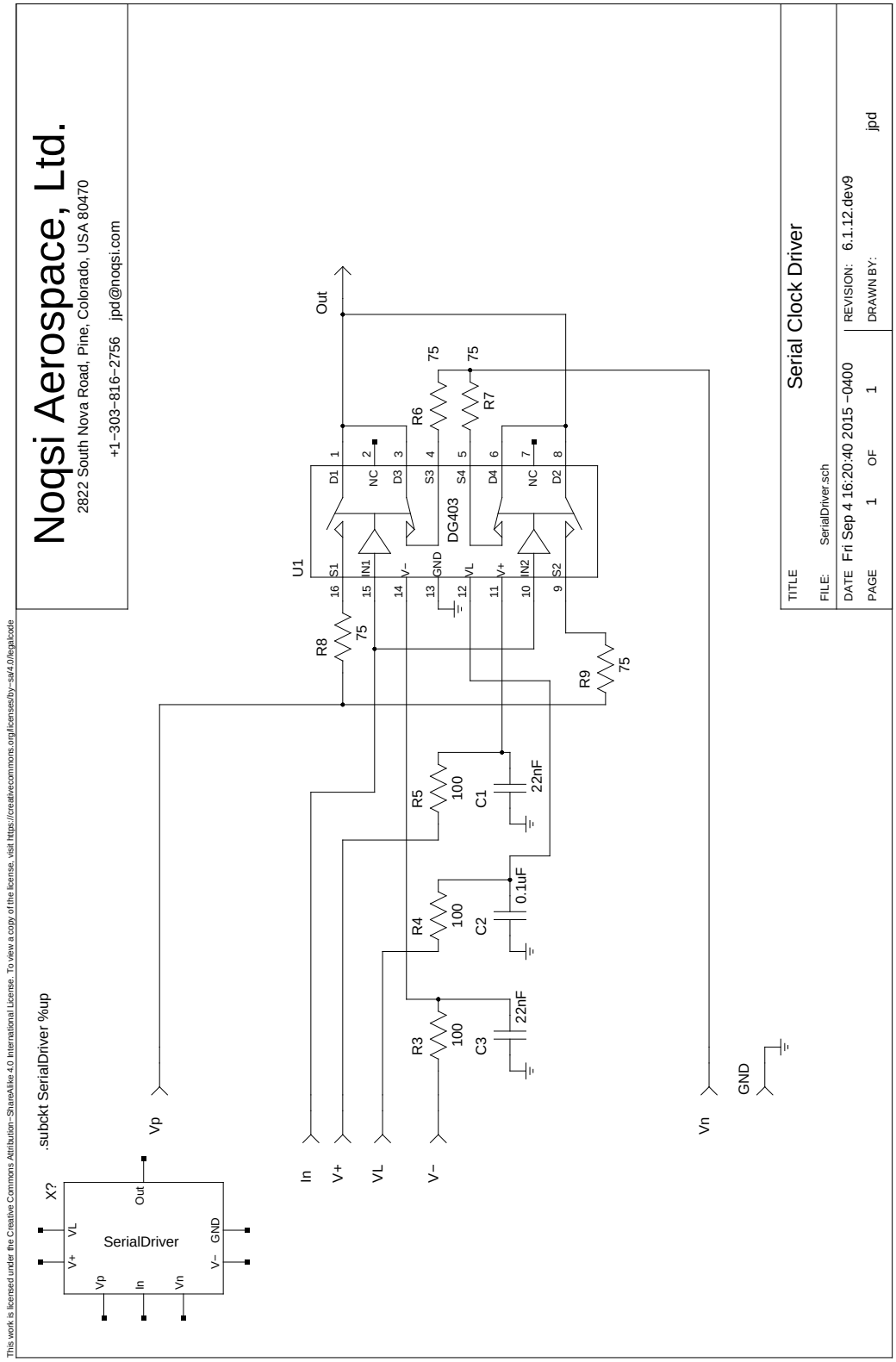

Figure 25: SerialDriver

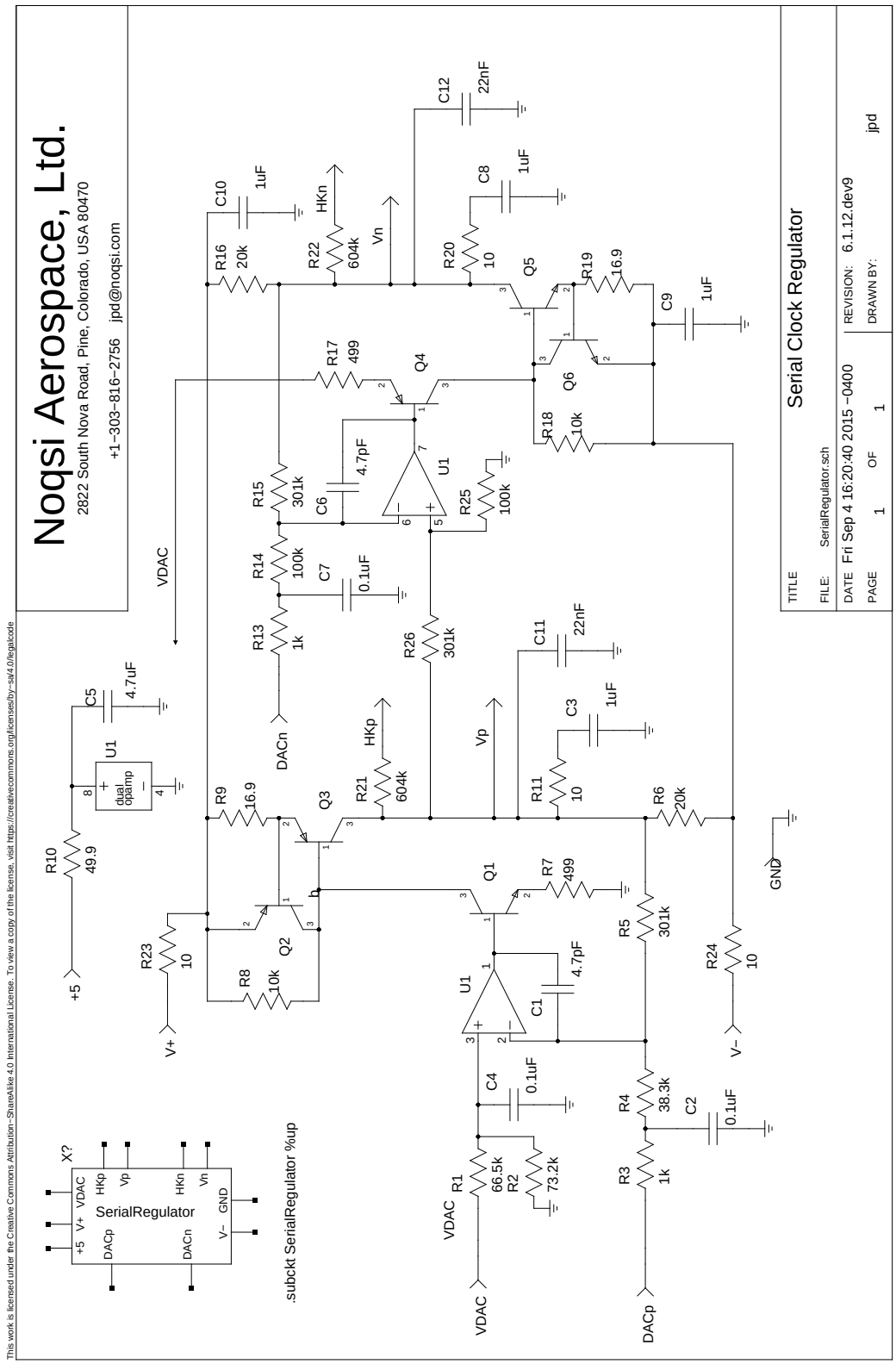

Figure 26: SerialRegulator

3.1.3 Clock drivers for one CCD

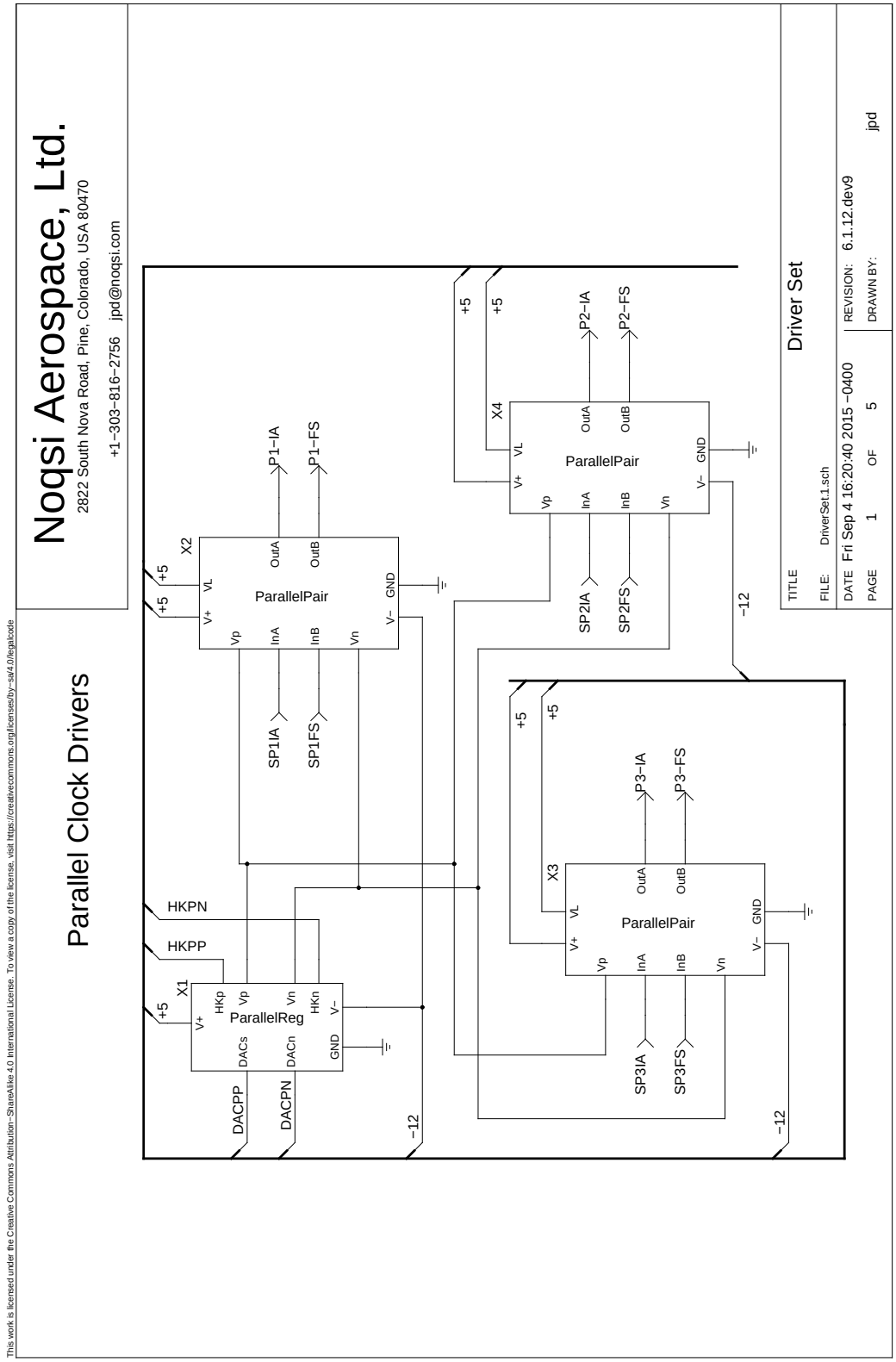

Figure 27: DriverSet.1

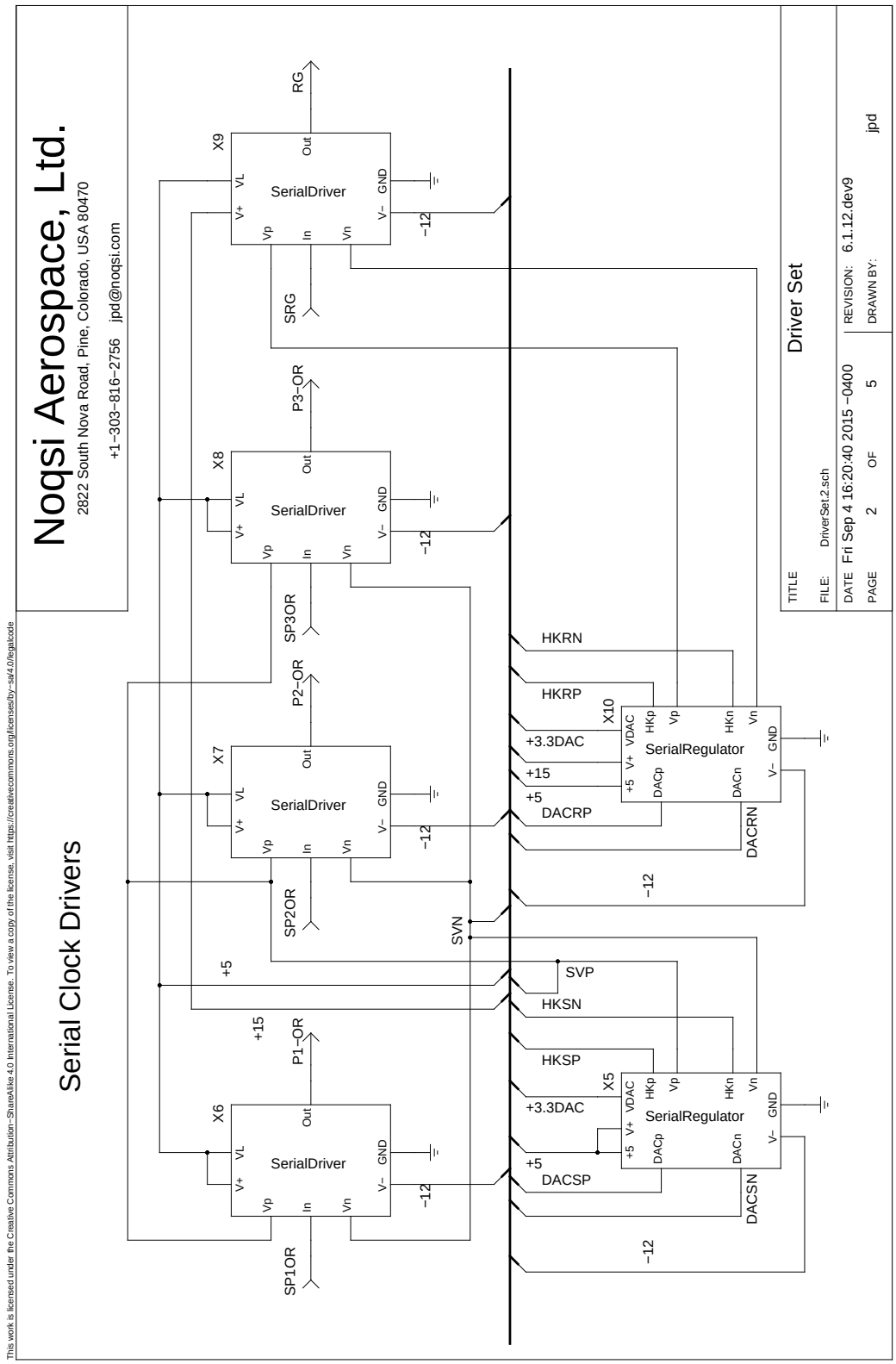

Figure 28: DriverSet.2

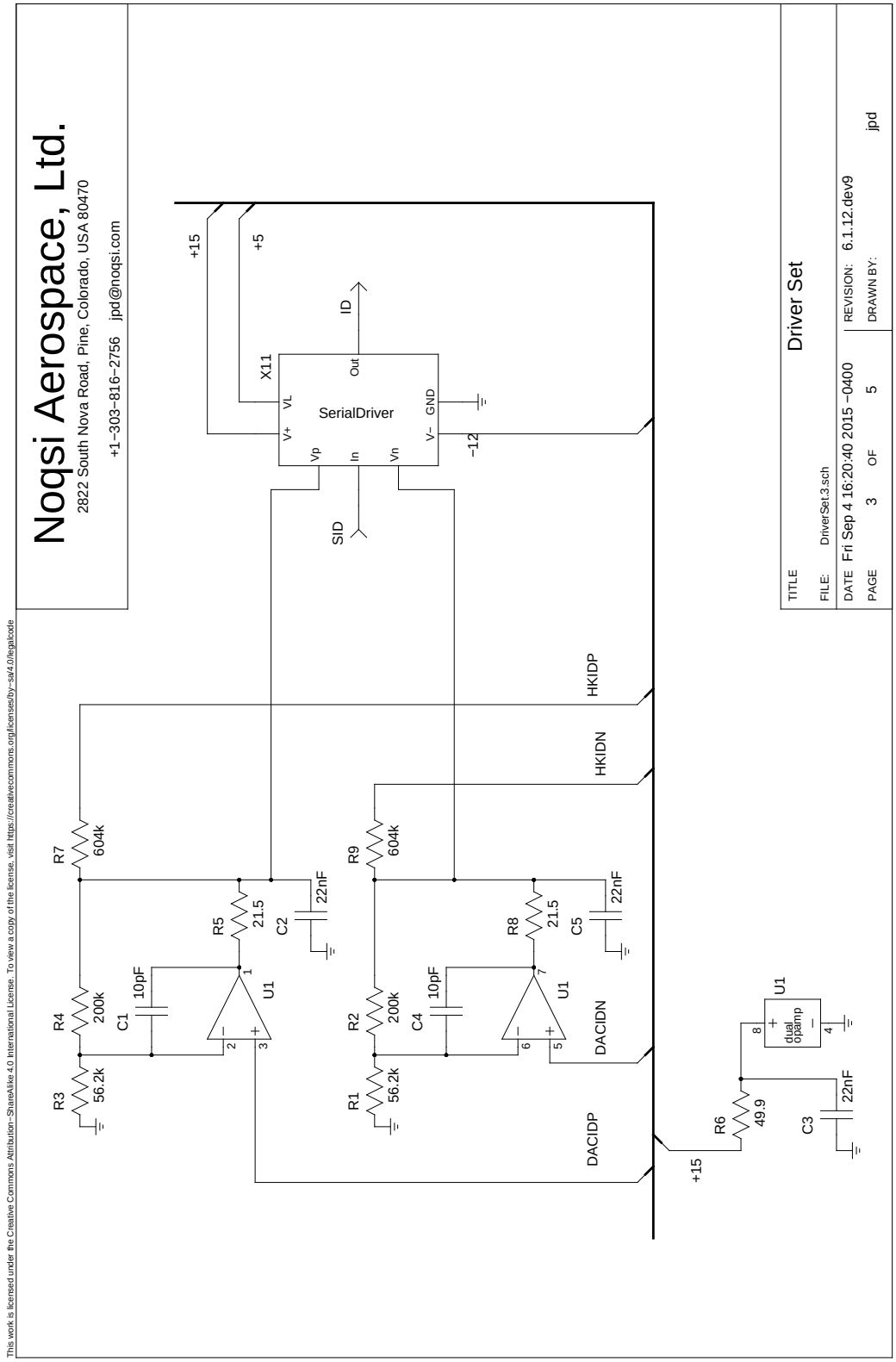

Figure 29: DriverSet.3

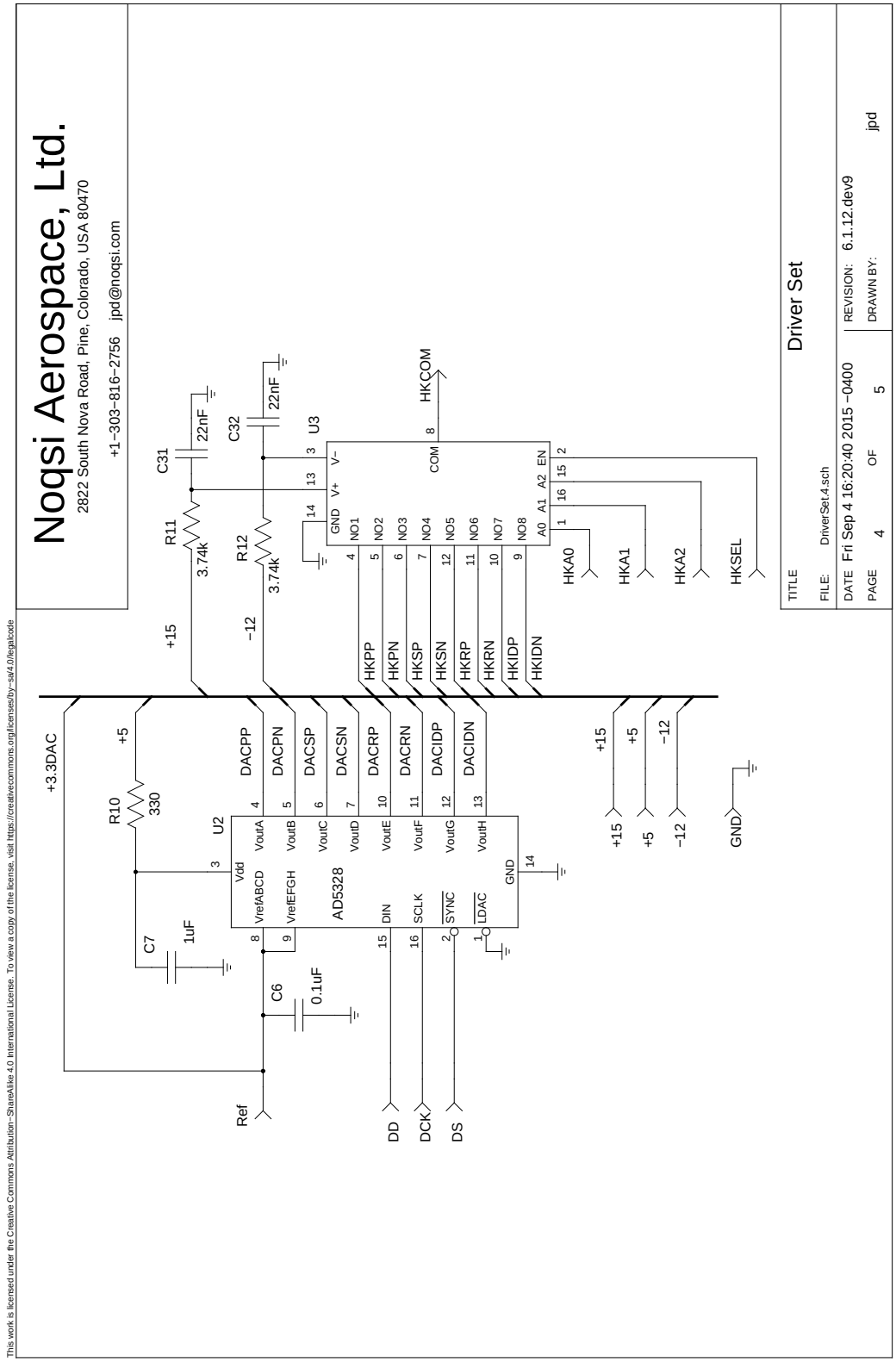

Figure 30: DriverSet.4

3.1.4 Power conditioning

Figure 31 shows the power regulators for the Artix FPGA. An RC filter on the reference insures that the 1.8V AUX power rises more slowly than the 1V core power. The 2.5V and 3.3V IO power follow the 1.8V AUX power with additional delays. This insures proper initialization. Q5 pulls down the 3.3V IO power if the 1.8V level is low, insuring that the rated maximum 2.625V difference cannot be exceeded for more than the allowed time (see Xilinx data sheet DS181). The resistors on the collectors of the pass transistors limit the surge current, and are rated to handle the fault current if the FPGA should latch up.

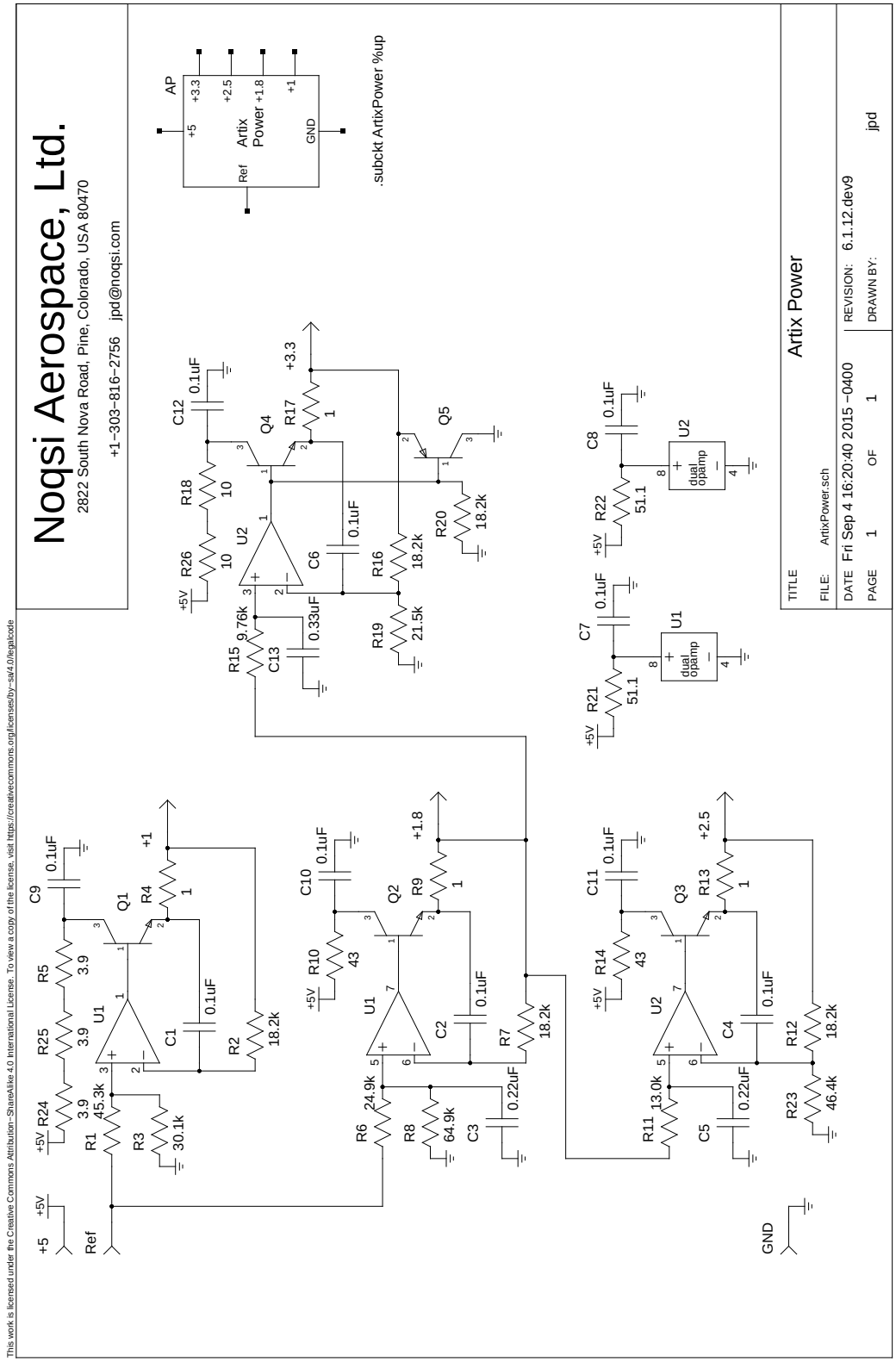

Figure 31: ArtixPower

3.2 Interface Board Top Level

Figure 32 shows the Artix FPGA (U4). Its pin connections are too complex to draw: Table 4 shows them. J9 is the JTAG header for FPGA debugging. J6 is the data connector to the DHU. J8 is test signals and configuration jumpers for the FPGA. Table 3 shows its pinout. For the pinouts of Js, the stacking connector, see Table 5.

Table 3: FPGA Test Header

Connector	Pin	Net
J8	1	GND
J8	2	ArtixDebug7
J8	3	GND
J8	4	ArtixDebug6
J8	5	GND
J8	6	DONE_0
J8	7	GND
J8	8	M0_0
J8	9	GND
J8	10	M1_0
J8	11	GND
J8	12	M2_0
J8	13	GND
J8	14	$\overline{\text{INIT}}$
J8	15	GND
J8	16	$\overline{\text{PROGRAM}}$

Table 4: Artix FPGA Connections

Pin	Net	Signal
F18	SP1-IA-4	CCD_IA1_pin[3]
B20	SP1-IA-3	CCD_IA1_pin[2]
E18	SP1-IA-2	CCD_IA1_pin[1]
A20	SP1-IA-1	CCD_IA1_pin[0]
B21	SP2-IA-4	CCD_IA2_pin[3]
A21	SP2-IA-3	CCD_IA2_pin[2]
C22	SP2-IA-2	CCD_IA2_pin[1]
B22	SP2-IA-1	CCD_IA2_pin[0]
C13	SP3-IA-4	CCD_IA3_pin[3]
B15	SP3-IA-3	CCD_IA3_pin[2]
B16	SP3-IA-2	CCD_IA3_pin[1]

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
B13	SP3-IA-1	CCD_IA3_pin[0]
D16	SP1-FS-4	CCD_FS1_pin[3]
E14	SP1-FS-3	CCD_FS1_pin[2]
C14	SP1-FS-2	CCD_FS1_pin[1]
E13	SP1-FS-1	CCD_FS1_pin[0]
E22	SP2-FS-4	CCD_FS2_pin[3]
E21	SP2-FS-3	CCD_FS2_pin[2]
D22	SP2-FS-2	CCD_FS2_pin[1]
D21	SP2-FS-1	CCD_FS2_pin[0]
D14	SP3-FS-4	CCD_FS3_pin[3]
D15	SP3-FS-3	CCD_FS3_pin[2]
C15	SP3-FS-2	CCD_FS3_pin[1]
E16	SP3-FS-1	CCD_FS3_pin[0]
L21	SDO-D-4	CCD_ADC_Sdi_pin[15]
K19	SDO-C-4	CCD_ADC_Sdi_pin[14]
H15	SDO-B-4	CCD_ADC_Sdi_pin[13]
G17	SDO-A-4	CCD_ADC_Sdi_pin[12]
K18	SDO-D-3	CCD_ADC_Sdi_pin[11]
G18	SDO-C-3	CCD_ADC_Sdi_pin[10]
J20	SDO-B-3	CCD_ADC_Sdi_pin[9]
J14	SDO-A-3	CCD_ADC_Sdi_pin[8]
J21	SDO-D-2	CCD_ADC_Sdi_pin[7]
M21	SDO-C-2	CCD_ADC_Sdi_pin[6]
L20	SDO-B-2	CCD_ADC_Sdi_pin[5]
J15	SDO-A-2	CCD_ADC_Sdi_pin[4]
J19	SDO-D-1	CCD_ADC_Sdi_pin[3]
H14	SDO-C-1	CCD_ADC_Sdi_pin[2]
H19	SDO-B-1	CCD_ADC_Sdi_pin[1]
N22	SDO-A-1	CCD_ADC_Sdi_pin[0]
V18	HKA2	HSK_ADC_Sel_pin[2]
V19	HKA1	HSK_ADC_Sel_pin[1]
AB20	HKA0	HSK_ADC_Sel_pin[0]
L18	ArtixDebug7	DebugStatus_pins[7]
K21	ArtixDebug6	DebugStatus_pins[6]
H18	$\overline{\text{RED}}$	DebugStatus_pins[5]
K22	$\overline{\text{ORANGE}}$	DebugStatus_pins[4]
G20	$\overline{\text{YELLOW}}$	DebugStatus_pins[3]
H20	$\overline{\text{GREEN}}$	DebugStatus_pins[2]
J22	$\overline{\text{BLUE}}$	DebugStatus_pins[1]
H22	$\overline{\text{WHITE}}$	DebugStatus_pins[0]
F13	Cam_ID-4	Cam_ID_pin[4]
E17	Cam_ID-3	Cam_ID_pin[3]

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
F15	Cam_ID-2	Cam_ID_pin[2]
F14	Cam_ID-1	Cam_ID_pin[1]
F16	Cam_ID-0	Cam_ID_pin[0]
E19	osc_clk	osc_clk_60_pin
Y18	cwclk	ChargePumpClk_pin
R18	SP1U	CCD_SU1_pin
N13	SP2U	CCD_SU2_pin
N14	SP3U	CCD_SU3_pin
R17	SP1OR	CCD_S1_pin
N17	SP2OR	CCD_S2_pin
P17	SP3OR	CCD_S3_pin
R16	SRG	CCD_RstGate_pin
P15	SID	CCD_InDiode_pin
P22	Clamp	CCD_ADC_Clamp_pin
U18	DeInt	CCD_ADC_DeInt_pin
T18	Int	CCD_ADC_Int_pin
K16	CNV	CCD_ADC_Cnv_pin
K17	ArtSCK	CCD_ADC_Sck_pin
R22	D422	Cmd_DIN_pin
U20	C422	Cmd_SCK_pin
G15	DATA-A	dataA_out_pin_p
H13	DATA-B	dataB_out_pin_p
G16	$\overline{\text{DATA-A}}$	dataA_out_pin_n
G13	$\overline{\text{DATA-B}}$	dataB_out_pin_n
AA21	HKC	HSK_ADC_Sck_pin
Y22	HKD	HSK_ADC_Sdi_pin
AA20	$\overline{\text{HKCS}}$	HSK_ADC_Cnv_pin
W21	HK0	HSK_ADC_0_pin
W22	HK8	HSK_ADC_8_pin
U22	HK16	HSK_ADC_16_pin
V22	HK24	HSK_ADC_24_pin
Y21	HK32	HSK_ADC_32_pin
T19	HK40	HSK_ADC_40_pin
T20	HK48	HSK_ADC_48_pin
P21	HK56	HSK_ADC_56_pin
P19	HK64	HSK_ADC_64_pin
T21	HK72	HSK_ADC_72_pin
U21	HK80	HSK_ADC_80_pin
R19	HK88	HSK_ADC_88_pin
R21	HK96	HSK_ADC_96_pin
U17	HK104	HSK_ADC_104_pin
W17	HK112	HSK_ADC_112_pin

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
P20	HK120	HSK_ADC_120_pin
J17	$\overline{\text{DS0}}$	CLS_DCS_0_pin
M13	$\overline{\text{DS8}}$	CLS_DCS_8_pin
L13	$\overline{\text{DS16}}$	CLS_DCS_16_pin
K13	$\overline{\text{DS24}}$	CLS_DCS_24_pin
K14	$\overline{\text{DS32}}$	CLS_DCS_32_pin
N20	$\overline{\text{DS40}}$	CLS_DCS_40_pin
M20	$\overline{\text{DS48}}$	CLS_DCS_48_pin
N18	$\overline{\text{DS56}}$	CLS_DCS_56_pin
M15	$\overline{\text{DS64}}$	CLS_DCS_64_pin
M16	$\overline{\text{DS72}}$	CLS_DCS_72_pin
J16	$\overline{\text{DS80}}$	CLS_DCS_80_pin
H17	$\overline{\text{DS88}}$	CLS_DCS_88_pin
N19	$\overline{\text{DS96}}$	CLS_DCS_96_pin
M18	DD	CLC_DAC_Din_pin
L19	ArtDCK	CLC_DAC_Sck_pin
M9	GND	VN_0
L10	GND	VP_0
G11	DONE_0	DONE_0
N10	GND	DXP_0
K9	GND	GNDADC_0
K10	+1.8F	VCCADC_0
M10	GND	VREFP_0
E12	GND	VCCBATT_0
V12	TCK	TCK_0
N9	GND	DXN_0
L9	GND	VREFN_0
L12	C422	CCLK_0
U11	M0_0	M0_0
U10	M1_0	M1_0
U12	$\overline{\text{INIT}}$	INIT_B_0
R13	TDI	TDI_0
U13	TDO	TDO_0
U9	M2_0	M2_0
U8	+3.3F	3.30
N12	$\overline{\text{PROGRAM}}$	PROGRAM_B_0
T13	TMS	TMS_0
F12	+3.3F	VCCO_0
T12	+3.3F	VCCO_0
AA17	GND	VCCO_13
AB14	GND	VCCO_13
V16	GND	VCCO_13

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
W13	GND	VCCO_13
Y10	GND	VCCO_13
M14	+3.3F	3.30
P18	+3.3F	3.30
R15	+3.3F	3.30
T22	+3.3F	3.30
U19	+3.3F	3.30
Y20	+3.3F	3.30
G19	+2.5F	2.50
H16	+2.5F	2.50
J13	+2.5F	2.50
K20	+2.5F	2.50
L17	+2.5F	2.50
N21	+2.5F	2.50
A17	+3.3F	3.30
B14	+3.3F	3.30
C21	+3.3F	3.30
D18	+3.3F	3.30
E15	+3.3F	3.30
F22	+3.3F	3.30
AA7	GND	VCCO_34
AB4	GND	VCCO_34
R5	GND	VCCO_34
T2	GND	VCCO_34
V6	GND	VCCO_34
W3	GND	VCCO_34
C1	GND	VCCO_35
F2	GND	VCCO_35
H6	GND	VCCO_35
J3	GND	VCCO_35
M4	GND	VCCO_35
N1	GND	VCCO_35
D11	GND	MGTPRXP1_216
B10	GND	MGTPRXP2_216
D9	GND	MGTPRXP3_216
B8	GND	MGTPRXP0_216
C11	GND	MGTPRXN1_216
A10	GND	MGTPRXN2_216
C9	GND	MGTPRXN3_216
A8	GND	MGTPRXN0_216
F8	GND	MGTRREF_216
D8	GND	GND

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
A2	GND	GND
A3	GND	GND
A5	GND	GND
A7	GND	GND
A9	GND	GND
A11	GND	GND
A12	GND	GND
A22	GND	GND
AA2	GND	GND
AA12	GND	GND
AA22	GND	GND
AB9	GND	GND
AB19	GND	GND
B3	GND	GND
B12	GND	GND
B19	GND	GND
C3	GND	GND
C6	GND	GND
C10	GND	GND
C12	GND	GND
C16	GND	GND
D3	GND	GND
D4	GND	GND
D12	GND	GND
D13	GND	GND
E4	GND	GND
E5	GND	GND
E7	GND	GND
E9	GND	GND
E11	GND	GND
E20	GND	GND
F5	GND	GND
F11	GND	GND
F17	GND	GND
G5	GND	GND
G6	GND	GND
G7	GND	GND
G8	GND	GND
G9	GND	GND
G10	GND	GND
G12	GND	GND
G14	GND	GND

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
H1	GND	GND
H7	GND	GND
H9	GND	GND
H11	GND	GND
H21	GND	GND
J8	GND	GND
J10	GND	GND
J12	GND	GND
J18	GND	GND
K5	GND	GND
K7	GND	GND
K11	GND	GND
K15	GND	GND
L2	GND	GND
L8	GND	GND
L22	GND	GND
M7	GND	GND
M11	GND	GND
M19	GND	GND
N6	GND	GND
N8	GND	GND
N16	GND	GND
P3	GND	GND
P7	GND	GND
P9	GND	GND
P11	GND	GND
P13	GND	GND
R8	GND	GND
R10	GND	GND
R12	GND	GND
R20	GND	GND
T7	GND	GND
T9	GND	GND
T11	GND	GND
T17	GND	GND
U4	GND	GND
U14	GND	GND
V1	GND	GND
V11	GND	GND
V21	GND	GND
W8	GND	GND
W18	GND	GND

Table 4: Artix FPGA Connections (continued)

Pin	Net	Signal
Y5	GND	GND
Y15	GND	GND
H8	+1F	VCCINT
H10	+1F	VCCINT
J7	+1F	VCCINT
J9	+1F	VCCINT
K8	+1F	VCCINT
L7	+1F	VCCINT
M8	+1F	VCCINT
N7	+1F	VCCINT
P8	+1F	VCCINT
P10	+1F	VCCINT
R7	+1F	VCCINT
R9	+1F	VCCINT
T8	+1F	VCCINT
T10	+1F	VCCINT
H12	+1.8F	1.80
K12	+1.8F	1.80
M12	+1.8F	1.80
P12	+1.8F	1.80
R11	+1.8F	1.80
J11	+1F	VCCBRAM
L11	+1F	VCCBRAM
N11	+1F	VCCBRAM

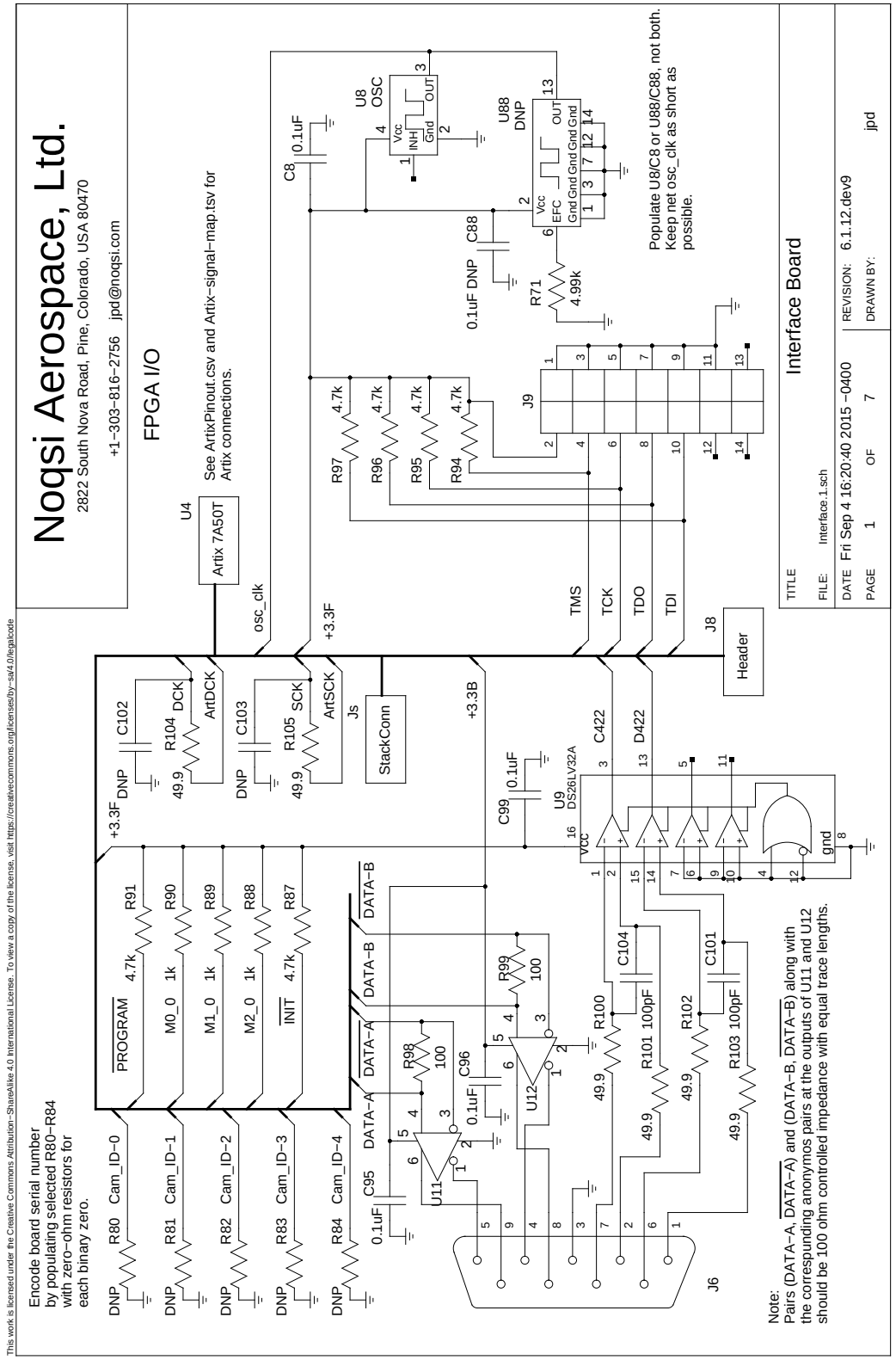

Figure 32: Interface.1

Figure 33 shows support for housekeeping and temperature measurement. HKCOM is the primary housekeeping analog bus. The selected housekeeping channel will drive a current into this bus. U5 converts the current to a voltage. Full scale is $\pm 27.3\,\mu$A. RTDCOM is a voltage input for the resistive temperature sensors on the CCD chips and the camera, U6 scales the voltage from the sensor circuitry on the Video board so that the full measurement range is $500\,\Omega$ to $1500\,\Omega$. The temperature range depends on the sensor: see Table 11 for the nominal ranges. U3 multiplexes some voltage measurements onto HKCOM. The sense resistors are $604\,\mathrm{k}\Omega$. $\pm 27.3\,\mu$A through $604\,\mathrm{k}\Omega$ is $\pm 16.5\,$V, so that's full scale on these housekeeping channels.

Figure 34 shows the housekeeping ADC subsystem. There are two sources of housekeeping voltage inputs to this: HKV and RTDV. Housekeeping addresses <112 use HKV, while the higher addresses use RTDV (see Figure 33). U1 selects which of these voltage sources to use. U6 creates a differential input for the ADC, U2.

Figure 35 shows the FPGA bypass capacitors. The smallest capacitors should be closest to the power pins on the FPGA.

Figures 36 and 37 show the connections of the Driver Sets for CCD chips 1 and 2. The Driver Sets for CCD chips 3 and 4 are on the Driver Board.

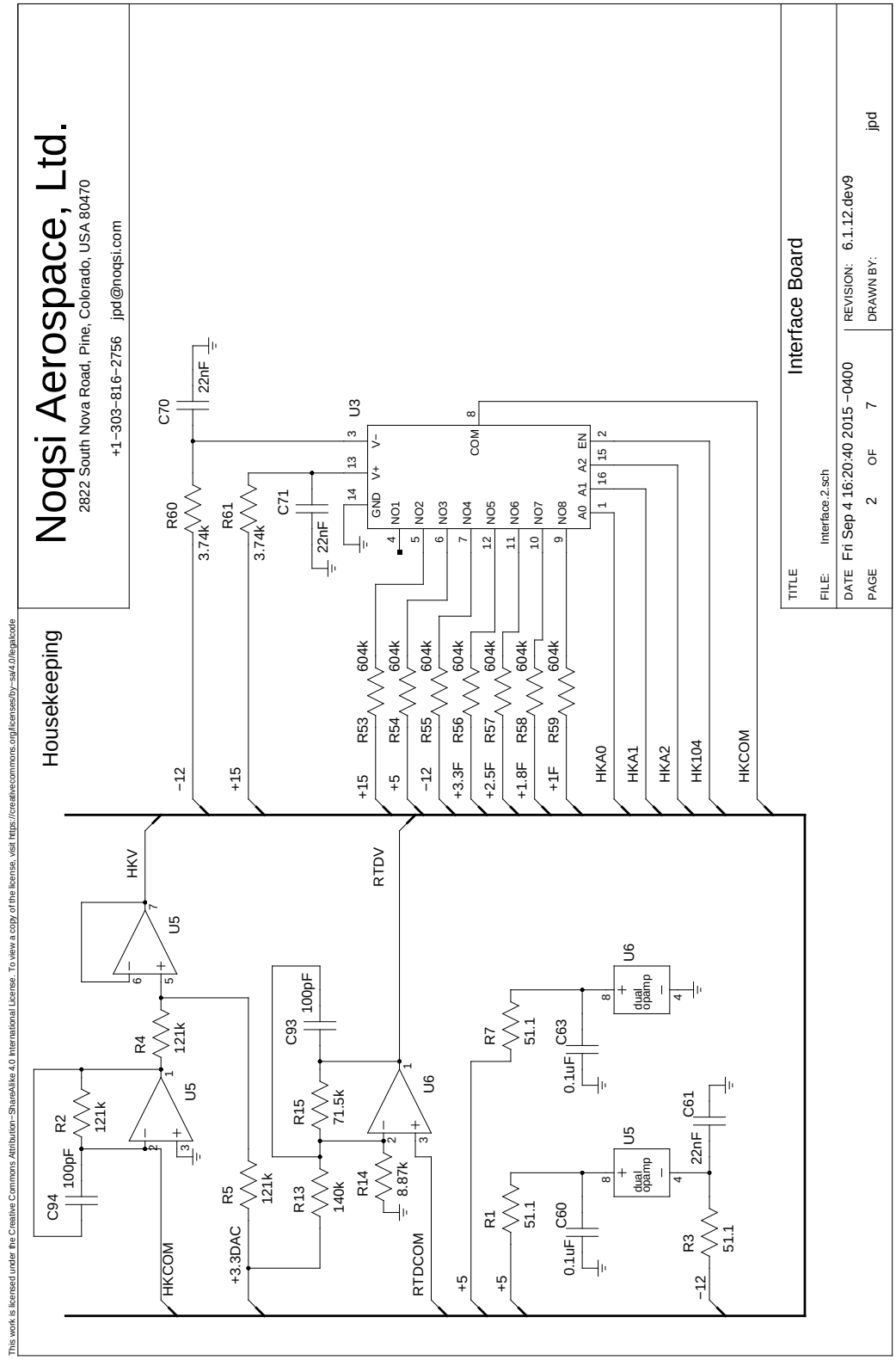

Figure 33: Interface.2

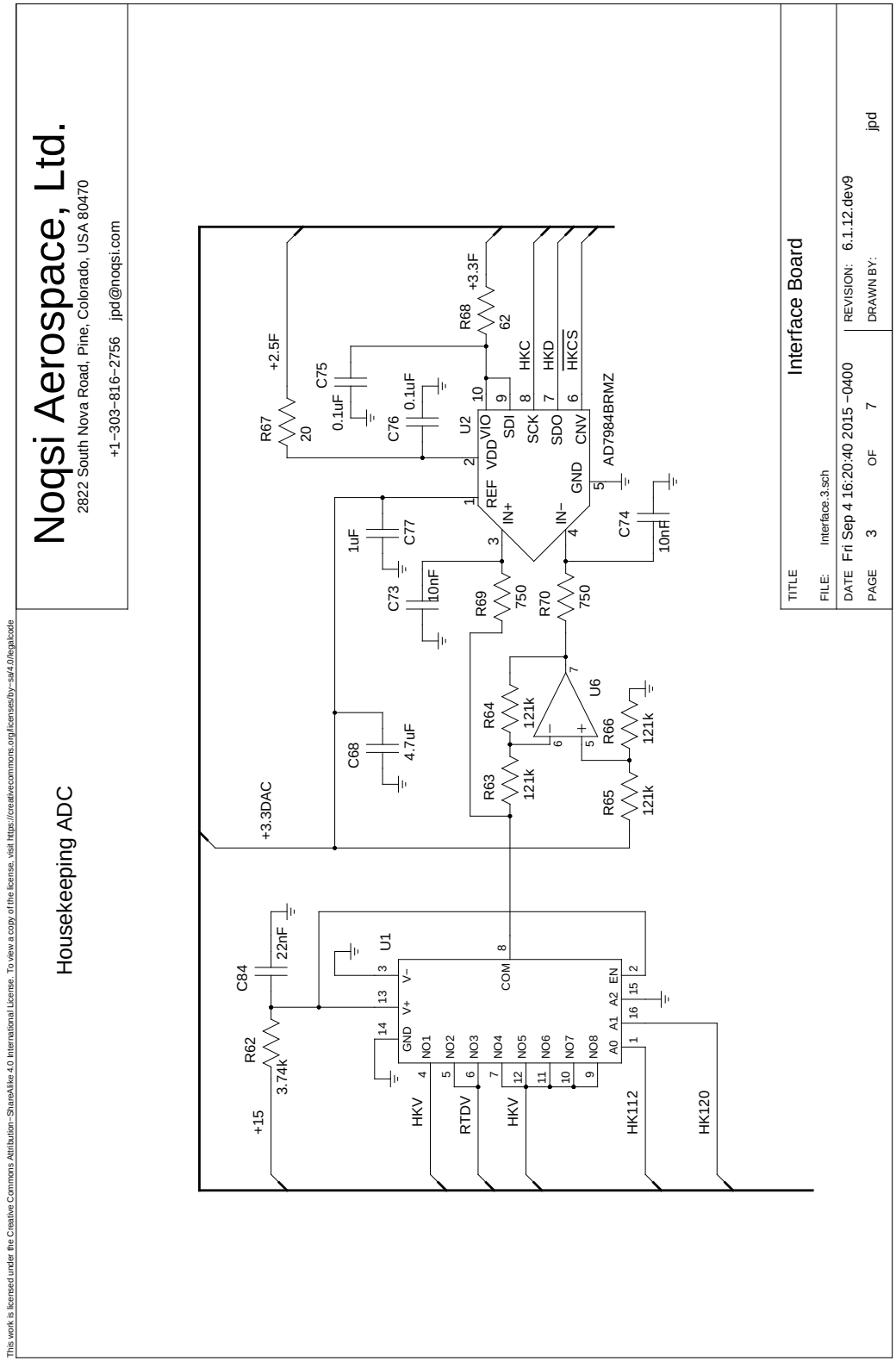

Figure 34: Interface.3

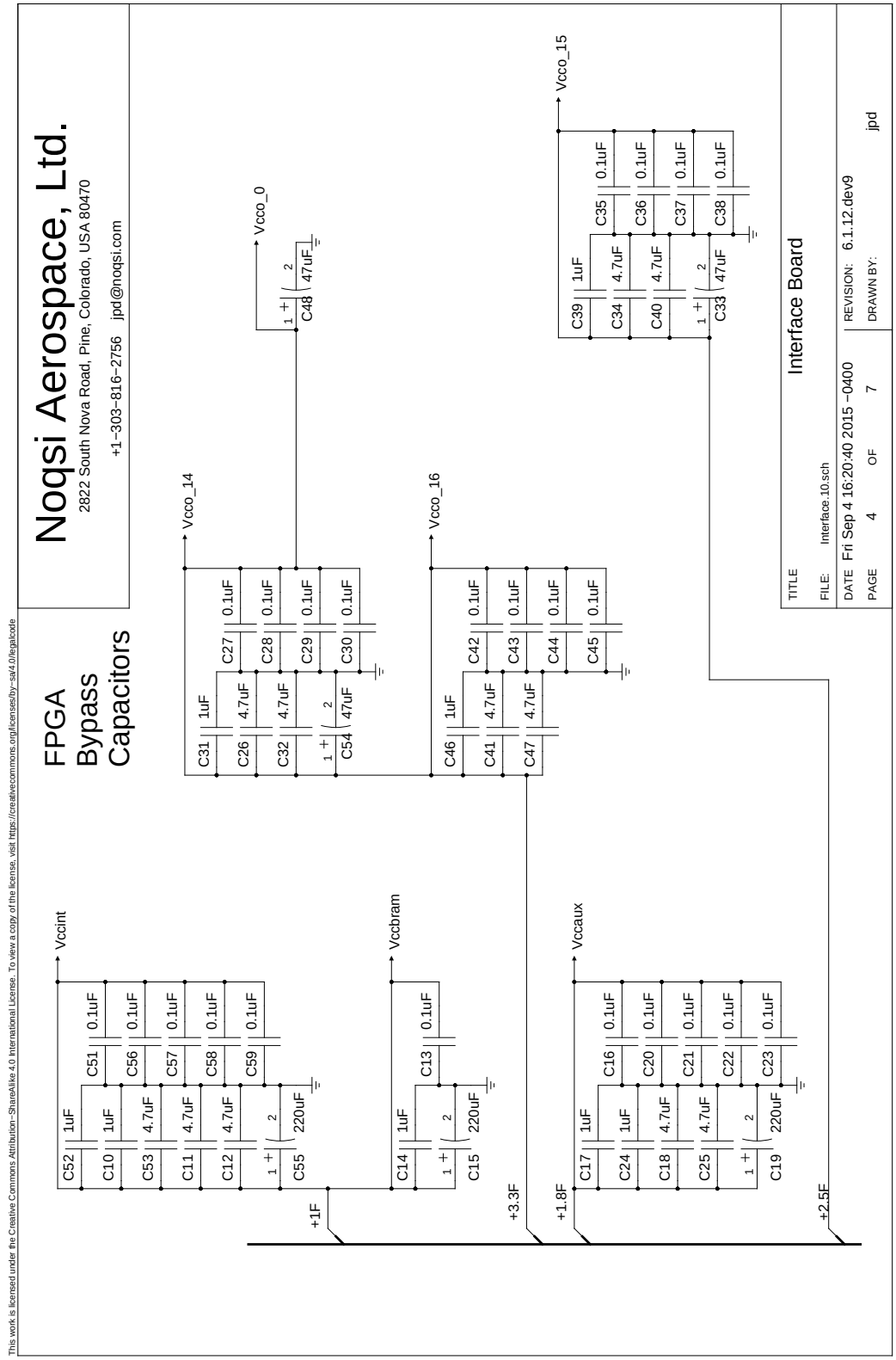

Figure 35: Interface.4

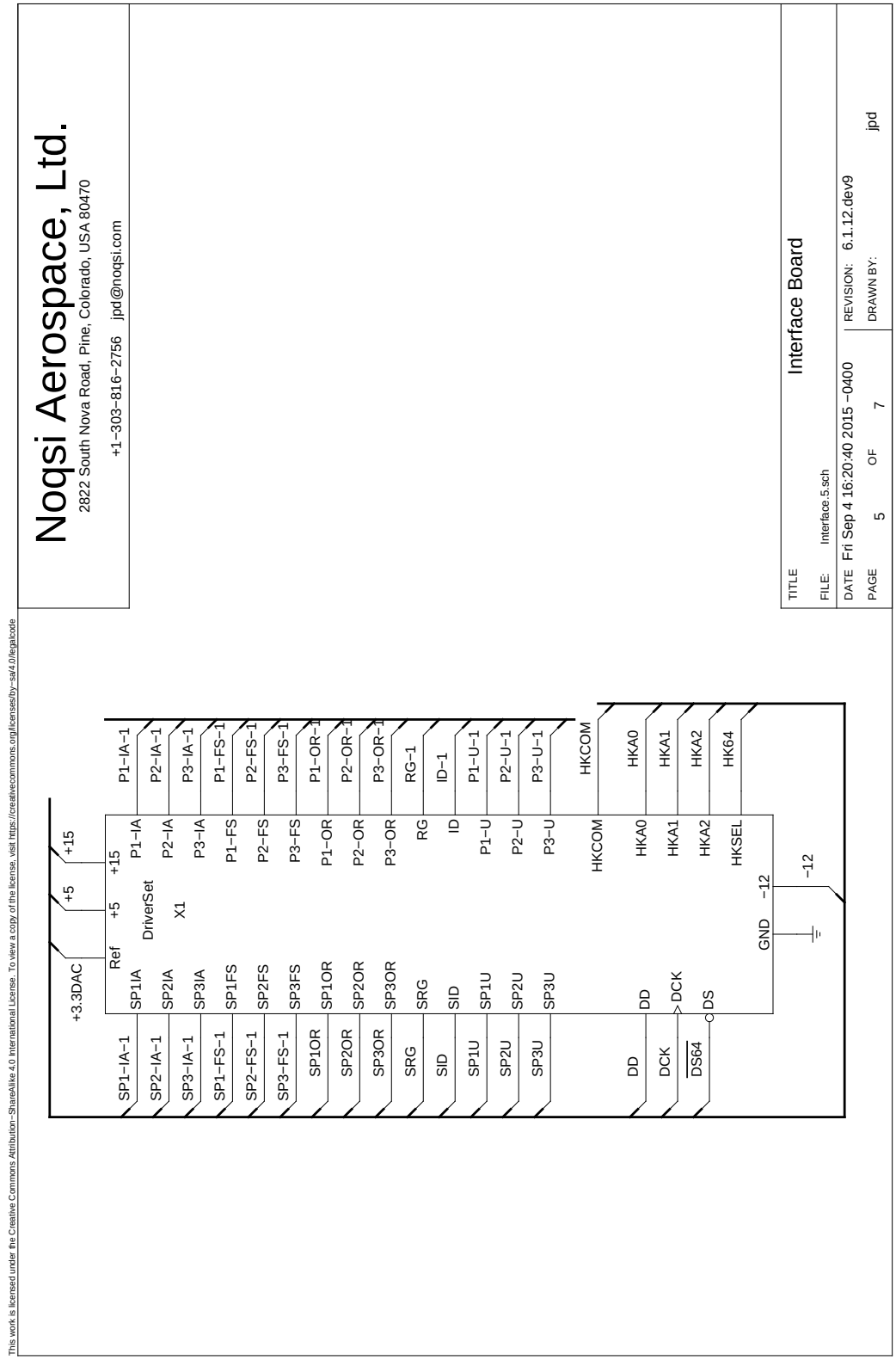

Figure 36: Interface.5

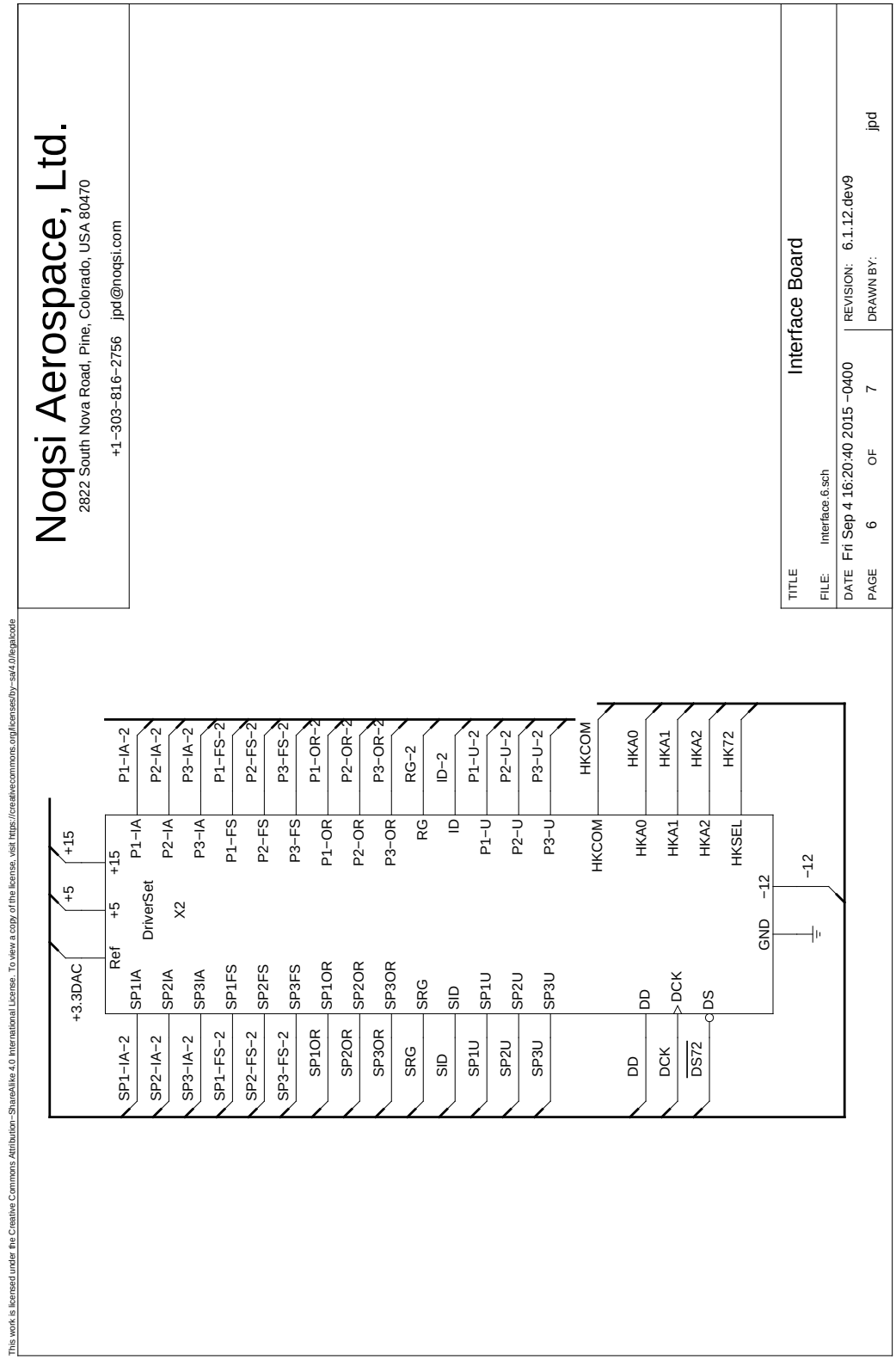

Figure 37: Interface.6

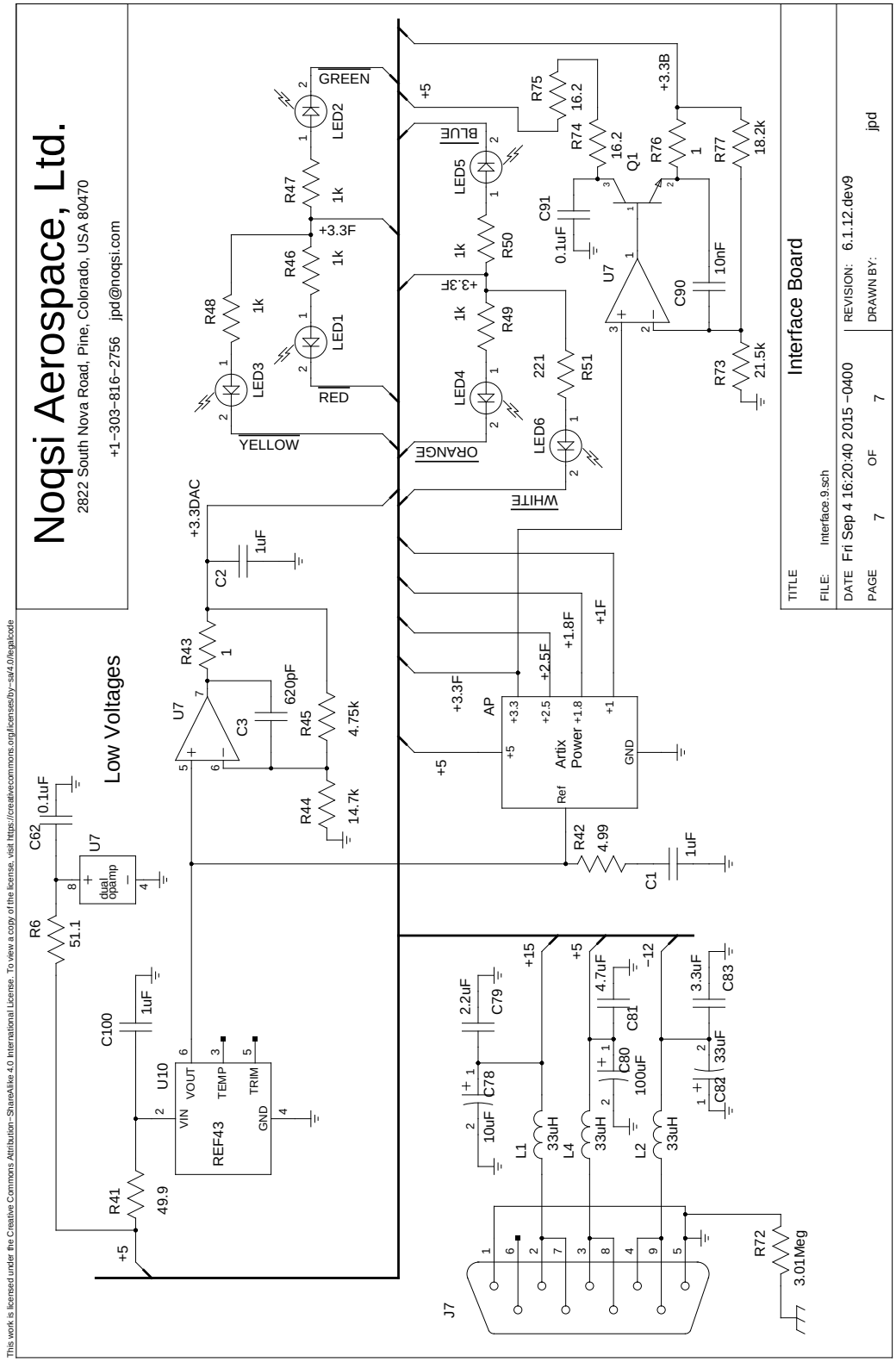

Figure 38: Interface.7

Figure 38 shows power input from the DHU (J7) and low voltage power conditioning. LEDs are for debugging: we will not install them on flight boards.

4 Driver Board

See the previous section for the DriverSet building blocks.

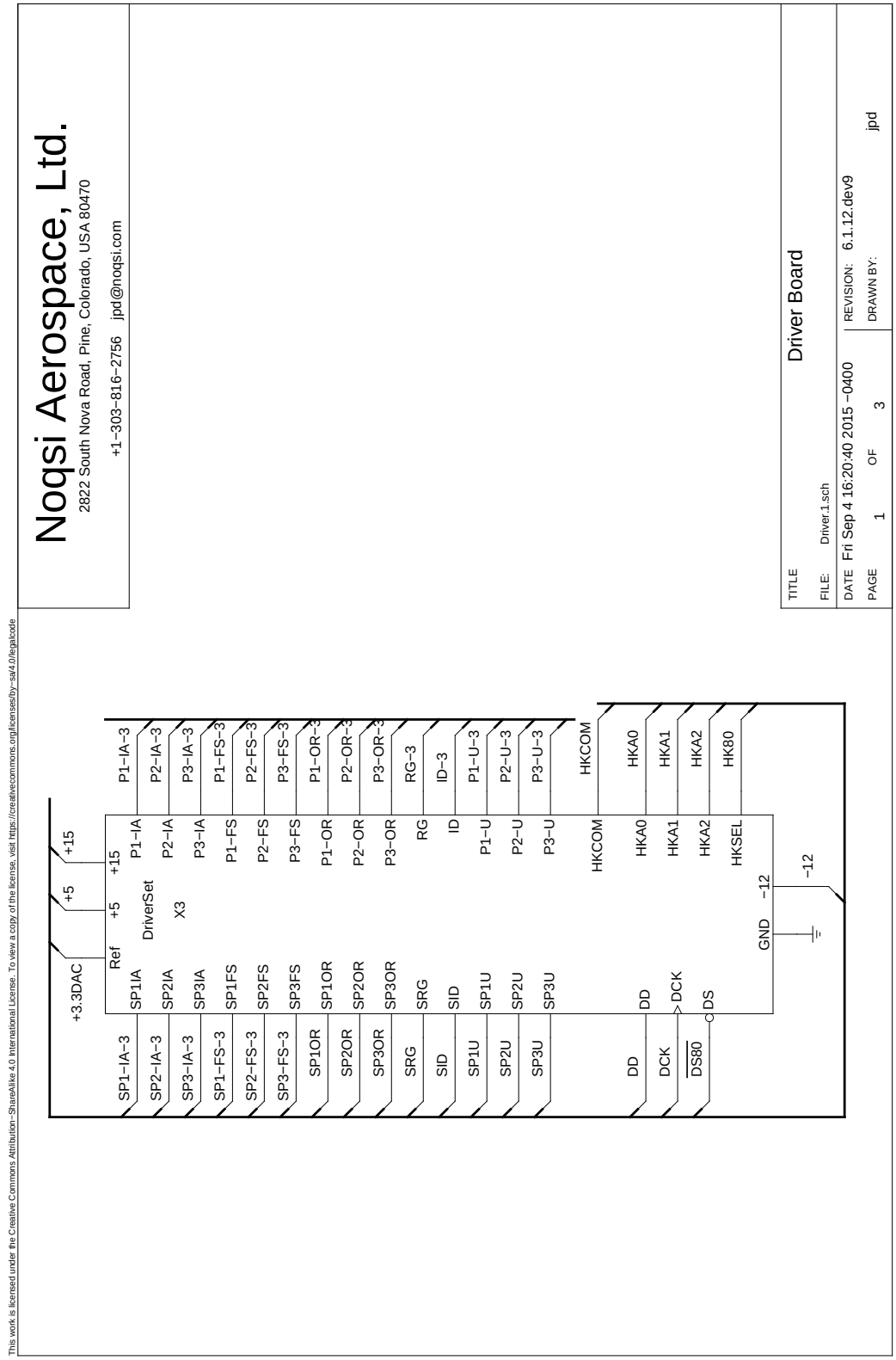

Figure 39: Driver.1

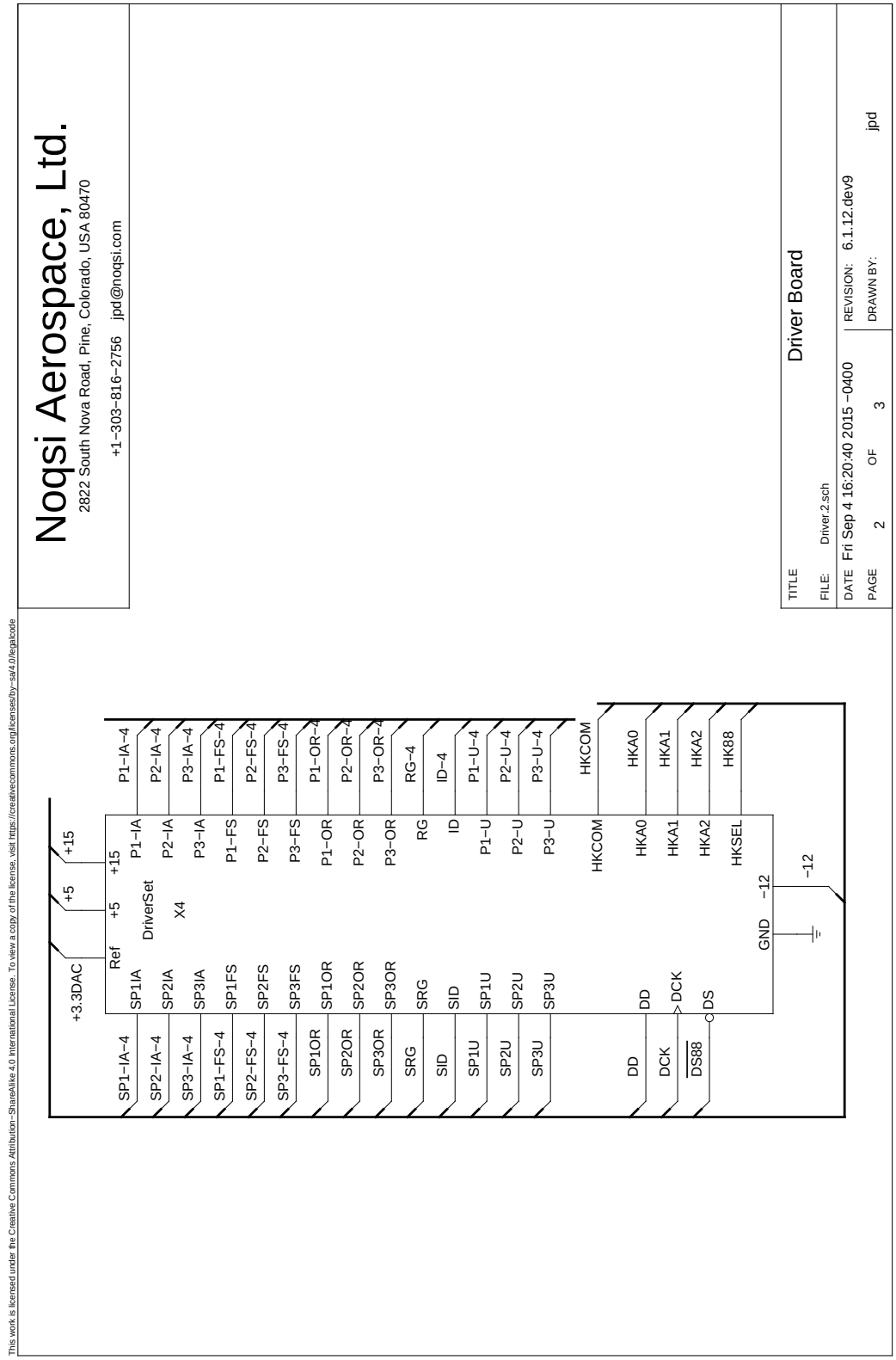

Figure 40: Driver.2

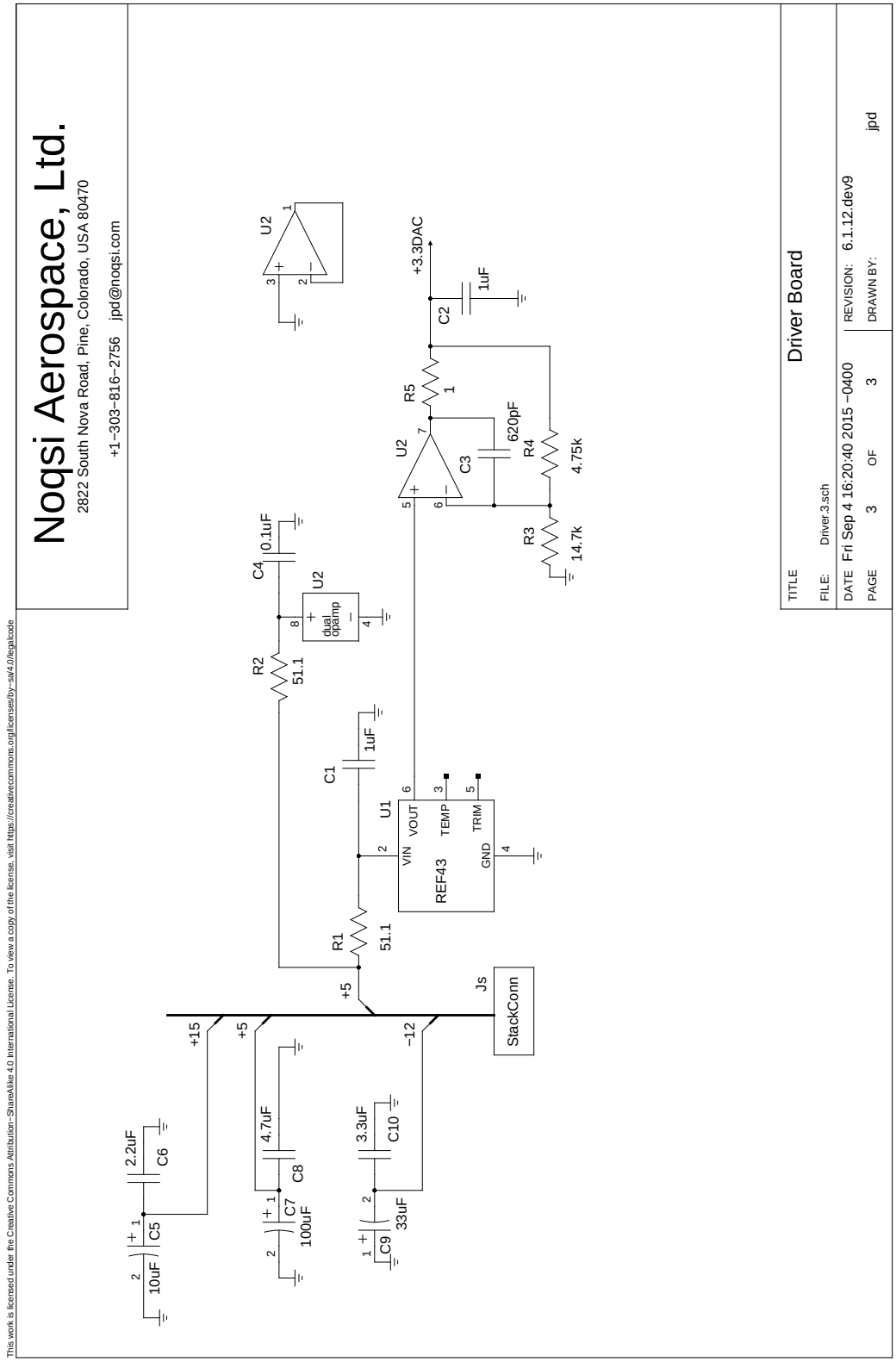

Figure 41: Driver.3

5 Stack Interconnection

Table 5: Inter-board Stack Connections

1	GND			101	ID-4		
		51	P1-FS-1			151	GND
2	SDO-A-1			102	P3-U-4		
		52	P2-FS-1			152	SDO-D-4
3	GND			103	P2-U-4		
		53	P3-FS-1			153	GND
4	SDO-B-1			104	P1-U-4		
		54	P3-OR-1			154	SDO-C-4
5	GND			105	P3-IA-4		
		55	P2-OR-1			155	GND
6	SDO-C-1			106	P2-IA-4		
		56	P1-OR-1			156	SDO-B-4
7	GND			107	P1-IA-4		
		57	RG-1			157	GND
8	SDO-D-1			108	RG-4		
		58	P1-IA-1			158	SDO-A-4
9	GND			109	P1-OR-4		
		59	P2-IA-1			159	GND
10	SCK			110	P2-OR-4		
		60	P3-IA-1			160	$\overline{\text{DS0}}$
11	GND			111	P3-OR-4		
		61	P1-U-1			161	GND
12	CNV			112	P3-FS-4		
		62	P2-U-1			162	$\overline{\text{DS8}}$
13	GND			113	P2-FS-4		
		63	P3-U-1			163	GND
14	Int			114	P1-FS-4		
		64	ID-1			164	$\overline{\text{DS16}}$
15	GND			115	SP3-FS-4		
		65	SP1-IA-1			165	GND
16	DeInt			116	SP2-FS-4		
		66	SP2-IA-1			166	$\overline{\text{DS24}}$
17	GND			117	SP1-FS-4		
		67	SP3-IA-1			167	GND
18	Clamp			118	SP3-IA-4		
		68	SP1-FS-1			168	$\overline{\text{DS32}}$
19	GND			119	SP2-IA-4		
		69	SP2-FS-1			169	GND
20	cwclk			120	SP1-IA-4		
		70	SP3-FS-1			170	$\overline{\text{DS40}}$
21	GND			121	HK80		
		71	HK0			171	GND
22	DD			122	HK88		
		72	HK8			172	SPARE
23	GND			123	HK96		
		73	HK16			173	GND
24	DCK			124	HK104		

		74	HK24			174	RTDCOM
25	GND			125	HK112		
		75	HK32			175	GND
26	SP1OR			126	HK120		
		76	HK40			176	+15
27	GND			127	HKA0		
		77	HK48			177	GND
28	SP2OR			128	HKA1		
		78	HK56			178	-12
29	GND			129	HKA2		
		79	HK64			179	GND
30	SP3OR			130	HKCOM		
		80	HK72			180	+5
31	GND			131	SP3-FS-3		
		81	SP1-IA-2			181	GND
32	SRG			132	SP2-FS-3		
		82	SP2-IA-2			182	$\overline{\text{DS48}}$
33	GND			133	SP1-FS-3		
		83	SP3-IA-2			183	GND
34	SID			134	SP3-IA-3		
		84	SP1-FS-2			184	$\overline{\text{DS56}}$
35	GND			135	SP2-IA-3		
		85	SP2-FS-2			185	GND
36	SP1U			136	SP1-IA-3		
		86	SP3-FS-2			186	$\overline{\text{DS64}}$
37	GND			137	ID-3		
		87	P1-FS-2			187	GND
38	SP2U			138	P3-U-3		
		88	P2-FS-2			188	$\overline{\text{DS72}}$
39	GND			139	P2-U-3		
		89	P3-FS-2			189	GND
40	SP3U			140	P1-U-3		
		90	P3-OR-2			190	$\overline{\text{DS80}}$
41	GND			141	P3-IA-3		
		91	P2-OR-2			191	GND
42	$\overline{\text{DS96}}$			142	P2-IA-3		
		92	P1-OR-2			192	$\overline{\text{DS88}}$
43	GND			143	P1-IA-3		
		93	RG-2			193	GND
44	SDO-A-2			144	RG-3		
		94	P1-IA-2			194	SDO-D-3
45	GND			145	P1-OR-3		
		95	P2-IA-2			195	GND
46	SDO-B-2			146	P2-OR-3		
		96	P3-IA-2			196	SDO-C-3
47	GND			147	P3-OR-3		
		97	P1-U-2			197	GND
48	SDO-C-2			148	P3-FS-3		
		98	P2-U-2			198	SDO-B-3
49	GND			149	P2-FS-3		

		99	P3-U-2			199	GND
50	SDO-D-2			150	P1-FS-3		
		100	ID-2			200	SDO-A-3

6 Operating Parameters and Housekeeping Channels

While the implementation details differ, the housekeeping channels and the DAC-controlled parameters share a common addressing scheme. An address is seven bits. All seven are provided to the multiplexors and their selection logic as HKA[6:0]. The most significant four bits DCS[3:0] drive the DAC selection logic: the least significant three bits are part of the serial command that sets a DAC.

Table 6: Address Map

Address Offset	CCD	Group
0	1	Bias Group
16	2	Bias Group
32	3	Bias Group
48	4	Bias Group
64	1	Clock Driver Group
72	2	Clock Driver Group
80	3	Clock Driver Group
88	4	Clock Driver Group
96		Heater Group
104		Interface Group
112		Thermal Group

The control ranges often go outside the actual range allowed for the parameters, which depend on circuit details and power supply voltages. I will document these limits in the future. Control is sometimes relative to another parameter. If the control range is not given, the parameter is not under DAC control.

6.1 Bias Group

Table 7: Bias Group

Address Offset	Signal	Housekeeping		Control		Range		Unit	Relative To
		Low	High	Low	High	Low	High		
0	Output Gate	-16.5	16.5	-8.0	4.0			V	
1	Input Gate 1	-16.5	16.5	-8.0	4.0			V	
2	Input Gate 2	-16.5	16.5	-8.0	4.0			V	
3	Scupper	-16.5	16.5	0	15.0			V	
4	Reset Drain	-16.5	16.5	0	15.0			V	
5	Backside	-16.5	16.5	0	5.0			V	
6	Substrate	-82	82	0	-50			V	
7	Board Temperature	-360	360					K	
8	Output Drain A	-27.3	27.3	0	10.0			V	Reset Drain
9	Output Drain B	-27.3	27.3	0	10.0			V	Reset Drain
10	Output Drain C	-27.3	27.3	0	10.0			V	Reset Drain
11	Output Drain D	-27.3	27.3	0	10.0			V	Reset Drain
12	Output Source A	-27.3	27.3					V	
13	Output Source B	-27.3	27.3					V	
14	Output Source C	-27.3	27.3					V	
15	Output Source D	-27.3	27.3					V	

6.2 Clock Driver Group

Table 8: Clock Driver Group

Address Offset	Signal	Housekeeping		Control		Range		Unit	Relative To
		Low	High	Low	High	Low	High		
0	Parallel High	-16.5	16.5	0	9.9			V	Parallel Low
1	Parallel Low	-16.5	16.5	0	-13.2			V	
2	Serial High	-16.5	16.5	13.2	-12			V	
3	Serial Low	-16.5	16.5	0	-9.9			V	Serial High
4	Reset High	-16.5	16.5	13.2	-12			V	
5	Reset Low	-16.5	16.5	0	-9.9			V	Reset High
6	Input Diode High	-16.5	16.5	0	15.0			V	
7	Input Diode Low	-16.5	16.5	0	15.0			V	

6.3 Heater Group

The Heater Group controls the three trim heaters on the lens barrel.

Table 9: Heater Group

Address Offset	Signal	Housekeeping		Control		Unit
		Low	High	Low	High	
0	Heater 1 Current	-273	273	0	227	mA
1	Heater 2 Current	-273	273	0	227	mA
2	Heater 3 Current	-273	273	0	227	mA

6.4 Interface Group

Table 10: Interface Group

Address Offset	Signal	Housekeeping		Unit
		Low	High	
1	+15	-16.5	16.5	V
2	+5	-16.5	16.5	V
3	-12	-16.5	16.5	V
4	+3.3F	-16.5	16.5	V
5	+2.5F	-16.5	16.5	V
6	+1.8F	-16.5	16.5	V
7	+1F	-16.5	16.5	V

6.5 Thermal Group

The Thermal Group (Table 11) sensors are external temperature-sensitive resistors. The nominal range for the circuitry is 500Ω to 1500Ω, which translates into the given temperature ranges. It may be useful to calibrate the board using external fixed resistors near the limits of the range.

Appendices

Table 11: Thermal Group

Address Offset	Signal	Housekeeping Low	Housekeeping High	Unit
0	Pt1000 sensor 1	-125	+130	C
1	Pt1000 sensor 2	-125	+130	C
2	Pt1000 sensor 3	-125	+130	C
3	Pt1000 sensor 4	-125	+130	C
4	Pt1000 sensor 5	-125	+130	C
5	Pt1000 sensor 6	-125	+130	C
6	Pt1000 sensor 7	-125	+130	C
7	Pt1000 sensor 8	-125	+130	C
8	Pt1000 sensor 9	-125	+130	C
9	Pt1000 sensor 10	-125	+130	C
10	Pt1000 sensor 11	-125	+130	C
11	Pt1000 sensor 12	-125	+130	C
12	AlCu sensor CCD1	-150	+40	C
13	AlCu sensor CCD2	-150	+40	C
14	AlCu sensor CCD3	-150	+40	C
15	AlCu sensor CCD4	-150	+40	C

A Default FPE Program

The following is the default *Sequencer DSL* FPE program associated with the observatory simulator.

```
/*
I've changed the phasing relative to the spreadsheet a little. The default stat
pixels now has P3–OR low, which makes a bit more sense before a row transfer to
*/

defaults {
    P1–IA–1 low P2–IA–1 high P3–IA–1 low
    P1–IA–2 low P2–IA–2 high P3–IA–2 low
    P1–IA–3 low P2–IA–3 high P3–IA–3 low
    P1–IA–4 low P2–IA–4 high P3–IA–4 low
    P1–FS–1 low P2–FS–1 high P3–FS–1 low
    P1–FS–2 low P2–FS–2 high P3–FS–2 low
    P1–FS–3 low P2–FS–3 high P3–FS–3 low
    P1–FS–4 low P2–FS–4 high P3–FS–4 low
    P1–OR low P2–OR high P3–OR low
    RG high ID high
    Int low DeInt low Clamp low CNV low
```

```
    }

/*
Another change is that I'm setting RG high as soon as Int goes low. There's no
RG circuit is much slower. We might be able to move RG low earlier for more Int
*/

sequence pixcycle {
    step
    P3-OR high step
    CNV high step
    step
    Clamp high step
    P2-OR low RG low step
    step
    step
    DeInt high Clamp low step
    P1-OR high step
    CNV low step
    step
    step
    P3-OR low DeInt low step
    step
    step
    step
    P2-OR high Int high step
    step
    step
    step
    P1-OR low step
    step
    Int low RG high step
    }

/*
For parallel to serial transfer, the serial clock machinations in the spreadshe
bit strange. From the CCD structure, it appears that having P1-OR and P2-OR hig
*/

sequence fr2serial {
    P3-FS-1 high P3-FS-2 high P3-FS-3 high P3-FS-4 high P1-OR high
    step(24)
    P2-FS-1 low P2-FS-2 low P2-FS-3 low P2-FS-4 low
    step(24)
    P1-FS-1 high P1-FS-2 high P1-FS-3 high P1-FS-4 high
```

```
    step(24)
    P3–FS–1 low P3–FS–2 low P3–FS–3 low P3–FS–4 low
    step(24)
    P2–FS–1 high P2–FS–2 high P2–FS–3 high P2–FS–4 high
    step(24)
    P1–FS–1 low P1–FS–2 low P1–FS–3 low P1–FS–4 low P1–OR low
    step(24)
}

/*
Bare bones frame transfer cycles: no serials.
*/

sequence frametransfer1 {
    P3–FS–1 high P3–IA–1 high
    step(24)
    P2–FS–1 low P2–IA–1 low
    step(24)
    P1–FS–1 high P1–IA–1 high
    step(24)
    P3–FS–1 low P3–IA–1 low
    step(24)
    P2–FS–1 high P2–IA–1 high
    step(24)
    P1–FS–1 low P1–IA–1 low
    step(24)
}

sequence frametransfer2 {
    P3–FS–2 high P3–IA–2 high
    step(24)
    P2–FS–2 low P2–IA–2 low
    step(24)
    P1–FS–2 high P1–IA–2 high
    step(24)
    P3–FS–2 low P3–IA–2 low
    step(24)
    P2–FS–2 high P2–IA–2 high
    step(24)
    P1–FS–2 low P1–IA–2 low
    step(24)
}

sequence frametransfer3 {
    P3–FS–3 high P3–IA–3 high
```

```
    step(24)
    P2-FS-3 low P2-IA-3 low
    step(24)
    P1-FS-3 high P1-IA-3 high
    step(24)
    P3-FS-3 low P3-IA-3 low
    step(24)
    P2-FS-3 high P2-IA-3 high
    step(24)
    P1-FS-3 low P1-IA-3 low
    step(24)
}

sequence frametransfer4 {
    P3-FS-4 high P3-IA-4 high
    step(24)
    P2-FS-4 low P2-IA-4 low
    step(24)
    P1-FS-4 high P1-IA-4 high
    step(24)
    P3-FS-4 low P3-IA-4 low
    step(24)
    P2-FS-4 high P2-IA-4 high
    step(24)
    P1-FS-4 low P1-IA-4 low
    step(24)
}

/*
Physical layout of CCID80.
*/

parameter rows = 2048;
parameter buffer_rows = 10;/* top and bottom */
parameter physical_rows = rows + 2 * buffer_rows;
parameter columns = 512;
parameter prescan = 11;
parameter physical_columns = prescan+columns;

/*
Other parameters.
*/

parameter preflush = 2; /* physical rows to flush before first row */
parameter overclock = 11; /* extra rows and columns to clock */
```

```
/*
The sequencer program.
*/

no_data ( physical_rows ) frametransfer1;
no_data ( physical_rows ) frametransfer2;
no_data ( physical_rows ) frametransfer3;
no_data ( physical_rows ) frametransfer4;

no_data ( preflush * physical_columns ) pixcycle; /* flush serials */
do (buffer_rows) {
    no_data ( 1 ) fr2serial;
    no_data ( physical_columns + overclock ) pixcycle
}

/* Now start taking data */

frame {
    do( rows ) {
    no_data ( 1 ) fr2serial;
    pixel_data ( physical_columns + overclock ) pixcycle;
    }
}

/* Clean up */

do (buffer_rows) {
    no_data ( 1 ) fr2serial;
    no_data ( physical_columns + overclock ) pixcycle;
}

hold pixcycle; /* clock serials between frames */
```