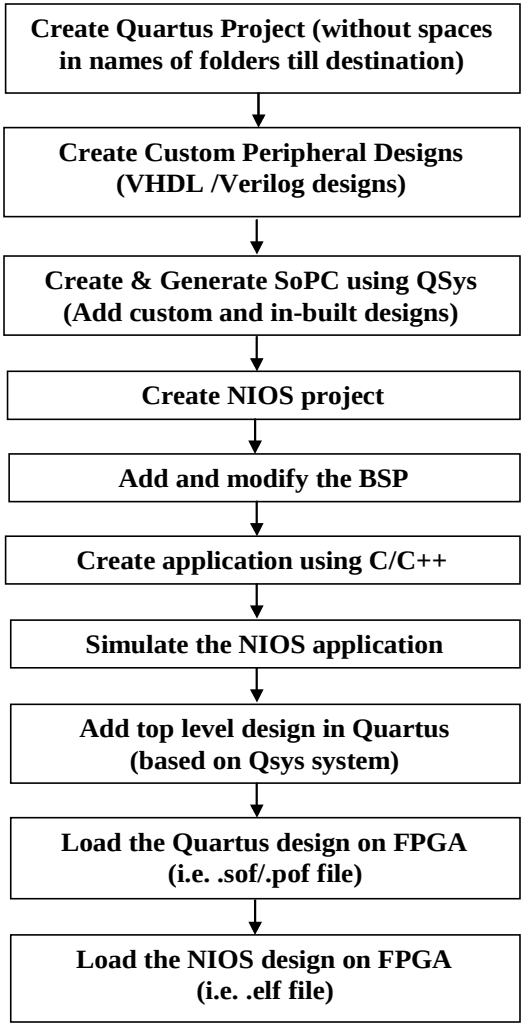
Create Quartus Project (without spaces in names of folders till destination)
Create Custom Peripheral Designs (VHDL /Verilog designs)
Create & Generate SoPC using QSys (Add custom and in-built designs)
Create NIOS project
Add and modify the BSP
Create application using C/C++
Simulate the NIOS application
Add top level design in Quartus (based on Qsys system)
Load the Quartus design on FPGA (i.e. .sof/.pof file)
Load the NIOS design on FPGA (i.e. .elf file)