INTEGRATED OPTICS I: SILICON PHOTONICS

SHIRAZ UNIVERSITY

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2015

PHOTONICS AND SILICON PHOTONICS

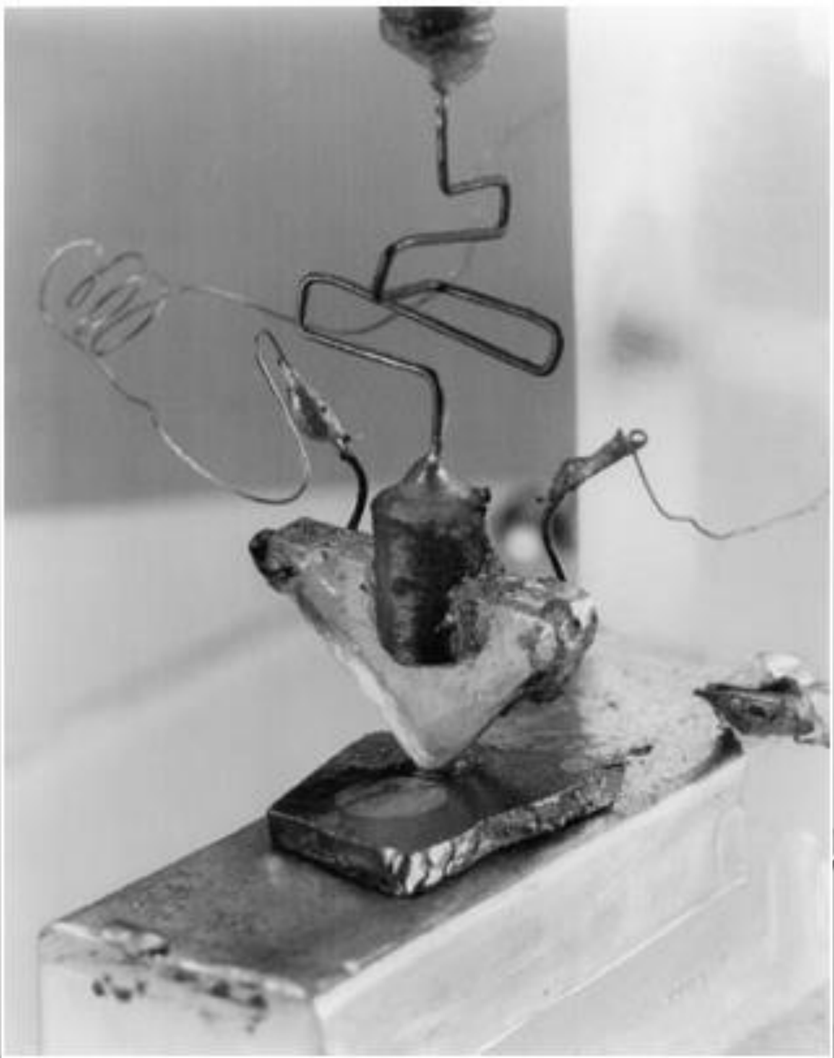
- PHOTONICS IS THE TECHNOLOGY ASSOCIATED WITH SIGNAL GENERATION, PROCESSING, TRANSMISSION AND DETECTION WHERE THE SIGNAL IS CARRIED BY PHOTONS (I. E. LIGHT)
- PHOTONIC DEVICES PRODUCED WITHIN STANDARD SILICON FACTORY AND WITH STANDARD SILICON PROCESSING

OUTLINE

- MICROELECTRONIC EVOLUTION
  - THREE RULES: SMALLER, CHEAPER, FASTER.
  - LIMITATIONS!
- OPTICAL COMMUNICATION EVOLUTION
- A NEW TECHNOLOGY PLATFORM: SILICON PHOTONICS
  - CURRENT STATUS
  - EXPECTATIONS

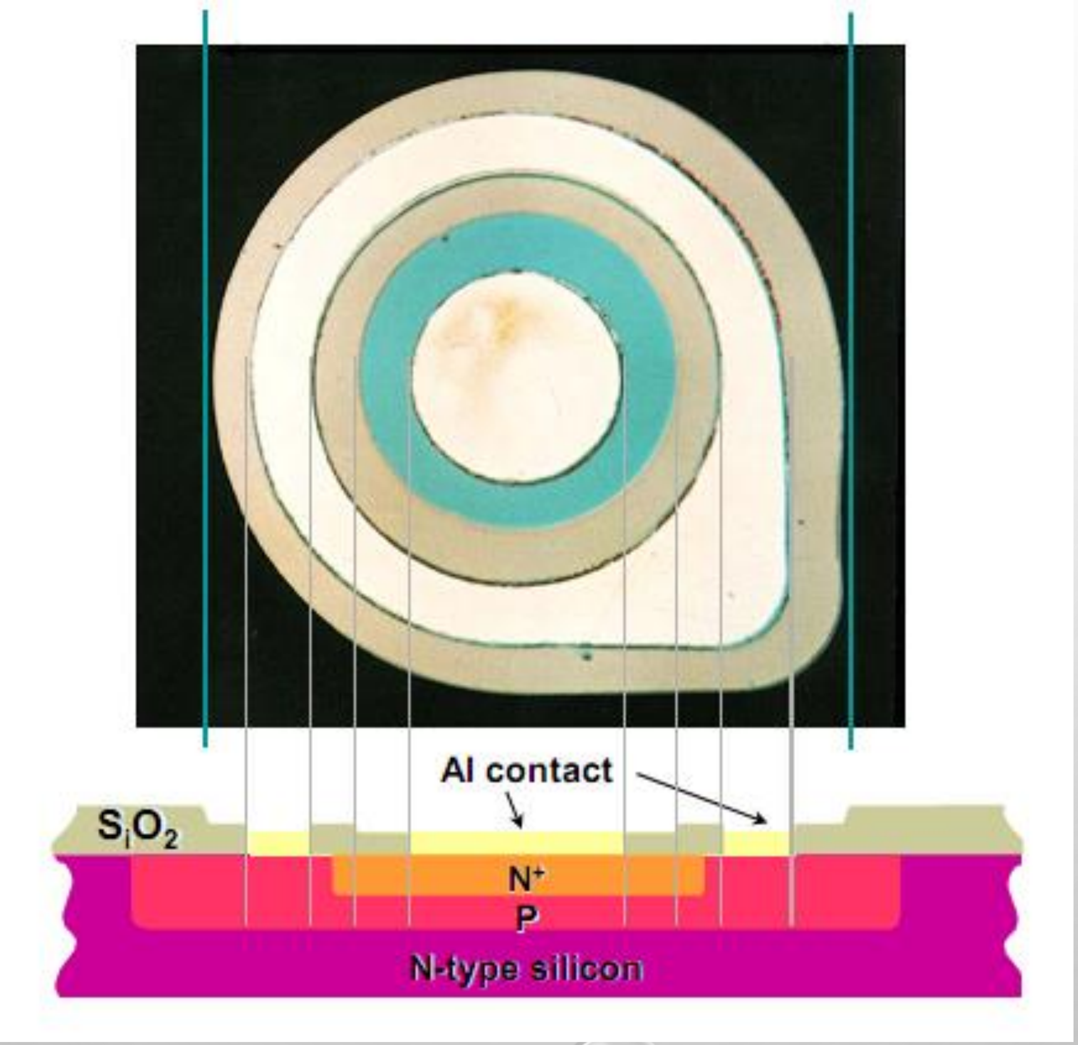
THE INVENTION OF THE TRANSISTOR

- 1947



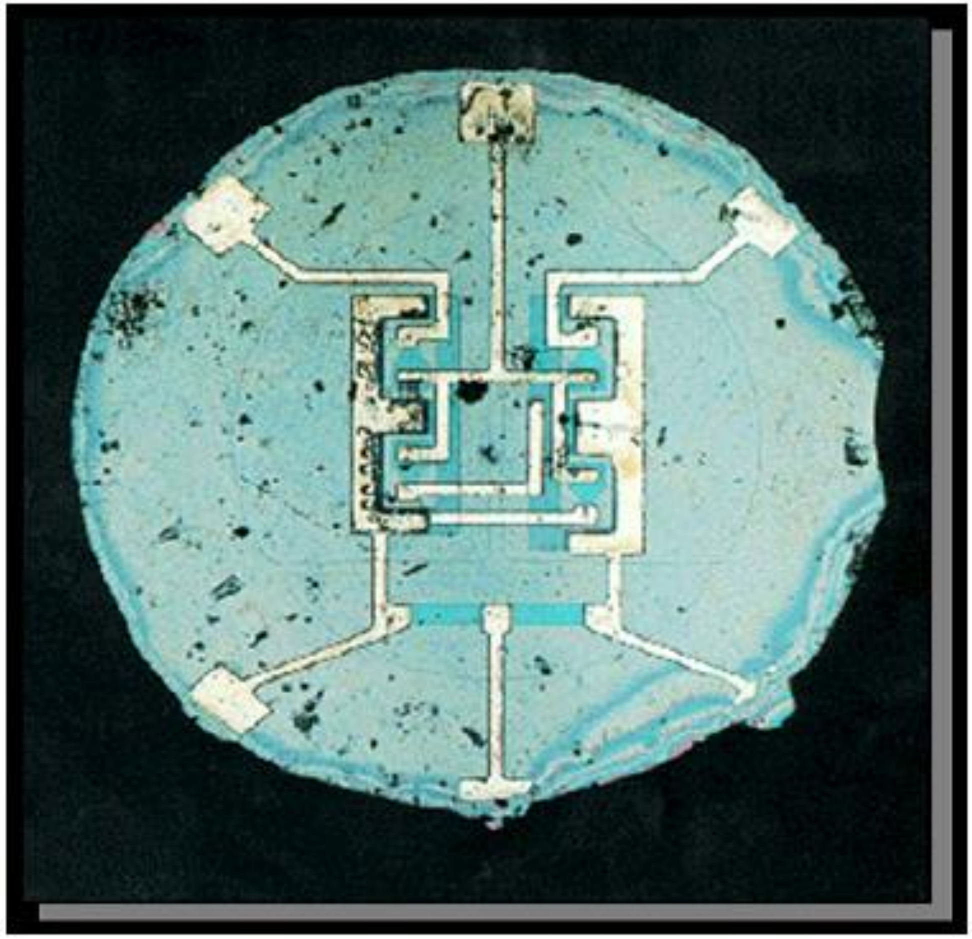
THE FIRST PLANAR TRANSISTOR

- 1959



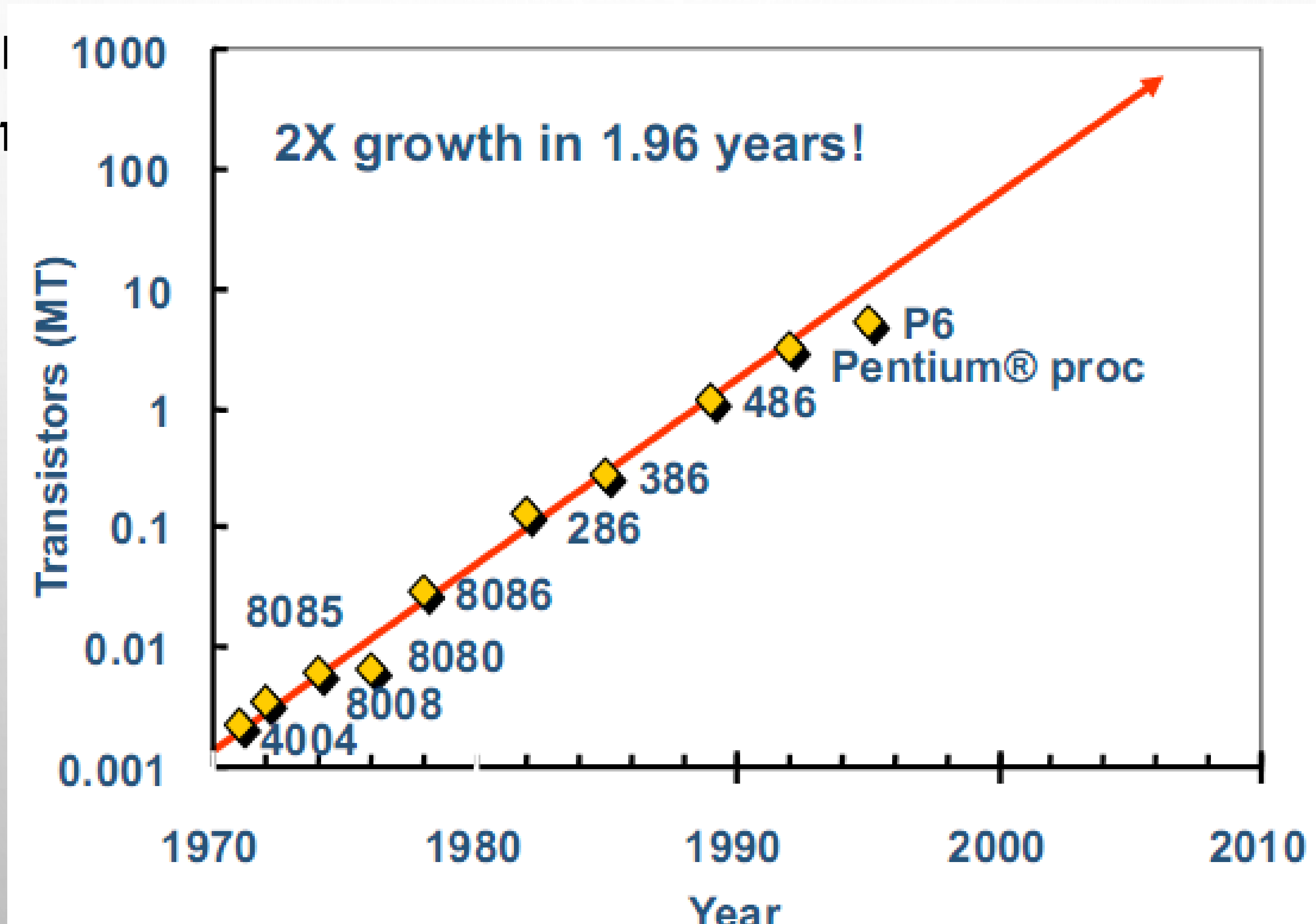
THE FIRST PLANAR INTEGRATED CIRCUIT

- 1961



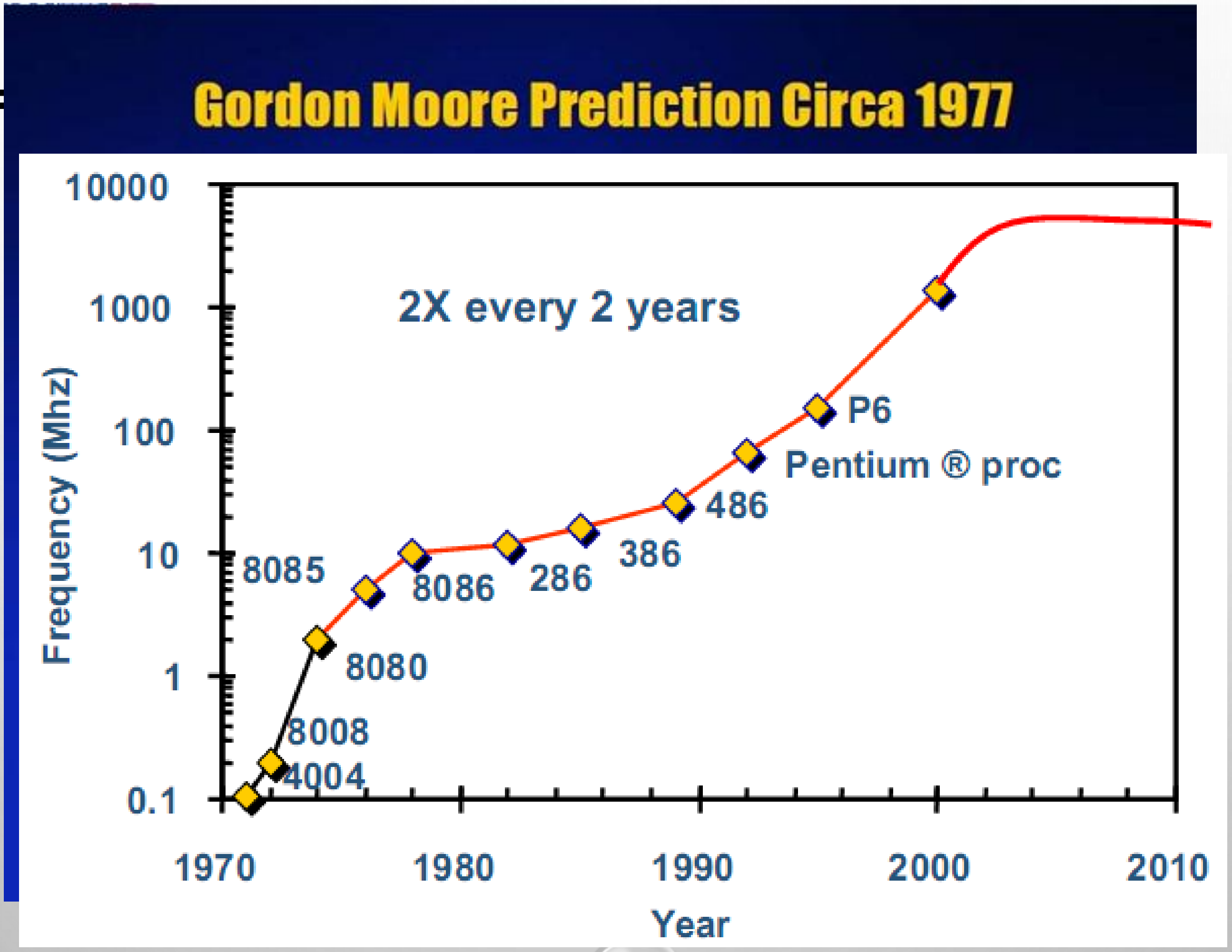
MOORE’S LAW

- **INTE**
  - 1

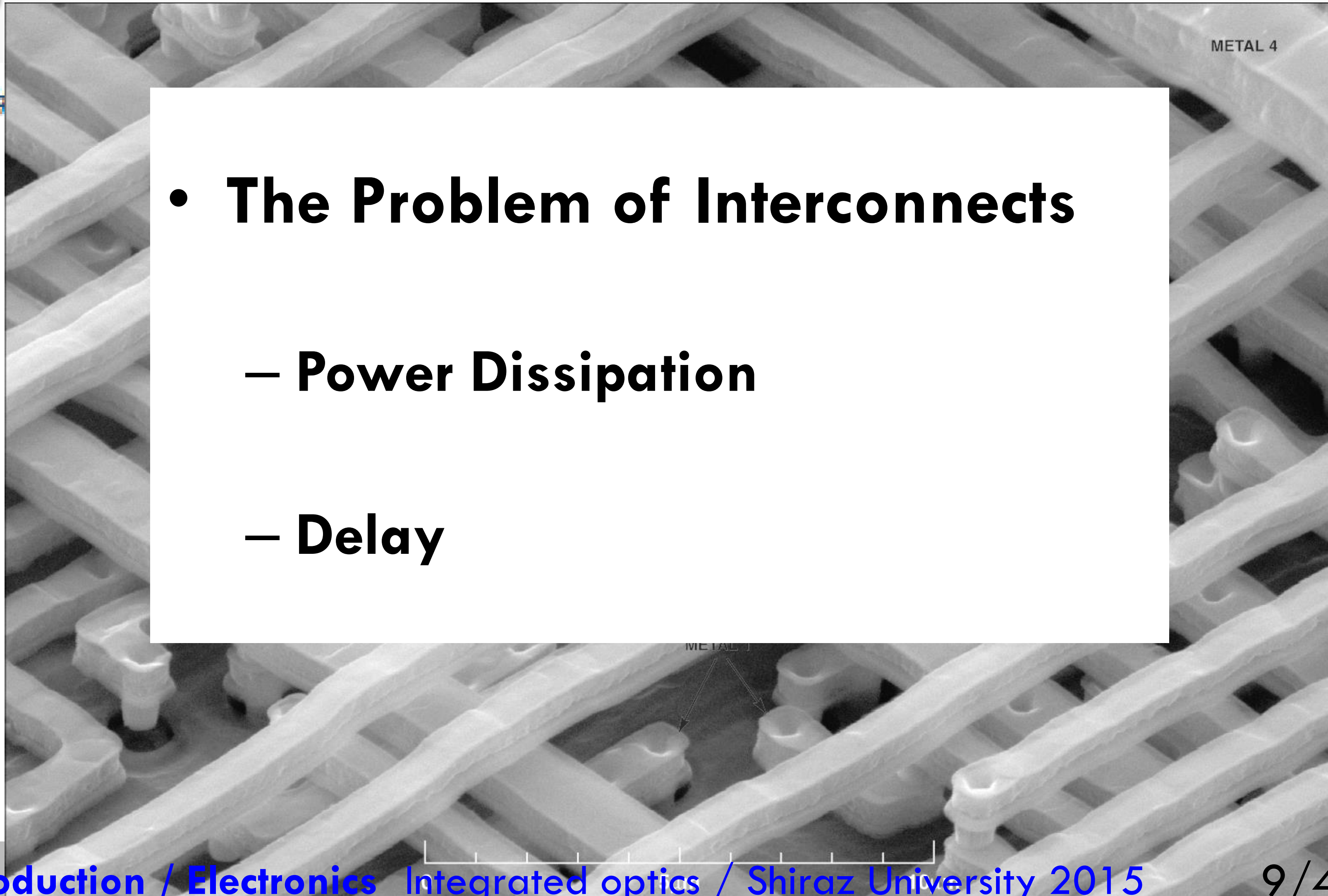


LIMITATIONS OF ELECTRONIC EVOLUTION

- CLOCK F



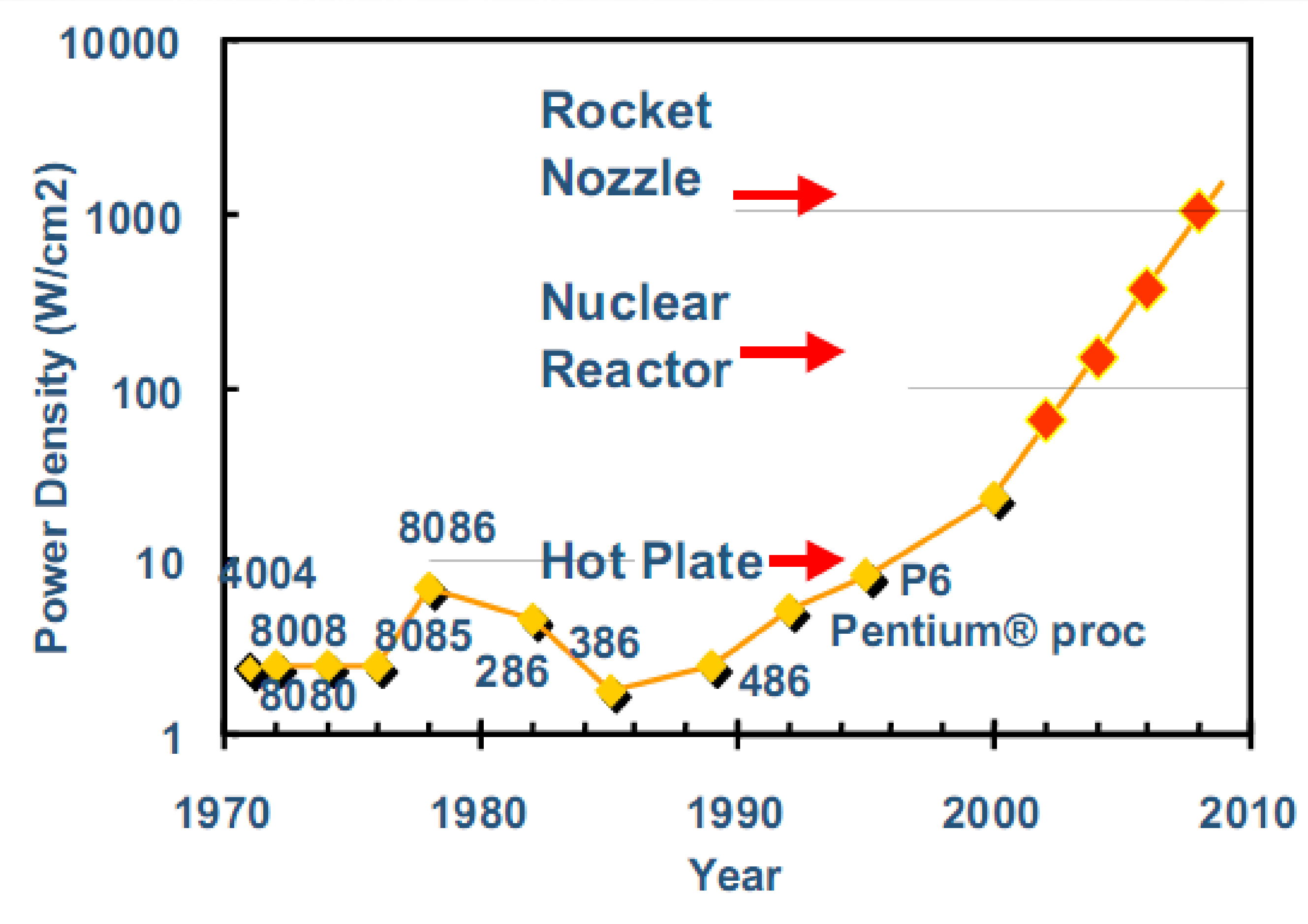
LIMITATIONS OF ELECTRONIC



- **The Problem of Interconnects**
  - **Power Dissipation**
  - **Delay**

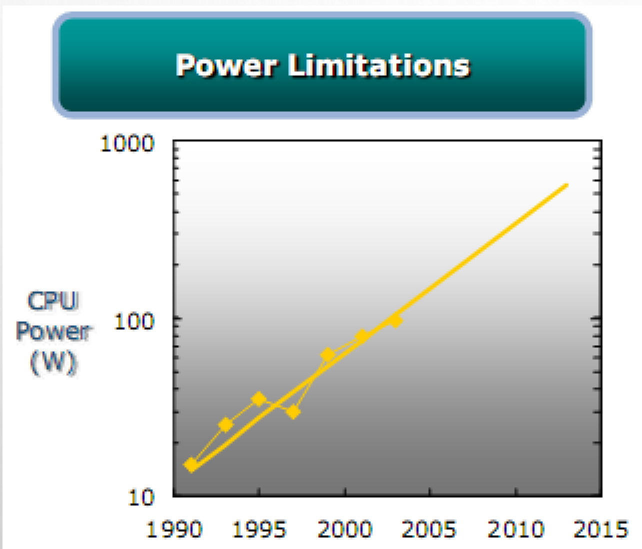
LIMITATIONS OF ELECTRONIC EVOLUTION

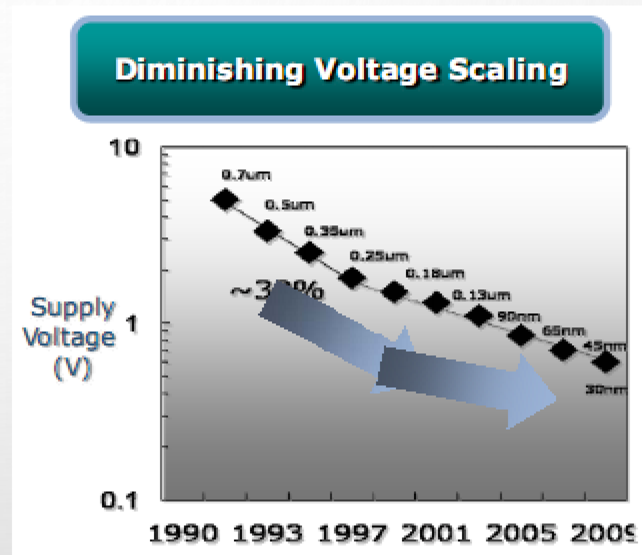
- **POWER DENSITY**



LIMITATIONS OF ELECTRONIC EVOLUTION

- **POWER DENSITY**





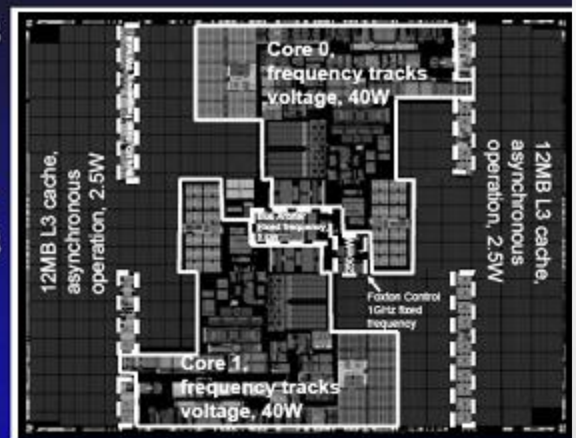
Power = Capacitance x Voltage^2 x Frequency
also
Power ~ Voltage^3

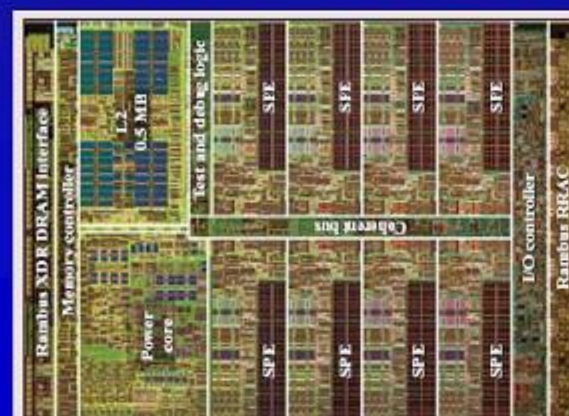
LIMITATIONS OF ELECTRONIC EVOLUTION

The Rise of Multi-Core Architectures

- Rise of parallel multi-core architectures to mitigate power dissipation
- Parallel architectures with multiple simpler processing cores provide better performance per watt than architectures based on a single complex processor
- State-of- the-art commercial chips feature more parallel and distributed architectures that are essentially multi-core chips
  - Montecito (Intel)
  - Cell (IBM, Toshiba, Sony)
- Key is to design robust, scalable, fast, and power-efficient:

intra-chip communication networks





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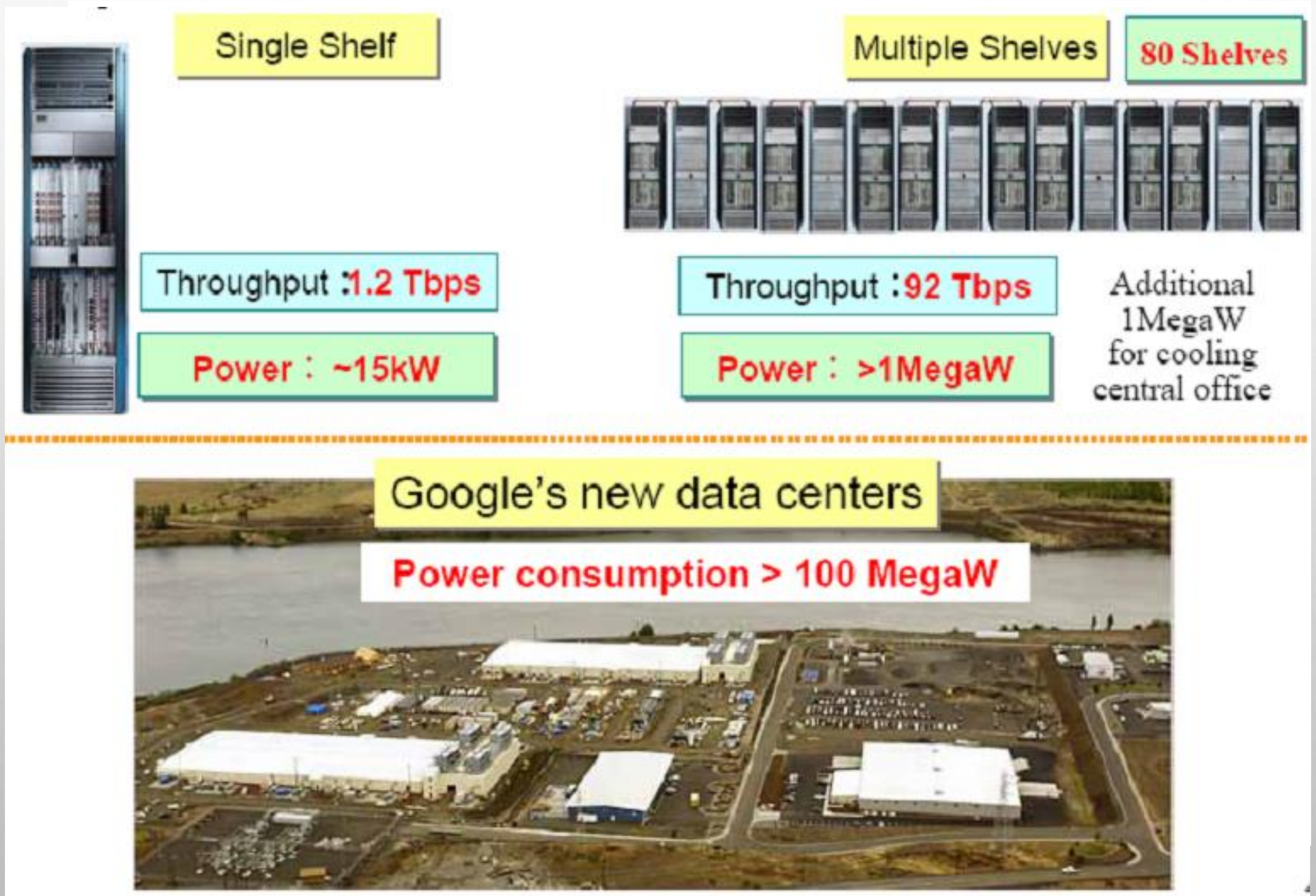
LIMITATIONS OF ELECTRONIC EVOLUTION

- **INTERCONNECTS POSE PROBLEMS NOT ONLY WITHIN THE CHIP**

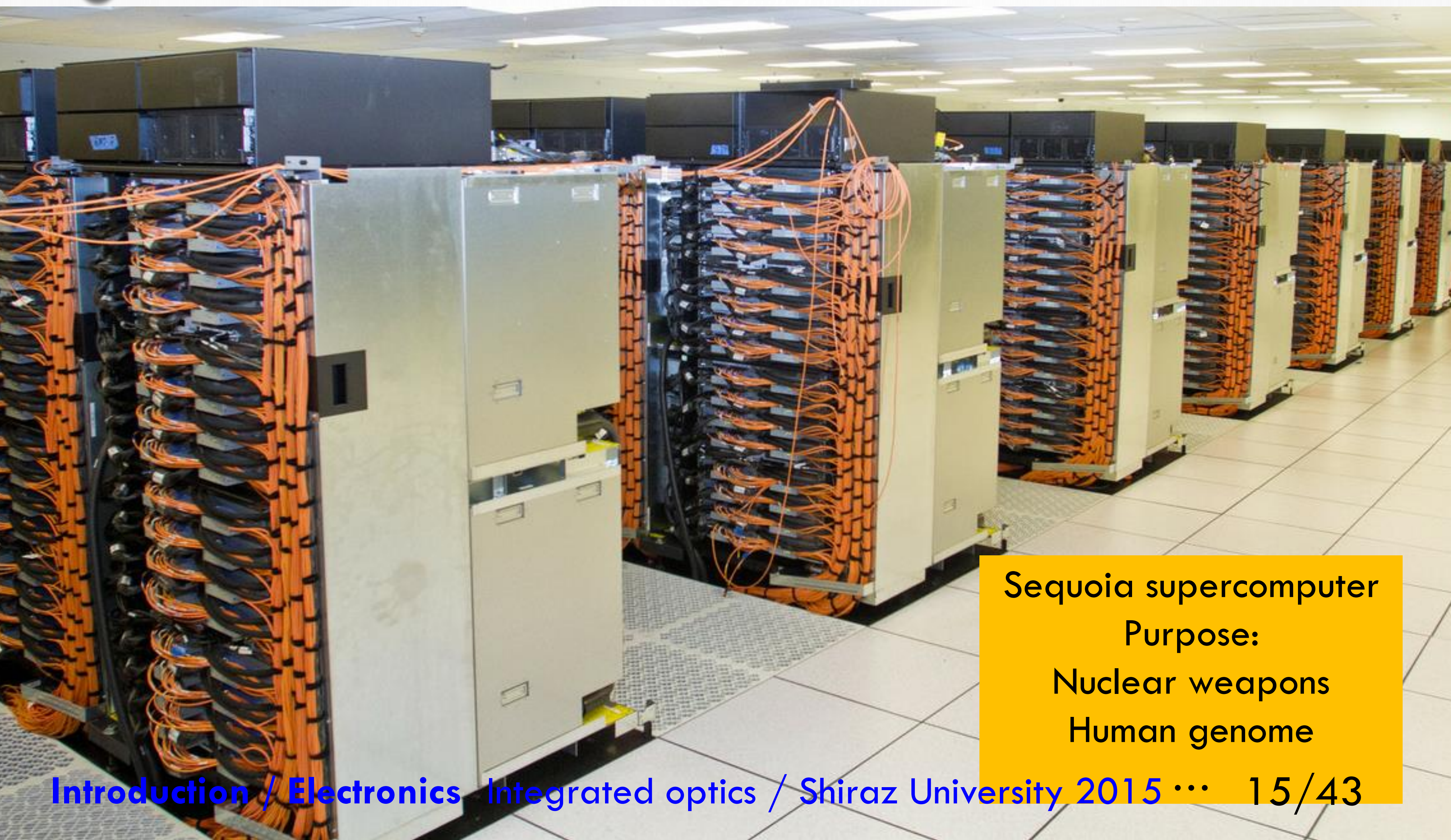


AN EXAMPLE

- **DATA SERVERS AND SUPERCOMPUTERS**

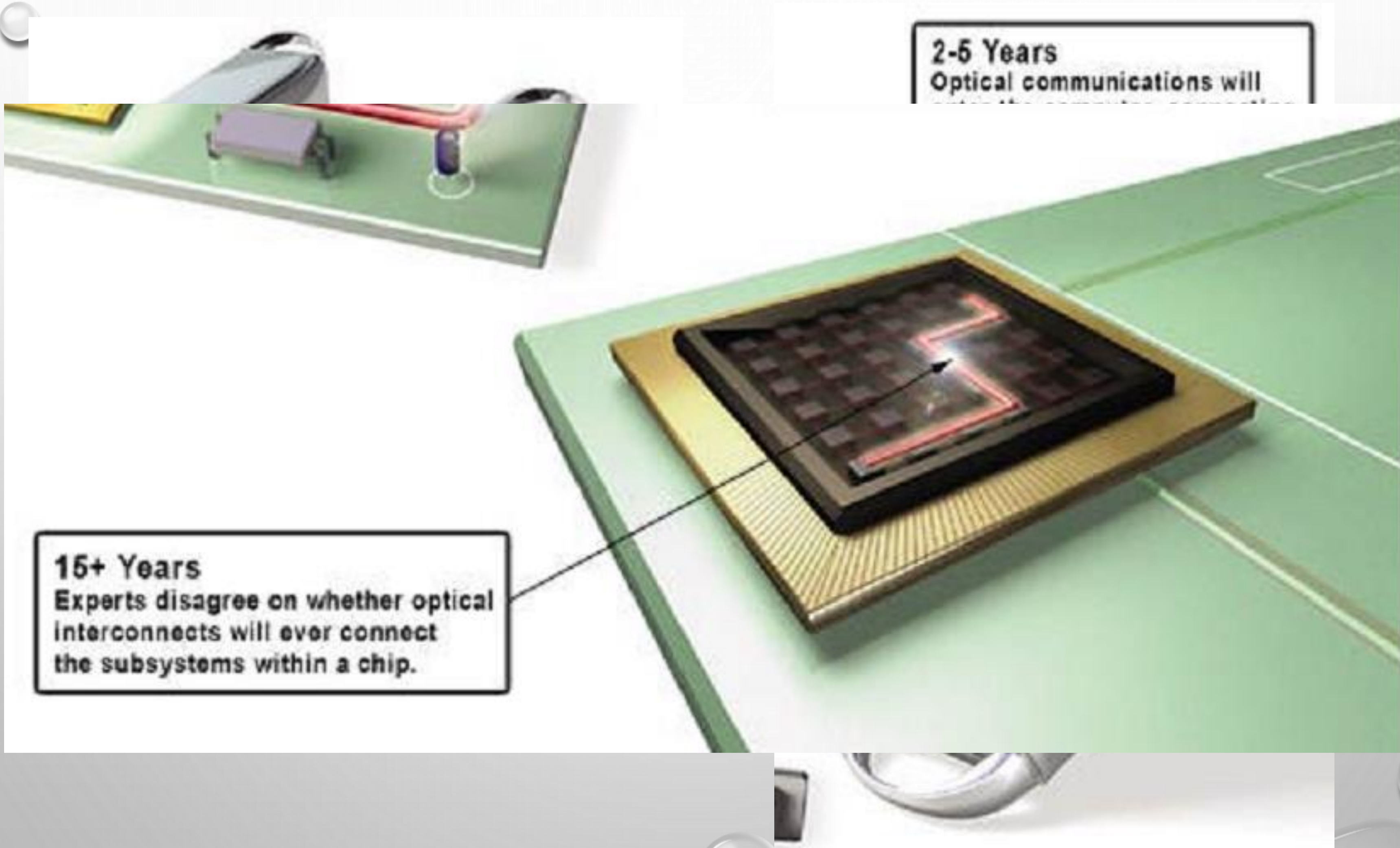
- Facebook datacenter
  - 130,000 m^2
  - 65 MW
  - 75% data traffic is inside datacenter

OPTICAL VS. ELECTRICAL DATA COMMUNICATION



Sequoia supercomputer
Purpose:
Nuclear weapons
Human genome

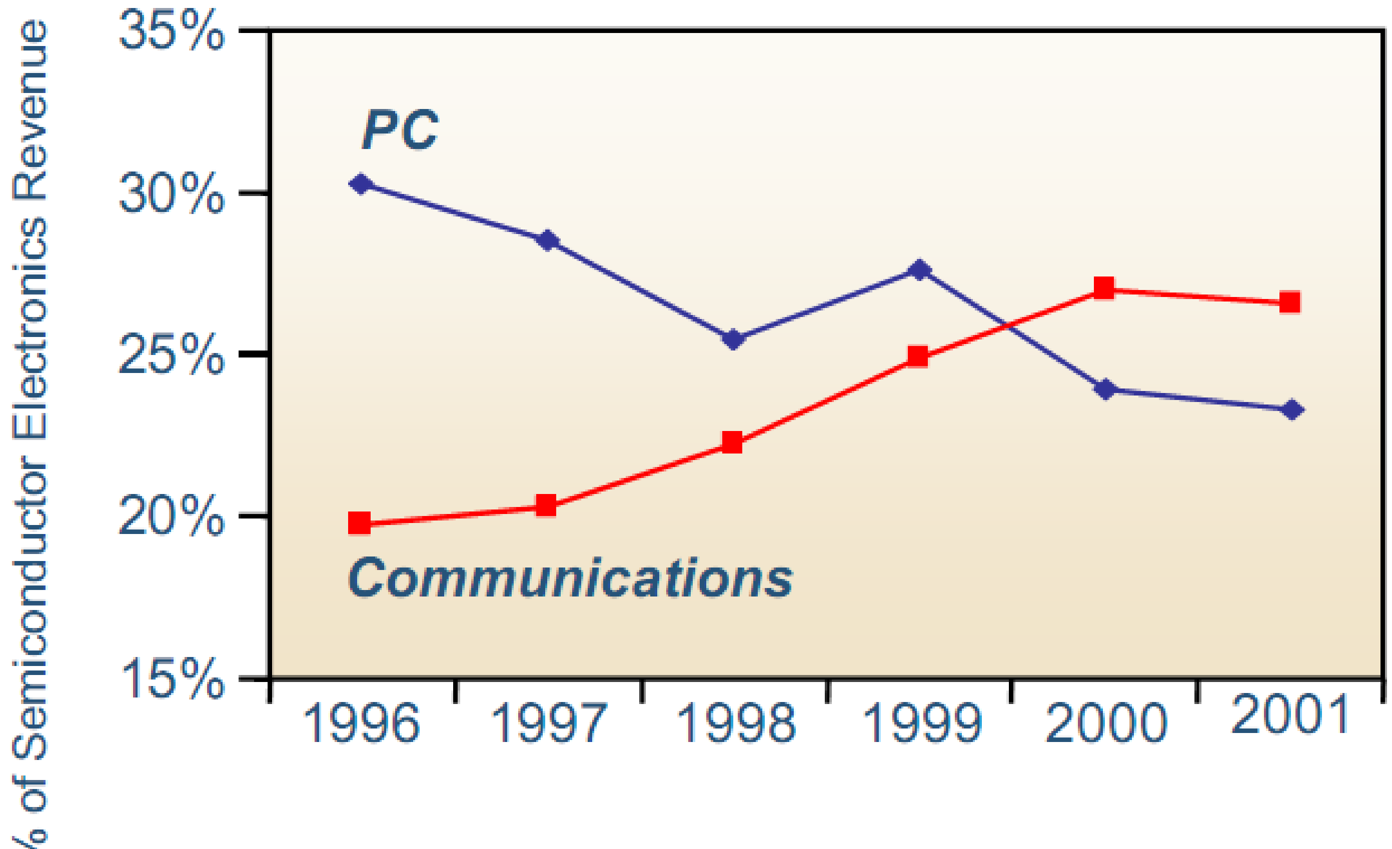
OPTICAL INTERCONNECTS



OPTICAL COMMUNICATIONS: A BRIEF HISTORY

- 1958-59 KAPANY CREATES OPTICAL FIBER WITH CLADDING
- 1960-TED MAIMAN DEMONSTRATES FIRST LASER IN RUBY
- 1962-4 GROUPS SIMULTANEOUSLY MAKE FIRST SEMICONDUCTOR LASERS
- 1970-FIRST ROOM TEMP. CW SEMICONDUCTOR LASER-HAYASHI & PANISH
- APRIL 1977-FIRST FIBER LINK WITH LIVE TELEPHONE TRAFFIC
  - GTE LONG BEACH 6 MB/S
- MAY 1977-FIRST BELL SYSTEM 45 MB/S LINKS 850NM MM
- EARLY 1980S-IN-GA-AS-P 1.3 µM LASERS
  - 0.5 DB/KM, LOWER DISPERSION-SINGLE MODE
- LATE 1980'S-SINGLE MODE TRANSMISSION AT 1.55 µM, 0.2 DB/KM
- 1989-ERBIUM DOPED FIBER AMPLIFIER
- 1996- 8 CHANNEL WDM

EVOLUTION OF COMMUNICATION



In 2000, for the first time, semiconductor revenues in communication exceeded revenues in PC sector.

WHY SILICON?

- TRANSPARENT IN 1.3-1.6 UM WAVELENGTH REGION
- COMS COMPATIBILITY
  - MATURE AND WIDESPREAD TECHNOLOGY
- LOW COST
  - CHEAPER THAN OTHER SEMICONDUCTORS
- HIGH INDEX CONTRAST → SMALL FOOT PRINT

WHY SILICON?

	Wafer size (R&D)	Wafer size (commercial)	Wafer cost (€)	mm² substrate cost (€)
Si	450 mm	300 mm	100	0.001
SOI	?	300 mm	800	0.008
InP	150 mm	100 mm	300	0.03
GaAs	200 mm	150 mm	300	0.013

PROBLEMS WITH SILICON

- NO DETECTION IN 1.3 – 1.6 UM BANDWIDTH
  - INDIRECT BANDGAP
- HIGH INDEX CONTRAST
  - → POOR COUPLING
- NO ELECTRO-OPTIC EFFECT
- LACKS EFFICIENT LIGHT EMISSION

SILICON PHOTONICS

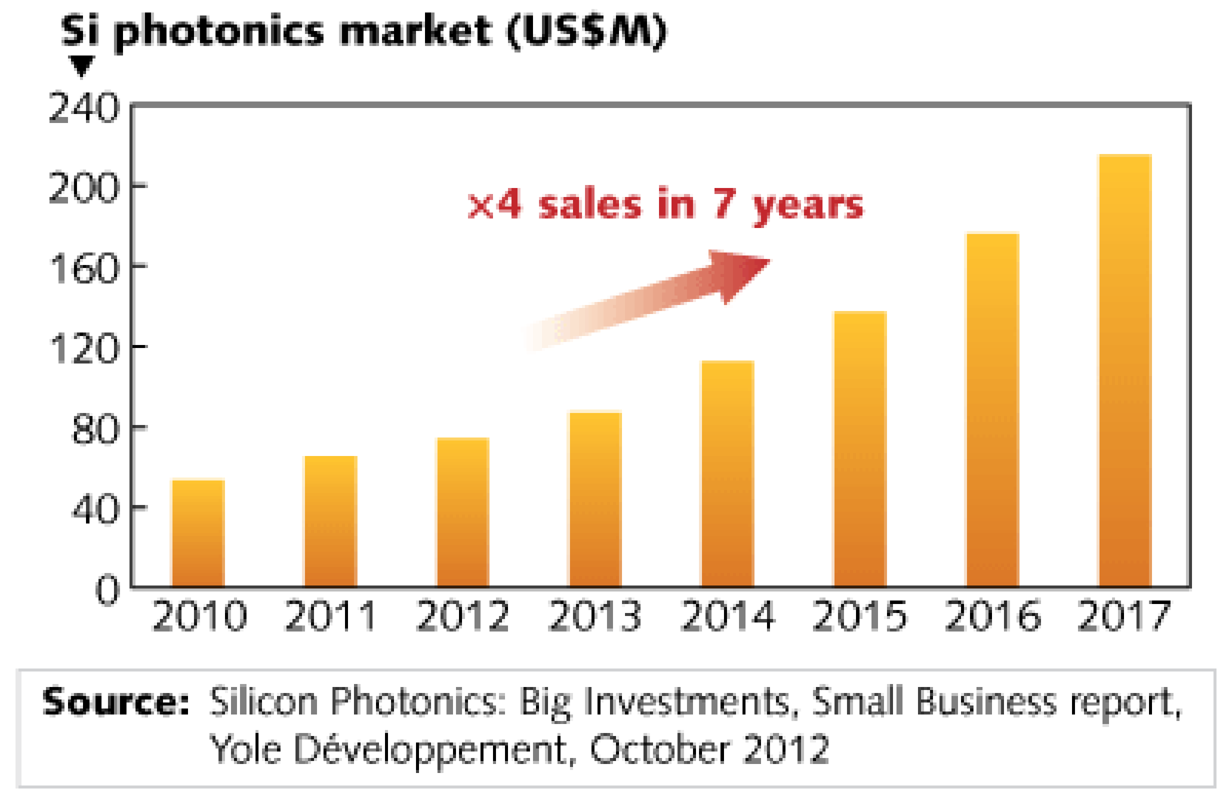
- APPLICATION OVERVIEW
- CURRENT STATUS AND PREDICTED NEAR FUTURE
- OPTO-ELECTRONIC INTEGRATED CIRCUIT (OEIC)
- BUILDING BLOCKS OF OEIC'S
  - WAVEGUIDES, WAVEGUIDE/FIBER COUPLERS
  - SOURCE AND DETECTOR
  - MODULATOR, MULTIPLEXER, DEMULTIPLEXER

APPLICATIONS

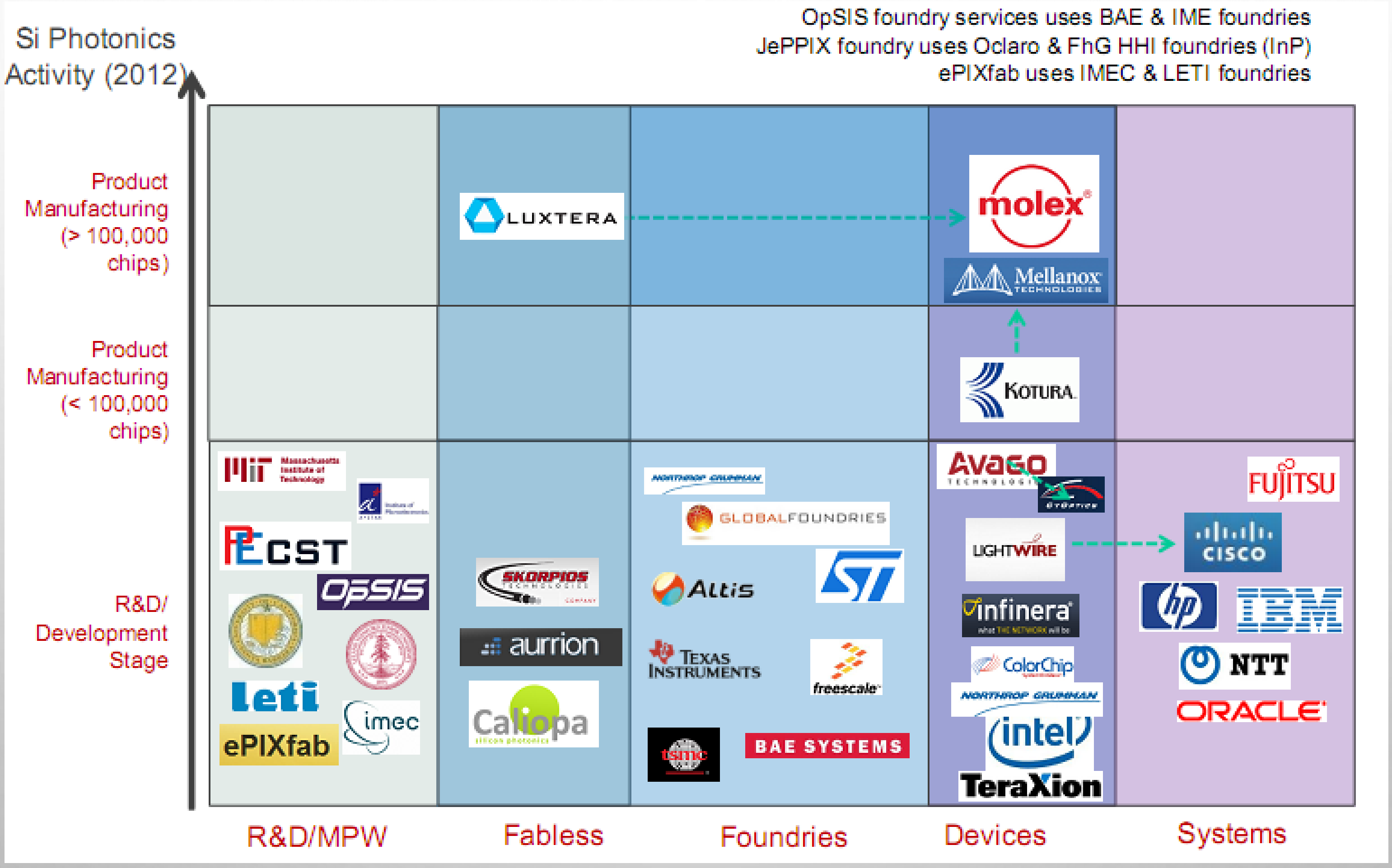
Applications	Examples	Data Rate
Telecom	Used in Metro (1 - 80Km) and long haul applications (40 - 1,000 Km)	10G, 40G, 100G, 400Gbps systems
Datacom	Used in data centers (<1m - 2Km) and campus applications (1 - 5Km)	10G, 25G, 40G, 100Gbps interconnects between systems
Consumer	Connecting desktop PC devices and PCs with HDTVs	5G - 50Gbps
HPC & Data Centers	One High Performance Computer "supercomputer" may consume 40,000 AOCs or 250,000 mid-board modules	Up to 100 Gbps
Commercial Video	Digital signage, digital cinemas, video recording and studios; 4xx2K displays and recording equipment	10G - 50Gbps interconnects
Metrology and Sensors	Measurement of time, temperature, sound, frequency, and stress, range	Typically low data rates but using special silicon photonics sensors
Medical	DNA, glucose, molecular and cellular analysis, etc.	Typically low data rates but using special silicon photonics Sensors
Military / Aerospace	Used in scientific instruments at corporate and national labs; aircraft, space, missiles, radar, imaging and intelligence applications.	High

CURRENT STATUS AND FUTURE

- **SILICON PHOTONICS MARKET**



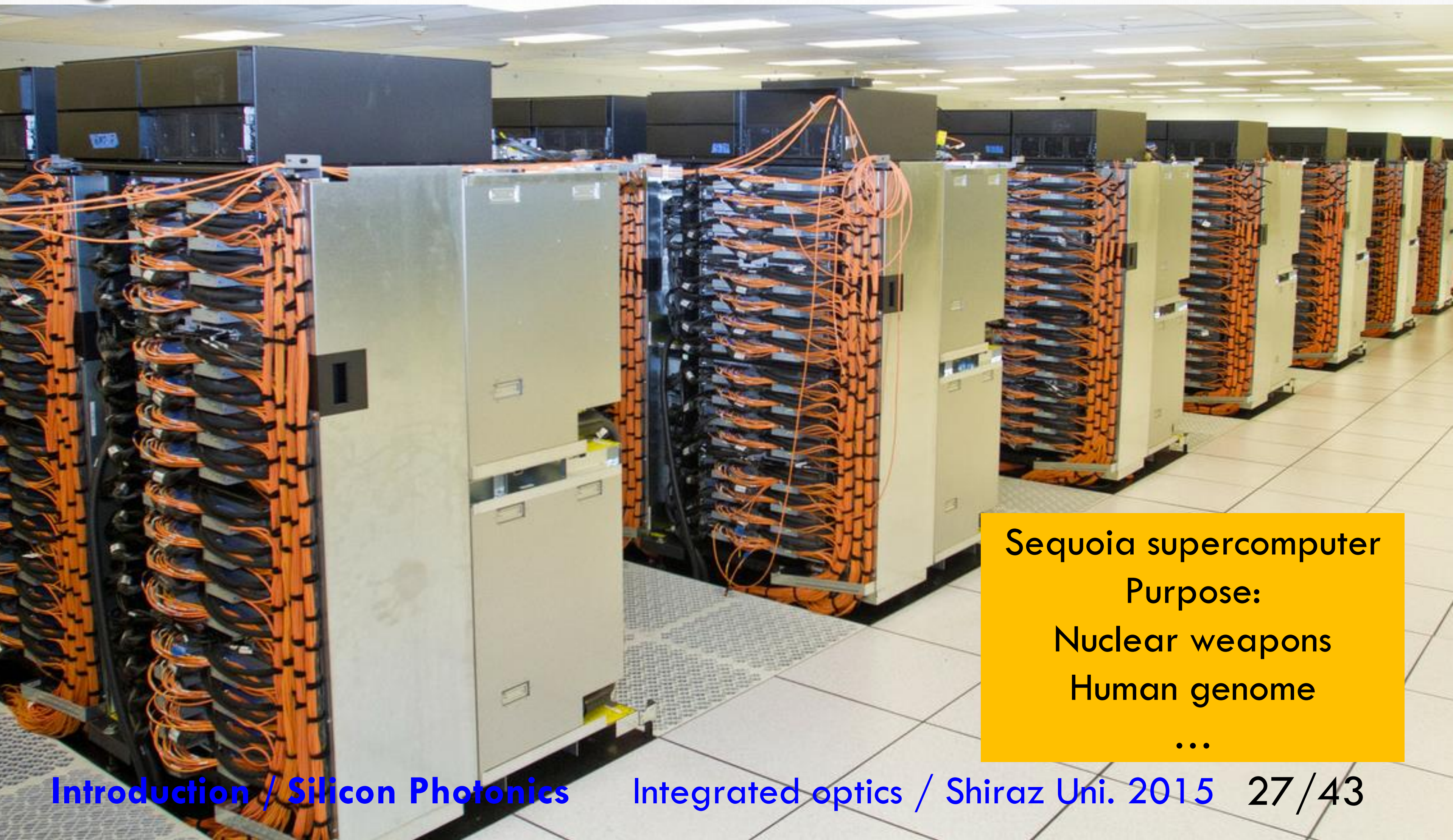
PLAYERS


Si Photonics Activity (2012)
OpSIS foundry services uses BAE & IME foundries
JePPIX foundry uses Oclaro & FhG HHI foundries (InP)
ePIXfab uses IMEC & LETI foundries
Product Manufacturing (> 100,000 chips)
Product Manufacturing (< 100,000 chips)
R&D/ Development Stage
R&D/MPW
Fabless
Foundries
Devices
Systems

AN EXAMPLE OF APPLICATIONS

- Facebook datacenter
  - 130,000 m^2
  - 65 MW
  - 75% data traffic is inside datacenter

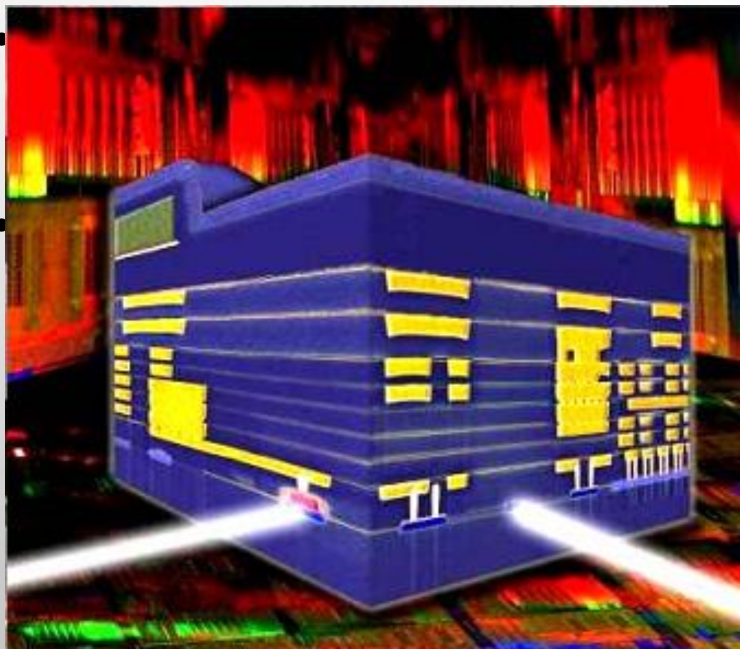
OPTICAL VS. ELECTRICAL DATA COMMUNICATION

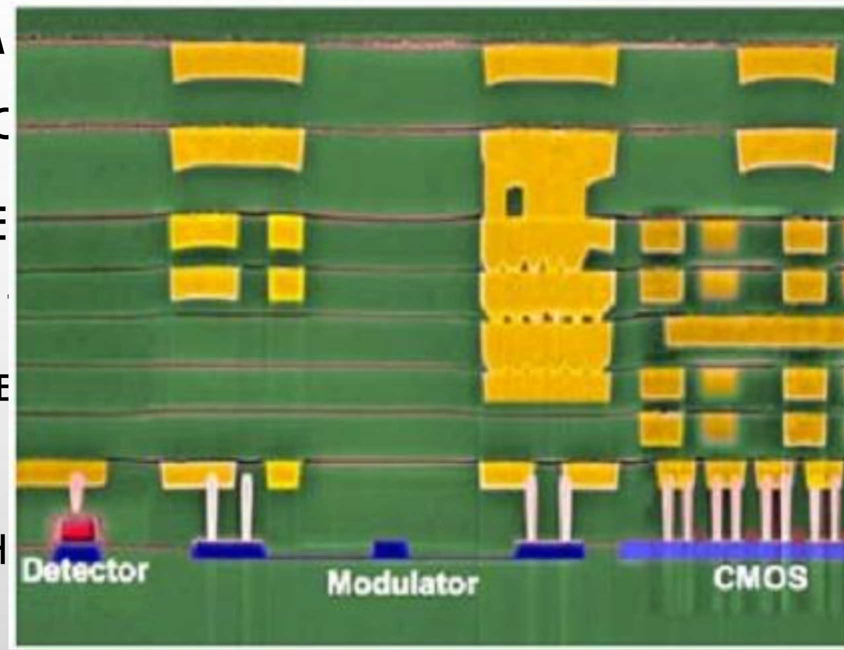


Sequoia supercomputer
Purpose:
Nuclear weapons
Human genome
...

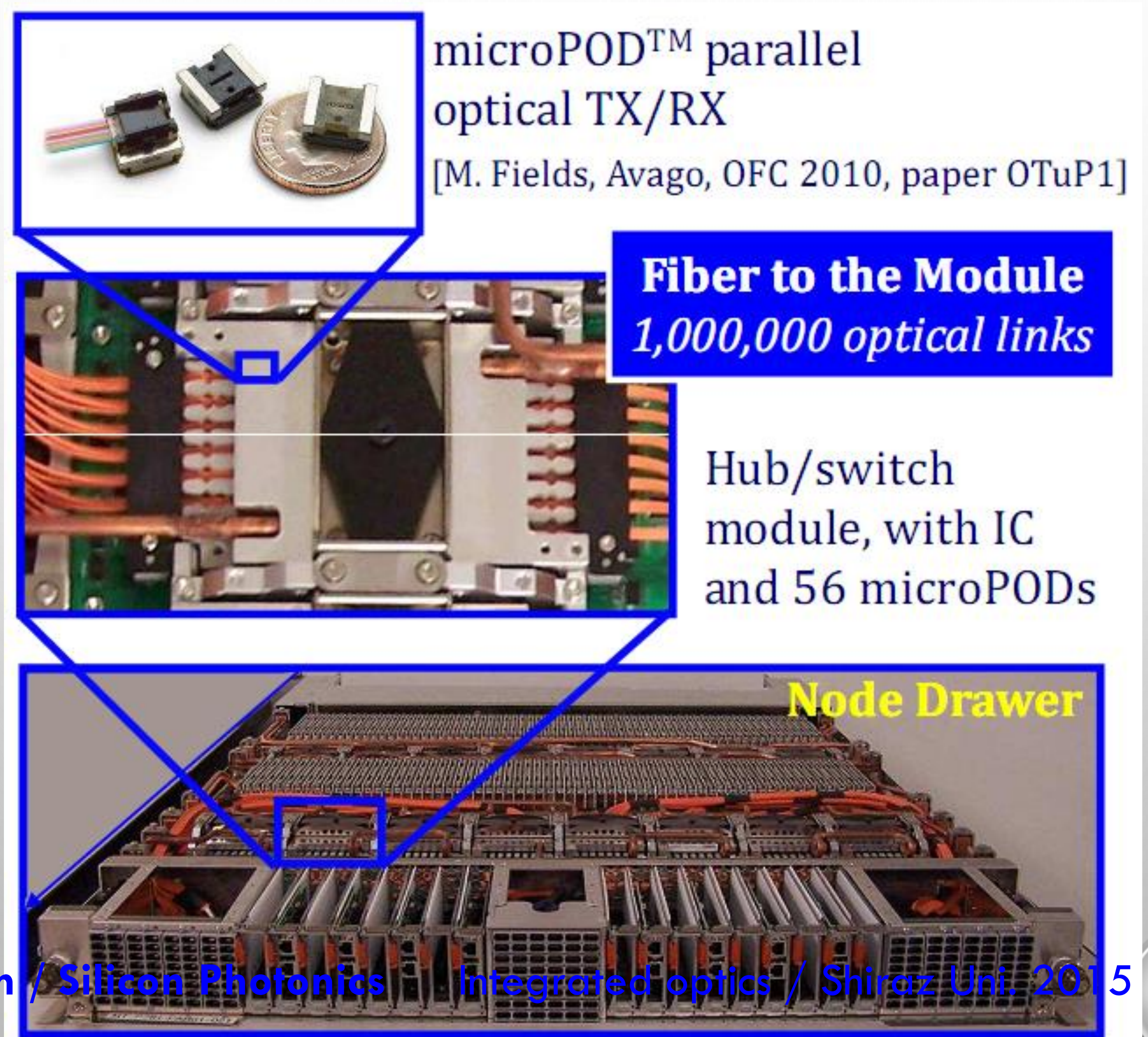
CURRENT TECHNOLOGY

- AM
  HIC
- GLE
  ER
  RGE
  TH



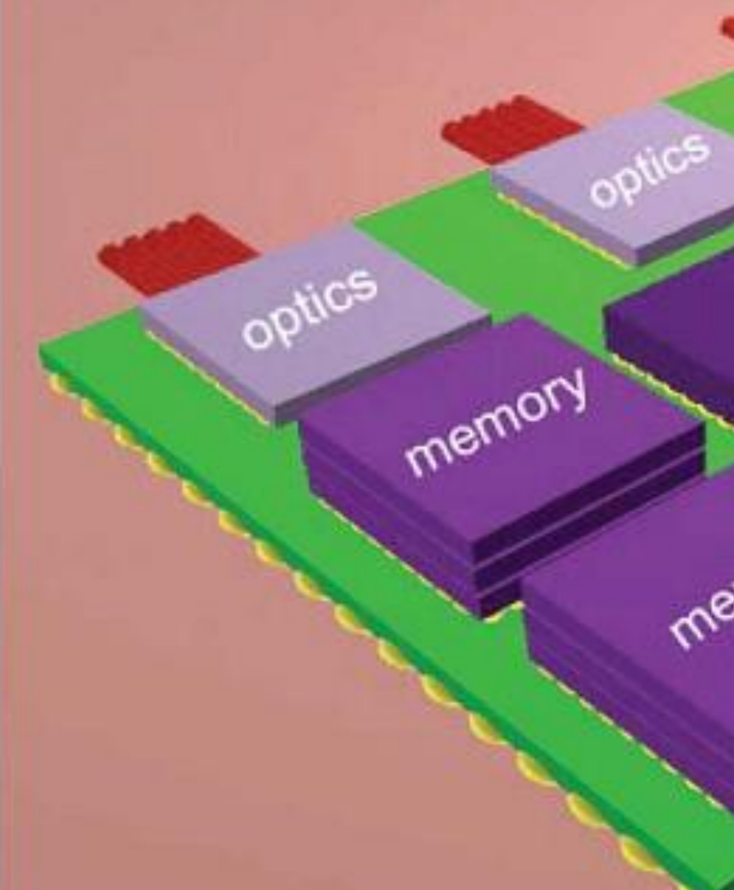


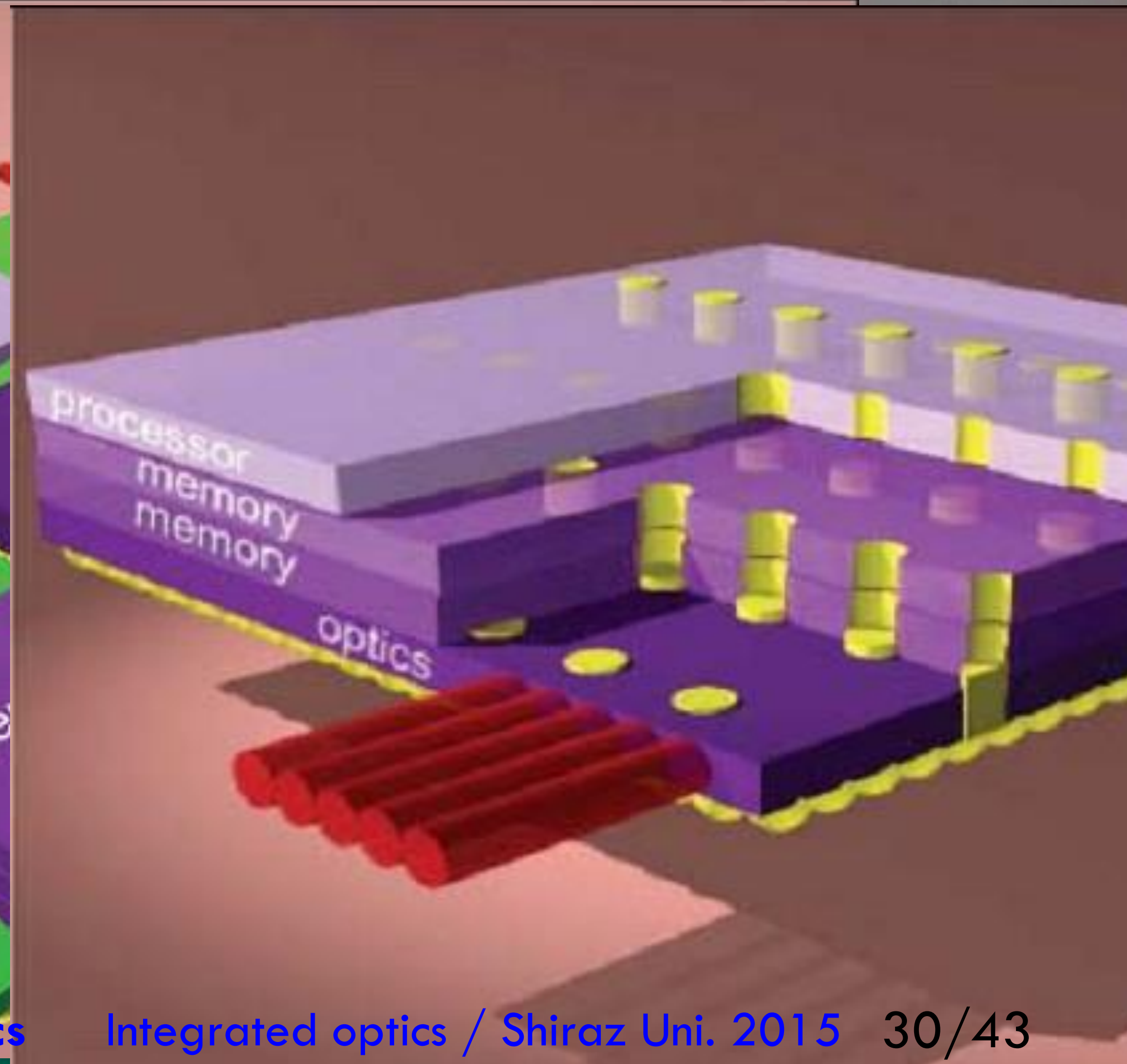
CURRENT TECHNOLOGY



INTEGRATED PHOTONIC ELECTRONIC CIRCUIT

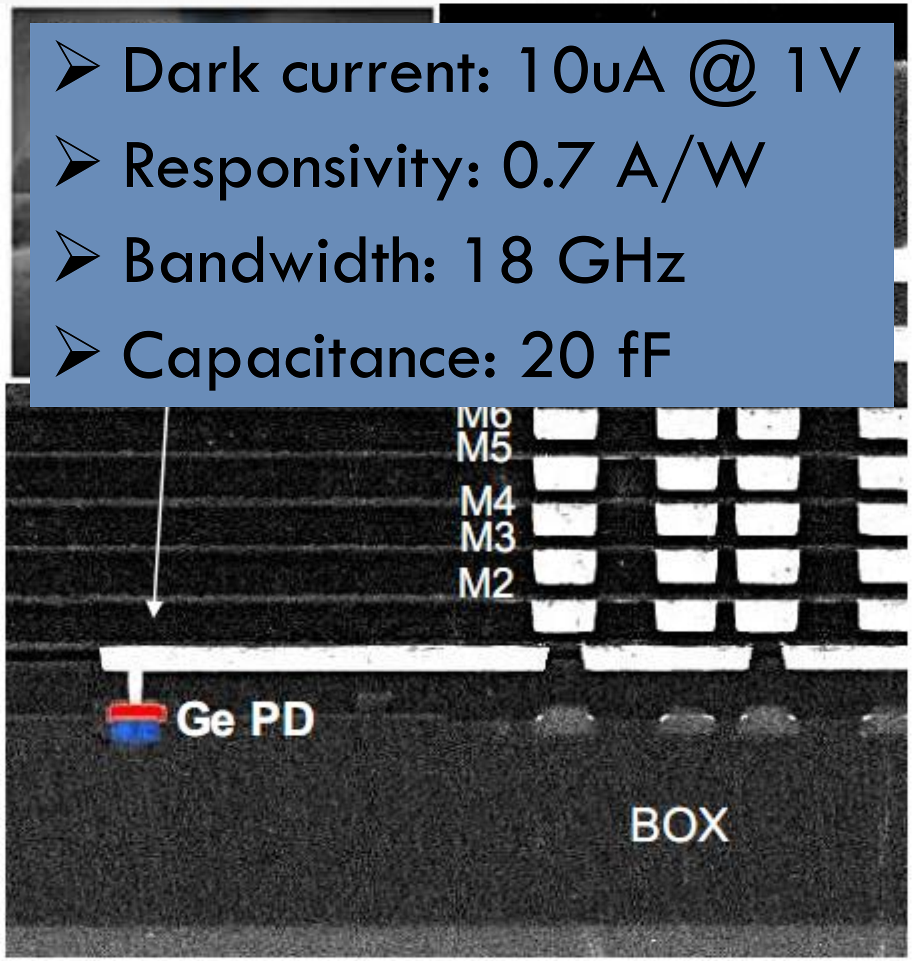
- **Future**

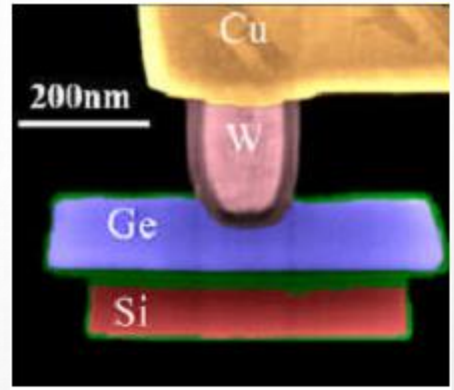


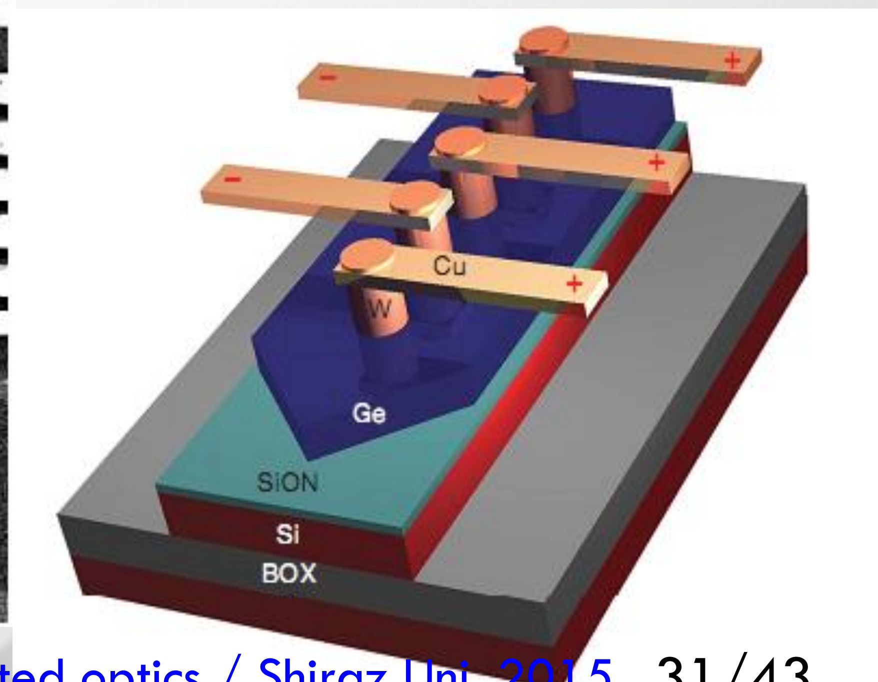


SILICON COMPATIBLE DETECTOR

- Dark current: 10uA @ 1V
- Responsivity: 0.7 A/W
- Bandwidth: 18 GHz
- Capacitance: 20 fF

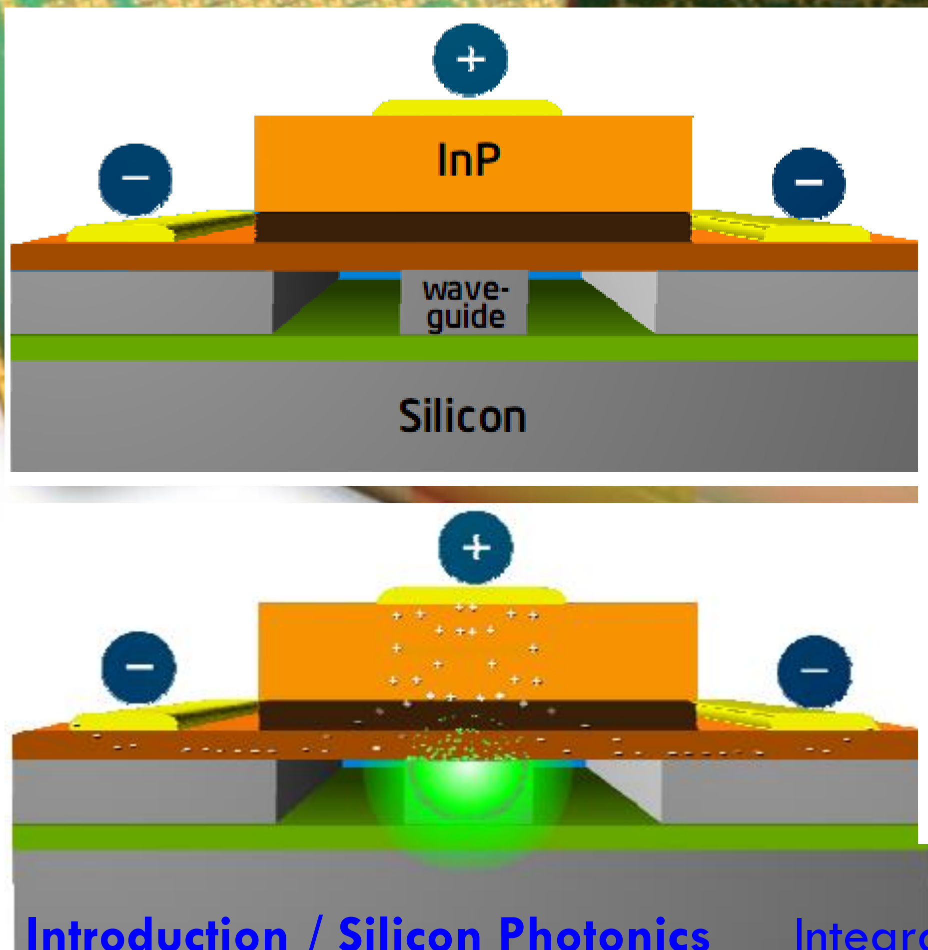


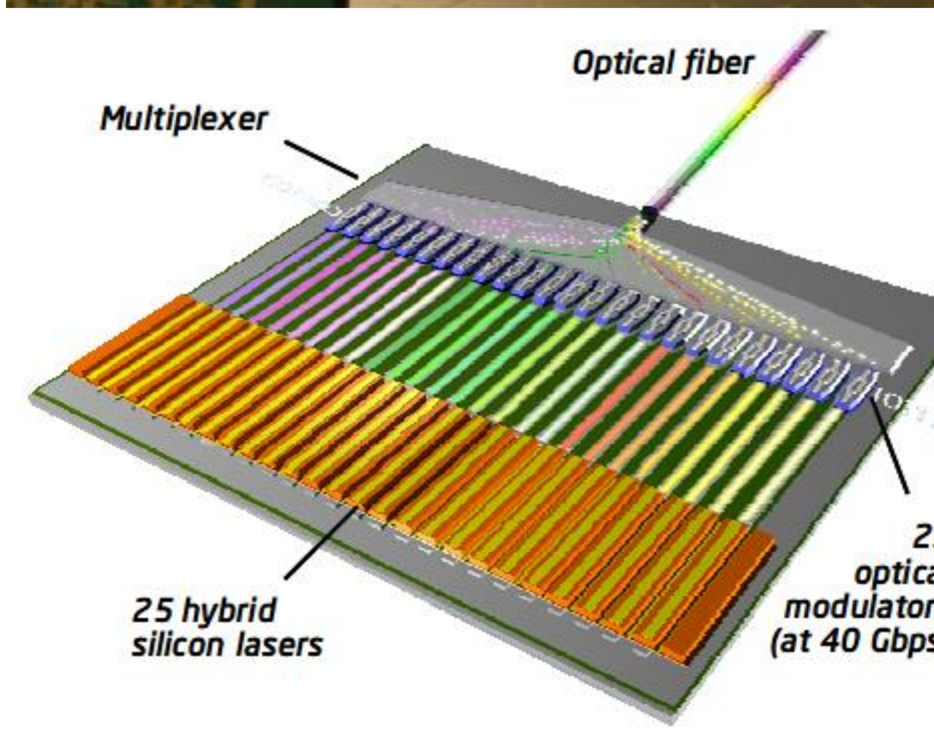




Hybrid Silicon Laser

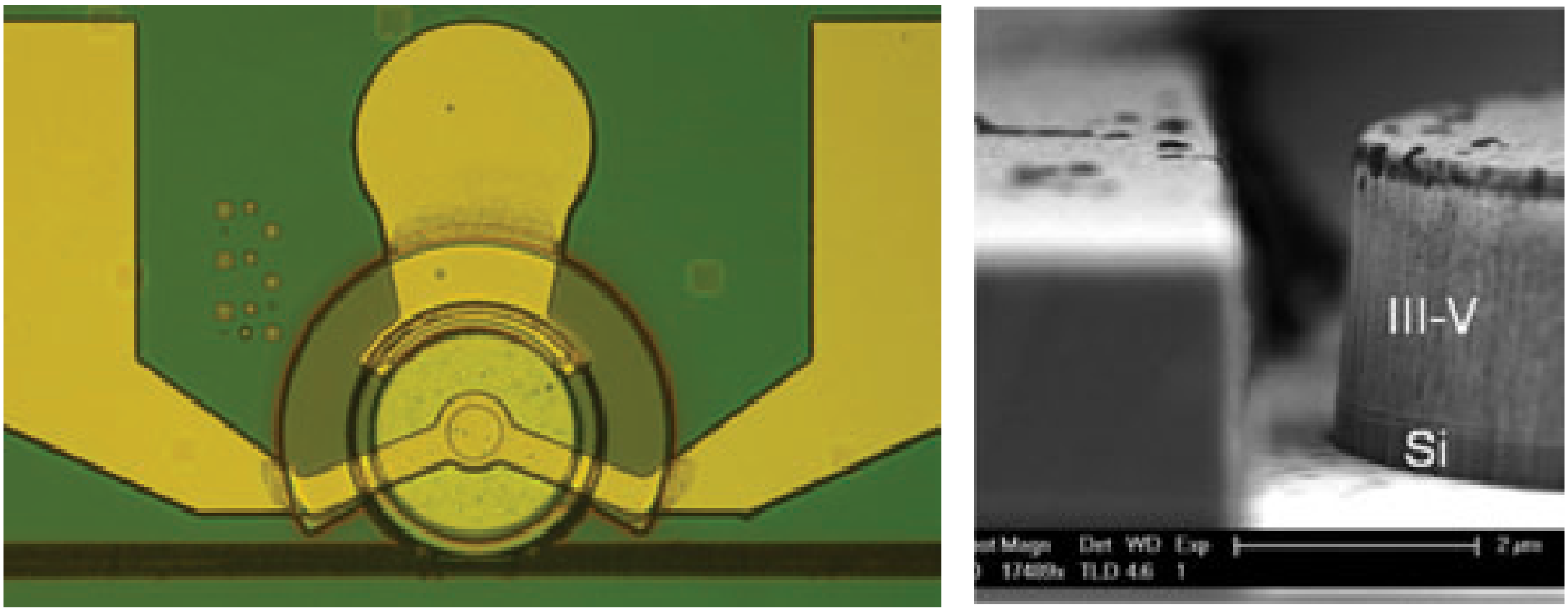
- Silicon / III-V bonded wafers





HYBRID SILICON LASERS

[Microring lasers]



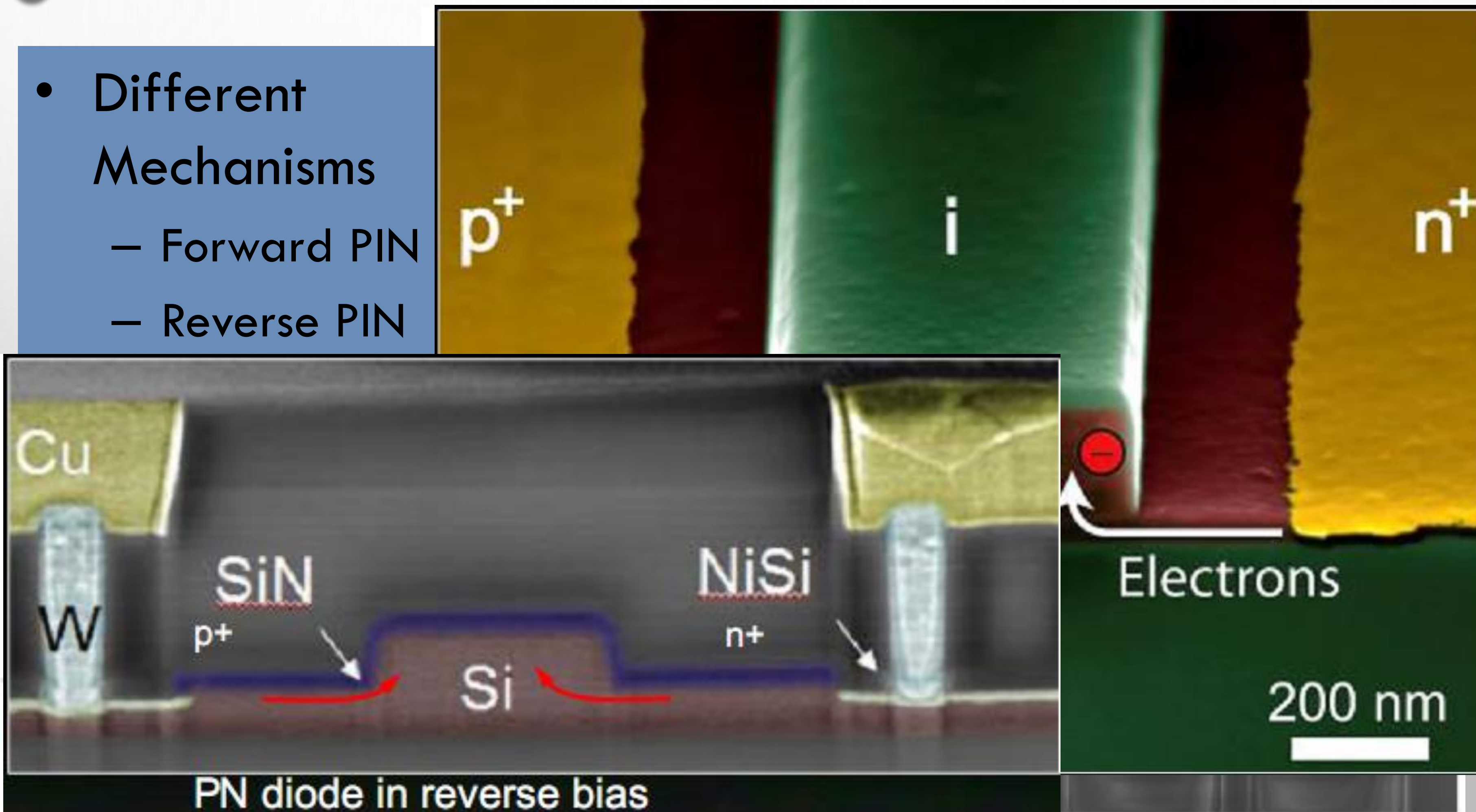
(Left) Photo of a hybrid silicon microring laser. (Right) SEM image of ring and output coupler.

SILICON PHOTONICS MODULATOR

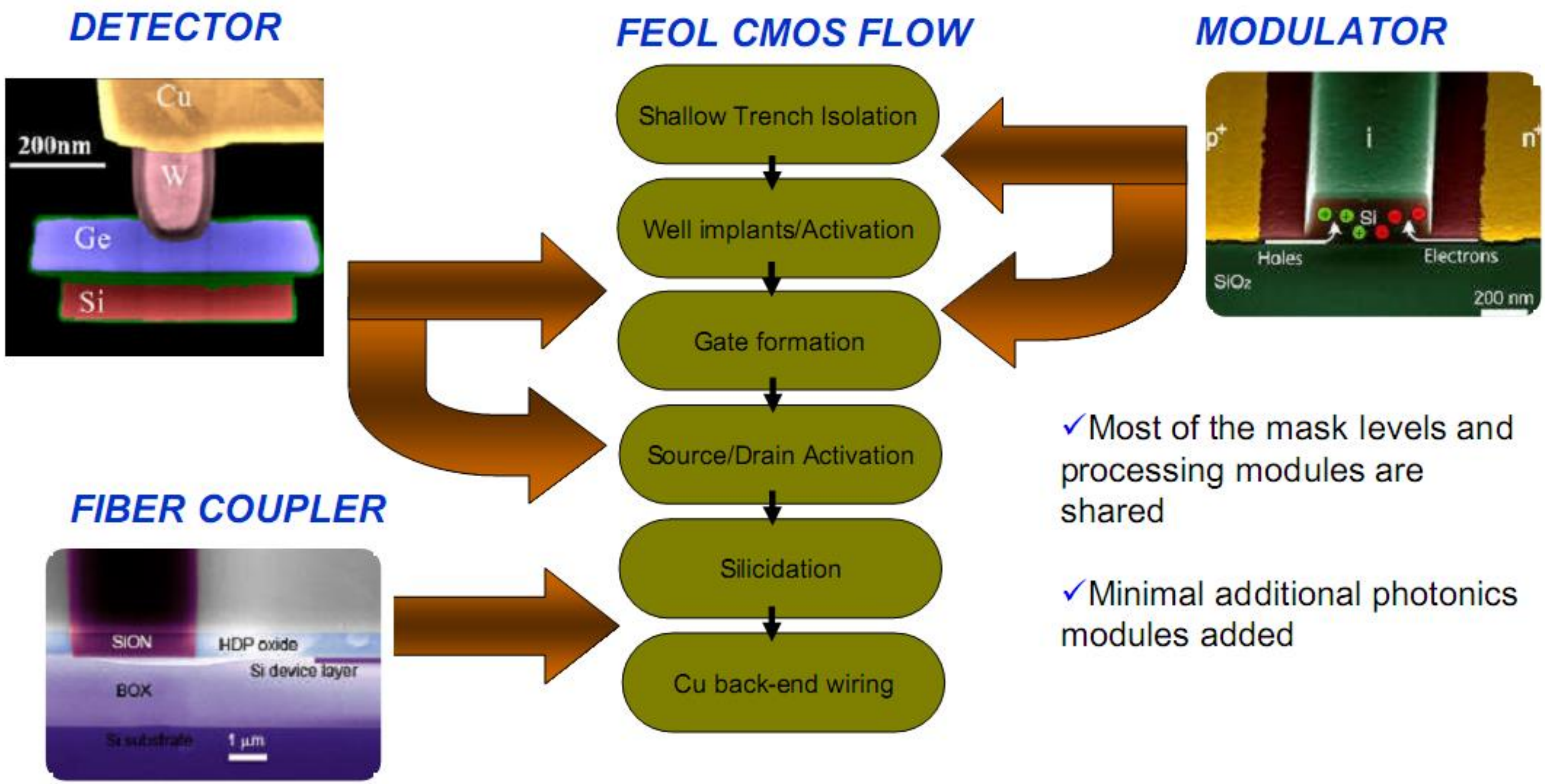
- MODULATION MECHANISMS
  - ELECTRO-OPTICAL REFRACTIVE INDEX CHANGE DUE TO:
    - FREE CARRIER INJECTION IS FORWARD BIASED SI PIN STRUCTURE
    - CARRIE ACCUMULATION IN REVERSED BIASED PIN STRUCTURE
    - CARRIER ACCUMULATION IN MOS CAPACITOR STRUCTURE
- MODULATOR STRUCTURES
  - MZI STRUCTURE
  - COUPLED WAVEGUIDE RING RESONATOR STRUCTURE

SILICON PHOTONICS MODULATORS

- Different Mechanisms
  - Forward PIN
  - Reverse PIN



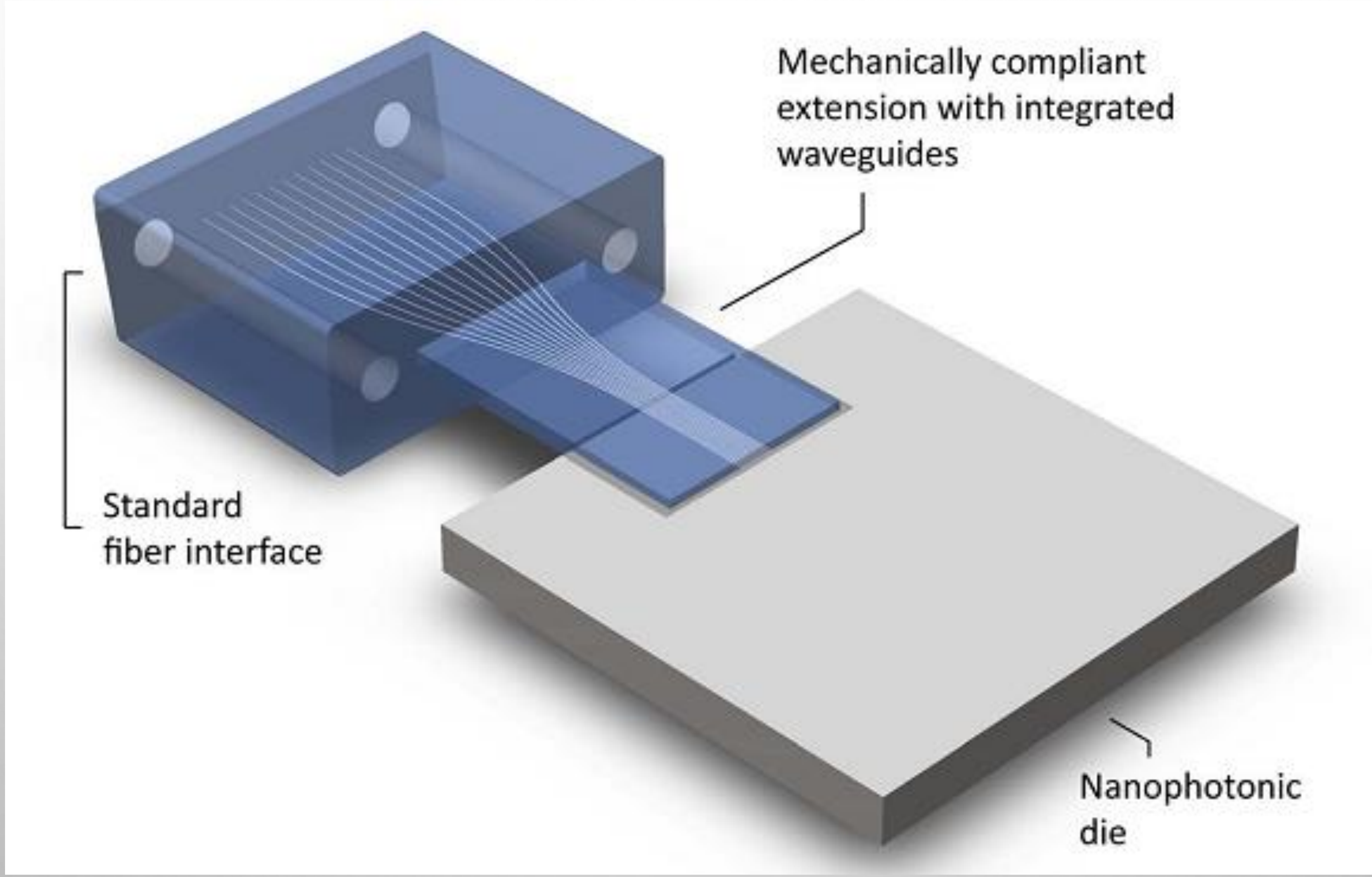
CMOS COMPATIBLE FABRICATION



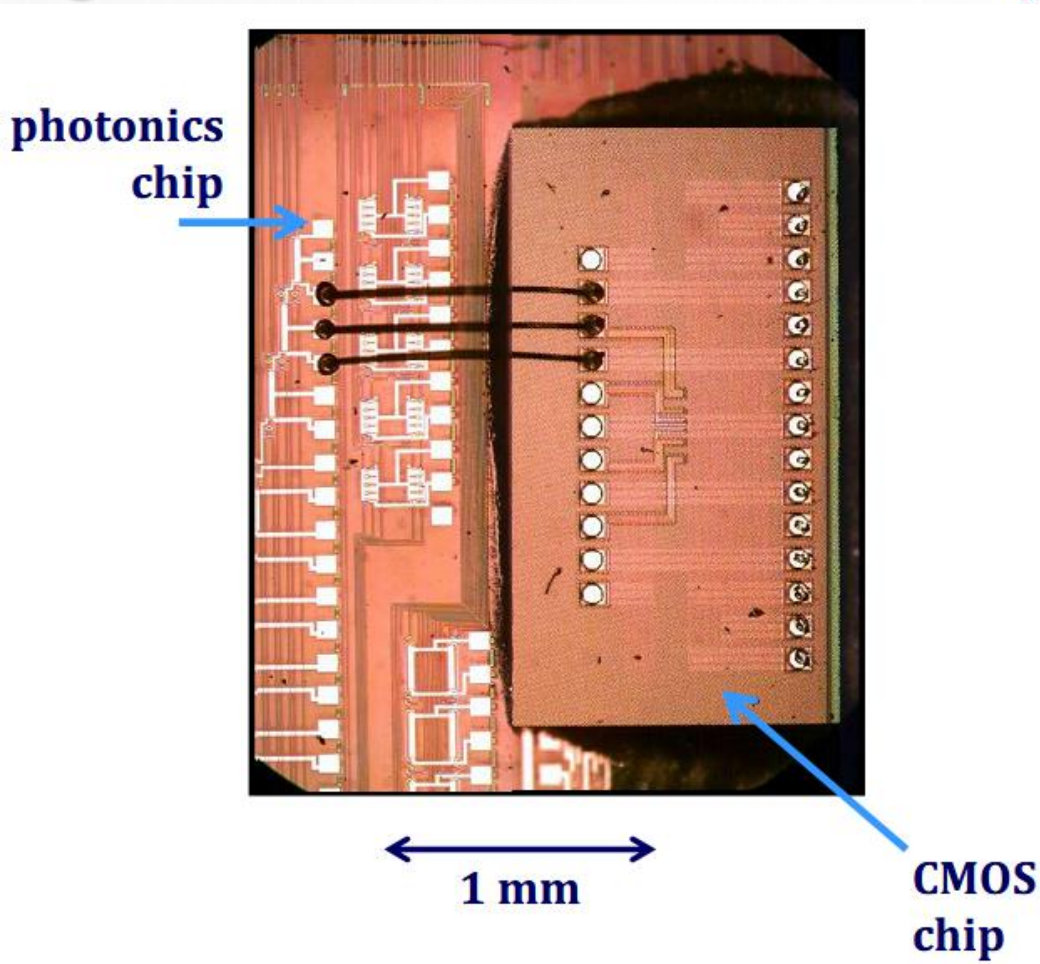
- ✓Most of the mask levels and processing modules are shared
- ✓Minimal additional photonics modules added

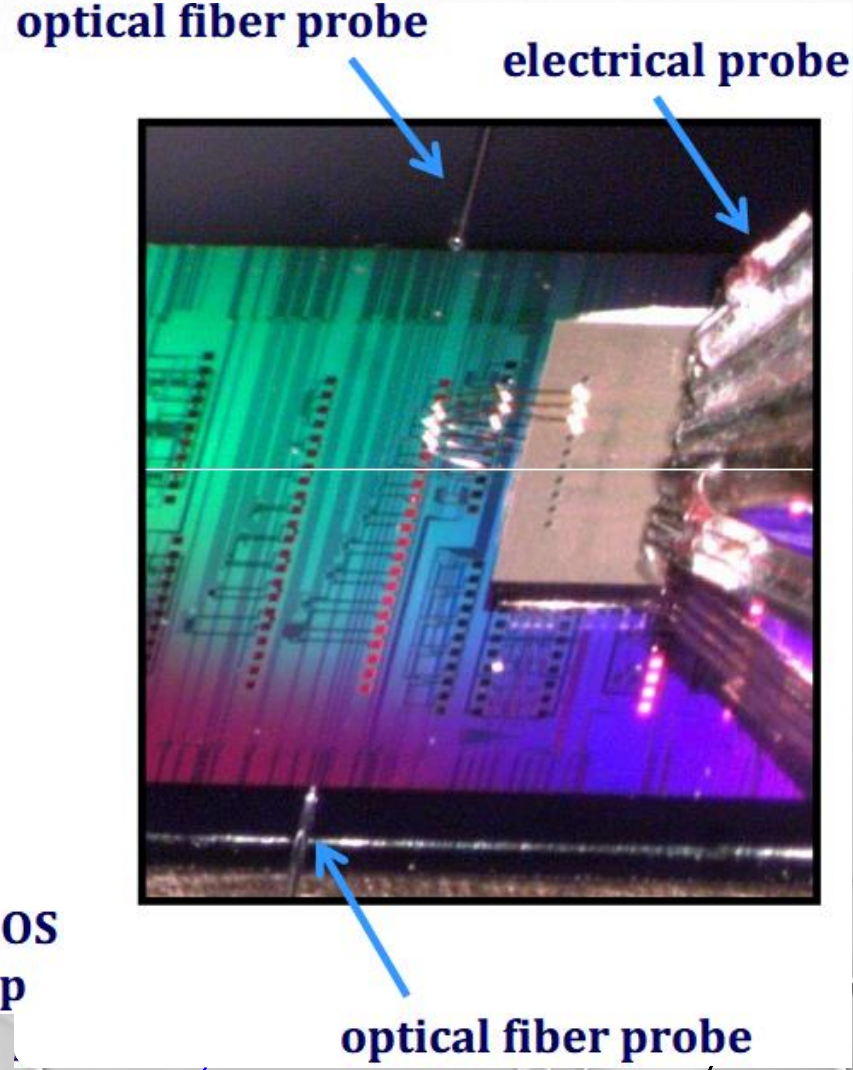
Photonics as a new feature in standard CMOS

FIBER TO WAVEGUIDE COUPLING (PACKAGING)



PACKAGING (PUTTING IT ALL TOGETHER)





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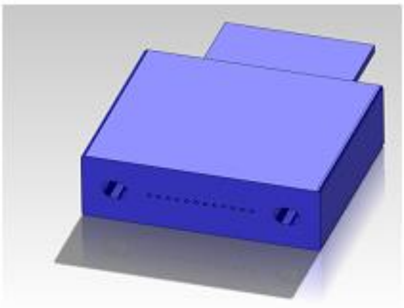
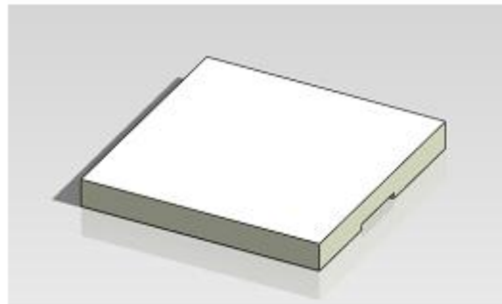
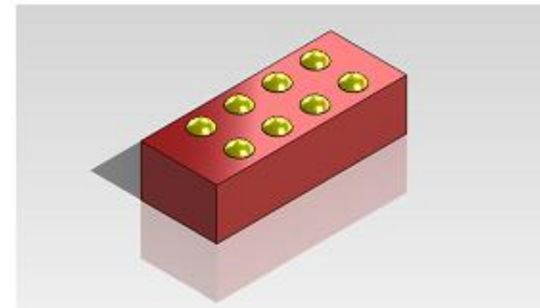


Fiber ferrule



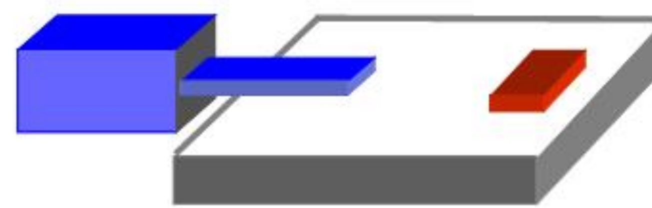
SiPh die



DFB laser array

2013

Pick & Place
Passive alignment of optical components



First level package

PACKAGING (PUTTING IT ALL TOGETHER)

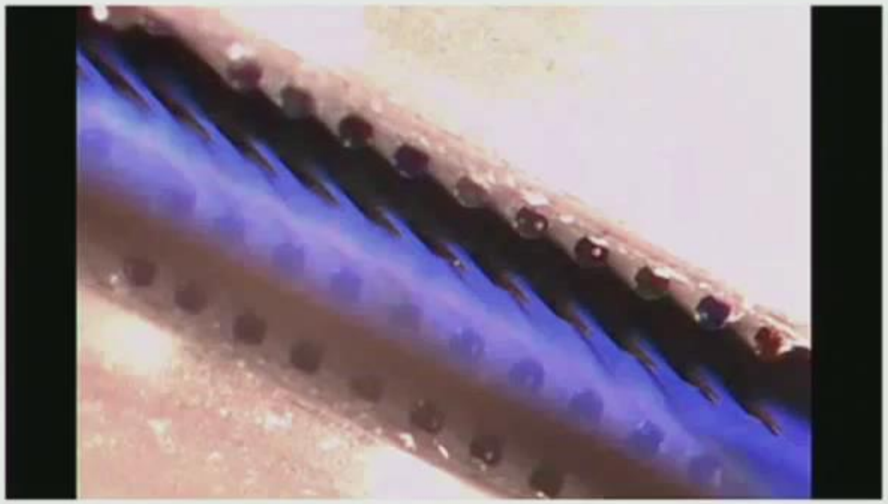
Automated assembly

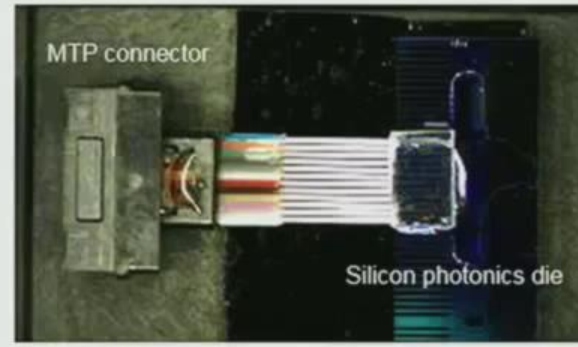
IBM Watson, NY USA
Interface design, Si fabrication
Tymon Barwicz and team

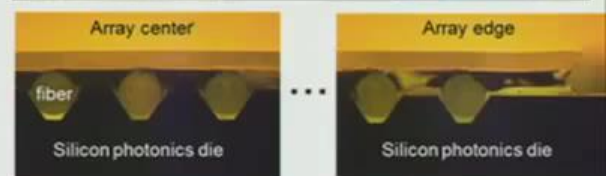
IBM Research - Tokyo
Ribbon to ferrule assembly
Yoichi Taira and team

IBM Bromont – C2MI
Ribbon to Si assembly
Paul Fortier and team

Partners: AFL — AFL Tele



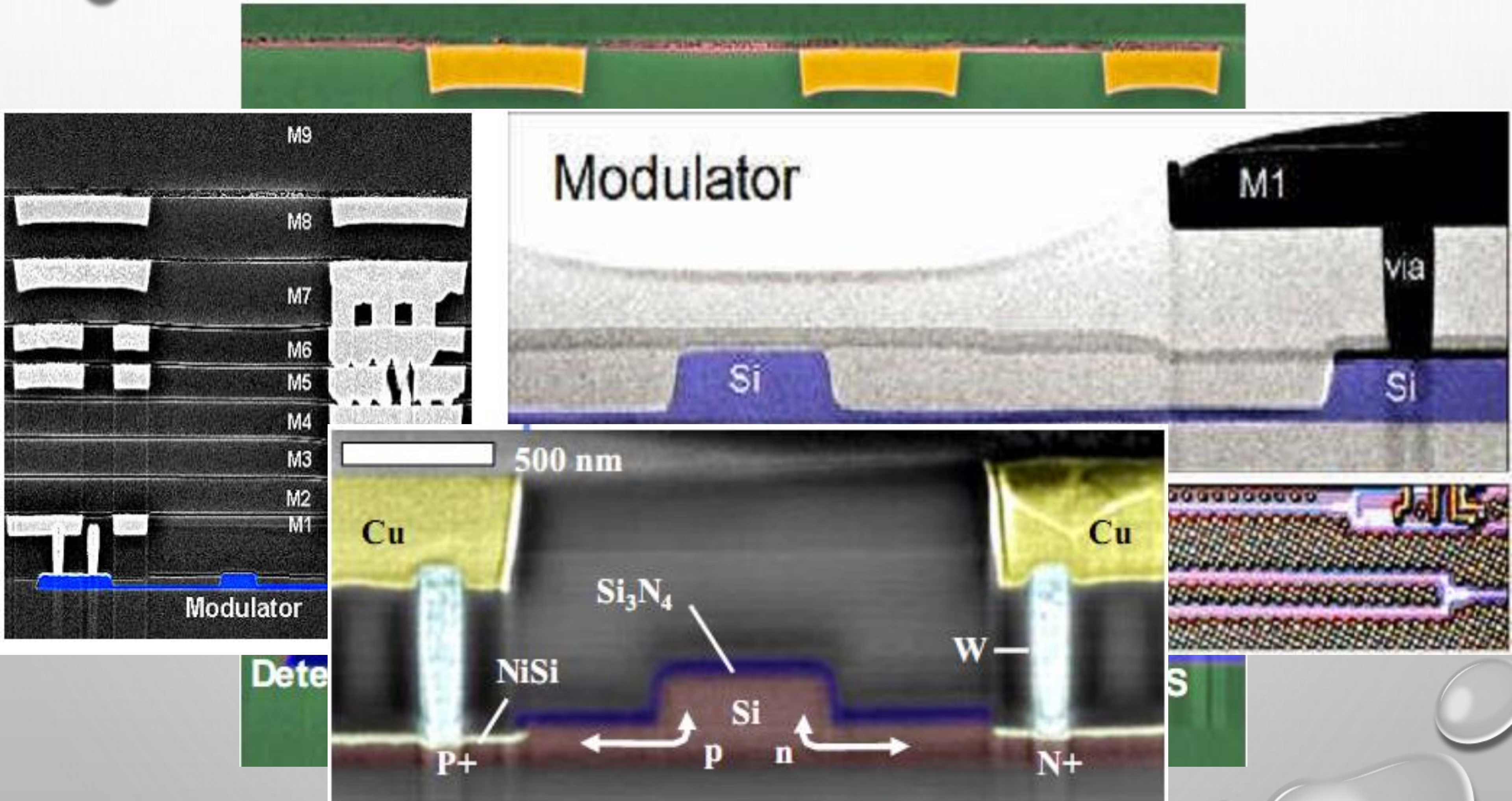




- ✓ Bandwidth 1260-1360nm
- ✓ Insertion loss -1.3dB
- ✓ Worst PDL 0.6dB
- ✓ Return loss -30dB

T. Barwicz et al., IEEE ECTC, 2015.
T. Barwicz, et al OFC 2015

OEIC SYSTEM EXAMPLES



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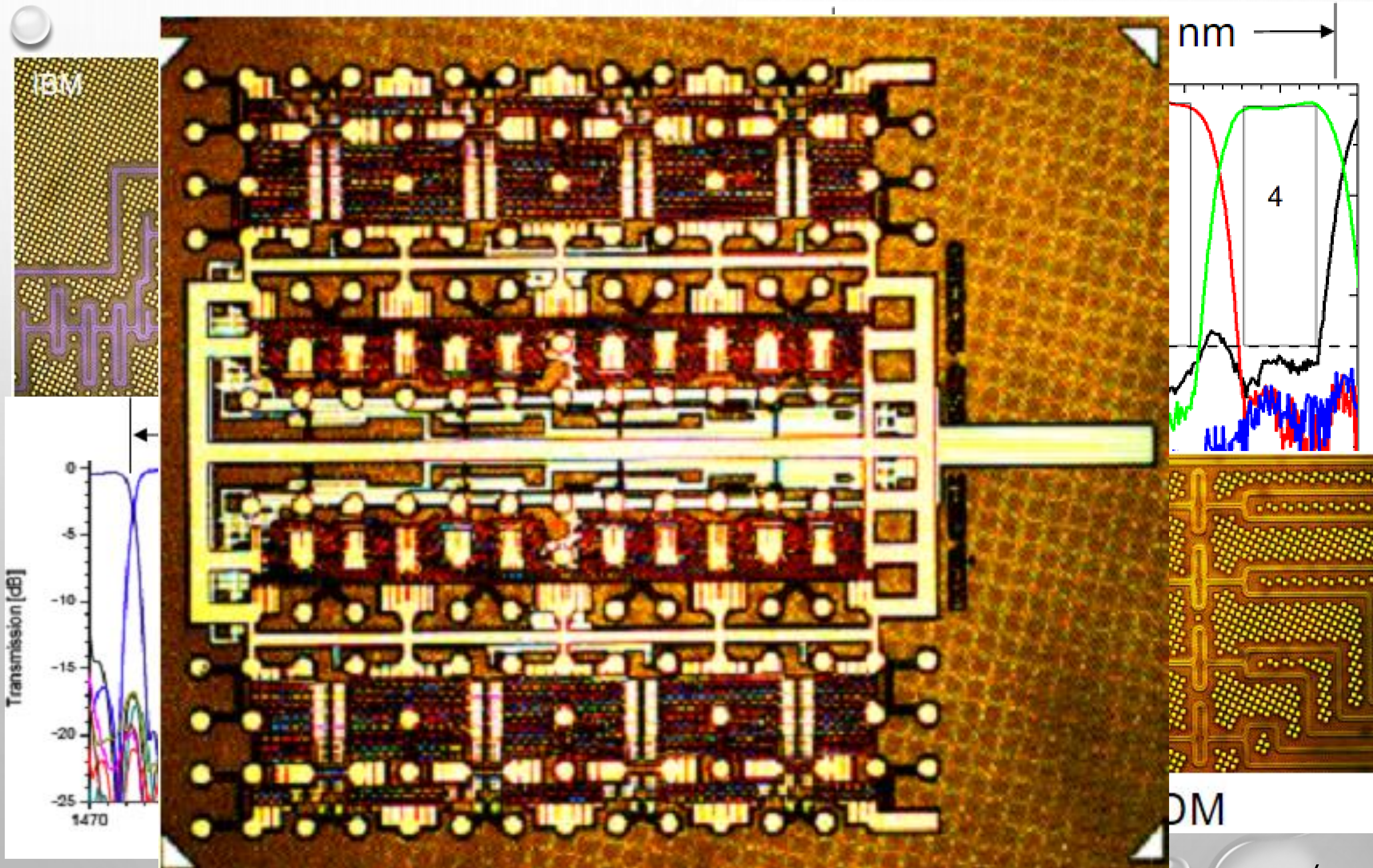
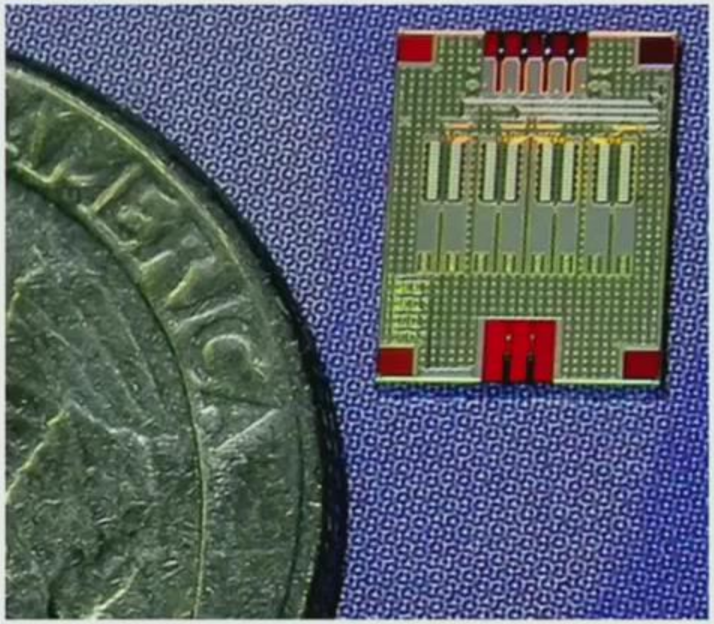


3x3mm 8-channel WDM TRX die

OEIC EXAMPLES

Reference Design: 4x25G CWDM Transceiver

- ✓ 4x25G Ge PD RX
- ✓ 4x25G TW MZITX
- ✓ CWDM 1310nm
- ✓ Polarization S&R
- ✓ DAC/ADC controllers
- ✓ SMF coupling
- ✓ Packaging structures



- ✓ Monolithic single-die 100Gbps silicon nanophotonics transceiver
- ✓ Fabrication tolerant and manufacturable