NSP
(v04.15.00)

Data Sheet

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1. Introduction

The Network Development Kit Support Package (NSP) contains the Ethernet driver implementation which plugs into the TI Network Development Kit (NDK). The NSP package in addition to supporting NIMU interface also supports TFDTP. TFDP driver is provided which bypasses NDK for optimized data path. This data sheet contains performance numbers for NSP on TDAxx family of devices.

The NSP for Vayu library supports the following

- **Ethernet GMACSW driver**
- **NDK Hardware HAL implementation (NIMU APIs)**
- **High performance APIs for raw data RX/TX (bypassing NDK stack)**
- **TI File Transfer Protocol (TFDTP) – TI custom protocol for high throughput Ethernet**

The benchmark numbers are collected using standalone NSP examples. The tests were initiated from a Linux host machine running the client tool. For detailed numbers, you can refer to 'reports' under NSP drv directory.

IMPORANT NOTE:

- This datasheet has performance and feature information about use-cases running on TDA2xx (EVM), TDA2Ex (EVM) and TDA3xx (EVM).
- The performance number mentioned in the document is based on the test configuration used.
- Tested with only release build profiles.

2. NSP_GMACSW Performance Summary

2.1 Target Platform Name: TDA2xx (Vayu)

2.1.1 *Test Setup*

- Cortex CPU(M4) Frequency : 212 MHz
- Cortex CPU(A15) Frequency : 1000 MHz
- DDR3 Clock : 532 MHz
- L3 Frequency : 266 MHz
- Packet size: 1500 Bytes.
- All performance data collected with **Null Stack use-case with Raw data API**
    - Detailed report @packages\ti\nsp\drv\reports\nsp_test_results_vayu_ipu1.txt and @packages\ti\nsp\drv\reports\nsp_test_results_vayu_mpu.txt

2.1.2 *Test Results*

Table 1. NSP Throughput with Cortex M4

Sr. No.	*Data Rate (Mbps)*	*PERFORMANCE STATISTICS (PERCENTAGE)*		
		HWI Load	Rx Packet Task Load	Overall CPU load
1	500	**4%**	**12.27%**	**18%**
2	900	**6%**	**22%**	**29.87%,**

Table 2. NSP Throughput with Cortex A15

Sr. No.	*Data Rate (Mbps)*	*PERFORMANCE STATISTICS (PERCENTAGE)*		
		HWI Load	Rx Packet Task Load	Overall CPU load
1	500	**2%**	**7%**	**11%**
2	900	**4%**	**13%**	**19%**

Table 3. HWI/SWI & Priorities

CONFIGURATION ID	HWI/SWI			
	HWI/SWI HANDLER	INTERRUPT VECTOR		XBAR SOURCE (IF ANY)
		CORTEX-M4	CORTEX-A15	
ALL	HwIntRx	58	58 + 32	NA
ALL	HwIntTx	59	59 + 32	NA
ALL	HwIntRxThresh	57	57 + 32	NA
ALL	HwIntMisc	60	60 + 32	NA

Table 4. Memory Statistics

CONFIGURATION ID	MEMORY STATISTICS [6]				
	PROGRAM MEMORY	DATA MEMORY			TOTAL
		INTERNAL	EXTERNAL	STACK	
ALL	20.2K	0	9.25	4	33.45

[6] All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes).

Table 5. Internal Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – INTERNAL [7]		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
ALL	0	0	0

[7] All memory requirements are expressed in kilobytes.

Table 6. External Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – EXTERNAL [8]		
	SHARED		INSTANCE
	CONSTANTS	DATA	
ALL	0	9.25	0

[9] All memory requirements are expressed in kilobytes.

2.2 Target Platform Name: TDA3xx

2.2.1 *Test Setup*

- Cortex CPU(M4) Frequency : 212 MHz
- DDR3 Clock : 532 MHz
- L3 Frequency : 266 MHz
- Packet size: 1500 Bytes.
- All performance data collected with **Null Stack use-case with Raw data API**
    - Detailed report @packages\ti\nsp\drv\reports\nsp_test_results_tda3xx_ipu.txt

2.2.2 *Test Results*

Table 7. NSP Throughput with Cortex M4

Sr. No.	*Data Rate (Mbps)*	*PERFORMANCE STATISTICS (PERCENTAGE)*		
		HWI Load	Rx Packet Task Load	Overall CPU load
1	500	4%	12.27%	18%
2	900	6%	22%	30%

3. TCP/IP Performance (with TI NDK)

3.1.1 *Test Setup*

- Cortex CPU(M4) Frequency : 212 MHz
- Cortex CPU(A15) Frequency : 1000 MHz
- DDR3 Clock : 532 MHz
- All performance data collected with NSP test server example and **performance numbers are only for receive**
    - Detailed report @packages\ti\nsp\drv\reports\nsp_test_results_vayu_ipu1.txt and @packages\ti\nsp\drv\reports\nsp_test_results_vayu_mpu.txt

3.1.2 *Test Results*

Sr. No.	***Core***	***PERFORMANCE STATISTICS (PERCENTAGE)***		
		Test set up	Throughput (Mbps)	CPU Load (%)
1	Cortex M4	*TCP*	10	**50.4%**
		UDP	60	**65%**
		RAW socket using NDK	100	**44.9%**
2	Cortex A15	*TCP*	10	**5%**
		UDP	60	**7%**
		RAW socket using NDK	100	**7%**

Table 1 NSP TCP/IP Throughput with NDK

4. TFDTP Performance

4.1.1 *Test Setup*

- Cortex CPU(M4) Frequency : 212 MHz
- Cortex CPU(A15) Frequency : 800 MHz
- DDR3 Clock : 532 MHz
- All performance data collected with TFDTP test server example
  - Number of Channels: 1
  - No. of TFDTP Packet buffers: 128
  - No. of TFDTP Application buffers: 3
  - TFDTP Frame size: 3MB
  - Detailed report @packages\ti\nsp\drv\reports\ tfdtp_tx_test_results_tda3xx_ipu.txt and X:\adas\ti_components\ethernet_nsp\packages\ti\nsp\drv\reports\tfdtp_tx_test_results_vayu_mpu.txt

4.1.2 *Test Results*

4.1.2.1 TFDTP RX

- **Network data rate for TFDTP Receive – 340Mbps**

Sr. No.	*Core*	*PERFORMANCE STATISTICS (PERCENTAGE)*		
		HWI Load	TFDTP Parser Task Load	Overall CPU load
1	Cortex M4	**3%**	**70%**	**75%**
2	Cortex A15	**1%**	**11%**	**15%,**

Table 2 TFDTP RX Throughput

4.1.2.1 TFDTP TX

- **Network data rate for TFDTP Transmit – 350Mbps**

Sr. No.	*Core*	*PERFORMANCE STATISTICS (PERCENTAGE)*		
		HWI Load	TFDTP Transmitter Task Load	Overall CPU load
1	Cortex M4	**3%**	**42%**	**47%**
2	Cortex A15	**2%**	**18%**	**21%,**

Table 3 TFDTP TX Throughput

5. Optimizations & Summary

This section covers GMAC HW benchmarking with different configuration options available with NSP like CPDMA descriptor location, interrupt pacing etc. This can be used by advanced users to further optimize networking use-case application with NSP.

5.1.1 *Test Setup*

- Cortex CPU(M4) Frequency : 212 MHz
- Cortex CPU(A15) Frequency : 800 MHz
- DDR3 Clock : 532 MHz
- All performance data collected with **Null Stack use-case with Raw data API**
    - **600Mbps Rx with ISR optimizations and packet reclaimed immediately (no packet processing).**
    - **Default intrrupt Pacing @500 ms**

5.1.2 Test Results

5.1.2.1 Optimization results for Cortex M4 & Cortex A15

Sr. No	*CPDMA Buffer Descriptors*	*PERFORMANCE STATISTICS (PERCENTAGE)*
		Overall CPU load
1.	CPSW	**35%**
2.	DDR	**35%**
3.	OCMC	**39%**
4.	IPU RAM	**33%**

Table 4 Optimization results for Cortex M4

Sr. No.	*Intrrupt Pacing*	*CPDMA Buffer Descriptors*	*PERFORMANCE STATISTICS (PERCENTAGE)*		
			HWI Load	NULL Rx Parser Task Load	Overall CPU load
1	**500 ms**	CPSW	**3%**	**9%**	**13%**
		DDR	**2%**	**6%**	**8%**
2	**1 Sec**	DDR	**2%**	**8%**	**10%**

Table 5 Optimization results for Cortex A15

5. Glossary & Acronyms

Glossary

Constants	Elements that go into .const memory section
Scratch Data	Memory space that can be reused across different instances of the algorithm Memory that go into .data and .bss sections
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

NSP	Network Support Package
NDK	Network Development Kit
TFDTP	TI File Transfer Data Protocol