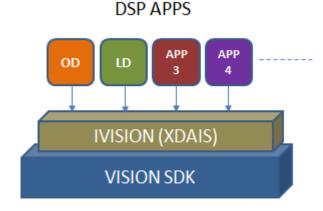
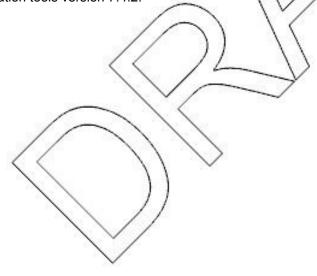


- IVISION (XDAIS) interface compliant
- Validated on TDA2x EVM
- Supports lane detection and lane departure warning
- Supports Canny edge detection, detecting upto 10000 edges in the ROI
- Supports Hough transform for lines between two different theta ranges for the right and left lanes respectively
- Kalman filter based tracking supported
- Supports user controlled thresholds to control the accuracy (False positive vs True Negative)



# Description

Lane detection module is TI's proprietary Vision and Imaging algorithm implemented on TMS320C66x DSP. Lane detection module is validated with Code Composer Studio version 5.1.0.09000 and code generation tools version 7.4.2.









### **Performance and Memory Summery**

**Table 1: Configuration Table** 

CONFIGURATION	ID
Lane Detection	LANDET_001

**Table 2: Performance Statistics** 

CONFIGURATION ID	TEST DESCRIPTION	TI C66X DSP PERFORMANCE STATISTICS		
CONFIGURATION ID		MIN (MEGA CYCLES)	MAX(MEGA CYCLES)	
LANDET_001	img0.y, img1.y,img9.y  ROI (576x240), maxRho – 624, Canny edge Th (20,30), Theta range(left –150, right– 150), theta Step Size – 1, tracking method – Kalman, Hough Maximas (detected – 6, tracked – 3)	2	2.6	

Performance is validated by running on TDA2x platform. DDR-532Mhz, DSP-600Mhz

**Table 3: Memory Statistics** 

				1 1	_	1 1			
CONFIGURATION			MEMORY STATISTICS <sup>1</sup>						
			DATA MEMORY						
ı	CONFIGURATION	RESOLUTION	PROGRAM MEMORY	INTERN AL	EXTERNAL			TOTAL	
					PERSISTE NT	SCRATC H	CON ST	STACK	
	LANDET_001	640x360	14.4	_23 \	3	1046	0.72	9	1096.1

All memory requirements are expressed in kilobytes (1 K-byte = 1024 bytes) and there could be a variation of around 1-2% in the numbers.

## Table 4: Internal Data Memory Split-up

	DATA MEMORY – INTERNAL <sup>2</sup>			
CONFIGURATION ID	SHARED		INSTANCE <sup>3</sup>	
	CONSTANTS	SCRATCH	INSTANCE	
LANDET_001	// 0	23	-	

<sup>2</sup> Internal memory refers to on chip memory. All memory requirements are expressed in kilobytes and there could be a variation of around 1-2% in numbers. LD requires 23kb of L1D-SRAM memory. This puts L1D cache to 8kb. Executing lane detection module along with other DSP algorithm which requires different L1D configuration could hinder performance.

3 I/O buffers are not included. Some of the instance memory buffers could be scratch.





### notes

- I/O buffers:
- Input buffer size = 225 K-bytes (For 640x360 resolution)
- Output buffer size = 39.1 K-bytes (For a maximum of 10000 points on lane per frame)
- Total data memory for N non pre-emptive instances = Constants + Runtime Tables + Scratch + N \* (Instance + I/O buffers + Stack)
- Total data memory for N pre-emptive instances = Constants + Runtime Tables + N \* (Instance + I/O buffers + Stack + Scratch)

#### references

LaneDetection\_DSP\_UserGuide.pdf

## glossary

Constants Elements that go into .const memory section

Scratch Memory space that can be reused across different instances of the algorithm

Shared Sum of Constants and Scratch

Instance Persistent-memory that contains persistent information - allocated for each instance of

the algorithm





# acronyms

CIF Common Intermediate Format

DMA **Direct Memory Access** 

DMAN3 **DMA Manager EVM Evaluation Module**  $\mathsf{MV}$ Motion Vector

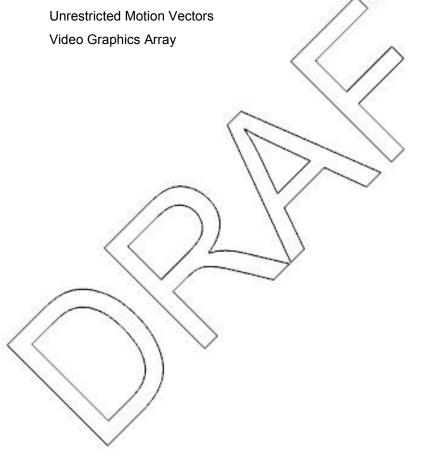
QCIF Quarter Common Intermediate Format

**QVGA** Quarter Video Graphics Array

Sub Quarter Common Intermediate Format **SQCIF** 

UMV

**VGA** 







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