EVE Subsystem Starterware User's Guide

Read This First

About This Manual

This document describes how to install and work with Texas Instruments' (TI) starter ware implementation on the EVE Subsystem. It also provides a detailed Application Programming Interface (API) reference and information on the sample application(s) that accompanies this component.

Intended Audience

This document is intended for system engineers who want to develop vision and imaging applications using EVE subsystem.

This document assumes that you are fluent in the C language, have a good working knowledge of embedded system and basic computer architecture concepts like DMA, Cache, interrupts etc.

How to Use This Manual

This document includes the following chapters:

- **Chapter 1 - Introduction** introduces the EVE subsystem and starterware components. It also provides an overview of supported features.

- **Chapter 2 - Installation Overview**, describes how to install, build, and run the starter ware.
- **Chapter 3 - API Reference** describes the data structures and interface functions used in the starter ware.
- **Chapter 4 - Sample Usage**, describes the sample usage of the starter ware and explains the different examples provided as part of starter ware component.
- **Chapter 5 - Frequently Asked Questions,** provides answers to few frequently asked questions related to using the starter ware.

Related Documentation From Texas Instruments

The following documents describe EVE subsystem details. To obtain a copy of any of these TI documents, visit the Texas Instruments website at www.ti.com.

- *Embedded Vector Engine (EVE) Programmer's Guide* (literature number SPRUHC1B) describes EVE architecture and all modules of EVE subsystem from programmer's view
- *EVE Subsystem Reference Guide* (literature number SPRUHF5A) describes the function description of EVE subsystem and its Register set
- *ARP32 CPU and Instruction Set* (literature number SPRUHC9) describes ARP32 architecture, Instruction Set and programming model
- Enhanced Direct Memory Access (EDMA3) Controller User's Guide (literature number SPRUEQ5) for complete details on the EDMA3
- VisionSurround28 Super/High/Mid Vision28 Super/High/Mid ADAS Applications Processor (SPRS884D)

The following abbreviations are used in this document.

Table 1-1. List of Abbreviations

Abbreviation	Description
ARP32	32-bit Advanced RISC Processor
DMEM	Data Memory in EVE Sub System
EVE	Embedded Vision Engine
EDMA	Enhanced Direct Memory Access
IBUF	Image Buffer in EVE Sub System
IPC	Inter-Processor Communication
MMU	Memory Management Unit
RAM	Random Access Memory

Abbreviation	Description
SCTM	Sub System Counter and Timer Module
SMSET	Software Message and System Event Trace
VCOP	Vision Co-Processor
WBUF	Work Buffer in EVE Sub System

Text Conventions

The following conventions are used in this document:

- Text inside back-quotes (‘‘) represents pseudo-code.
- Program source code, function and macro names, parameters, and command line commands are shown in a `mono-spaced` font.

Product Support

1.1 When contacting TI for support on this eve starterware software component, quote the product name *EVE Subsystem Starter ware* and version number. The version number of the product is included in the Release Notes that accompanies this product.

Trademarks

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Chapter 1

Introduction

The EVE subsystem consists of a vision co-processor (VCOP), several system modules including a mailbox, a cache controller, Memory Management Unit (MMU), an EDMA controller, and an interrupt controller, plus an ARP32 scalar processor that controls all of these modules. The EVE starterware package is an OS agnostic register level API that runs primarily on the ARP32 to configure and use the features of the various EVE modules. An additional small set of APIs run on a host (DSP or ARM) for communication with the ARP32.

This chapter provides brief overview of the hardware blocks in the EVE subsystem and what the starterware offers for each block. For detailed description, please refer to EVE Programmers Guide and EVE Subsystem Reference Guide. The purpose of this User's Guide is to provide detailed information regarding the software elements and test examples provided with EVE Starterware package.

1.1. Overview of EVE Subsystem

The Embedded Vision Engine (EVE) module is a programmable imaging and vision-processing engine, intended to be used in devices that serves consumer electronics imaging and vision applications. Its programmability allows late-in-development or post-silicon processing requirements to be met, and allows third party or customers to add differentiating features in imaging and vision products. The EVE module is instantiated in Vision super/High/Mid ADAS Application Processors

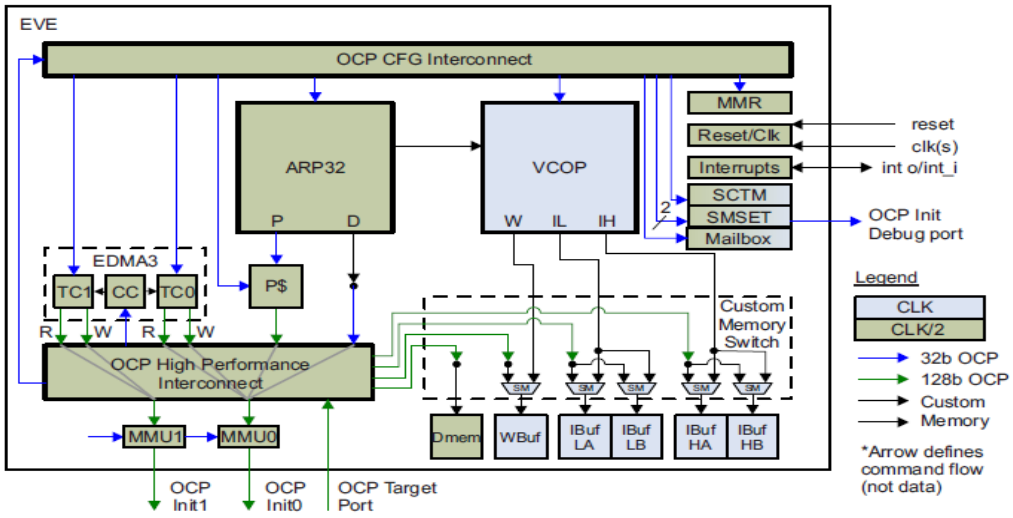

Figure 1-1. Block diagram of EVE Subsystem

As shown in Figure 1-1 there are different programmable module in EVE subsystem like EDMA, Mailbox, SCTM, MMU, Program Cache, Interrupts, ARP32 and VCOP. VCOP is main compute engine for vector processing and ARP32 is the scalar processor. Other blocks are control and data transfer modules.

1.2. Overview of EVE starterware

The EVE starterware package is an OS agnostic register level API that runs primarily on the ARP32 to configure and use the features of the various EVE control and data transfer modules. An additional small set of APIs run on a host (DSP or ARM) to configure the EVE subsystem modules. Host APIs are direct configuration of EVE subsystem modules from external processor other than the ARP32 of EVE subsystem, these are not Inter processor communication to ARP32 to configure these modules. Primary purpose of this package is to abstract low level details of EVE subsystem and share a rich example code to show case the usage of these APIs for different purpose. The starterware along with low level DMA functions, also provides high level DMA utilities to abstract most commonly required data transfer pattern in vision and imaging applications

1.3. Supported Services and Features

This user guide accompanies EVE starterware library and example source code. This version of the library has the following supported features.

- APIs to configure below modules on ARP32
  - Mailbox
  - Interrupt controller
  - MMU
  - Program Cache
  - SCTM
- APIs to configure below modules on DSP (C66x)
  - Mailbox
  - MMU
  - Program Cache
- Examples for below use cases
  - eve_bfswtch_arp32_error_intr
  - eve_bfswtch_vcop_error_intr
  - mailbox_dsp1_all_eves(vayu only)
  - mailbox_eve1_to_dsp1
  - mailbox_eve1_to_dsp1_inorder_ack
  - program_cache_block_inv
  - program_cache_global_inv
  - program_cache_software_prefetch
  - ref_mmu_tlb
  - ref_mmu_tlb_miss_tlw_dis
  - sctm_counters_observing_8_events

- sctm_vcop_busy_time
- vcop_done_intr
- vcop_error_intr
- vcop_max_iters_intr

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Chapter 2

Installation Overview

This chapter provides a brief description on the system requirements and instructions for installing the starterware component. It also provides information on building and running the example application.

2.1. System Requirements

This section describes the hardware and software requirements for the normal functioning for this component.

2.1.1. Hardware

The starterware has been built and tested on the EVE subsystem based devices like TDA1MEV /Vision28 Super (Vayu). In this document vme implies TDA1MEV and Vayu implies Vision28 Super.

2.1.2. Software

Kindly refer to EVE SW getting started guide which is located at docs folder at EVE SW root directory.

2.2. Installing the Component

The starterware component is released as a windows/unix installer along with other software modules for EVE. Figure 2-1 shows the sub-directories created after installation.

> Note:
>
> The source folders under drivers are not present in case of a library based (object code) release. In this document vme implies TDA1MEV and Vayu implies Vision28 Super.

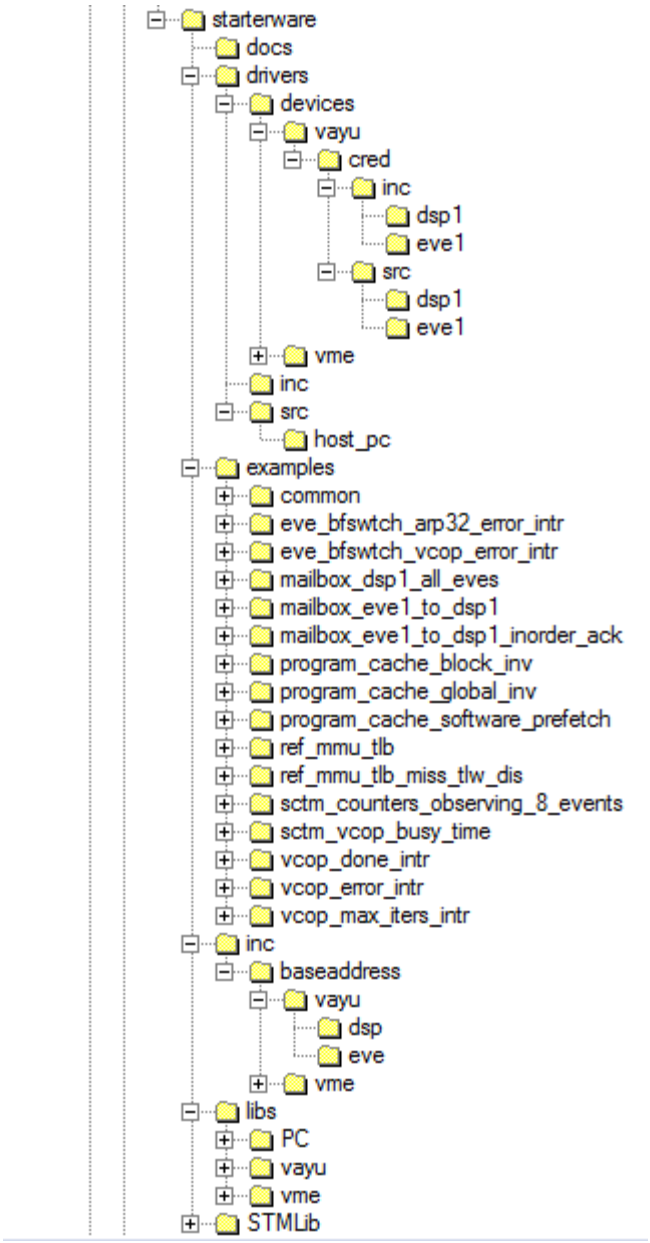

Figure 2-1. Component Directory Structure

Table 2-1 provides a description of the sub-directories created in the starterware directory.

Table 2-1. Component Directories

Sub-Directory	Description
/docs	Contains Documents related to Starterware

Sub-Directory	Description
/drivers/devices/vayu/cred/inc	Contains CRED header files for vayu platform
/drivers/devices/vayu/cred/src	Contains CRED src files for vayu platform
/drivers/devices/vme/cred/inc	Contains CRED header files for vme platform
/drivers/devices/vme/cred/src	Contains CRED src files for vme platform
/drivers/inc	Contains internal header files needed for starterware. This folder will not be present for library based release
/drivers/src	Contains src files needed for starterware. This folder will not be present for library based release
/drivers/src/host_pc	Contains src for host/PC emulation for Starterware
/examples/common	Contains common src and headers needed by example code
/examples/common/dsp/inc	Contains API's to configure DSP interrupts
/examples/common/dsp/src	Contains source code for DSP interrupt setupt
/examples/common/vayu	Contains boot_arp32.asm file for vayu. This is needed by all examples and contains interrupt vector mapping for ARP32
/examples/common/vme	Contains boot_arp32.asm file for vme. This is needed by all examples and contains interrupt vector mapping for ARP32
/examples	Contains examples illustrating various usage of starterware API's. More details on examples is provided in 0.
/inc/baseaddresses/vayu/eve	Contains header files which contains base addresses for eve subsystem and is sub modules for vayu platform for eve core
/inc/baseaddresses/vayu/dsp	Contains header files which contains base addresses for eve subsystem and is sub modules for vayu platform for dsp core
/inc/baseaddresses/vme/eve	Contains header files which contains base addresses for eve subsystem and is sub modules for vme platform for eve core
/inc/baseaddresses/vme/dsp	Contains header files which contains base addresses for eve subsystem and is sub modules for vme platform for dsp core
/inc	Contains API's of starterware
/libs/vayu/eve	This folder will be created once you build starterware library and contains library for eve starterware for vayu platform, which can be called from eve host.
/libs/vayu/dsp	This folder will be created once you build starterware library and contains library for eve starterware for vayu platform, which can be called from dsp host.

Sub-Directory	Description
/libs/vme/eve	This folder will be created once you build starterware library and contains library for eve starterware for vme platform, which can be called from eve host.
/libs/vme/dsp	This folder will be created once you build starterware library and contains library for eve starterware for vme platform, which can be called from dsp host.
/STMlib	This folder contains source and API's which can be used by for using SMSET functionality. Currently this is not supported by Code Composer Studio on vayu platform. For details on its usage please refer SMSET chapter of EVE's Programmer guide .

2.3. Building Starterware Libraries

Starterware Libraries can be found at libs folder present in top most folder in starterware directory. This libs folder contains four libraries of starterware depending on platform and host.

Platform : vayu Host: eve

Platform : vayu Host: dsp

Platform : vme Host: eve

Platform : vme Host: dsp

Starterware build uses GNU make system for building. For Building Starterware first you will need to set following four environment variable in your system:

ARP32_TOOLS : Directory pointing to ARP32 compiler (can be found inside CCS installation at following location <CCS_INSTALLATION_DIR>/ccsv5/tools/compiler/)

DSP_TOOLS : Directory pointing to DSP compiler (can be found inside CCS installation at following location

<CCS_INSTALLATION_DIR >/ccsv5/tools/compiler/)

EVE_SW_ROOT : Directory Pointing to EVE softwares root directory

UTILS_PATH : Directory pointing to utils command like mkdir, rm (can be found inside CCS installation at following location on windows :

<CCS_INSTALLATION_DIR>/ccsv5/utils/cygwin

On linux this directory is same as /bin

Once you set the above-mentioned four variables, you are all set to build starterware libraries. For building we use gmake command provided by GNU make.

Gmake command can take three inputs for building different libraries for different core and different platform. Following are the three variables:

TARGET_SOC: this is to specify the platform for which library is required to be build. Currently it can take two values: vayu and vme, for building on vayu platform or on vme platform respectively.

CORE: this is to specify the host for which library is required to be build. Currently it can take two values: eve and dsp, for building for eve host or dsp host respectively.

TARGET_BUILD: this is to specify whether to build library in release mode or debug mode. It can take two values: release and debug.

Rules.make file will configure various variables needed for build based on these three inputs. If you do not give any inputs by default, these variables will take following values: TARGET_SOC = vayu, CORE=eve and TARGET_BUILD=release.

For building EVE starterware library for vayu platform and eve as host:

gmake TARGET _SOC=vayu CORE=eve

Alternatively, you can use just gmake for this particular case as this case uses default.

Library will be created and placed at:

<STARTERWARE_DIR>/libs/vayu/eve/libevestarterware_eve.lib

Building EVE starterware library for vayu platform and dsp as host :

gmake TARGET_SOC=vayu CORE=dsp

Alternatively, you can use just gmake CORE=dsp for this particular case as this case TARGET_SOC is same as default.

Library will be created and placed at:

<STARTERWARE_DIR>/libs/vayu/dsp/libevestarterware_dsp.lib

Similarly, you can build library for vme platform also, final libraries will be located at following places:

<STARTERWARE_DIR>/libs/vme/eve/libevestarterware_eve.lib

<STARTERWARE_DIR>/libs/vme/dsp/libevestarterware_dsp.lib

2.4. Building Starterware Examples

Starterware examples also use similar procedure as described above. Each example contains its own Makefile present in src folder of respective examples directory. Some examples needs hosts for configuration, those example contains folder for host (dsp) and eve. By default each example is built in debug mode only. If you want to build it in release mode change it in make file.

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Chapter 3

API Reference

This chapter provides a detailed description of various API provided for sub module like Cache, EDMA, mailbox, mmu, interrupts etc by eve starterware

3.1. Mailbox

EVE has an internal mailbox to support synchronization and message passing between ARP32 and system level hosts. The mailbox function supports 2-way communication between maximum 4 users. This function relies on internal sub-modules, each supporting 1-way communication between one user referred to as the sender, and another user referred to as the receiver. The allocation of the mailbox sub-module to the communication between two users is done by software. Whenever a message is written in the appropriate sub-module, the associated interrupt is sent to the appropriate receiver, provided the interrupt is enabled. Each interrupt has its own interrupt status register and interrupt enable register. The line interrupt signal indicates when one or more events are detected by the hardware, for the corresponding user. Each event is independently maskable. Since interrupt status register are independent from one user to another, the associated interrupt line behavior are independent from each other as far as user doesn't access not owned mailbox. Please refer to EVE programmer's guide for more details

API NAME	**Description**
EVE_MBOX_Read	Read a value from the specified mailbox
EVE_MBOX_Write	Write value to specified mailbox
EVE_MBOX_Reset	Soft reset of mailbox
EVE_MBOX_IsFull	Check if mailbox is full
EVE_MBOX_GetNumMsg	Get number of messages in mailbox
EVE_MBOX_IrqEnable	Enable interrupt for user/mailbox
EVE_MBOX_IrqDisable	Disable interrupt for user/mailbox
EVE_MBOX_IrqGetStatusAll	Get interrupt status for all users of a mailbox
EVE_MBOX_IrqGetStatus	Get interrupt status for a specific user
EVE_MBOX_IrqClearStatus	Clears interrupt status for user/mailbox

Paths:

Sources- starterware/drivers/src/mbox.c

Prototypes - starterware/inc/mbox.h

Library- starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_eve.lib

starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_dsp.lib

3.2. Interrupt Controller

The interrupt controller handles incoming interrupts, merging them with internal interrupt sources to drive ARP32's interrupt inputs. The interrupt controller also allows ARP32 to generate outgoing interrupts or events to synchronize with system ARM, DSP, and EDMA. It supports up to 32 active-high level interrupt inputs, and outputs 5 active high level interrupt outputs. Its architecture allows both hardware and software prioritization. Please refer to EVE programmer's guide for more details.

API NAME	**Description**
EVE_INTCTL_LevelInit	Configure the priority and interrupt kind
EVE_INTCTL_OneITEnable	Enable the specified interrupt
EVE_INTCTL_AllITEnable	Enable all the interrupts
EVE_INTCTL_Ack	Read the interrupt status register
EVE_INTH_InterruptEnable	Enable one interrupt
EVE_INTH_InterruptDisable	Disable one interrupt

Paths:

Sources – starterware/drivers/src/INTCTL.c

Starterware/drivers/src/INTH.c

Prototypes – starterware/inc/INTH.h

Library- starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_eve.lib

starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_dsp.lib

3.3. Cache Controller

The Program Cache in EVE is always enabled, and all ARP32 fetch accesses are cacheable. For cache hits, the interface between ARP32 and Program Cache handles back to back requests with 0 cycle latency in order to provide full throughput/program execution for the ARP32. For Cache Misses, the Program Cache controller will stall the ARP32 until the return of the cache line. The Program Cache also contains a software and performance transparent 256-b line buffer to minimize power consumption by minimizing accesses to the underlying Cache/SRAM in the case of back to back hits to the same line. Please refer to EVE programmer's guide for more details.

API NAME	**Description**
EVE_PROGCACHE_BlockInvalidate	Program cache block invalidate

EVE_PROGCACHE_GlobalInvalidate	Program cache global invalidate
EVE_PROGCACHE_Prefetch	Program cache pre-fetch

Paths:

Sources – starterware/drivers/src/pcache.c

Prototypes – starterware/inc/pcache.h

Library- starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_eve.lib

starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_dsp.lib

3.4. MMU

There are two MMUs that are accessible via the interconnect loopback path. Each of the two TCs is mapped to one of the two MMUs. One of the MMUs is also shared with ARP32 program and data accesses. The ARP32 Program Cache and Data accesses share an MMU in order to provide a convenient mechanism whereby ARP32 debug accesses have a single/consistent view of the system that is equivalent to ARP32 software's view. For the EDMA paths, the two MMUs are required to provide maximum concurrency for each TC and its respective accesses to system memory.

API NAME	**Description**
EVE_MMU_CurrentVictimSet	Set current victim
EVE_MMU_CurrentVictimGet	Get current victim
EVE_MMU_TlbLockSet	Set base lock value
EVE_MMU_TlbLockGet	Get base lock value
EVE_MMU_GlobalFlush	MMU global flush
EVE_MMU_TlbEntryFlush	MMU TLB entry flush
EVE_MMU_SoftReset	Reset MMU
EVE_MMU_IrqGetStatus	Get MMU interrupt status
EVE_MMU_IrqClearStatus	Clear MMU interrupt status
EVE_MMU_IrqEnable	Enable MMU interrupt
EVE_MMU_IrqDisable	Disable MMU interrupt
EVE_MMU_WtlEnable	Enable walking table logic
EVE_MMU_WtlDisable	Disable walking table logic
EVE_MMU_Enable	Enable MMU
EVE_MMU_Disable	Disable MMU
EVE_MMU_TlbEntrySet	Configure selected TLB entry

Paths:

Sources – starterware/drivers/src/mmu.c

Prototypes – starterware/inc/mmu.h

Library- starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_eve.lib

starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_dsp.lib

3.5. Memory Switch and Mapping

The custom memory switch provides a statically multiplexed low latency/high bandwidth switch between a master (VCOP/System/EDMA/ARP32) and internal EVE memories. Based on the value in the MMR register buffer ownership register programmed by the RISC core, either the VCOP or the System is designated as the master of the memory. The ARP32 read/write accesses and EDMA accesses are multiplexed and designated as the System master. Buffer switch MMRs are configured by ARP32 during run-time. Memory block structure is chosen in hardware to facilitate concurrent ping/pong DMA vs. processing, where the EDMA/ARP32 (System) may own one block of memory and VCOP may own another block of memory.

These are simple operations for which no APIs are provided. The applets 4.1.4 and 4.1.5 in 'examples' folder illustrates the use of buffer switching.

3.6. SCTM (Sub System Counter and Timer Module)

The SCTM module provides a specification for a generic counter timer module that can be instantiated within the processor subsystem and functions as a centralized profiling module for the entire subsystem. This module will map a large number of system /subsystem event signals to a smaller number of counter resources, controlled by user software. Some of the counter resources in the module can be configured for timer functionality where system and/or debug events can be generated when designated intervals are matched. It provides a unified programmers view of all profiling resources within the subsystem, which is accessible by either debug tools and/or the application. In addition to profiling functions, resources in this module address the need for application counter/timer functions such as OS timers to generate periodic interrupts or schedule periodic tasks.

API NAME	**Description**
EVE_SCTM_Enable	Enable SCTM hardware
EVE_SCTM_CounterReset	Reset SCTM counter
EVE_SCTM_ChainModeEnable	Enable 2 counters in chained 64-bit mode
EVE_SCTM_CounterTimerEnablev	Enable counter working as a timer
EVE_SCTM_CounterTimerDisable	Disable counter working as a timer
EVE_SCTM_MultipleCountersEnable	Enable multiple counters at once in sync
EVE_SCTM_MultipleCountersDisable	Disable multiple counters at once in sync
EVE_SCTM_TimerInterruptEnable	Enable timer to generate interrupt
EVE_SCTM_CounterRead	Read counter value
EVE_SCTM_OverflowCheck	Check for overflow in counter
EVE_SCTM_CounterConfig	Configure counter
EVE_SCTM_CounterChainModeConfig	Configure counter in chain mode

EVE_SCTM_TimerConfig	Configure timer

Paths:

Sources – starterware/drivers*/src/eve1/sctm.c*

Prototypes – starterware/inc /sctm.h

Library- starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_eve.lib

starterware/libs/$(PLATFORM)/$(CORE)/ libevestarterware_dsp.lib

3.7. SMSET (Software Message and System Event Trace)

The SMSET is a trace module used for monitoring key system events, and transferring software messages. SMSET can be used by programmers to understand the performance of EVE at a macro level. While SCTM is used to drill down on performance of specific loops, SMSET can be used to monitor performance of complete tasks, and perform in system monitoring, that can then be viewed as a performance log. Please refer to EVE programmer's guide for more details.

API NAME	**Description**
STMXport_open	Opens a physical STM channel
STMXport_printf	Prints a statically formatted string
STMXport_logMsg	Prints 32-bit integers, using a formatted string
STMXport_putWord	Transports a single 32-bit value
STMXport_putShort	Transports a single 16-bit value
STMXport_putByte	Transports a single 8-bit value
STMXport_getBufInfo	Check Buffer status for number of messages queued
STMXport_flush	Flush all buffered or pending data
STMXport_getVersion	Get revision number of library
STMXport_close	Closes the STM channel

Paths:

As STM HW block is present in several processors, it is maintained as a separate library.

Sources – starterware/drivers/src/StmLibrary.c

Prototypes – starterware/STMLib/include/StmLibrary.h

Library – starterware/STMLib/lib/stm_eve_elf.lib

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Chapter 4

Sample Usage

This chapter provides a detailed description of the sample test examples that accompanies this eve starterware component

4.1. Overview of the Example Application

The example applications are present in examples folder in starterware repository. This folder contains examples describing usage of various eve starterware sub modules like mailbox, interrupt controller, MMU, SCTM etc. Build procedure for building examples is same as the one described in section 2.4. Each example contains its own Makefile. These make file in turn are dependent on Rules.make present at the starterware directory inside EVE software component and common.mk (present in examples/common/common.mk). These make files populate variables needed to build example codes. Example code directory structure is as shown in the Figure 2-1.

Note: All mailbox examples expects that interrupts from EVE sub systems are connect to the DSP interrupts line. For vayu platform this can be done by configuring the crossbar properly. Cross bar can be configured in multiple ways. For these examples we are using gel files to configure crossbar. Gel files for configuring crossbars is located at modules/gels/<PLATFORM> folder. For TDA2x and TDA3x platform you should use xbar_config.gel to configure cross bar. This gel file should be run from A15 before connecting to EVE. Kindly refer to Starterware/examples/common/examples_platform.h file to see figure out the interrupt number used for mail boxes.

For VME there are two gel files located in modules/gels/vme. DM814x_EVM_PG2_1_HDMI.gel should be run from A8 and eden_arp32.gel should be run from ARP32.

4.1.1.Mailbox_eve1_to_dsp1

The mailbox hardware can be used to sustain unidirectional communication. In order to do this, we need to write code on both the DSP and the EVE. In this example, we model EVE as the sender of messages, and DSP as the receiver of the messages. Further, we want to model, asynchronous nature of messages, where the sender can send messages without the receiver, immediately reading those messages, as it may be busy with actual processing.

This example consists of two programs, one running on EVE and other running on DSP. In EVE side, we first configure EVE interrupt controller by attaching and interrupt handler to mailbox interrupt (MBOX_INTO). This will ensure that whenever an interrupt occurs in mailbox this interrupt handler gets invoked. Then we enable mail box interrupt in EVE's mailbox module which will raise this interrupt whenever a new message is received by mailbox.

Similarly on DSP side we first setup DSP interrupt controller and and then we enable mailbox interrupt for DSP which will raise an interrupt whenever a new message is received by DSP from EVE. There is a difference between mailbox user id for DSP in case of Vision28 Super and TDA1MEV platforms. In Vision28 Super mailbox user id for DSP is MBOX_USER_1 whereas in case of TDA1MEV it is MBOX_USER_2.

In this example, first EVE writes a message to its mailbox and once DSP receives this message it will acknowledge back to EVE buy writing in mailbox.

Note: While building mailbox example make sure you give proper PLATFORM name for Vision28 Super(vayu) and TDA1MEV (vme)

4.1.2.Mailbox_eve1_to_dsp1_inorder_ack

This example is very similar to the above example. Only difference is that this will continue for 100 iteration. Eve will first write a message mailbox for DSP and DSP will acknowledge back by writing a message to EVE's mailbox. This will continue for 100 iterations.

Note: While building mailbox example make sure you give proper PLATFORM name for Vision28 Super(vayu) and TDA1MEV (vme)

4.1.3.Mailbox_dsp1_all_eves

This example is specifically meant to be run only Vision28 Super (vayu) platform, the reason being this example requires multiple EVE's (in this case 4 EVE's). All the interrupt and mailbox configurations are similar to above examples. From EVE side, each EVE will write into mailbox for DSP. On DSP side, DSP will get interrupt from each EVE and will keep incrementing a count. DSP will wait till it gets interrupt from all the four EVE's. DSP will keep on acknowledging interrupts from EVE mailbox module by writing message back to mailbox. Once it receives interrupt from all the messages it will return PASS value.

Note: While building mailbox example make sure you give proper PLATFORM name for Vision28 Super(vayu)

4.1.4.Eve_bfswtch_arp32_error_intr

The buffer switch controls the ownership of the individual buffers, through the buffer view register and the buffer switch register. The "EVE_MSW_CTL" that controls ownership, and the memory view is implemented by "EVE_MEMMAP". These registers are explained in Section 10.3 of programmers guide. It was discussed that an error in programming the buffer switch, can be detected by use of the "EVE_MSW_ERR_INT".

In this example we enable the "EVE_MSW_ERR_INT" event, which corresponds to the buffer switch error interrupt. In this example, we purposefully set the buffer switch with the incorrect settings and perform an ARP32 data access to a buffer for which ARP32 is not the master. In this example the Bfswitch_error_Intr_Handler" handles the buffer switch error interrupt, In the interrupt service routine we read the registers "EVE_MSW_ERR" which tells us who generated the error, and the address from "EVE_MSW_ERR_ADDR" to which an access was made, when buffer switch setting was incorrect.

4.1.5.Eve_bfswtch_vcop_error_intr

This example is very similar to the above example. In this example again we make use of "EVE_MSW_ERR_INT" interrupt to detect error because of vcop buffer switch. Here we allocate data buffers in "WBUF", "IBUFLA" and "IBUFHA", but purposefully hand off "WBUF", "IBUFFLB" and "IBUFFHB" to VCOP, so that we can trigger a buffer switch error. In interrupt service routine after reading "EVE_MSW_ERR_IRQSTATUS", we write back to it, to clear the interrupt status, so that we can respond to future interrupts.

4.1.6.Program_cache_global_inv

This example shows how to do a global invalidate of program cache present in EVE module. The program cache global invalidate register can be set to invalidate all the lines in the L1P cache by resetting all valid bits. Any CPU fetches put out during the invalidate-all operation will stall until the invalidate-all operation completes, and will subsequently miss in the program cache.

4.1.7.Program_cache_block_inv

The program cache controller supports a programmable invalidate mechanism with which the starting address and the number of words to invalidate can be specified to fire off a range-based invalidation sequence. The programming model for the invalidation mechanism consists of two memory-mapped registers: the Start Address Register that holds the start address and the Byte Count Register that holds the number of bytes to be invalidated.

This example shows how to make use of this feature. The invalidate operation begins immediately on writing into the Byte Count register (max = 0x8000). The application must first set the Start Address Register and then the Byte Count Register to ensure correct operation. The operation itself involves cycling through addresses starting from the Start Address Register value in increments of the cache line size, doing tag lookups to check if the line exists in the cache and if it does, resetting the corresponding valid bit. The Byte Count Register field is reset to zero when the invalidate completes. As the Byte Count Register is readable, a check for zero provides a synchronization event for the application to execute from the region being invalidated or before issuing another range based invalidate. In the course of such an invalidation sequence, any further writes to the Start Address Register or the Byte Count Register is ignored. Note that start the Start Address can be any arbitrary byte address; whereas, the invalidate operation occurs on cache-lines (that is, 32-bit aligned). Thus, the range invalidated is effectively rounded down to the nearest cache-line address relative to the start address, and rounded up to include the entire cache line relative to the end address.

As in the global invalidate case, any CPU program fetches put out during the invalidate-range operation will stall until the invalidation completes. The underlying invalidate operation will begin after any in-flight requests are completed. The single address invalidate feature is mainly for breakpoints set by the debugger, and hence you need not leverage this feature, as it is primarily for the debugger.

4.1.8.Program_cache_software_prefetch

This example shows how to use software directed preload (SDP) capability of program cache module inside EVE subsystem.

Software directed preload (SDP) allows you to request that a range of system memory to be preloaded into the Program Cache. You set the Preload Base Address register, along with a Preload Byte Count (max = 0x8000). Hardware will issue a cache line fill request to the system for the associated line for the programmed address range. Once the data is returned for each line, it is written to the cache (32-B per write, to minimize program stalls) and the tag is marked valid for the new address. This is repeated for every cache line in the requested range. When the operation is complete, the Preload Byte Count register will be read as 0. Software must verify that the previous operation has completed before issuing another SDP operation. Writes to the Preload Base Address or Byte Count while the previous operation is ongoing will be ignored.

Note that the Start Address can be any arbitrary byte address; whereas the preload operation occurs on cache-lines (that is, 32-bit aligned). Thus, the range preloaded is effectively rounded down to the nearest cache-line address relative to the start address, and rounded up to include the entire cache line relative to the end address.

Preload requests operate in parallel with the demand based prefetch block and do not use the buffering provided by the Demand Based Prefetch block. Instead, the return data for Software Directed Preload is written directly to the program cache as highest priority, thus minimizing buffering required and minimizing impact on the system.

4.1.9.Ref_mmu_tlb

This example shows how to program Memory Management Unit (MMU) of eve subsystem. In this example we implement manual TLB programming on the DSP, to setup the basic entries that are needed to run EVE applications. We need to always take up one TLB entry to map the virtual address of 0, which is where ARP32 resets to a valid physical address. The first TLB entry is used to do this, by mapping with the smallest memory size of 4K bytes. The second TLB entry maps the DDR address range with the identity transformation, where we are just saying that for the first 16 Mbytes of DDR, virtual address is the same as physical address. This is the reason why VIRTUAL_ADDRESS2 is the same as PHYSICAL_ADDRESS2. The third TLB region is used to show that if we intend to access say a system address of 4803 0000h and a 1MB region starting at this address. We also take two more TLB addresses to carve up level-3 L3 memory, referred to as on-chip memory OCMCRAM, into two regions of size 4KB and 64KB.

The 4KB page size and 64KB page sizes are normally used for partitioning code segments, while the 1MB and 16MB larger page sizes are used for large data arrays. After setting up the TLB entries, in this example we can access these memories using the virtual address as from EVE side.

You will notice that we have taken the small memory page to map the reset vector. We are leveraging virtual memory address translation on TLB entries 4 and 5, where the virtual address and it's corresponding physical addresses are indeed different. For this example, we choose to map a virtual address of 5030 0000h, maps to a physical address of 4030 0000h. We have also chosen to designate all these TLB entries as mapping little-endian memory regions, with the access width being decided based on CPU access size. Additionally we have decided to lock down these TLB entries from being evicted by setting the preserve bit. This prevents the TLB entry from being flushed, as TLB misses get serviced, allowing to preserve a fast real time response for memory requests that access the regions programmed by these TLB entries. After configuring the required number of TLB entries to carve out a specific virtual memory to physical memory mapping, we enable the MMU hardware. At this point, we can release the ARP32 processor out of reset, by having the DSP write to the appropriate register at the SOC level. The ARP32 processor resets at virtual address 0, which is mapped to 8000 0000h in our example, which is why the reset vector is linked at this address in the EVE software examples.

4.1.10. Ref_mmu_tlb_miss_tlw_dis

This example demonstrates the concept of TLB miss in EVE subsystems MMU.

When EVE makes an access to an address region for which there are no corresponding entries in the MMU, there is a translation look aside buffer miss. This causes EVE to be stalled for a response until the MMU has responded to the TLB miss. The way to catch such events, is to enable the MMU interrupt support, which is routed to the EVE interrupt controller as one of the events. Unlike other interrupt events which can be serviced by ARP32 the MMU interrupt needs to be serviced by an external host most typically an ARM. In order to do this, EVE has up to four output interrupts, which can be routed to external hosts. Please also refer to registers EVE_INTX_OUT_IRQ raw, status, set and clear to figure out which of the 32 events, you want an external host to respond to. The MMU error interrupt is a good example of an interrupt which should be serviced by an external host.

In this example, we use the DSP once again to program the TLB entries. We configure the MMU. We continue to poll on the IRQ raw register to see, if a MMU error interrupt has occurred. On a normal SOC platform, we would have enabled this as an interrupt source. When the MMU error has been detected, we read the fault address and status register to determine why the error was generated.

We program the TLB for the fault address, clear the MMU IRQ status, and return. In a normal SOC platform the function “MMU_Intr_Handler” will run as an interrupt service routine on whichever host is tasked with the job of servicing the MMU error interrupt.

4.1.11. Vcop_done_intr

This example shows the usage of VCOP_DONE interrupt of interrupt controller. In this example , we setup the “vcop_done” event to interrupt “INT4” and enable it. The use of detecting “vcop_done” as an interrupt is fairly limited, as you will be polling because you have sent a “VWDONE” in order to receive an interrupt. This is one of the main reasons that most EVE software examples use polling, as it is possible to finish everything else you can finish within a task of computation, and then poll at the end as opposed to using interrupts, which always has a context switch overhead. The function “vcop_done_intr_Handler” is the interrupt handler for the event “vcop_done”, which is registered in the array “inth_Irq_Handler”. The disabling of the interrupt is done at the end of the test case by calling the “EVE_INTH_InterruptDisable” function, to disable the event.

4.1.12. Vcop_error_intr

The VCOP hardware will report error status due to various error conditions in the VCOP Error register, in addition to generating an interrupt for ARP32 to service. Section 9.3 of EVE’s programmer guide presents the details of various VCOP registers, including the error register. Errors can be triggered due to various conditions such as illegal instructions, incorrectly formed loops, parameter pointer to the loop is not aligned on a 32-bit boundary, parameter register points to out of bound memory region, exceeded maximum iterations as specified in “MAX_ITERS” register, load or store out of bound access from IBUFL, IBUFH, or WBUF, error due to force abort request received.

These error scenarios do not occur during normal code execution. However, when they do occur, it is convenient to receive an interrupt, read and clear the VCOP status register before issuing the next vector core loop for execution. Hence, it is convenient and, in fact, a good recommended practice, to have the vcop error interrupt enabled even during code or application development to catch various errors due to incorrect programmation, as opposed to running incorrect code and the difficulties involved with debugging such code.

This example shows the code for a vector core error interrupt test case, where we purposefully inject this error, by passing the vector core function “my_eve_array_add_uns_char_custom” a parameter pointer which is not 32-bit aligned. The vector core always reads the parameter registers each of which are 16- bits, 16 at a time, taking advantage of the vector core’s 256-bit bandwidth on any given memory. In this example, we map the vector core error interrupt to interrupt 4. We will see in output that interrupt handler “vcop_error_Intr_handler” being executed twice, and the value of the VCOP_ERROR register to be 4, which corresponds to bit 2, of the register. Section 9.3 of EVE’s programming guide shows that this bit is set, if the parameter register is not 32-bit aligned.

4.1.13. Vcop_max_iters_intr

This example shows how to use maximum iteration register. The vector core maximum iterations register is a safety register, by which the user can indicate the maximum number of iterations that no individual loop will exceed. The programmer is expected to analyze his application and program a safe value, which none of the loops are supposed to exceed. This feature is disabled on EVE reset, and the maximum iteration register has a zero value. This feature is intended to catch and stop the vector core as soon as possible, in cases where it receives illegal parameters from memory, and hence gets into a run-away situation. It is possible that without this check, the vector core can run for several iterations, as it supports four nested loops, and each loop count can be a 16-bit value.

In this example we are setting up the interrupt controller to detect interrupts for vector core completion and for vector core error. We have a common interrupt handler function by way of "vcop_done_Intr_Handler", to handle both vector core done, and vector core error events.

Upon seeing a vector core error, all remaining vector core instructions, including instructions of back to back loops will be decoded and flushed, until the vector core sees a "VWDONE" instruction, on which it will send both a vector core done, and a vector core error event, which can raise an interrupt. In our case, since we have both events enabled, we see both a done interrupt, and an error interrupt with the ninth bit, or bit 8 set, which is why vcop_error register has the value of 256. It is the user's responsibility to read and clear the vector core error register. On clearing the error register, we can resume processing, and since we send the same erroneous sequence, we see the interrupt again.

4.1.14. Sctm_vcop_busy_time

Several events of interest can be measured using SCTM. To understand the performance of VCOP on a given loop, we can instrument our code to measure how long VCOP was busy. The vcop_busy SCTM signal indicates the decode time and execution time. The SCTM hardware allows you to drill down into one loop or a sequence of back-to-back loops, and obtain a detailed view of how VCOP or program cache is behaving in the actual hardware and collects this information, without altering the program execution. This example shows how to get vcop busy cycles using SCTM module of EVE subsystem.

4.1.15. sctm_counters_observing_8_events

This example shows how to use multiple counters to observe multiple events simultaneously. We can use all eight counters, and be monitoring multiple events of interest in parallel, as shown in the code. In this example we are monitoring the start of individual VCOP loops, the finishing of the individual VCOP loops (these are pulse events, we get 1 pulse every time VCOP starts or stops), duration VCOP was busy (duration event), number of reads to IBUFL, IBUFH, WBUF, number of writes to IBUFH and WBUF, as the events of interest. We have 2 loops that are called back-to-back, for execution on VCOP, so that the decode of the second loop can happen in the background as the first loop executes.

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Chapter 5

Frequently Asked Questions

This chapter provides answers to few frequently asked questions related to using this starterware.

5.1. Release Package

Question	Answer
Can this starterware release be used on any eve based platform?	Yes, you can use it. But there are some examples involving multiple EVE's and hence can only be validated on vayu platform
Where are the host (DSP) API's in this release	Host API's are same as the API's for EVE starterware. You just have to link using correct library from the libs folder (Libs folder contain separate libraries for DSP hosts). It is to be noted that not all eve starterware API's are supported from host. For the list of API's supported on DSP kindly refer to section 0
Where are API's to configure DSP interrupts	As DSP interrupts configuration is not part of eve starterware API's, in this release we have moved these API's to examples folder (starterware/examples/common/dsp). Each example currently build these API's as a part of their own build
This is EVE Starterware release why there is a DSP folders inside it	Some of the EVE Starterware API's can also be called from hosts like DSP and hence we have DSP folders which contains DSP specific details

5.2. Code Build and Execution

Question	Answer
Build is not working and not giving any error	Ensure that you have set proper environment variables as described in section 2.3.
Starterware build is not working on windows, giving error "gmake: *** No rule to make target"	Ensure that you have set proper environment variables as described in section 2.3. Make sure that your EVE_SW_ROOT path is not too long. If this path is too long in windows, build can fail. Other way to fix this problem is to create a link to this path. For this you can use subst utility in windows. This will create a new drive with the content of you directory. subst <DRIVE NAME> PATH e.g. subst X: $(EVE_SW_ROOT)
Starterware build not working on windows: Makefile:9: D:workvayueve/modules/starterware/examples/common/common.mk: No such file or directory	Make sure in your environment variable all paths use forward slash "/" instead of backward slash "\". Also do not use any quotes or spaces in the path names. If there are some spaces in path then usethe following way, if we want to set ARP32 compiler path as C:/Program Files/Texas Instruments/ARP32_tools, use set ARP32_TOOLS=C:/PROGRA~1/TEXASI~1/ARP32_tools

Question	Answer
Where can I file gel files needed for running mailbox examples	Kindly look into gel folder present in gels folder located at EVE software root directory. It contains two separate folders for vayu and vme platform.

5.3. Issues with tools

Question	Answer
What tools are required for using this starterware release?	Kindly see section 0 for the list of tools required.