PDK/PDK TDA Release Notes

PDK TDA Version 01.10.02

Release Notes
4th January 2019

Important Note

This release is for TDA3xx, TDA2Px, TDA2xx, TDA2Ex and TDA2Ex 17x17 platforms.

Introduction

This release notes provides important information that will assist you in using the PDK software package. This document provides the product information and known issues that are specific to the PDK software package.

New in this Release

- RADAR
  - PDK-3337: The support for the TDA2x Cascade Radar board Rev 2.0 has been added which uses different SPI lines and GPIO lines to talk to the 4 chip AWR1243 cascade configuration.
  - PDK-3339: An example has been added which showcases how the TDA2x on the cascade radar board Rev 2.0 and 1.0 can talk to the SPI flash associated with the FPGA which converts CSI to parallel. This is useful for flashing a new FPGA image that is to be loaded without connecting the Lattice USB 2B cable.

Installation and Usage

Installation and Usage of the PDK package could be found at PDK Software Developer Guide

Upgrade and Compatibility Information

- None

Dependencies

This release requires following tools/packages to be installed.

- Code Composer Studio Version: CCS 5.4, CCS 5.5, CCS 6 or CCS 7
- XDC Tools Version: 3.32.01.22_core
- BIOS Version: 6.46.06.00
- CG Tool (TMS470) Version: 16.9.2.LTS
- CG Tool (C6000) Version: 8.2.4
- CG Tool (ARP32) Version: 1.0.7
- GCC Tool (Linaro) Version: 4.9-2015q3
- EDMA LLD: 02.12.00.21
- MMWAVE DFP: 01.02.00.00 (Only for AR1xx Radar)
- MSHIELD DK: 4.5.3 (Only for TDA2xx HS build)

Devices Supported

- TDA3xx PG1.0, PG2.0
- TDA2xx PG1.0, PG1.1, PG2.0
- TDA2Px PG1.0
- TDA2Ex PG1.0, PG2.0
- TDA2Ex_17x17 PG1.0

Application Boards Supported

- Base Board
  - TDA3xx Base EVM
  - TDA2xx Base EVM
  - TDA2Px Base EVM
  - TDA2Ex Base EVM
  - TDA2Ex 17x17 Base EVM
- Daughter Board
  - LCD board (480P, 720P, 1080P)
  - TDA3xx Multi-deserializer board
  - TDA3xx UB960 EVM
  - TDA3xx RVP board
  - TDA2xx/TDA2Ex/TDA2Px Vision application board
  - TDA2xx/TDA2Ex/TDA2Px Vision application board with Multi-deserializer board
  - TDA2xx/TDA2Ex/TDA2Px JAMR3 application board

What is Supported

- CSL:
  - UART, I2C, GPIO, McASP, McSPI, QSPI, PWM
  - Mailbox, Spinlock, EDMA, OCMC, MMU, Timer
  - MMCSD, PCIe, GPMC
  - DCAN, MCAN
  - RTI, CRC, ESM, ADC, DCC, L3FW, L4FW, WDTimer
  - UNICACHE, AMMU, CACHE_A15, MMU_A15, IPU ECC, MPU L2 RAM ECC, C66x XMU, C66x MPU
- VPS Drivers:
  - VIP Capture
  - VPE M2M
  - DSS Display
  - DSS Capture Writeback
  - DSS M2M Writeback
  - CAL Capture
  - ISS M2M
  - ISS M2M SIMCOP
- Secondary Bootloader (SBL)
  - SBL Library
  - SBL Utility Library
  - QSPI Flash Library
  - NOR Flash Library

  - SBL Application
- BSP LLD (GIO/IOM drivers): UART, McSPI, I2C
- STW LLD: FATLIB, I2C LLD, UART console
- PM: PMHAL, PMLIB
- IPC LITE Library
- L3/L4 Firewall Library
- Diagnostics Library

Features

For details on features, refer to PDK_Requirement_to_Test_Traceability_Report.xlsx under <PDK_INSTALL>/docs/traceability folder.

Supported/Validated Examples

For details on supported/validated examples, refer to test report of each platform under <PDK_INSTALL>/docs/test_report/<platform> folder.

Fixed in this Release

The patches for few critical bugs are shared at this location: http://processors.wiki.ti.com/index.php/PDK/PDK_Patches

Fixed in this Release

ID	Headline	Module	Affected Versions	Affected Platforms
PDK-3396	CAL : Second PHY Error notification not enabled	CAL	All previous versions	TDA2Ex-EVM, TDA2Px-EVM
PDK-3379	CAL : TDA2Px : Cannot operate 2nd PHY alone	CAL	All previous versions	TDA2Ex-EVM, TDA2Px-EVM
PDK-2952	[VPS] RT params are not handled in case application updates buffer at the time of frame repeat Closed	DSS	All previous versions	TDA2xx-EVM, TDA2Ex-EVM, TDA3xx-EVM, TDA2Px-EVM
PDK-3380	[RADAR][FPGA]: FPGA image is built for 81 pin package and does not work for 80 pin Lattice FPGA on cascade radar EVM	RADAR	PDK_TDA_01.10.00, PDK_TDA_01.10.01	TDA2xx-EVM
PDK-3383	Bsp_ar12xxGetWidthHeight() API assumes Advance frame config "numSubFrames" has valid value Resolved	RADAR	PDK_TDA_01.10.00, PDK_TDA_01.10.01	TDA2xx-EVM
PDK-3399	Update PM Data base for MPU frequency as per latest DM	PM	All previous versions	TDA2xx-EVM, TDA2Ex-EVM, TDA3xx-EVM, TDA2Px-EVM
PDK-3434	[sbl] TDA2px opphigh is not setting the ISS clock to 535MHz Closed	SBL	PDK_TDA_01.10.00, PDK_TDA_01.10.01	TDA2Px-EVM
PDK-3440	Update multicore image generator tool to allow more than 10 input files Resolved	SBL	All previous versions	TDA2xx-EVM, TDA2Ex-EVM, TDA2Px-EVM

PDK-3375	Wrong values used for enabling GPIO in PRCM	CSL	All previous versions	TDA2xx-EVM, TDA2Ex-EVM, TDA3xx-EVM, TDA2Px-EVM
PDK-3391	[DCC] Example enables DCC1 when using DCC4	CSL	All previous versions	TDA3xx-EVM
PDK-3455	MPU Wugen should enable interrupt lookup for MPU Core 1 when Core 1 is enabled	CSL	All previous versions	TDA2xx-EVM

Known Issues

None

Known Limitations

VIP Capture Driver

- PDK-2107: Black screen seen with HDMI capture using ADV7611 when run back to back. This is suspected to be ADV EDID programming issue. Restarting the usecase works fine. Applicable for TDA2xx, TDA2Ex, TDA2Px platforms.
- PDP-935: After POR, HDMI Capture fails on ADV vision app board with laptop HDMI input. Disconnecting and connecting the HDMI cable again after power on reset is the known workaround. Applicable for TDA2xx, TDA2Ex, TDA2Px, TDA3xx platforms
- In case of ADV7611 HDMI in capture, first few frames in the first run after power cycle might have artifacts. This is because when the ADV7611 is configured, it programs the internal EDID for 1080p60 and does Hot Plug Assert (HPA). When this happens the video source will read the EDID and reconfigure itself for the new timing. At this time the video might be corrupted.
- In TDA2xx/TDA2Ex, HDMI capture from SIL9127 is not supported when Multi-serdes board is connected to VISION daughter card. This is because of the I2C address conflict between SIL9127 and the deserializer (This is a board limitation).
- 24-bit RAW capture - No support in EVM
- RGB888 input to VIP - No support in EVM
- Various discrete sync modes except HSYNC/VSYNC mode - No support in EVM
- In case of dual output streams from same capture source, below limitations applies
  - YUV422SP output should always be stream 0 (first stream)
  - For YUV422I scaled and YUV420SP non-scaled outputs, YUV422I scaled output should always be stream 0 (first stream)
  - Scaled outputs on both the streams are not supported

DSS Display Driver

- PDK-2075: Croping is not working with the mem to mem writeback. Write the full frame in the WB path is the known workaround. Applicable for TDA3xx platform. TDA2xx/TDA2Ex/TDA2Px DSS doesn't support cropping in WB path.
- PDP-1425: YUV422I 1080P input downscaled to YUV420SP 720P on write-back path does not work with the mem to mem writeback. Use the scalar in the input pipeline and do 1x scaling in the write-back path as a workaround. Applicable for TDA2xx, TDA2Ex, TDA2Px, TDA3xx platforms.
- PDP-1402: DSS M2M driver with input pipe from GRPX is not working. Workaround is to use video pipeline as video pipeline also supports RGB input format. Applicable for TDA2xx, TDA2Ex, TDA2Px platforms.

- In TDA3xx SD Venc writeback in RGB format could result in extra bytes write, Below is the explaination for the same and the driver configuration parameters to handle this.
  - With the implementation of the errata i873, where venc size is increased by 2 pixels, and fwd pipe position is also shifted by 2 pixels while programming the DSS registers.
  - With following change in input parameter extra bytes will not be written.
    - Driver takes the overlay size as an input parameter. It should be given as 722 (insted of 720) in case of SD Venc writeback for NTSC or PAL format (with 2 extra pixels per line).
      ```
      Vps_CaptDssWbParams->inFmt.width = 722;
      ```
    - Following are the three options for writeback and the driver config parameters:
      1. Do not scale the image and writeback 722 pixels per line; This will have first 2 blank pixels and 720 actual video pixels. App should allocate buffer for 722 pixels per line.
      ```
      Vps_CaptDssWbParams->outStreamInfo[0].outFmt.width = 722;
      Vps_CaptDssWbParams->inCropCfg.cropHeight = 722;
      ```
      2. Scale the writeback buffer; 2 blank + 720 actual video pixels scaled to total 720 pixels in written back buffer. App should allocate buffer for 720 pixels per line.
      ```
      Vps_CaptDssWbParams->outStreamInfo[0].outFmt.width = 720;
      Vps_CaptDssWbParams->inCropCfg.cropHeight = 722;
      ```
      3. Use region based writeback to crop the image from 2 to 722 pixels per line from overlay. App should allocate 720 pixels per line and writeback without any blank pixels.
      ```
      Vps_CaptDssWbParams->outStreamInfo[0].outFmt.width = 720;
      Vps_CaptDssWbParams->inCropCfg.cropHeight = 720;
      Vps_CaptDssWbParams->outStreamInfo[0].cropEnable = TRUE;
      ```
- The region based writeback on TDA3xx has few limitation like writing extra bytes or drop in writeback frame rate.
  Please refer the VPS Display Driver UserGuide.
- In TDA3xx, when OPP_HIGH performance point is selected and the usecase demands GMAC and Display to be functional, the DPLL_EVE_VID_DSP is used to drive both the DSP 745 MHz clock and the DSS VID Pix Clock. This creates a limitation on the video pixel clock to 149 MHz and integer division of the same (eg. 149MHz, 74.5MHz, 37.25MHz etc.). The 7 inch LCD display which requires 29.232MHz will not be supported on the TDA3xx when the OPP_HIGH is set. Other OPPs do not share this problem.

Serial Drivers

- When UART driver's configuration is in interrupt mode and when the RX buffer size is bigger than FIFO size and when UART driver receives data of same length as FIFO size, the GIO_read function does not return until it receives next data due to H/W specification as given below. To workaround this limitation, RX FIFO size and RX buffer size needs to configured as same length.
  - As per the UART IP (given in TRM section 24.3.4.8.1.3.7.1 Time-out Counter), when there is a break in the continuous UART character received, it will timeout so that the driver can read the last bytes out of the UART FIFO when the bytes received is less that the FIFO threshold. In the above case, since the user has given (Receive data size == FIFO threshold), the driver get the FIFO threshold interrupt instead of timeout interrupt. And the driver reads this out of the FIFO before the UART IP times out. Since this is not a timeout, the driver will wait for few more bytes (since RX size is greater than FIFO size) and doesn't return with timeout.
- UART single byte transfer is supported in polled/interrupt Mode and not in DMA Mode
- Junk characters are observed in the UART terminal whenever we do reset on the board. This is present in TDA3xx-EVM only.
- PDK-3283: McSPI Slave driver FIFO mode, does not support less than FIFO size transfers

- workaround is in case of slave mode, disable FIFO or have the transfer size of multiple of FIFO size

CAL/ISS Driver

- PDK-2136: Pixel Corruption is seen for 12bit MIPI format. Applicable for TDA3xx and TDA2Px platforms.

OV10640 Sensor Drivers

- On some TDA3xx EVMs, I2C register write for the OV10640 sensor is failing at 400KHz I2C frequency. In this case, change the I2C frequency to 100KHz in `gBoardTda3xxI2cInstData[1].busClkKHz` in `packages/ti/drv/vps/src/boards/src/bsp_boardTda3xx.c` file.

```
diff --git a/packages/ti/drv/vps/src/boards/src/bsp_boardTda3xx.c b/packages/ti/drv/vps/src/boards/src/boarindex
--- a/packages/ti/drv/vps/src/boards/src/bsp_boardTda3xx.c
+++ b/packages/ti/drv/vps/src/boards/src/bsp_boardTda3xx.c
@@ -281,7 +281,7 @@ static Bsp_BoardI2cInstData gBoardTda3xxI2cInstData[] =
        BSP_DEVICE_I2C_INST_ID_1,           /* instId */
        SOC_I2C2_BASE,                      /* baseAddr */
        CSL_INTC_EVENTID_I2CINT2,           /* intNum */
-       400U                                /* busClkKHz */
+       100U                                /* busClkKHz */
    }
};
```

- I2C transaction fails on address 0x33 for some of the OV10640 Parallel sensor. In this case, change the I2C address to 0x31 for the macro BOARD_OV10640_I2C_ADDR_CPI in the file `packages/ti/drv/vps/src/boards/src/bsp_boardPriv.h`
- Please refer "User Guide" that came with this release, for EVM modifications required for I2C

Sensor Tuning

- Tuning the sensor is beyond the scope of this product. An higher level software (such as SDK) will have to tune sensor for the required quality.
- Quality of the sensor (and/or processing) should not be judged based on the ISS demo applications.

A15 Arch Library

- A15 architecture library has assembly code which does not support thumb mode operation.
- User should ensure A15 is executing in arm mode while calling these APIs.

Validation Information

- This release is validated on TDA2xx, TDA2Px, TDA2Ex/TDA2Ex 17x17 and TDA3xx EVM for the above mentioned components

Technical Support and Product Updates

For further information or to report any problems, contact http://e2e.ti.com or http://community.ti.com or http://support.ti.com.

Archived

- PDK TDA Release Note 1.07.00 [1]
- PDK TDA Release Note 1.08.00 [2]
- PDK TDA Release Note 1.08.01 [3]
- PDK TDA Release Note 1.09.00 [4]
- PDK TDA Release Note 1.10.00 [5]
- PDK TDA Release Note 1.10.01 [6]

References

[1] http://processors.wiki.ti.com/index.php?title=PDK/PDK_TDA_Release_Notes&oldid=229221
[2] http://processors.wiki.ti.com/index.php?title=PDK/PDK_TDA_Release_Notes&oldid=231160
[3] http://processors.wiki.ti.com/index.php?title=PDK/PDK_TDA_Release_Notes&oldid=232436
[4] http://processors.wiki.ti.com/index.php?title=PDK/PDK_TDA_Release_Notes&oldid=233776
[5] http://processors.wiki.ti.com/index.php?title=PDK/PDK_TDA_Release_Notes&oldid=234995
[6] http://processors.wiki.ti.com/index.php?title=PDK/PDK_TDA_Release_Notes&oldid=235644

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