ResearchGate

See discussions, stats, and author profiles for this publication at: https://www.researchgate.net/publication/251945208

Application of simulated annealing to cluster-boundary search algorithm for macrocell placement optimization

Article · May 2010

DOI: 10.1109/ICCCE.2010.5556748

CITATIONS
0

READS
28

1 author:

Mustahsan Mir
Ajman University

45 PUBLICATIONS **273** CITATIONS

SEE PROFILE

Some of the authors of this publication are also working on these related projects:

Project

Autonomous UAV for Civil Defense Applications View project

All content following this page was uploaded by Mustahsan Mir on 20 October 2015.

The user has requested enhancement of the downloaded file.

Application of Simulated Annealing to Cluster-Boundary Search Algorithm for Macrocell Placement Optimization

Mustahsan Mir
Department of Electrical Engineering
Ajman University of Science & Technology
U.A.E.
mmir@ieee.org

Abstract— **This paper presents a hybrid technique for macrocell placement optimization. The presented technique integrates the probabilistic hill-climbing feature of simulated annealing with the (deterministic) cluster-boundary search algorithm in order to minimize the likelihood of local optimal solutions. It optimizes the placement as well as orientation of macrocells and produces overlap-free designs satisfying constraints on interconnect length bounds. The technique is computationally efficient and can generate high-quality solutions for large-sized placement problems. Test results for placement optimization problems involving up to 100 macrocells are presented and analyzed to determine the effectiveness of the presented hybrid technique.**

Keywords- placement optimization; simulated annealing; hybrid techniques; VLSI floorplan design; computer-aided design.

I. INTRODUCTION

Macrocell placement optimization problem is a complex optimization problem that involves determining the optimal placement of macrocells on a 2-D plane such that a given objective function is minimized subject to some specified set of constraints. It may be considered as a special case of VLSI floorplan design in which all the modules (macrocells) are rigid, that is, having fixed areas and aspect ratios. Generally, the objective is to either minimize the total interconnect wire length or the chip area or a weighted sum of both wire length and chip area [1-3]. The constraints include non-overlapping of macrocells, upper bounds on net delays, alignment and preplace constraints, etc. [4,5]. As no general solution exists for this complex optimization problem, numerous heuristic techniques including those based on simulated annealing (SA) and genetic algorithms (GA) have been developed to efficiently solve this problem for a near-optimal solution [6-10]. The heuristic techniques, in general, do not consider the geometrical specifications, that is, *actual* dimensions of the macrocells, during the initial phase of finding the relative placement but have been quite successful as they are capable of finding good solutions taking into account a variety of practical constraints in macrocell placement and VLSI floorplan design. While most of the earlier and some recent analytical techniques have also ignored the geometrical specifications of macrocells during the optimization process [11-13], other analytical techniques have successfully incorporated the geometrical specifications in their mathematical formulation [14-17].

Analytic techniques that incorporate the actual dimensions of macrocells in their mathematical formulation have the distinct advantage of producing optimal placements without any overlaps. This is in contrast to many other placement techniques that need a subsequent stage after optimization to remove the overlapping of macrocells and thus obtain a feasible design [18,19]. However, most analytic techniques are based on deterministic search algorithms and are therefore susceptible to getting stuck at some local minima. To minimize the likelihood of a local optimal solution, some hybrid techniques have been developed by combining certain features of well-known heuristic techniques such as simulated annealing and genetic algorithms with analytic procedures to obtain better optimization results [20].

An efficient and promising analytic technique for large-sized macrocell placement problems is based on cluster-boundary search algorithm [16]. It is a constructive procedure that finds the optimum position of a macrocell with respect to the already formed cluster of macrocells by performing one-dimensional search along the cluster boundary. The search domain includes the entire feasible design space and therefore at each move, a macrocell is placed at its optimum position, on a continuous 2-D plane, with respect to the already placed macrocells. This, however, does not ensure that the final placement is the global optimum solution as the ordering of macrocells in a constructive procedure plays an important role and the possibility of getting stuck at local optima still exists because macrocells that are yet to be placed are not taken into consideration while determining the optimum position of the current macrocell. In order to minimize the probability of local optimal solutions, a hybrid technique that integrates the probabilistic hill-climbing feature of simulated annealing with the (deterministic) cluster-boundary search algorithm is presented in this paper. The technique is tested for different placement problems including large-sized problems of up to 100 macrocells. Test results are presented and analyzed to determine the effectiveness of the developed hybrid technique.

978-1-4244-6235-3/10/$26.00 ©2010 IEEE

II. MATHEMATICAL FORMULATION

The macrocell placement optimization problem, defined in terms of the input data and the required output, is stated in the following for the presented technique.

Input:

1. A set of n rectangular macrocells M = { m_1, m_2, ..., m_n }, each having fixed width and height specified as (w_i , h_i), i = 1, 2,..., n.
2. A set of two-terminal nets N = { n_{ij} } describing the connectivity relationship for each pair of macrocells m_i and m_j, i,j =1,2,......, n.
3. A set of bounds B = { b_{ij} } that defines the maximum allowed interconnect length b_{ij} for each two-terminal net n_{ij}, i,j =1,2,......, n.

Output:

An optimal placement of macrocells on a continuous 2-D plane is desired such that:

1. Each macrocell is placed at its optimal position defined by its centroid (x_i , y_i).
2. The orientations of macrocells are also optimized.
3. There is no overlapping of macrocells at any stage of the optimization process.
4. The upper bounds on interconnect wire lengths are not violated.
5. A cost function F, based on either the total wirelength or weighted sum of total wirelength and chip area (area of the bounding rectangle that encloses all the macrocells) is minimized.

Mathematically, this problem can be stated as:

Minimize F (**X**)

subject to

$$\beta_{ij} \le 0 \qquad i=1,2,..., n-1 ;\ j= i+1 \text{ to } n$$

$$d_{ij} \le b_{ij} \qquad i=1,2,..., n-1;\ j= i+1 \text{ to } n \qquad (1)$$

where,

$$F(\mathbf{X}) = \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} n_{ij} d_{ij} + \omega A_R \qquad (2)$$

Here, β_{ij} is the overlap area between two macrocells m_i and m_j, and d_{ij} is the distance between their centroids. Also, A_R is the area of bounding rectangle that encloses macrocells placed on 2-D plane and ω is the corresponding weight. If ω=0, then only the wirelength is minimized. The overlap area β_{ij} between two macrocells m_i and m_j is defined such that it will have a positive value if and only if there is an overlapping of these macrocells. Otherwise, its value will be negative satisfying the constraint specified in Eqn. (1). The following definition of β_{ij} fulfills this condition:

$$\beta_{ij} = \lambda_{ij} (\Delta X_{ij})(\Delta Y_{ij}) \qquad (3)$$

where,

$$\Delta X_{ij} = \left(\frac{w_i + w_j}{2}\right) - | x_i - x_j | \qquad (4)$$

$$\Delta Y_{ij} = \left(\frac{h_i + h_j}{2}\right) - | y_i - y_j | \qquad (5)$$

$$\lambda_{ij} = -1 \quad \text{for} \quad \Delta X_{ij} \le 0 \ \ and \ \ \Delta Y_{ij} \le 0$$
$$= +1 \quad \text{otherwise} \qquad (6)$$

III. OPTIMIZATION PROCEDURE

The proposed optimization procedure for solving the above stated problem is a hybrid procedure that integrates the analytic cluster-boundary search procedure with simulated annealing heuristic. Optimization steps for the hybrid procedure are explained in the following.

Step #1 (Ordering)

Prior to starting the optimization process, an ordering of the macrocells is determined since in a constructive procedure one macrocell is placed at a time at its optimal position. The first macrocell to be placed is the one with the highest value of ordering function φ_i defined as follows.

$$\varphi_i = \mu \sum_{j=1}^{n} n_{ij} + \gamma \sum_{j=1}^{n} \frac{1}{b_{ij}} \qquad i = 1,2,\dots, n;\ j \ne i \qquad (7)$$

where μ and γ are the weights for wirelength and interconnect bounds, respectively. The ordering for the remaining macrocells is determined on the basis of the descending values of the ordering function ξ_p defined as follows:

$$\xi_p = \mu \sum_{q=1}^{r} n_{pq} + \gamma \sum_{q=1}^{r} \frac{1}{b_{pq}} \qquad p = r+1 \text{ to } n \qquad (8)$$

where 'p' and 'q' refer to the unplaced and placed macrocells, respectively, and r is the number of placed macrocells at any stage.

The above ordering criterion can produce a number of ordering sequences for a given placement problem simply by changing the values of weights μ and γ. Accordingly, the user has the option to generate more than one solution for a given problem.

Step #2 (Placement of First and Second Macrocells)

Place the macrocell with the highest value of φ_i in the center of a two-dimensional continuous plane and then select the next macrocell 'p' with the highest value of ξ_p to be placed at its optimal position. This optimal position will be somewhere along the edges (sides) of the first placed macrocell because placing it away from the edges will increase the value of the cost function F and placing it any closer will result in overlapping with the first macrocell. To determine the optimal position of the second macrocell, one-dimensional search is carried out, using the modified quadratic-fit procedure [21], along all the four sides of the first placed macrocell and for both possible orientations of the second macrocell. For each position determined by the 1-D search for a given orientation, the interconnect bound violations for the placed macrocell are checked. Any position/orientation resulting in a constraint violation will be marked as infeasible. Among the feasible optimal positions, the second macrocell is placed at a position (with appropriate orientation) that corresponds to the minimum value of the cost function.

Step #3 (Placement of Next Macrocell)

The procedure of step #2 is repeated for the next macrocell in order. However, this time 1-D search will be carried out along the four edges of each placed macrocell. Furthermore, in addition to checking for interconnect bound violations, overlap constraint violations will also be checked. If a one-dimensional search results in an overlap with other macrocell(s), the new macrocell is moved from its just determined position by a distance X_{ij} or Y_{ij} (depending upon the direction of 1-D search) in order to remove this overlap. If this move also results in overlaps with some other macrocells, a penalty function approach is used and the value of the cost function is increased by an arbitrary large value indicating that 1-D search on this particular edge has failed to obtain a feasible solution. Otherwise, the value of the cost function is calculated for the current non-overlapping optimal position of the new macrocell on that particular edge. Among all the feasible optimal positions, the new macrocell, in a purely deterministic procedure, shall be placed at a position (with appropriate orientation) that corresponds to the minimum (best) value of the cost function. However, since this position is determined in the absence of remaining unplaced macrocells, there is some likelihood that it may give rise to local optimum solution when the remaining macrocells are subsequently placed. To get around the problem of local minima, a stochastic approach based on simulated annealing concept is introduced as explained below.

Consider T as a heuristic parameter called "Temperature" and let η be a uniformly generated pseudo random number in the range [0,1]. Let δ represent the absolute value of percentage difference in the cost function values of the best and the second-best placements for the incoming macrocell among all the edges of the placed macrocells. If $\eta \geq e^{-\delta/T}$ the new macrocell is placed at a position (with appropriate orientation) that corresponds to the minimum (best) value of the cost function. Otherwise, it is placed at a position (with appropriate orientation) that corresponds to the next best value of cost function. This ensures that the procedure is no more a purely deterministic procedure and at the same time perturbations do not result in placements with significant increase in the value of cost function. The value of "Temperature" parameter at k^{th} iteration T_k is updated at the $(k+1)^{th}$ iteration as $T_{k+1} = \alpha T_k$, where α is a constant; $0 < \alpha < 1$. In other words, the probability of placing a new macrocell at the second best position decreases in a pre-determined fashion as the number of placed macrocells increases.

Step #4 (Re-optimization of Placed Macrocells)

After the addition of each new macrocell, as explained in step #3, the positions/orientations of the already placed macrocells are once again optimized in the presence of the newly added macrocell. This is done by selecting one of the placed macrocells at a time and determining its optimum position/orientation by performing 1-D searches along the edges of all other placed macrocells including the newly placed macrocell. This process is repeated for each placed macrocell until there is no further improvement in the value of the cost function. This step is included to make the search process dynamic in the sense that all placed macrocells are continually moved to their optimum positions until no more improvement is possible.

Steps #3 and #4 are repeated for the next macrocell in order and so on until all the macrocells have been placed at their optimal positions with optimal orientations.

IV. TEST RESULTS

The presented hybrid technique was implemented in a computer program and after extensive testing with different placement problems, values for heuristic parameters T and α were selected as 0.5 and 0.99, respectively. These values are used in all test results presented in this paper. In order to demonstrate the application of the presented hybrid technique for large-sized placement problems and evaluate its performance, benchmark problems involving 28, 50, 75, and 100 unequal-area modules (macrocells) given in the user's manual of a general-purpose layout optimization program PLANOPT [22] were solved. It may be mentioned here that PLANOPT program utilizes a pseudo-exhaustive search technique especially developed for solving large-sized placement problems. For all these problems, the results are given for the cost function to minimize the total wirelength without any upper bounds on interconnect lengths. Accordingly, for the sake of comparing the results, optimization parameters were set as follows: ω=0, γ=0, and μ =1. The test results are presented in Table 1. It may be observed that for all four test problems the presented hybrid technique has produced better solutions as compared to those produced by PLANOPT. The optimal placement obtained for test problem 2 is shown in Figure 1. The program was run on Pentium 4, 3GHz PC and for the largest problem with 100 macrocells it took less than two minutes of PC time. This shows that the technique is computationally efficient for solving large-sized placement problems.

The program was also tested for problems involving upper bounds on interconnect lengths. In most cases the program converged in single run. However, in some problems with relatively large number of interconnect bounds, more runs with different ordering were needed to obtain converged solutions without any constraint violation. In other words, as is the case for any constructive procedure, the presented technique is also sensitive to ordering of macrocells.

Table 1: Comparison of results for test problems

Test No.	Number of Modules (Macrocells)	Cost Function Value	
		PLANOPT	Hybrid Technique
1	28	6559	6332
2	50	79234	78694
3	75	34967	34694
4	100	547990	544870

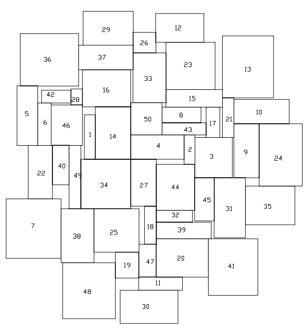

Figure 1: Optimal placement for test problem 2

V. CONCLUSION

A hybrid optimization technique is presented for optimizing the placement of macrocells on a continuous plane. The search domain for the analytic procedure includes the entire feasible design space formed by the cluster of previously placed macrocells and therefore at each optimization step a macrocell is placed at its optimum position. The concept of simulated annealing is integrated with the analytic procedure in order to minimize the probability of obtaining final placement as a local optimal solution. The technique has been implemented in a computer program and tested for different placement problems including large-sized problems of up to 100 macrocells. Test results are presented and analyzed to determine the effectiveness of the developed hybrid technique. It is shown that the presented technique is computationally efficient and can generate high-quality overlap-free placement solutions for large-sized problems. As is the case with any constructive procedure, the presented technique is also sensitive to the ordering of macrocells.

REFERENCES

[1] A.B. Kahng and S. Reda, "Wirelength minimization for min-cut placements via placement feedback", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* Vol. 25, No. 7, pp. 1301-1309, July 2006.

[2] X. Tang, R. Tian and D.F. Wong, "Minimizing wirelength in floorplanning", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* Vol. 25, No. 9, pp. 1744-1753, July 2006.

[3] L. Zhang, R. Raut, Y. Jiang and U. Kleine, "Placement algorithm in analog-layout designs", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* Vol. 25, No. 10, pp. 1889-1902, Oct. 2006.

[4] E.F.Y. Young, C.C.N. Chu, and M.L. Ho, "Placement constraints in flooplan design", *IEEE Trans. on VLSI Systems* Vol. 12, No. 7, pp. 735-745, July 2004.

[5] S. Chen, S. Dong, X. Hong, Y. Ma and C.K. Cheng, "VLSI block placement with alignment constraints", *IEEE Trans. on Circuits and Systems,* Vol. 53, No. 8, pp. 622-626, Aug. 2006.

[6] S. M. Sait and H. Youssef, VLSI Physical Design Automation: Theory and Practice, McGraw-Hill Book Company, Europe (also co-published by IEEE Press), 1995.

[7] S.Y. Ho, S.J. Ho, Y.K. Lin, and W. C. Chu, "An orthogonal simulated annealing algorithm for large floorplanning problems", *IEEE Trans. on VLSI Systems* Vol. 12, No. 8, pp. 874-877, Aug. 2004.

[8] U. Brenner and M. Struzyna, "Faster and better global placement by a new transportation algorithm", *Proceedings of 42nd Design Automation Conference*, pp. 591-596, June 2005.

[9] H. Esbensen and P. Mazumder, "SAGA: A unification of the genetic algorithm with simulated annealing and its application to macrocell placement", *Proc. IEEE Int. Conf. on VLSI Design*, 1994.

[10] J.P. Cohoon, S.U. Hedge, W.N. Martin and D.S. Richards, "Distributed genetic algorithms for the floorplan design problem", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 4, pp. 483-492, 1991.

[11] N.R. Quinn and M.A. Breur, "A force directed component placement procedure for printed circuit boards", *IEEE Trans. Circuits & Syst.*, Vol. 26, No. 6, pp. 377-388, 1979.

[12] A. Kennings and K. P. Vorwerk, "Force-directed methods for generic placement", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 10, pp. 2076-2084, 2006.

[13] G.J. Nam, S. Reda, C.J. Alpert, P.G. Villarrubia and A.B. Kahng, "A fast hierarchical quadratic placement algorithm", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 4, pp. 678-687, 2006.

[14] S. Sutanthavibul, E. Shragowitz and J.B. Rosen, "An analytical approach to floorplanning design and optimization", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 6, pp. 761-769, 1991.

[15] M. Mir and M. H. Imam, "Analytic annealing for macrocell placement optimization", *J. Computers and Electrical Engineering*, Vol. 22, No. 2, pp. 169-177, 1996.

[16] M. Mir and M. Al-Saleh, "A constructive procedure for optimizing the placement of macrocells", *Proceedings of 2001 IEEE Int'l. Symposium on Circuits and Systems*, Vol. 5, pp. 57-60, 2001.

[17] M. Mir, "Analytical technique for macrocell placement optimization with multiple constraints", *10th IEEE Int'l Conference on Electronics, Circuits and Systems*, pp. 503-506, Dec. 14-17, 2003.

[18] Y. Feng and D.P. Mehta, "Module relocation to obtain feasible constrained floorplans", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 5, pp. 856-865, 2006

[19] S. Alupoaei and S. Katkoori, "Ant colony system application to macrocell overlap removal", *IEEE Trans. on VLSI Systems*, Vol. 12, No. 10, pp. 1118-1122, Oct. 2004.

[20] M. Mir, "A novel hybrid technique for macrocell placement optimization", *J. IEEEP*, Vol. 36, pp. 26-37, 1998.

[21] M. Mir and M. H. Imam, "A gradient-based method for module placement", *Computers and Elect. Engng*, Vol. 16, No. 2, pp. 109-113, 1990.

[22] PLANOPT User's Manual (Ver. 4), Engineering Optimization Software (USA).

View publication stats