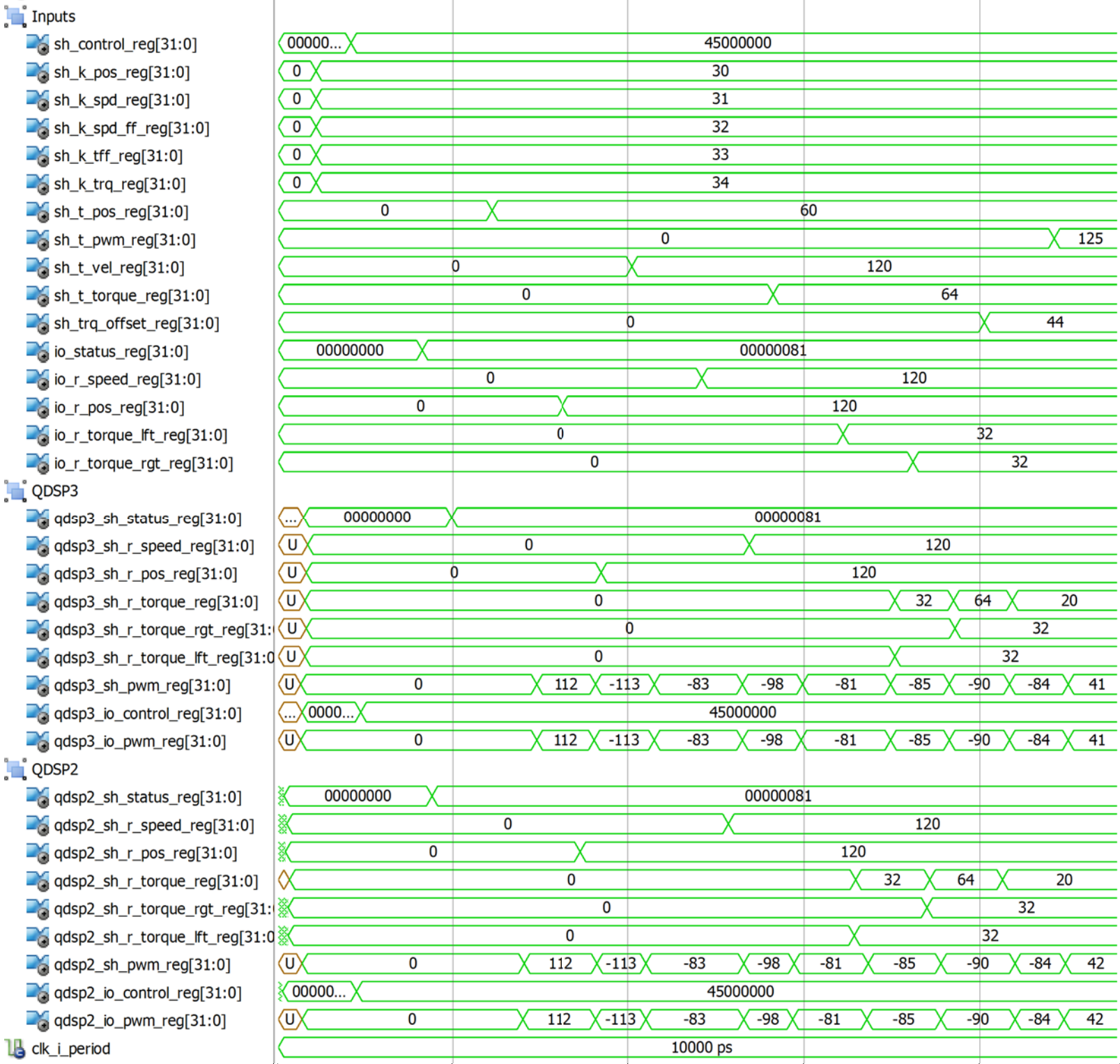
Inputs
sh_control_reg[31:0]
00000...
45000000
sh_k_pos_reg[31:0]
0
30
sh_k_spd_reg[31:0]
0
31
sh_k_spd_ff_reg[31:0]
0
32
sh_k_tff_reg[31:0]
0
33
sh_k_trq_reg[31:0]
0
34
sh_t_pos_reg[31:0]
0
60
sh_t_pwm_reg[31:0]
0
125
sh_t_vel_reg[31:0]
0
120
sh_t_torque_reg[31:0]
0
64
sh_trq_offset_reg[31:0]
0
44
io_status_reg[31:0]
00000000
00000081
io_r_speed_reg[31:0]
0
120
io_r_pos_reg[31:0]
0
120
io_r_torque_lft_reg[31:0]
0
32
io_r_torque_rgt_reg[31:0]
0
32
QDSP3
qdsp3_sh_status_reg[31:0]
...
00000000
00000081
qdsp3_sh_r_speed_reg[31:0]
U
0
120
qdsp3_sh_r_pos_reg[31:0]
U
0
120
qdsp3_sh_r_torque_reg[31:0]
U
0
32
64
20
qdsp3_sh_r_torque_rgt_reg[31:
U
0
32
qdsp3_sh_r_torque_lft_reg[31:0
U
0
32
qdsp3_sh_pwm_reg[31:0]
U
0
112
-113
-83
-98
-81
-85
-90
-84
41
qdsp3_io_control_reg[31:0]
...
0000...
45000000
qdsp3_io_pwm_reg[31:0]
U
0
112
-113
-83
-98
-81
-85
-90
-84
41
QDSP2
qdsp2_sh_status_reg[31:0]
00000000
00000081
qdsp2_sh_r_speed_reg[31:0]
0
120
qdsp2_sh_r_pos_reg[31:0]
0
120
qdsp2_sh_r_torque_reg[31:0]
0
32
64
20
qdsp2_sh_r_torque_rgt_reg[31:
0
32
qdsp2_sh_r_torque_lft_reg[31:0
0
32
qdsp2_sh_pwm_reg[31:0]
U
0
112
-113
-83
-98
-81
-85
-90
-84
42
qdsp2_io_control_reg[31:0]
00000...
45000000
qdsp2_io_pwm_reg[31:0]
U
0
112
-113
-83
-98
-81
-85
-90
-84
42
clk_i_period
10000 ps