Heriot-Watt University

Masters Thesis

Hardware acceleration with mixed-precision

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A thesis submitted in fulfilment of the requirements for the degree of MSc. Network Security

in the

School of Mathematical and Computer Sciences

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Declaration of Authorship

I, Quentin Ducasse, declare that this thesis titled, 'Hardware acceleration with mixed-precision' and the work presented in it is my own. I confirm that this work submitted for assessment is my own and is expressed in my own words. Any uses made within it of the works of other authors in any form (e.g., ideas, equations, figures, text, tables, programs) are properly acknowledged at any point of their use. A list of the references employed is included.

Signed: ____

Date: ____

"Thanks to my solid academic training, today I can write hundreds of words on virtually any topic without possessing a shred of information, which is how I got a good job in journalism."

Dave Barry

Abstract

The Thesis Abstract is written here (and usually kept to just this page).

Acknowledgements

The acknowledgements and the people to thank go here, don't forget to include your project advisor :)

Contents

Declaration of Authorship i

Abstract iii

Acknowledgements iv

Contents v

List of Figures vi

List of Tables vii

1 Introduction 1
- 1.1 Main Section 1 . . . 1
  - 1.1.1 Subsection 1 . . . 1
  - 1.1.2 Subsection 2 . . . 1
- 1.2 Main Section 2 . . . 2

2 Literature Review 3
- 2.1 Main Section 1 . . . 3
  - 2.1.1 Subsection 1 . . . 3
  - 2.1.2 Subsection 2 . . . 3
- 2.2 Main Section 2 . . . 4

3 Requirements Analysis 5
- 3.1 Main Section 1 . . . 5
  - 3.1.1 Subsection 1 . . . 5
  - 3.1.2 Subsection 2 . . . 5
- 3.2 Main Section 2 . . . 6

4 Professional, Legal, Ethical and Social issues 7
- 4.1 Main Section 1 . . . 7
  - 4.1.1 Subsection 1 . . . 7
  - 4.1.2 Subsection 2 . . . 7
- 4.2 Main Section 2 . . . 8

5 Project Plan **9**
5.1 Main Section 1 9
5.1.1 Subsection 1 9
5.1.2 Subsection 2 9
5.2 Main Section 2 10

6 Conclusion **11**
6.1 Main Section 1 11
6.1.1 Subsection 1 11
6.1.2 Subsection 2 11
6.2 Main Section 2 12

A Appendix Title Here **13**

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Main Section 1

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Chapter 2

Literature Review

2.1 Background

The question of the representation of numbers as we, humans, use them in a world of electronics has been central in the creation of computers and their associated arithmetics. Several problems are contained in the simple question of: How to translate our arithmetic and number operations in a piece of hardware?

2.1.1 Number Representation

The first thing to note is that electronics can represent two states, a presence or absence of an electric impulsion. The states of "on" and "off" is embedded in transistors that can represent both. The transistor is the hardware representant of this duality while a bit is the software counter-part. This is the underlying reason of why computers, even the first fully electronical computer ENIAC - Electronical Numerical Integrator and Computer -, are using a binary system. If this system is handy to translate our base 10 arithmetic and simple numbers such as integers, it is harder to translate more complex numbers such as reals and floating point operations. The meaning of an N-bit binary word is entirely dependent of the interpretation we choose to use. This interpretation consists of both a representation (the type of the object the memory represents) as well as its associated mapping. Common number representations consists of unsigned integers, signed integers (using two's complement), floating point reals as well as fixed-point reals.

2.1.1.1 Integer Representation

The representation of integers and especially unsigned integers is straightforward as it consists of a change form base 10 to base 2. This number representation can be done in 16-bits, 32-bits or 64-bits depending on its type, the supporting hardware and the space we need to contain it. Representing a number in base 2 from base 10 or vice versa is straightforward as it only demands simple and exact basic operations to be performed.

Now, if we want to represent a signed integer, we have to use a method called the two's complement in order to bring the sign in while keeping the basic behavior of the addition to work on numbers whether they are positive or negative. The method consists in changing the value of all the bits of a given number then adding one to the result.

Those two representation allow a complete mapping of integers up to a certain range: signed 32-bits integer can represent base 10 numbers between -2,147,483,648 and 2,147,483,647 while unsigned integers can represent base 10 numbers between 0 and 4,294,967,295.

2.1.1.2 Floating-Point Representation

Representing floating-point numbers has been a concern since the 1980's and the industrial development of several computing modules and interfaces. The need for a consensus in this domain and particular applications has been answered by the IEEE-754 standard in 1985. This standard defines both the floating-point number representations and exceptions conditions along with their default handling. This norm was reviewed fondamentally in 2008, extending it to 64-bits and 128-bits length. The last dated revision of the norm is from 2019.

Floating-point numbers following this representation are composed of three distinct elements:

1. A sign bit
2. An exponent
3. A mantissa

Those three elements compose the number by using the following formula:

$$(sign)\ mantissa * 2^{exponent} \tag{2.1}$$

In order to present both positive and negative exponents and as using the two's complement on the exponent would complexify the computation of floating-point numbers, a bias is used in the exponent. This bias corresponds to

$$2^e - 1 \tag{2.2}$$

where e is the number of bits of the exponent part.

When referring to single-precision floating-point representation we are talking about 32-bit long memory representation. They are mapped as follows:

- Sign bit: 1 bit
- Exponent: 8 bits
- Mantissa: 23 bits
- Exponent Bias: 127

Referring to double precision floating-point representation means looking at 64-bit long memory representation, mapped as follows:

- Sign bit: 1 bit
- Exponent: 11 bits
- Mantissa: 52 bits
- Exponent Bias: 127

Along this representations, IEEE-754 introduces representations of special numbers such as positive and negative infinity as well as NaN and zero. Moreover, it adds methods to round floating-point numbers to positive or negative infinity, zero or to the nearest value.

2.1.1.3 Fixed-Point Representation

Another way to look at the decimals is to fix the radix point to be at a certain place and keep it thoughout all the computations and representations using this arithmetic. A fixed-point representation consists of three components:

1. A sign indicator

2. An integer corresponding to the total number of bits
3. Another integer corresponding to the size of the fractional part

Representing a number with this representation can be done by simply concatenating the base 2 representation of each side of the radix point.

As shown in the above example, several representations can depict the same decimal number. Finding the correct amount of bits to allocate to each side of the radix point is what will qualify the representation. Allocating fewer bits than needed may lead to overflow while allocating too much may increase quantisation errors. Along with this new representation comes a whole new arithmetic. While this format can help tailor your needs in terms of variable types, it comes with an additional cost. The operations performed in this arithmetic are non-trivial as addition and multiplication are not associative and distributive anymore. This means the order of the operations will have an impact on the final result. Moreover, the round-off error underlying this representation is often non-trivial to grasp. However, those operations are low demanding in terms of computing power.

2.1.2 Performance benchmarks

Floating-point representation (in either single or double precision) allows extreme precision at the cost of space in memory. On the other hand, fixed-point representation, even if it comes with a more complex arithmetic and insidious round-off errors, allows to tailor the type to your needs. If you want to store the values of the size and mass of planets in floating-point precision, you will end up not using the majority of the range of values you selected while you could tailor a correct type in fixed-point representation.

2.2 Main Section 2

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Chapter 3

Requirements Analysis

3.1 Main Section 1

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Chapter 4

Professional, Legal, Ethical and Social issues

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Chapter 5

Project Plan

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Chapter 6

Conclusion

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Appendix A

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