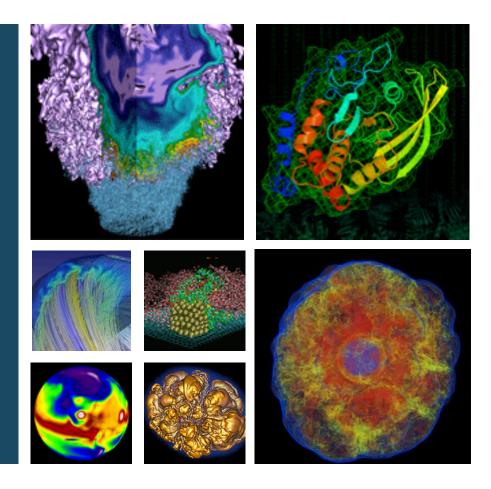
Optimizing EXX Performance on Intel Xeon Phi





Thorsten Kurth

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Xeon Phi 7250 Features



- important hardware features
 - 68 cores@1.2 Ghz, 272 threads in total
 - complicated memory topology: configurable 2D on-chip interconnect, shared L2 cache per tile
 - 512bit-wide vector units with FMA support and additional fast reduced precision intrinsics
 - 16 GB high-bandwidth on-package memory (HBM/ MCDRAM), configurable as cache, flat or hybrid cache/flat
- KNL-ready applications should exploit some of these features

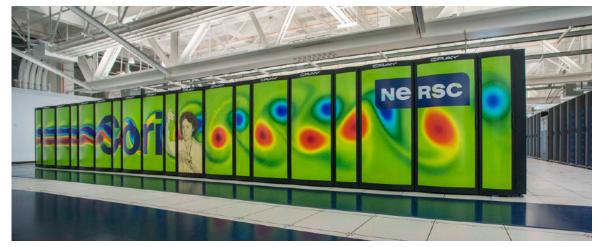




Cori System Description



- Cray XC40 supercomputer
- Phase I: 2004 Haswell nodes, 1.92 PFlops/sec
- Phase II: 9304 Xeon Phi 7250 nodes, 27.9 PFlops/sec
- Cray Aries high-speed interconnect with Dragonfly topology
- Aggregate memory: 203 TB (Phase I), 1 PB (Phase II)

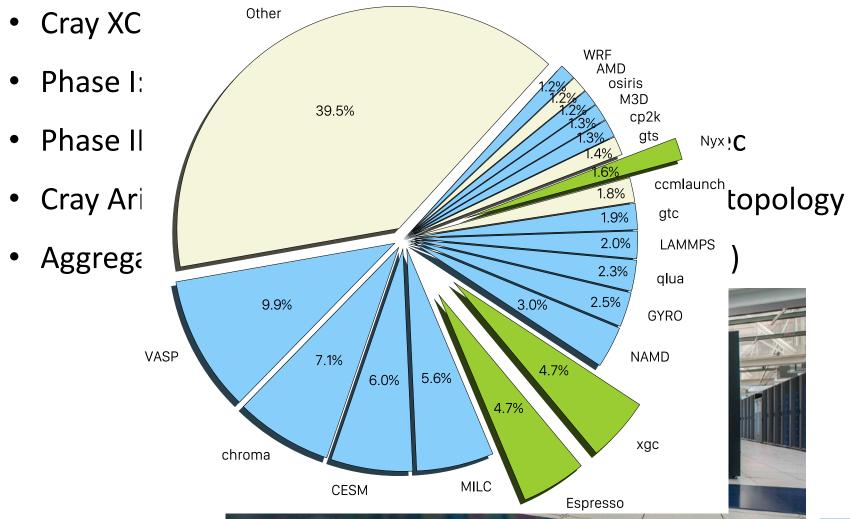






Cori System Description









Introducing OpenMP



 focus on exact-exchange calculation (vexx)

$$(\hat{K}\psi_i)(\mathbf{r}) =$$

$$-\sum_{j=1}^n \psi_j(\mathbf{r}) \int d^3r' \frac{\psi_j^*(\mathbf{r}')\psi_i(\mathbf{r}')}{|\mathbf{r} - \mathbf{r}'|}$$

```
1: procedure VEXX

2: ...

3: for i in 1:n do

4: ...

5: c(\mathbf{g}) = \text{FFT}[1/|\mathbf{r}' - \mathbf{r}|]

6: for j in 1:n do

7: \rho_{ij}(\mathbf{r}) = \psi_j^*(\mathbf{r})\psi_i(\mathbf{r})

8: \rho_{ij}(\mathbf{g}) = \text{FFT}[\rho_{ij}(\mathbf{r})]

9: v_{ij}(\mathbf{g}) = c(\mathbf{g})\rho_{ij}(\mathbf{g})

10: v_{ij}(\mathbf{r}) = \text{FFT}^{-1}[v_{ij}(\mathbf{g})]

11: (\hat{K}\psi_i)(\mathbf{r}) += \psi_j(\mathbf{r})v_{ij}(\mathbf{r})
```





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 first step: use OpenMP do speed-up scalar-products

```
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```

```
D0 j=1, n

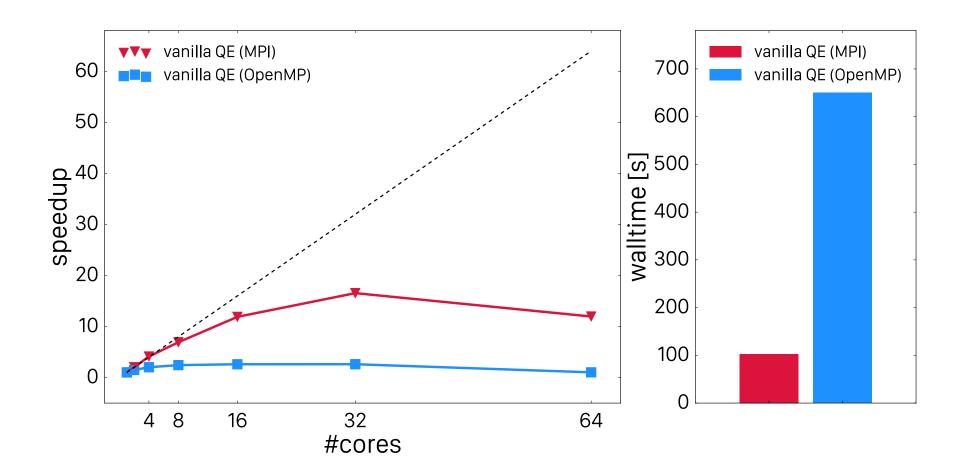
!$omp parallel do ...
    D0 ir=1, nr
        rho(ir,j)=conjg(psi(ir,j))
        * psi(ir,i)

ENDDO
!$omp end parallel do
...
ENDDO
```



Baseline Results (16 H₂0)









Reduce Fork-Join Operations



move OpenMP into the outer loops to create enough work

for threads

```
DO j=1:n
      DO ir=1:nr
     ENDDO
     FFT[...]
      DO ir=1:nr
     ENDDO
     IFFT[...]
ENDDO
```

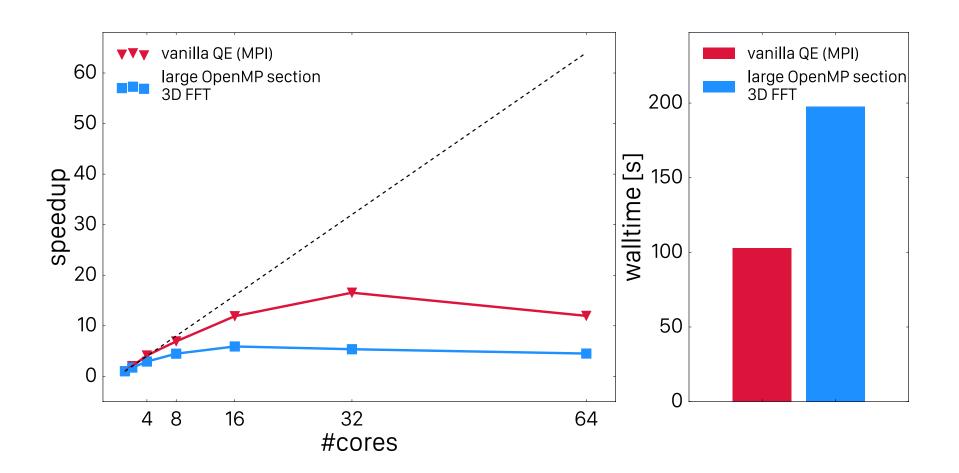


```
DO j=1:n
      DO ir=1:nr
      ENDDO
ENDDO
DO j=1:n
      FFT3D[...]
ENDDO
DO j=1:n
      DO ir=1:nr
      ENDDO
ENDDO
DO j=1:n
      IFFT3D[...]
ENDDO
DO j=1:n
ENDDO
```



Large OpenMP Sections (16 H₂0)









Tile Loops



• problem: with collapse(2), many scatter-gather instructions generated although data access is contiguous (compiler bug?)





Tile Loops



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- solution: manual blocking/tiling





Tile Loops



- problem: with collapse(2), many scatter-gather instructions generated although data access is contiguous (compiler bug?)
- solution: manual blocking/tiling

```
nblock = 2048
nrt = nr / nblock
!$omp parallel do collapse(2)...
D0 ist = 1, nrt
        D0 j=1, n
            ir_start = (irt - 1) * nblock + 1
            ir_end = min(ir_start+nblock-1,nr)
            D0 ir = ir_start, it_end
                  rho(ir,j)=conjg(psi(ir,j)) * psi(ir,i)
            ENDD0
        ENDD0
ENDD0
!$omp end parallel do
```

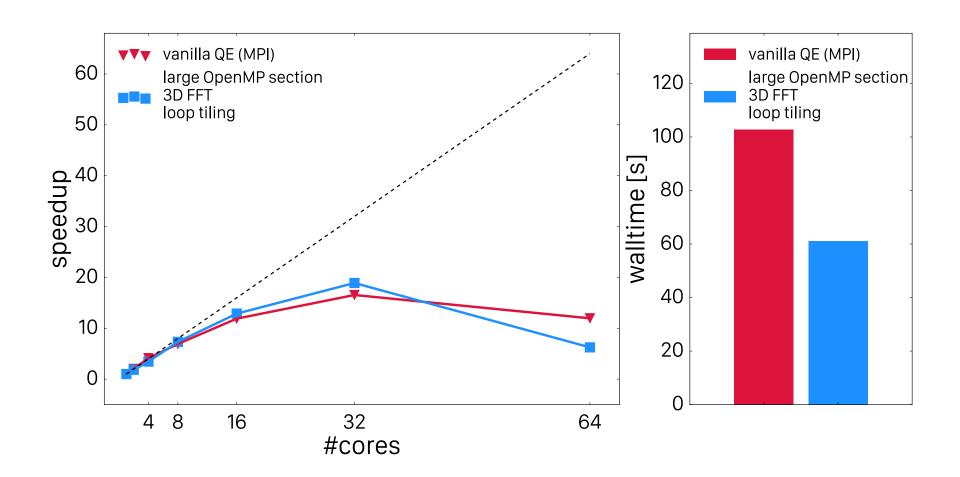
 future improvement: factor these routines into subroutines to hide code complexity





Large Sections + Tiling (16 H₂0)





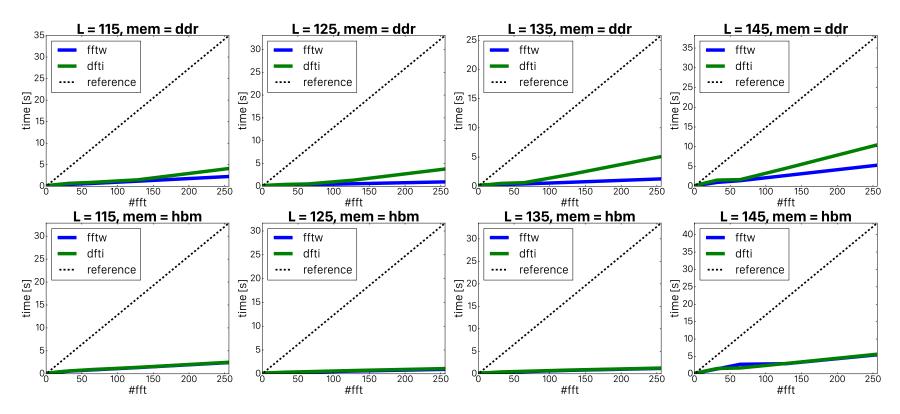




Batch-Process FFTs



pool FFTs in order to perform multiple at once (reorganize:
 3D FFTs can be performed locally)

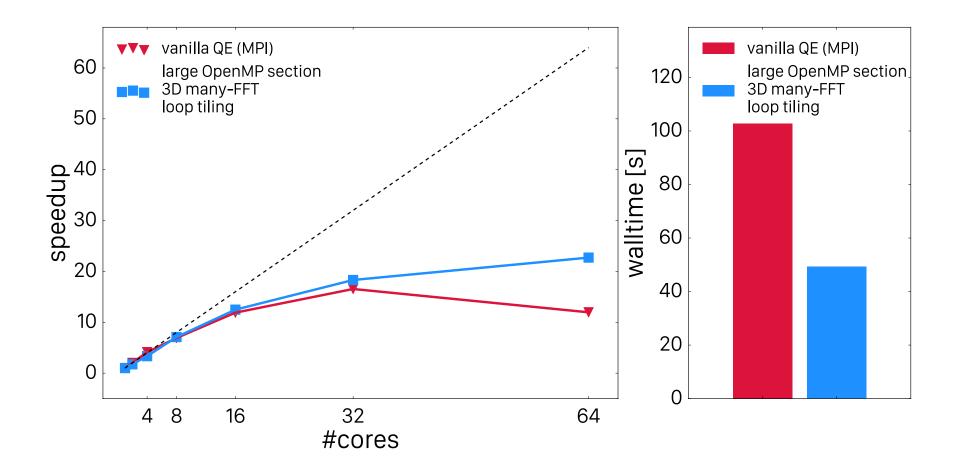






Large Sections + Tiling + FFT-Batching (16 H₂0) Nersc









Summary



- improved code shows significant better OpenMP scaling (effect bigger for bigger systems)
- outperforms all-MPI mode
- EXX part is now subdominant, especially when ACE is used
- need to work on the PBE part, especially the diagonalization







Thank you



