

# SpiNNaker

Universal Spiking Neural Network Architecture

SpiNNaker Application Programming Interface  
version 0.0  
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## About this Document

### Background

SpiNNaker was designed at the University of Manchester within an EPSRC-funded project in collaboration with the University of Southampton, ARM Limited and Silistix Limited. Subsequent development took place within a second EPSRC-funded project which added the universities of Cambridge and Sheffield to the collaboration. The work would not have been possible without EPSRC funding, and the support of the EPSRC and the industrial partners is gratefully acknowledged.

### Intellectual Property rights

All rights to the SpiNNaker design and its associated software are the property of the University of Manchester with the exception of those rights that accrue to the project partners in accordance with the contract terms.

### Disclaimer

The details in this design document are presented in good faith but no liability can be accepted for errors or inaccuracies. The design of a complex chip multiprocessor and its associated software is a research activity where there are many uncertainties to be faced, and there is no guarantee that a SpiNNaker system will perform in accordance with the specifications presented here.

The APT group in the School of Computer Science at the University of Manchester was responsible for all of the architectural and logic design of the SpiNNaker chip, with the exception of synthesizable components supplied by ARM Limited and interconnect components supplied by Silistix Limited. All design verification was also carried out by the APT group. As such the industrial project partners bear no responsibility for the correct functioning of the device.

### Error notification and feedback

Please email details of any errors, omissions, or suggestions for improvement to Steve Furber <steve.furber@manchester.ac.uk>

### Change history

version	date	changes
0.0	20/05/2011	Initial draft

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## Application programming interface (API)

### 0.1 Event-driven programming model

The SpiNNaker Programming Model (PM) is a simple, event-driven model. Applications do not control execution flow, they can only indicate the functions, referred to as callbacks, to be executed when specific events occur, such as the arrival of a packet, the completion of a Direct Memory Access (DMA) transfer or the lapse of a periodic time interval. An Application Run-time Kernel (ARK) controls the flow of execution and schedules/dispatches application callback functions when appropriate.

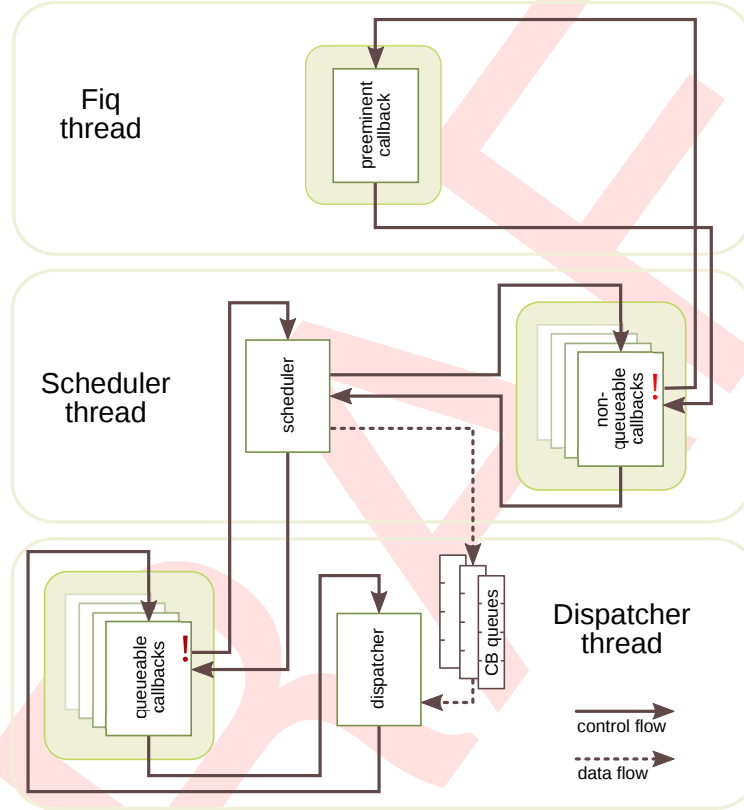


Figure 1: SpiNNaker event-driven programming framework.

Fig. 1 shows the basic architecture of the event-driven framework. Application developers write callback routines that are associated with events of interest and register them at a certain priority with the kernel. When the corresponding event occurs the scheduler either executes the callback immediately and atomically (in the case of a non-queueable callback) or places it into a scheduling queue at a position according to its priority (in case of a queueable callback). When control is returned to the dispatcher (following the completion of a callback) the highest-priority queueable callback is executed. Queueable callbacks do not necessarily execute atomically: they may be pre-empted by non-queueable callbacks if a corresponding event occurs during their execution. The dispatcher goes to sleep (low-power consumption state) if the pending callback queues are empty and will be awakened by an event. Application developers can designate one non-queueable callback as the preminent callback, which has the highest priority and can pre-empt other non-queueable callbacks as well as all queueable ones.

The preminent callback is associated with a FIQ interrupt while other non-queueable callbacks are associated with IRQ interrupts. The API provides different functions to

disable interrupts: `spin1_irq_disable` disables IRQs, `spin1_fiq_disable` disables FIQs while `spin1_int_disable` disables both FIQs and IRQs. The use of `spin1_fiq_disable` may lead to priority inversion.

### 0.1.1 Design considerations

- Non-queueable callbacks are available as a method of pre-empting long running tasks with short, high priority tasks. The allocation of application tasks to non-queueable callbacks must be carefully considered. The selection of the preeminent callback can be particularly important. Long-running operations should not be executed in non-queueable callbacks for fear of starving queueable callbacks.
- Queueable callbacks may require critical sections (*i.e.*, sections that are completed atomically) to prevent pre-emption during access to shared resources. Critical sections may be achieved by disabling interrupts before accessing the shared resource and re-enabling them afterwards. Applications are executed in a privileged mode to allow the callback programmer to insert these critical sections. This approach has the risk that it allows the programmer to modify peripherals –such as the system controller– unchecked.
- Non-queueable callbacks may also require critical sections, as they can be pre-empted by the preeminent callback.
- Events –usually triggered by interrupts– have priority determined by the programming of the Vectored Interrupt Controller (VIC). This allows priority to be determined when multiple events corresponding to different non-queueable callbacks occur concurrently. It also affects the order in which queueable callbacks of the same priority are queued.

## 0.2 Programming interface

The following sections introduce the events and functions supported by the API.

### 0.2.1 Events

The SpiNNaker PM is event-driven: all computation follows from some event. The following events are available to the application:

event	trigger
<b>MC packet received</b>	reception of a multicast packet
<b>DMA transfer done</b>	successful completion of a DMA transfer
<b>Timer tick</b>	passage of specified period of time
<b>SDP packet received</b>	reception of a SpiNNaker Datagram Protocol packet
<b>User event</b>	software-triggered interrupt

In addition, errors can also generate events:

— events not yet supported —	
event	trigger
<b>MCP parity error</b>	multicast packet received with wrong parity
<b>MCP framing error</b>	wrongly framed multicast packet received
<b>DMA transfer error</b>	unsuccessful completion of a DMA transfer
<b>DMA transfer timeout</b>	DMA transfer is taking too long

Each of these events is handled by a kernel routine which may schedule or execute an application callback, if one is registered by the application.

### 0.2.2 Callback arguments

Callbacks are functions with two unsigned integer arguments (which may be NULL) and no return value. The arguments may be cast into the appropriate types by the callback. The arguments provided to callbacks (where 'none' denotes a superfluous argument) by each event are:

event	first argument	second argument
MC packet received	uint key	uint payload
DMA transfer done	uint transfer_ID	uint tag
Timer tick	uint simulation_time	uint none
SDP packet received	uint *mailbox	uint destination_port
User event	uint arg0	uint arg1

### 0.2.3 Pre-defined constants

logic value	value	keyword
true	(0 == 0)	TRUE
false	(0 != 0)	FALSE

function result	value	keyword
failure	0	FAILURE
success	1	SUCCESS

transfer direction	value	keyword
read (system to TCM)	0	DMA_READ
write (TCM to system)	1	DMA_WRITE

packet payload	value	keyword
no payload	0	NO_PAYLOAD
payload present	1	WITH_PAYLOAD

event	value	keyword
MC packet received	0	MC_PACKET_RECEIVED
DMA transfer done	1	DMA_TRANSFER_DONE
Timer tick	2	TIMER_TICK
SDP packet received	3	SDP_PACKET_RX
User event	4	USER_EVENT

## 0.2.4 Pre-defined types

type	value	size
<b>uint</b>	unsigned int	32 bits
<b>ushort</b>	unsigned short	16 bits
<b>uchar</b>	unsigned char	8 bits
<b>callback_t</b>	void (*callback_t) (uint, uint)	32 bits
<b>sdp_msg_t</b>	struct (see below)	292 bytes
<b>diagnostics_t</b>	struct (see below)	44 bytes

## SDP message structure

```

typedef struct sdp_msg      // SDP message (=292 bytes)
{
    struct sdp_msg *next;    // Next in free list
    ushort length;          // length
    ushort checksum;        // checksum (if used)

    // sdp_hdr_t

    uchar flags;            // SDP flag byte
    uchar tag;              // SDP IPtag
    uchar dest_port;        // SDP destination port
    uchar srce_port;        // SDP source port
    ushort dest_addr;       // SDP destination address
    ushort srce_addr;       // SDP source address

    // cmd_hdr_t (optional)

    ushort cmd_rc;          // Command/Return Code
    ushort seq;             // Sequence number
    uint arg1;              // Arg 1
    uint arg2;              // Arg 2
    uint arg3;              // Arg 3

    // user data (optional)

    uchar data[SDP_BUF_SIZE]; // User data (256 bytes)

    uint _PAD;              // Private padding
} sdp_msg_t;

```

## diagnostics variable structure

```

typedef struct
{
    uint exit_code;          // simulation exit code
    uint warnings;          // warnings type bit map
    uint total_mc_packets;   // total routed MC packets during simulation
    uint dumped_mc_packets; // total dumped MC packets by the router
    uint discarded_mc_packets; // total discarded MC packets by API
    uint dma_transfers;     // total DMA transfers requested
    uint dma_bursts;        // total DMA bursts completed
    uint dma_queue_full;    // dma queue full count
    uint task_queue_full;   // task queue full count
    uint tx_packet_queue_full; // transmitter packet queue full count
    uint writeBack_errors;  // write-back buffer error count
} diagnostics_t;

```

### 0.2.5 Pre-declared variables

variable	type	function
leadAp	uchar	TRUE if appointed chip-wise application leader
diagnostics	diagnostics_t	returns diagnostic information (if turned on in compilation)

### 0.2.6 Kernel services

The kernel provides a number of services to the application programmer:

#### Simulation control functions

Start simulation		
function	arguments	description
uint spin1_start	void	no arguments
<b>returns:</b> EXIT_CODE (0 = NO ERRORS)		
<b>notes:</b> <ul style="list-style-type: none"> <li>transfers control from the application to the ARK.</li> <li>use spin1.kill to indicate a non-zero EXIT_CODE.</li> </ul>		

Stop simulation		
function	arguments	description
void spin1_stop	void	no arguments
<b>returns:</b> no return value		
<b>notes:</b> <ul style="list-style-type: none"> <li>transfers control from the ARK back to the application.</li> </ul>		

Stop simulation and report error		
function	arguments	description
void spin1_kill	uint error	error code to report
<b>returns:</b> no return value		
<b>notes:</b> <ul style="list-style-type: none"> <li>transfers control from the ARK back to the application.</li> <li>The argument is used as the return value for spin1_start.</li> </ul>		

Set the timer tick period		
function	arguments	description
void spin1_set_timer_tick	uint period	timer tick period (in microseconds)
<b>returns:</b> no return value		

Request simulation time		
function	arguments	description
uint spin1_get_simulation_time	void	no arguments
<b>returns:</b> timer ticks since the start of simulation.		



DEPRECATED!	Indicate which cores are involved in the simulation	
function	arguments	description
<b>void spin1_set_core_map</b>	uint chips	number of chips
	uint * core_map	bit map array of cores
<b>returns:</b> no return value		
<b>notes:</b> <ul style="list-style-type: none"> <li>• sets the map of the cores that need to synchronise to start the simulation.</li> <li>• the numbers of chips &amp; cores default to 1, thus no synchronisation is attempted.</li> </ul>		

### Core Map Examples

```
// chips are identified using Cartesian coordinates.
// Note that the core map is a uni-dimensional array but
// describes a bi-dimensional array of chips in x-major format
// i.e., the order is (0, 0), (0, 1), ... , (1, 0), (1, 1), ...

// 2 x 2 core map on SpiNN-2, SpiNN-3 and SpiNN-4 boards - 2 cores on each chip
uint const NUMBER_OF_CHIPS = 4; // virtual 2 x 2 array of chips
uint core_map[NUMBER_OF_CHIPS] =
{
    0x6,      0x6,      // (0, 0), (0, 1)
    0x6,      0x6      // (1, 0), (1, 1)
};

// "hexagonal" 8 x 8 core map on SpiNN-4 board - 16 cores on each chip
uint const NUMBER_OF_CHIPS = 64; // virtual 8 x 8 array of chips
uint core_map[NUMBER_OF_CHIPS] =
{
    0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0, 0, 0, 0,
    0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0, 0, 0,
    0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0, 0,
    0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0,
    0, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe,
    0, 0, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe,
    0, 0, 0, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe,
};

// "notched" 5 x 5 core map on SpiNN-4 board - variable number of cores
uint const NUMBER_OF_CHIPS = 64; // virtual 8 x 8 array of chips
uint core_map[NUMBER_OF_CHIPS] =
{
    6,      6,      2,      2,      0,      0,      0,      0,
    6,      6,      2,      2,      2,      0,      0,      0,
    6,      6,      2,      2,      2,      0,      0,      0,
    2,      2,      6,      2,      2,      0,      0,      0,
    2,      2,      2,      2,      2,      0,      0,      0,
    0,      0,      0,      0,      0,      0,      0,      0,
    0,      0,      0,      0,      0,      0,      0,      0,
    0,      0,      0,      0,      0,      0,      0,      0
};

// NOTE: core maps with "holes" may not synchronise in the current version.
// INCORRECT 8 x 8 core map on SpiNN-4 board - 7 cores on each chip
uint const NUMBER_OF_CHIPS = 64; // virtual 8 x 8 array of chips
uint core_map[NUMBER_OF_CHIPS] =
{
    0xfe, 0xfe, 0xfe, 0xfe, 0, 0, 0, 0,
    0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0, 0, 0,
    0, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0, 0,
    0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0,
    0, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe,
    0, 0, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe,
    0, 0, 0, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe
};
```

Indicate which cores are involved in the simulation		
function	arguments	description
<b>void spin1_application_core_map</b>	uint xchips	map x dimension
	uint ychips	map y dimension
	uint * core_map	bit map array of cores
<b>returns:</b> no return value		
<b>notes:</b> <ul style="list-style-type: none"> <li>• sets the map of the cores that need to synchronise to start the simulation.</li> <li>• the numbers of chips &amp; cores default to 1, thus no synchronisation is attempted.</li> </ul>		

### Core Map Examples

```
// chips are identified using Cartesian coordinates.

// 2 x 2 core map on SpiNN-2, SpiNN-3 and SpiNN-4 boards - 2 cores on each chip
uint const NUMBER_OF_XCHIPS = 2; // virtual 2 x 2 array of chips
uint const NUMBER_OF_YCHIPS = 2;
uint core_map[NUMBER_OF_XCHIPS][NUMBER_OF_YCHIPS] =
{
    {0x6,    0x6}, // (0, 0), (0, 1)
    {0x6,    0x6} // (1, 0), (1, 1)
};

// "hexagonal" 8 x 8 core map on SpiNN-4 board - 16 cores on each chip
uint const NUMBER_OF_XCHIPS = 8; // virtual 8 x 8 array of chips
uint const NUMBER_OF_YCHIPS = 8;
uint core_map[NUMBER_OF_XCHIPS][NUMBER_OF_YCHIPS] =
{
    {0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0,    0,    0,    0},
    {0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0,    0,    0},
    {0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0,    0},
    {0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0},
    {0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe},
    {0,    0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe},
    {0,    0,    0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe},
    {0,    0,    0,    0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe, 0x1ffe}
};

// "notched" 4 x 5 core map on SpiNN-4 board - variable number of cores
uint const NUMBER_OF_XCHIPS = 4; // virtual 4 x 5 array of chips
uint const NUMBER_OF_YCHIPS = 5;
uint core_map[NUMBER_OF_XCHIPS][NUMBER_OF_YCHIPS] =
{
    {6,    6,    2,    2,    O},
    {6,    6,    2,    2,    2},
    {6,    6,    2,    2,    2},
    {2,    2,    2,    2,    2}
};

// NOTE: core maps with "holes" may not synchronise in the current version.
// INCORRECT 6 x 7 core map on SpiNN-4 board - 7 cores on each chip
uint const NUMBER_OF_XCHIPS = 6; // virtual 6 x 7 array of chips
uint const NUMBER_OF_YCHIPS = 7;
uint core_map[NUMBER_OF_XCHIPS][NUMBER_OF_YCHIPS] =
{
    {0xfe, 0xfe, 0xfe, 0xfe, 0,    0,    0},
    {0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0,    0},
    {O,    0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0},
    {0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe},
    {0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe},
    {0,    0xfe, 0xfe, 0xfe, 0xfe, 0xfe, 0xfe}
};
```

## Event management functions

Register <b>callback</b> to be executed when <b>event_id</b> occurs		
function	arguments	description
<b>void spin1_callback_on</b>	uint event_id	event that triggers callback
	callback_t callback	callback function pointer
	uint priority	priority <0 denotes preeminent priority 0 denotes non-queueable priorities >0 denote queueable

**returns:** no return value

- notes:**
- a callback registration overrides any previous ones for the same event.
  - only one callback can be registered as preeminent.
  - a second preeminent registration is demoted to non-queueable.

Deregister <b>callback</b> from <b>event_id</b>		
function	arguments	description
<b>void spin1_callback_off</b>	uint event_id	event that triggers callback
<b>returns:</b> no return value		

Schedule a <b>callback</b> for execution with given <b>priority</b>		
function	arguments	description
<b>uint spin1_schedule_callback</b>	callback_t callback	callback function pointer
	uint arg0	callback argument
	uint arg1	callback argument
	uint priority	callback priority
<b>returns:</b> SUCCESS (=1) / FAILURE (=0)		
<b>notes:</b> <ul style="list-style-type: none"> <li>• this function allows the application to schedule a callback without an event.</li> <li>• priority &lt;= 0 must not be used (unpredictable results).</li> <li>• function arguments are not validated.</li> </ul>		

Trigger a <b>user event</b>		
function	arguments	description
<b>uint spin1_trigger_user_event</b>	uint arg0	callback argument
	uint arg1	callback argument
<b>returns:</b> SUCCESS (=1) / FAILURE (=0)		
<b>notes:</b> <ul style="list-style-type: none"> <li>• FAILURE indicates a trigger attempt before a previous one has been serviced.</li> <li>• arg0 and arg1 will be passed as arguments to the registered callback.</li> <li>• function arguments are not validated.</li> </ul>		

## Data transfer functions

Request a DMA transfer		
function	arguments	description
<b>uint spin1_dma_transfer</b>	uint tag void *system_address void *tcm_address uint direction uint length	for application use address in system NoC address in TCM DMA_READ / DMA_WRITE transfer length (in bytes)
<b>returns:</b> unique transfer identification number (TID)		
<b>notes:</b> <ul style="list-style-type: none"> <li>• completion of the transfer generates a DMA transfer done event.</li> <li>• a registered callback can use TID and tag to identify the completed request.</li> <li>• DMA transfers are completed in the order in which they are requested.</li> <li>• TID = FAILURE (= 0) indicates failure to schedule the transfer.</li> <li>• function arguments are not validated.</li> <li>• may cause DMA error or DMA timeout events.</li> </ul>		
Copy a block of memory		
function	arguments	description
<b>void spin1_memcpy</b>	void *dst void const *src uint len	destination address source address transfer length (in bytes)
<b>returns:</b> no return value		
<b>notes:</b> <ul style="list-style-type: none"> <li>• function arguments are not validated.</li> <li>• may cause a data abort.</li> </ul>		

## Communications functions

Send a multicast packet		
function	arguments	description
uint spin1_send_mc_packet	uint key	packet key
	uint data	packet payload
	uint load	1 = payload present / 0 = no payload
<b>returns:</b> SUCCESS (=1) / FAILURE (=0)		

Flush software outgoing multicast packet queue		
function	arguments	description
uint spin1_flush_tx_packet_queue	void	no arguments
<b>returns:</b> SUCCESS (=1) / FAILURE (=0)		
<b>notes:</b> • queued packets are thrown away (not sent).		

Flush software incoming multicast packet queue		
function	arguments	description
uint spin1_flush_rx_packet_queue	void	no arguments
<b>returns:</b> SUCCESS (=1) / FAILURE (=0)		
<b>notes:</b> • queued packets are thrown away.		

### SpiNNaker Datagram Protocol (SDP)

Send an SDP message		
function	arguments	description
<b>uint spin1_send_sdp_msg</b>	sdp_msg_t * msg uint timeout	pointer to message transmission timeout
<b>returns:</b> SUCCESS (=1) / FAILURE (=0)		
Request a free SDP message container		
function	arguments	description
<b>sdp_msg_t * spin1_msg_get</b>	void	no arguments
<b>returns:</b> pointer to message (NULL if unsuccessful)		
Free an SDP message container		
function	arguments	description
<b>void spin1_msg_free</b>	sdp_msg_t *msg	pointer to message
<b>returns:</b> no return value		

## Critical section support functions

Disable IRQ interrupts		
function	arguments	description
uint spin1_irq_disable	void	no arguments
<b>returns:</b>		contents of CPSR before interrupt flags altered.
Disable FIQ interrupts		
function	arguments	description
uint spin1_fiq_disable	void	no arguments
<b>returns:</b>		contents of CPSR before interrupt flags altered.
Disable ALL interrupts		
function	arguments	description
uint spin1_int_disable	void	no arguments
<b>returns:</b>		contents of CPSR before interrupt flags altered.
Restore core mode and interrupt state		
function	arguments	description
void spin1_mode_restore	uint status	CPSR state to be restored
<b>returns:</b>		no return value.

# System resources access functions

Get core ID		
function	arguments	description
uint spin1_get_core_id	void	no arguments
<b>returns:</b> core ID in bits [4:0].		

Get chip ID		
function	arguments	description
uint spin1_get_chip_id	void	no arguments
<b>returns:</b> chip ID in bits [15:0].		
<b>notes:</b> • chip ID contains x coordinate in bits [15:8], y coordinate in bits [7:0].		

Get ID		
function	arguments	description
uint spin1_get_id	void	no arguments
<b>returns:</b> chip ID in bits [20:5] / core ID in bits [4:0].		

Control state of board LEDs		
function	arguments	description
void spin1_led_control	uint p	new state for board LEDs
<b>returns:</b> no return value.		
<b>notes:</b> • the number of LEDs and their colour varies according to board version. • to turn LEDs 0 and 1 on: spin1_led_control (LED_ON (0) + LED_ON (1)) • to invert LED 2: spin1_led_control (LED_INV (2)) • to turn LED 0 off: spin1_led_control (LED_OFF (0))		

Set up a multicast routing table entry		
function	arguments	description
uint spin1_set_mc_table_entry	uint entry	table entry
	uint key	entry routing key field
	uint mask	entry mask field
	uint route	entry route field
<b>returns:</b> SUCCESS (=1) / FAILURE (=0).		
<b>notes:</b> • see SpiNNaker datasheet for details of the MC table operation. • entries 0 to 999 are available to the application. • routing keys with <b>bit[15] = 1 and bit[10] = 0</b> are reserved. • function arguments are not validated.		



## Memory allocation

Allocate a new block of DTCM		
function	arguments	description
<b>void * spin1_malloc</b>	uint bytes	size of the memory block in bytes
<b>returns:</b> pointer to the new memory block.		
<b>notes:</b> <ul style="list-style-type: none"><li>• memory blocks are word-aligned.</li><li>• memory is allocated in DTCM.</li><li>• there is no support for freeing a memory block.</li></ul>		

## Miscellaneous

Wait for a given time		
function	arguments	description
<b>void spin1_delay_us</b>	uint time	wait time (in microseconds)
<b>returns:</b> no return value		
<b>notes:</b> <ul style="list-style-type: none"> <li>• the function busy waits for the given time (in microseconds).</li> <li>• prevents any queueable callbacks from executing (use with care).</li> </ul>		
Generate a 32-bit pseudo-random number		
function	arguments	description
<b>void spin1_rand</b>	void	no arguments
<b>returns:</b> 32-bit pseudo-random number		
<b>notes:</b> <ul style="list-style-type: none"> <li>• Function based on example function in:</li> <li>• "Programming Techniques", ARM document ARM DUI 0021A.</li> <li>• Uses a 33-bit shift register with exclusive-or feedback taps at bits 33 and 20.</li> </ul>		
Provide a seed to the pseudo-random number generator		
function	arguments	description
<b>void spin1_srand</b>	uint seed	32-bit seed
<b>returns:</b> no return value		

### 0.2.7 Application Programme Structure

In general, an application programme contains three basic sections:

- **Application Functions:** General application functions to support the callbacks.
- **Application Callbacks:** Functions to be associated with run-time events.
- **Application Main Function:** Variable initialisation, callback registration and transfer of control to main loop.

The structure of a simple application programme is shown on the next page. Many details are left out for brevity.

```
// declare application types and variables
neuron_state state[1000];
spike_bin bins[1000][16];
. . .

/* ----- */
/* ----- application functions ----- */
/* ----- */
void izhikevich_update(neuron_state *state){
    . . .
    spin1_send_mc_packet(key, 0, NOPAYLOAD);
    . . .
}

syn_row_addr lookup_synapse_row(neuron_key key)
{
    . . .
}

void bin_spike(neuron_key key, axn_delay delay, syn_weight weight)
{
    . . .
}

/* ----- */
/* ----- application callbacks ----- */
/* ----- */
void update_neurons()
{
    . . .
    if (spin1_get_simulation_time() > 1000) // simulation time in "ticks"
        spin1_stop();
    else
        for (i=0; i < 1000; i++) izhikevich_update(state[i]);
    . . .
}

void process_spike(uint key, uint payload)
{
    . . .
    row_addr = lookup_synapses(key);
    tid = spin1_dma_transfer(tag, row_addr, syn_buffer, READ, row_len);
    . . .
}

void schedule_spike()
{
    . . .
    bin_spike(key, delay, weight);
    . . .
}

/* ----- */
/* ----- application main ----- */
/* ----- */
void c_main()
{
    // initialise variables and timer tick
    . . .
    spin1_set_timer_tick(1000); // timer tick period in microseconds
    . . .
    // register callbacks
    spin1_callback_on(TIMER_TICK, update_neurons, 1);
    spin1_callback_on(MCPACKET_RECEIVED, process_spike, 0);
    spin1_callback_on(DMA_TRANSFER_DONE, schedule_spike, 0);
    . . .
    // transfer control to the run-time kernel
    spin1_start();
    // control returns here on execution of spin1_stop()
}

```