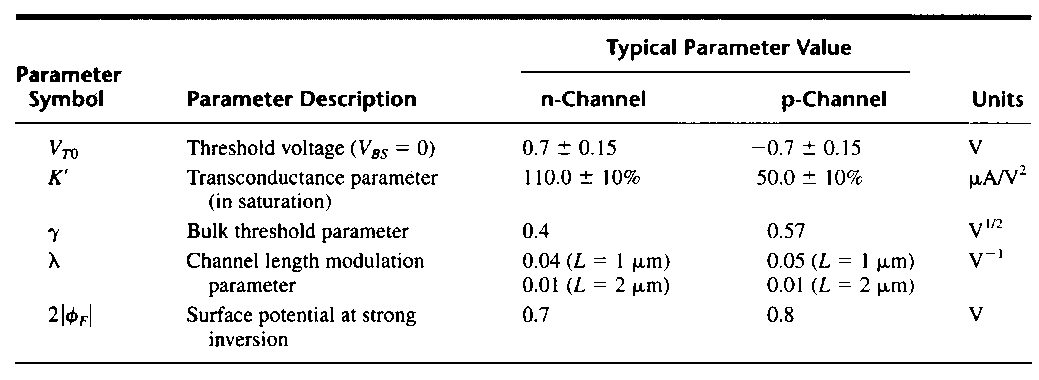
|  |  |  |
| --- | --- | --- |
| 浙江大学电气工程学院 | **模拟与数模混合集成电路** | 吴晓波，赵梦恋 |
| 2018-2019学年夏学期 | 2018年5月 |

Table 4.1



* 1. An active resistive voltage divider was shown in Figure 4.1. If VDD=5V, VSS=0V, VOUT=2.5V, I=15μA, using model parameters in Table 4.1, determine the W/L ratio of M1 and M2. Assume λ=0.

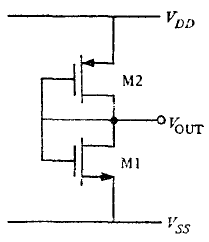


Figure 4.1

Solution:

* 1. Determine the current *I* in Figure 4.2 and calculate its TC (Temperature Coefficient) using CN20 process shown in Table 4.2. Neglect oxide encroachment and assume that M5 is operating in the saturation region. All unlabeled n-channels are 15/5 and all unlabeled p-channels are 70/5. Assume Resistor *R* is polysilicon and has a temperature coefficient of 1500ppm/℃, threshold voltage *V*T has a temperature coefficient of .

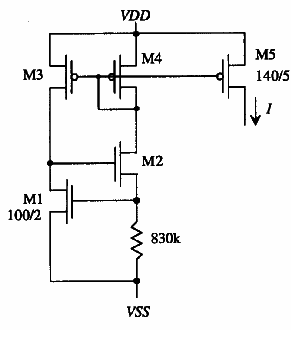
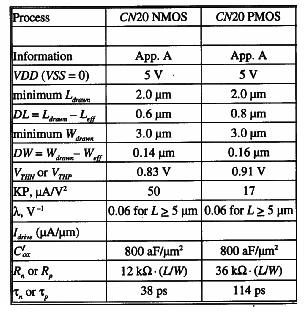


Figure 4.2

Table 4.2



Solution:

Using CMOS20 NMOS model, since ,



The more accurate solution can be derived as









where



.

thus



* 1. Figure 4.3 illustrates various ways to implement the layout of a resistor divider. Choose the layout that **best** achieves the goal of a 2:1 ratio. Explain why the other choices are not optimal.

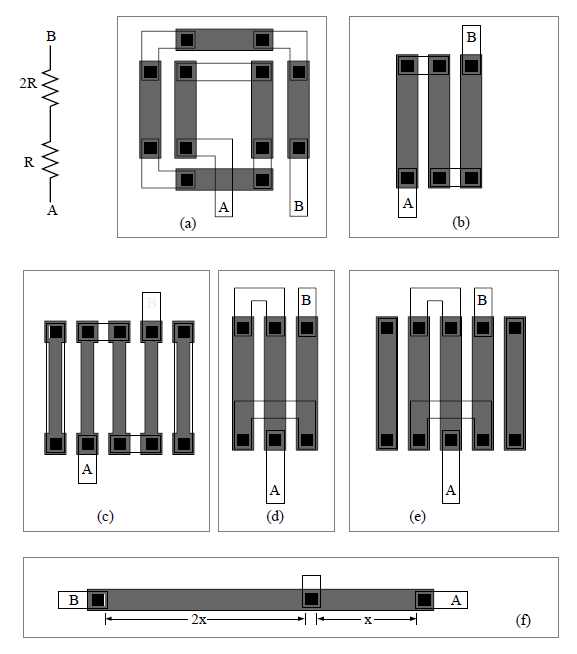


Figure 4.3

**Solution:**

Option A suffers the following:

- Orientation of the 2R resistor is partly orthogonal to the 1R resistor. Matched resistors should have the same orientation.

- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.

Option B suffers the following:

- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.

* Resistors do not share a common centroid as they should.

Option C suffers the following:

- Resistors do not share a common centroid as they should.

- Uncertainty is introduced with the additional notch at the contact head.

Option D suffers the following:

- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.

Option E suffers the following:

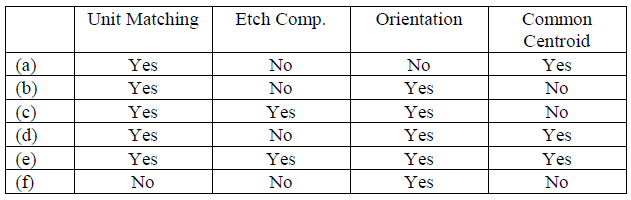
- Nothing

Option F suffers the following:

- Violates the unit-matching principle

- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.

- Resistors do not share a common centroid as they should.



Clearly, option (e) is the best choice.

* 1. Determine Vref (Output Voltage) in Fig 4.4 and the conditions under which the TC of Vref is zero. Assume K=10.

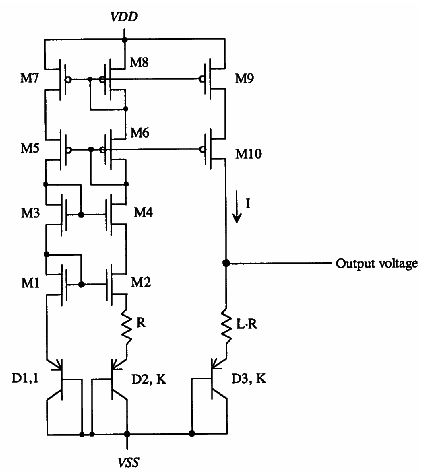


Figure 4.4

解：

For the circuit in Fig 6.1, we get

.

*V*ref is dependent on temperature and we get



 and 

Let *V*ref has zero temperature coefficient and get



It can be derived that while *L·lnK*=2/0.085=23.5，, or .

Assuming *K*=10，the corresponding *L*＝10.2≈10

Under these conditions the *Vref* that has zero TC is

* 1. Derive an expression for Iout in Fig 4.5. Assume all transistors are in saturation region, and (W/L)4=(W/L)3, λ=0.



Figure 4.5

解：



解得：



* 1. The circuit of Fig 4.6 is designed with R3=1kΩ, and a current of 50μA through it. Calculate R1 and n for a zero TC. Assume R1=R2.



Figure 4.6

解：







解得：，