Quiz 4
CMPE 364
Spring 2017

Name:
Student ID:

1. Consider the following ARM assembly code:

```
ldrb r1, [r4]
add r1, r1, #5
sub r2, r3, r8
```

Fill in the following table showing the pipeline contents during each cycle. The first two cycles have been done for you:

Cycle	**Fetch**	**Decode**	**ALU**	**LS1**	**LS2**
1	ldrb				
2	add	ldrb			
3	sub	add	ldrb		
4		sub	add	ldrb	
5			add		ldrb
6			add		
7			sub		

2. Re-order the instructions to minimize the stalls, but still accomplish the same functionality:

```
ldrb r1, [r4]
sub r2, r3, r8
add r1, r1, #5
```

Fill in the table again for the re-ordered instructions:

Cycle	**Fetch**	**Decode**	**ALU**	**LS1**	**LS2**
1	ldrb				
2	sub	ldrb			
3	add	sub	ldrb		
4		add	sub	ldrb	
5			add		ldrb
6			add		