

CM5_GPIO.SchDoc

Status: **Released**
 Variant: **MFG**
 Revision: **1.0**
 Version: **1.0**

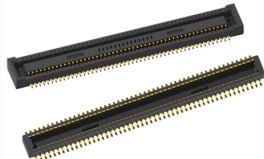
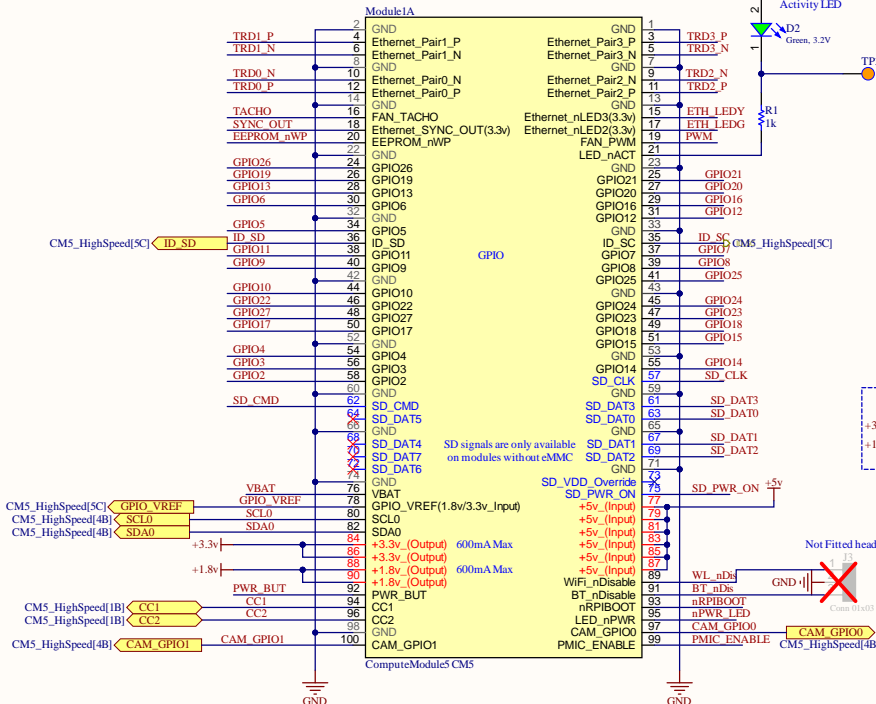
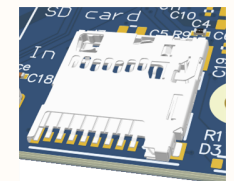
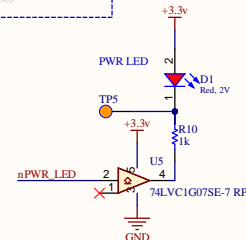
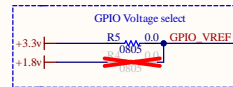
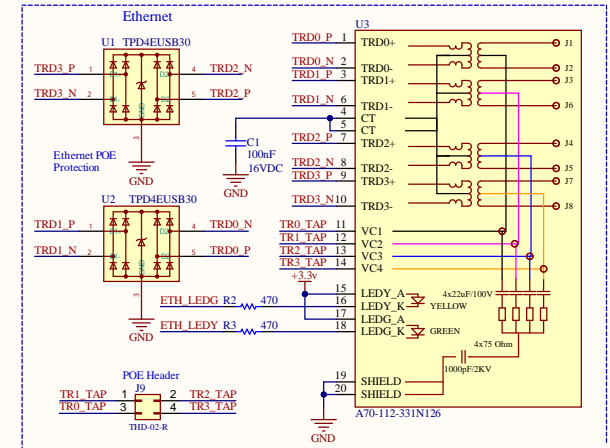
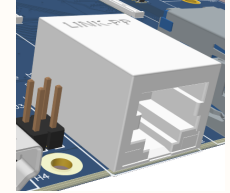
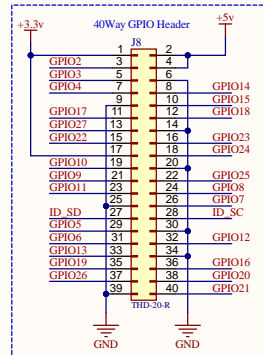
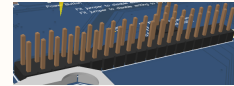


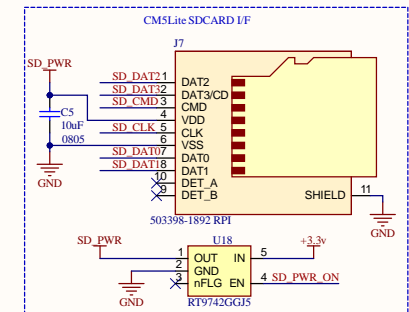
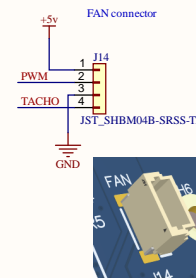
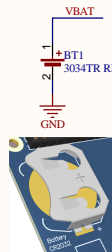
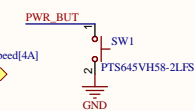
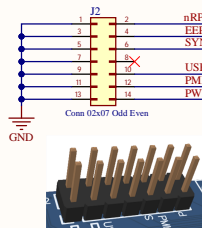
Figure 1: Showing Bergstrip 0.6mm pitch family of product.

J15

10164227-1001A1RLP



Force RPIBOOT = Jumper Pins 1-2



Title CM5_GPIO.SchDoc		Q-Wave Systems Co., Ltd No.1 Sukarawat 33/1 Ratburana Bangkok Thailand	
Size: A3	DrawnBy: Amornthep P.	CheckBy: Amornthep P.	Sheet * of *
Date: 4/7/2025	Number: *	File: C:\HW_Product\QWA256 CM5IO_Altium_V2\CM5_GPIO.SchDoc	

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PCIe-M2.SchDoc

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