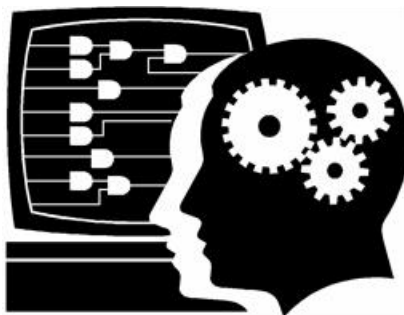


数字系统设计与Verilog HDL

(第6版)



第3章 Quartus Prime使用指南

3.1 Quartus Prime原理图设计

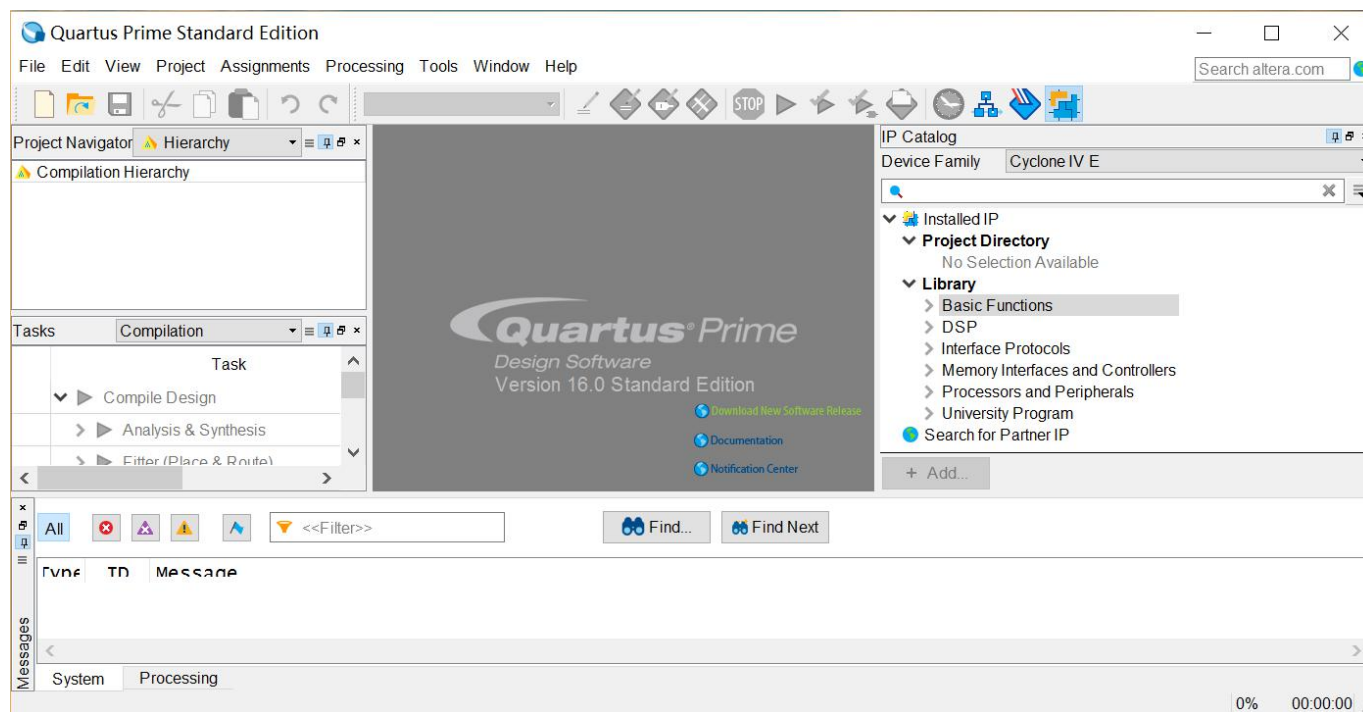
3.2 基于IP核的设计

3.3 SignalTap II的使用方法

3.4 Quartus Prime的优化设置与时序分析

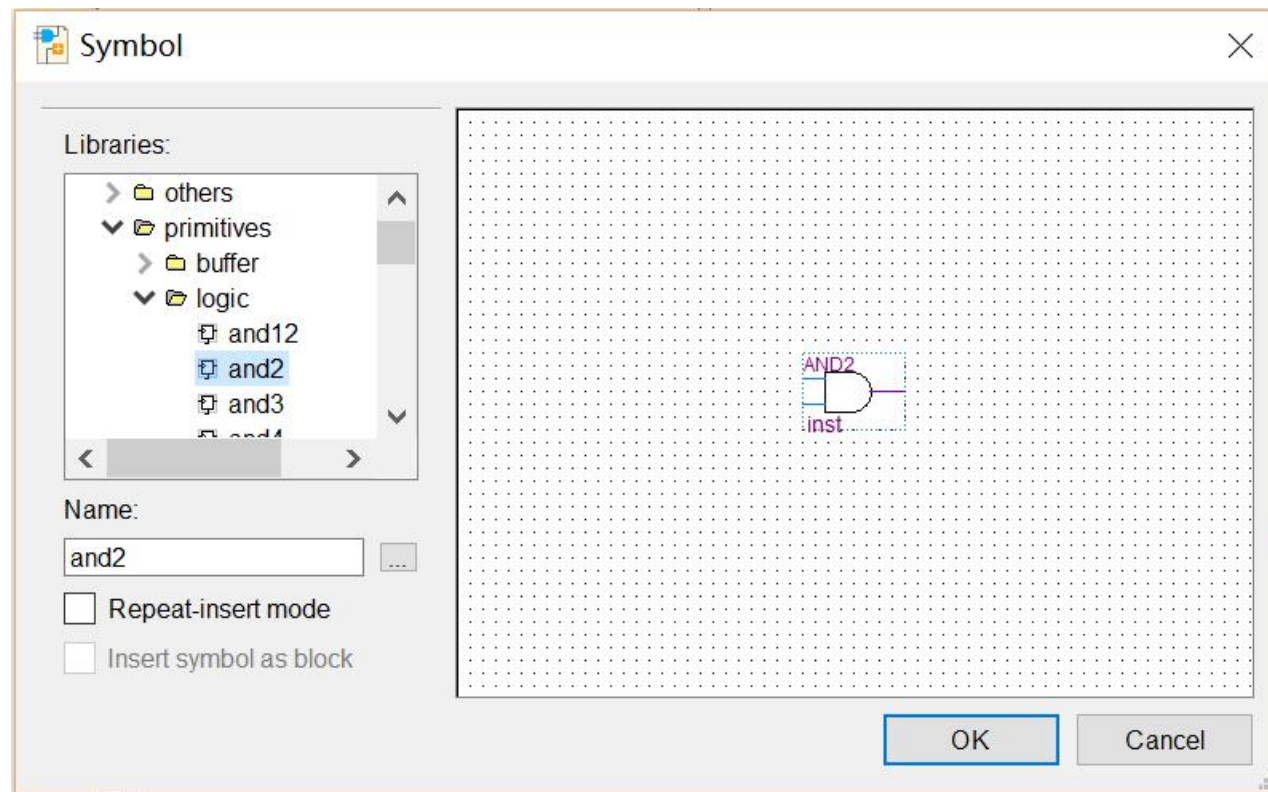
3.1 Quartus Prime原理图设计

3.1.1 半加器原理图设计输入



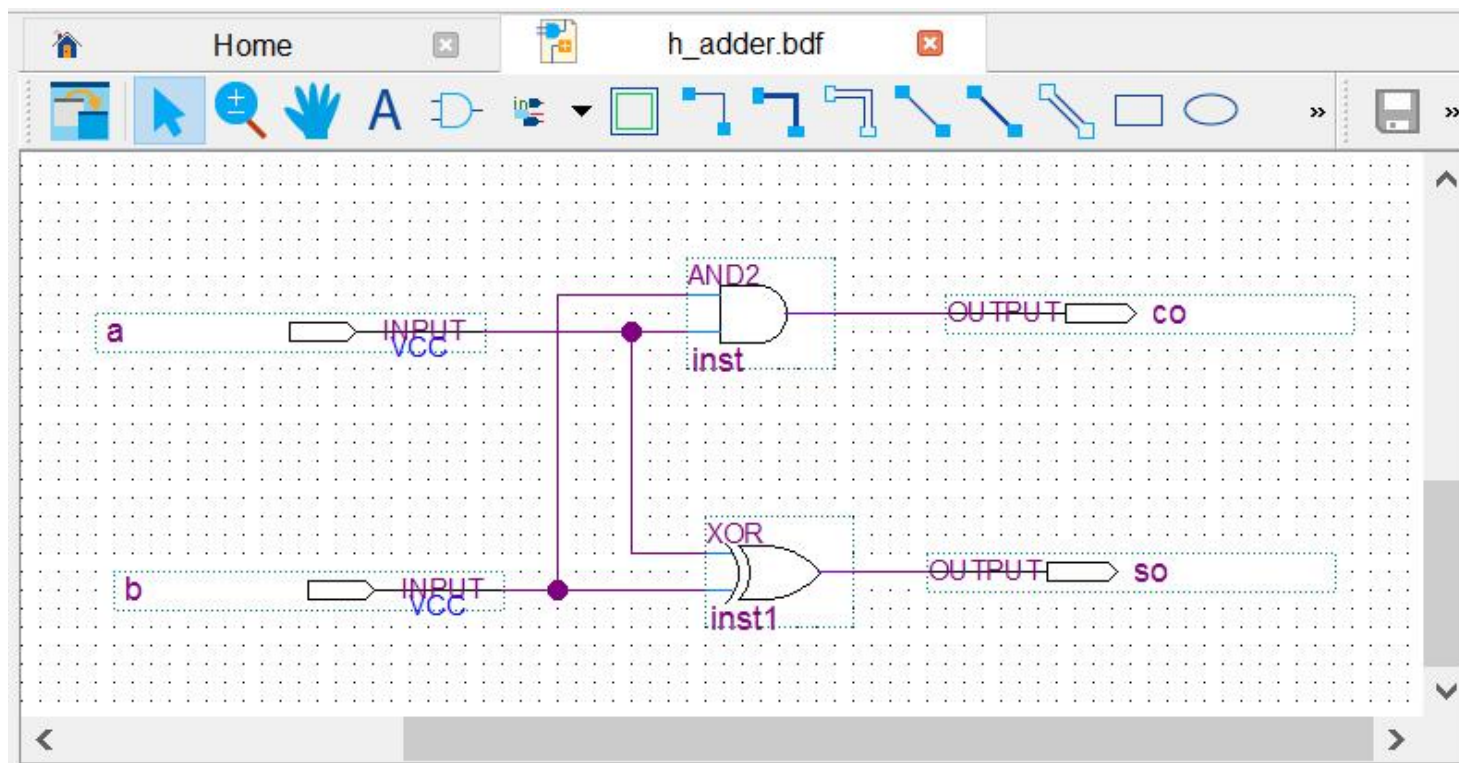
Quartus Prime的主界面

3.1.1 半加器原理图设计输入



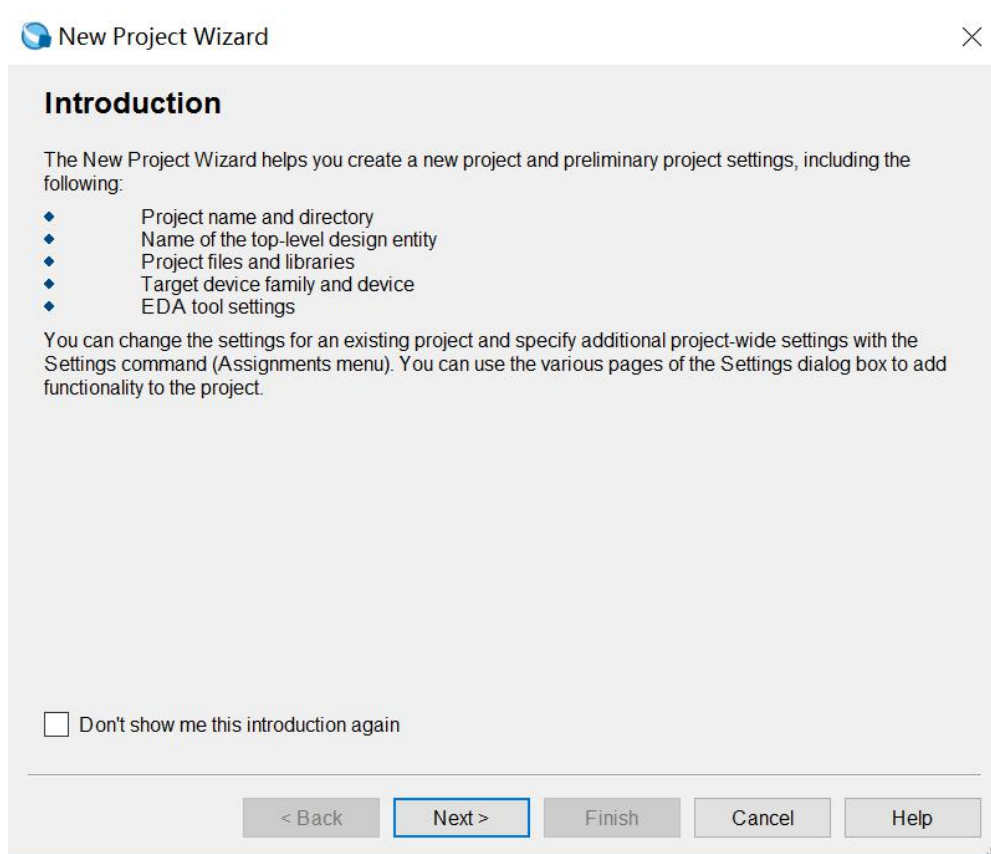
输入元件

3.1.1 半加器原理图设计输入



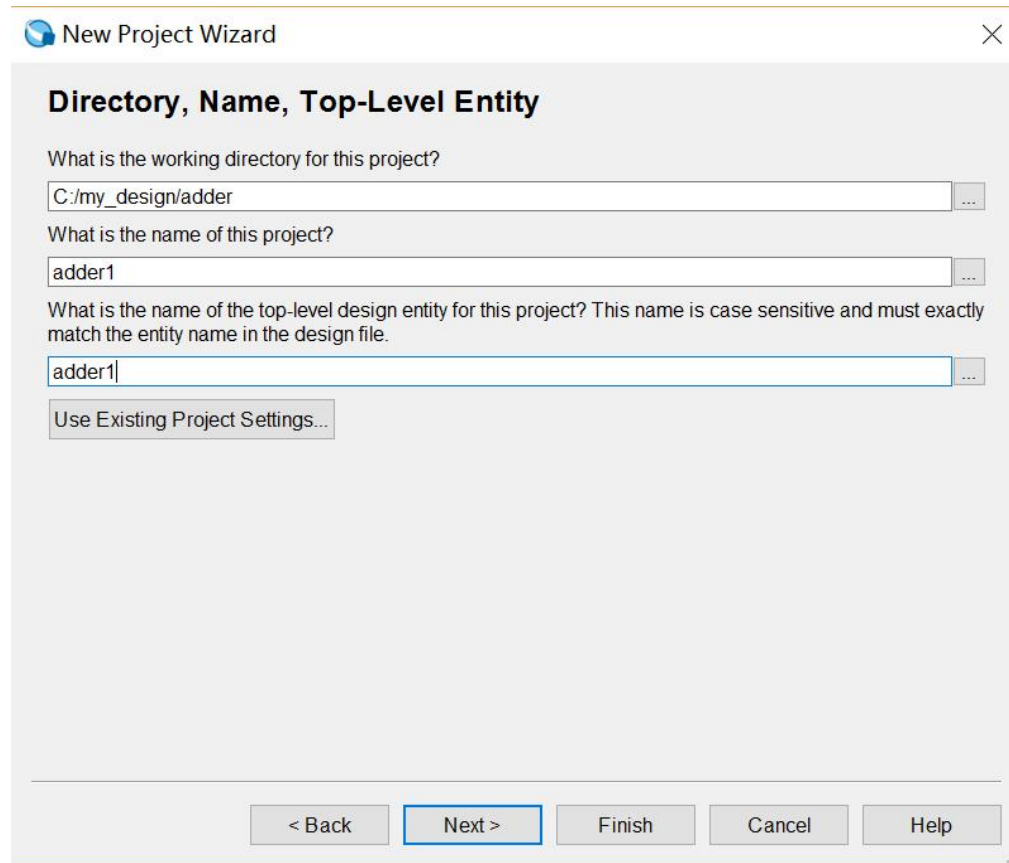
半加器电路图

3.1.1 半加器原理图设计输入



使用New Project Wizard创建工程

3.1.1 半加器原理图设计输入



The image shows a 'New Project Wizard' dialog box with the title bar 'New Project Wizard' and a close button. The main content area is titled 'Directory, Name, Top-Level Entity'. It contains three text input fields, each with a browse button (three dots) to its right. The first field is labeled 'What is the working directory for this project?' and contains the text 'C:/my_design/adder'. The second field is labeled 'What is the name of this project?' and contains the text 'adder1'. The third field is labeled 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' and contains the text 'adder1'. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom of the dialog are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a blue border.

Directory, Name, Top-Level Entity

What is the working directory for this project?
C:/my_design/adder ...

What is the name of this project?
adder1 ...

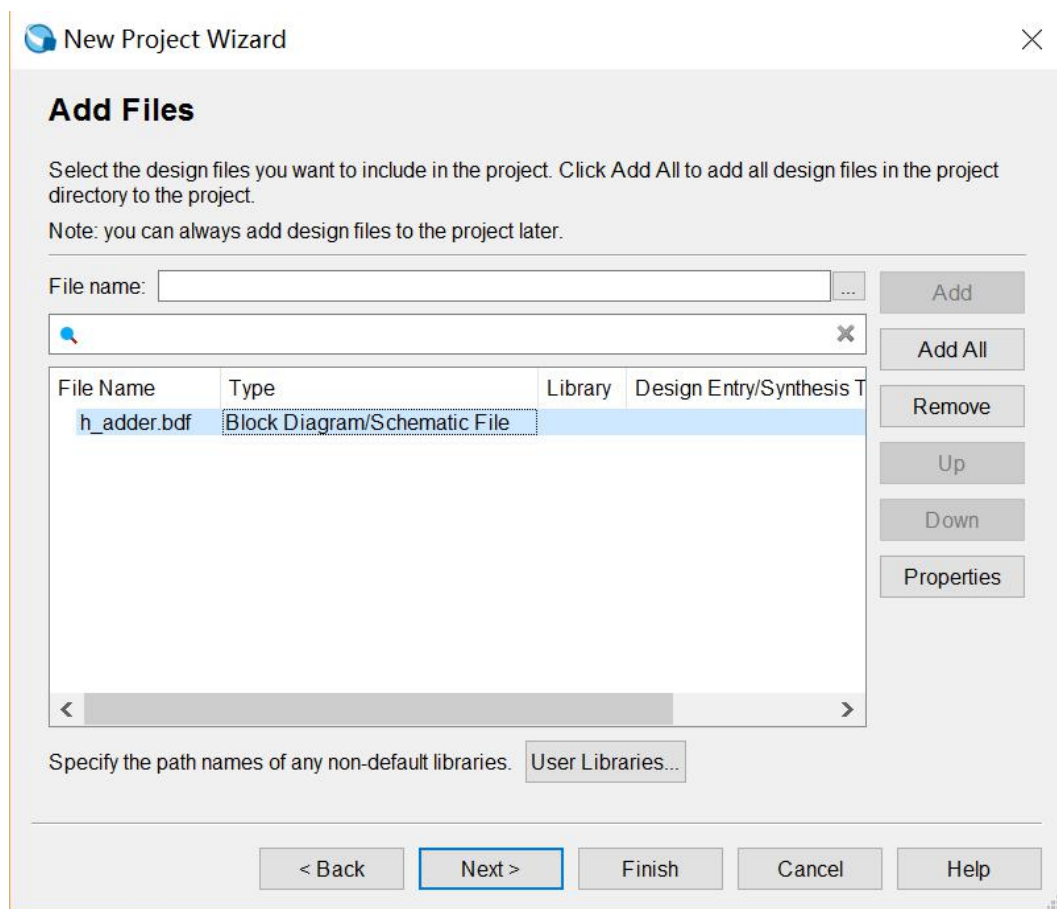
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
adder1 ...

Use Existing Project Settings...

< Back Next > Finish Cancel Help

设置Directory, Name, Top-Level Entity对话框

3.1.1 半加器原理图设计输入



将设计文件加入当前工程中

3.1.1 半加器原理图设计输入

New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone IV E

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core Speed grade: Any

Name filter:

☒ Show advanced devices

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multip
EP4CE115F29C7	1.2V	114480	529	529	3981312	532
EP4CE115F29C8	1.2V	114480	529	529	3981312	532

< >

< Back Next > Finish Cancel Help

选择目标器件

3.1.1 半加器原理图设计输入

New Project Wizard

EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

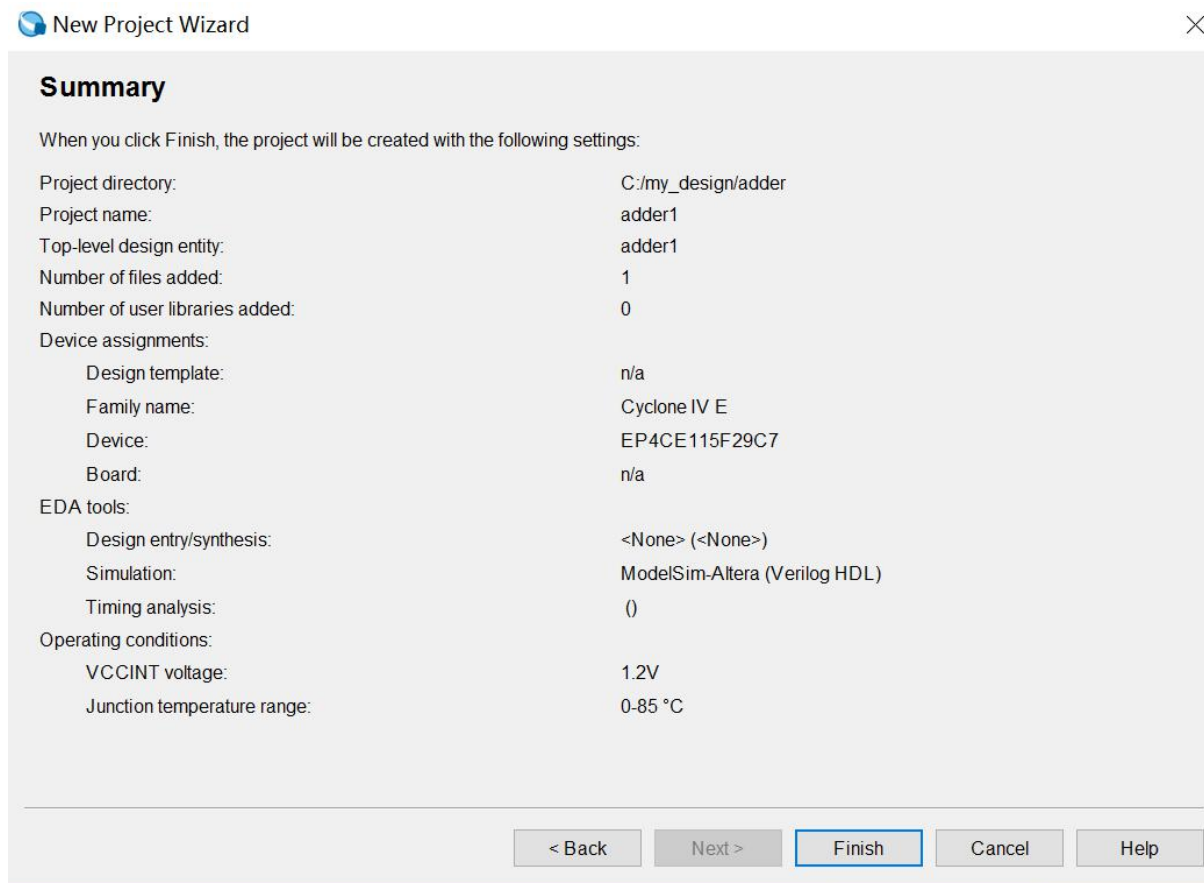
EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	Verilog HDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel Help

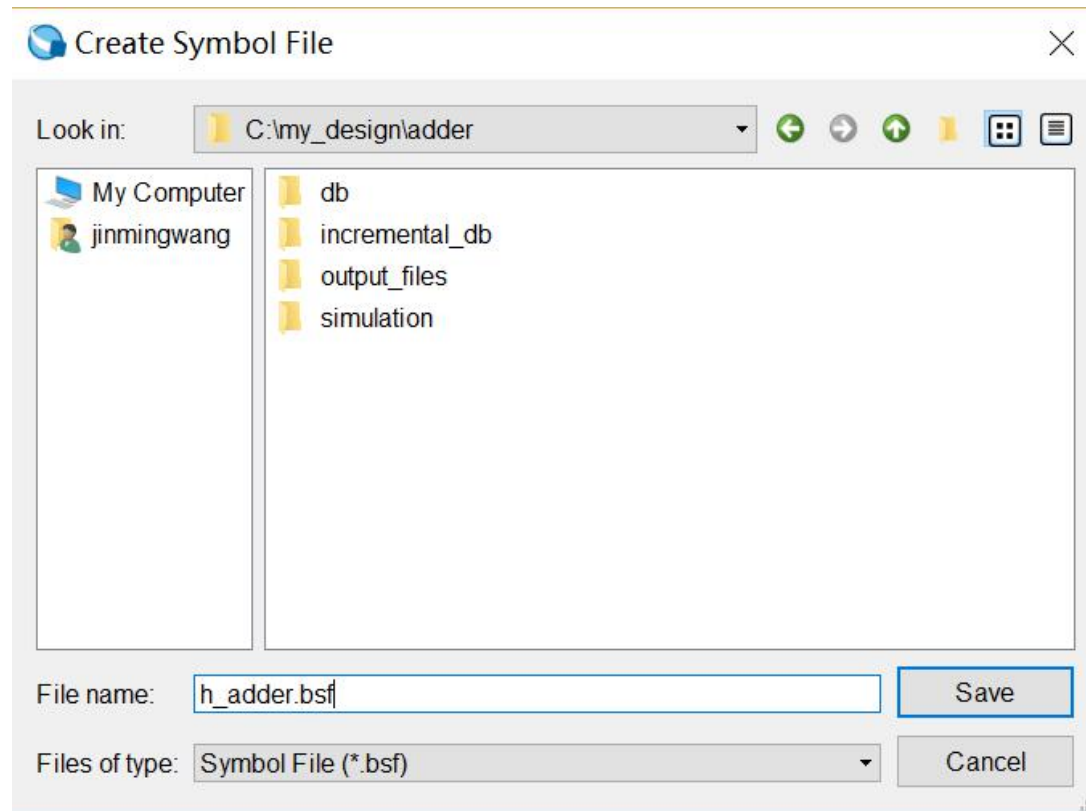
选择综合器、仿真器

3.1.1 半加器原理图设计输入



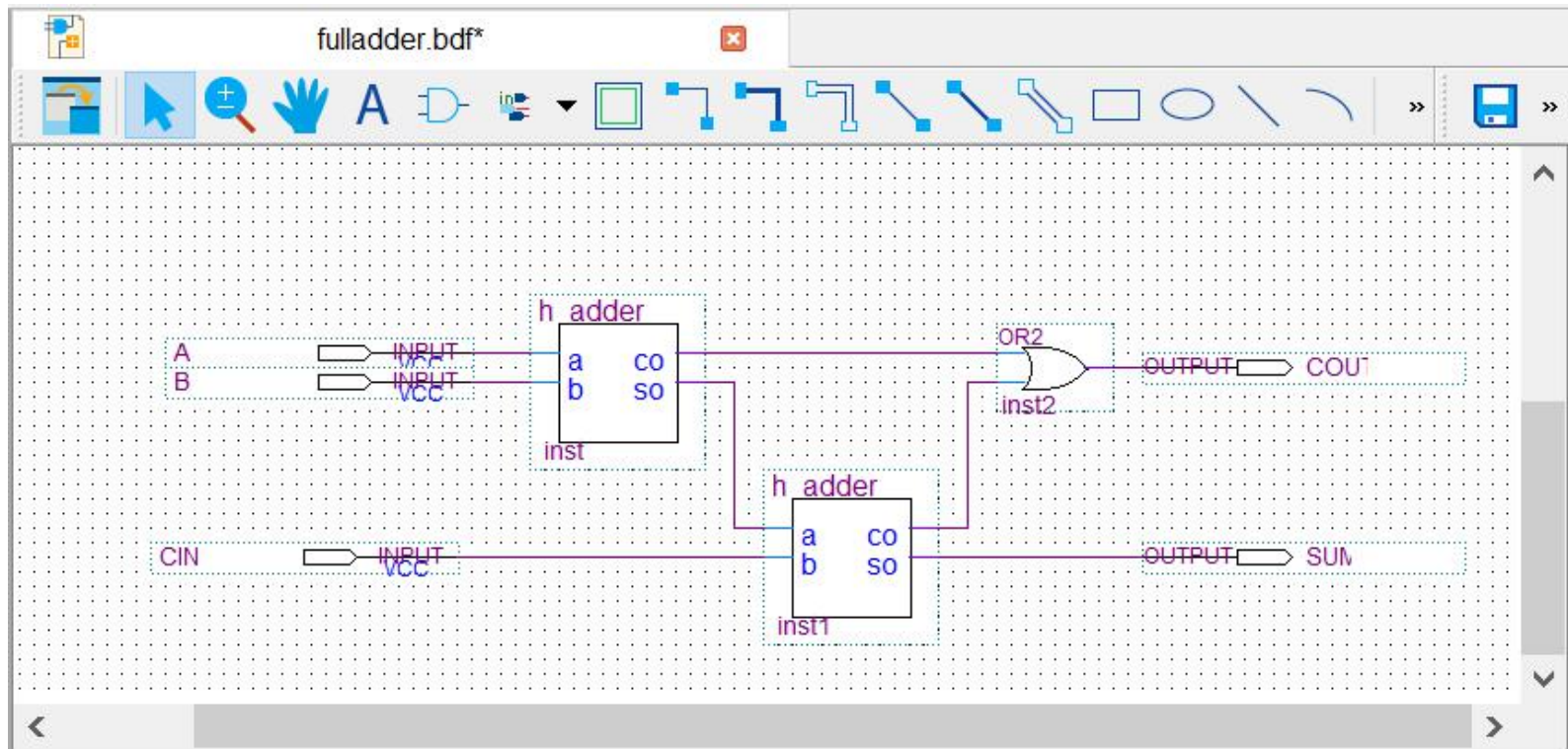
工程信息汇总显示

3.1.2 1位全加器设计输入



创建元件符号对话框

3.1.2 1位全加器设计输入



1 位全加器原理图

3.1.3 1位全加器的编译

选择菜单**Processing→Start Compilation**，或者单击按钮，即启动了完全编译，完全编译包括如下5个过程：

分析与综合（**Analysis & Synthesis**）；

适配（**Fitter**）；

装配（**Assembler**）；

定时分析（**TimeQuest Timing Analysis**）；

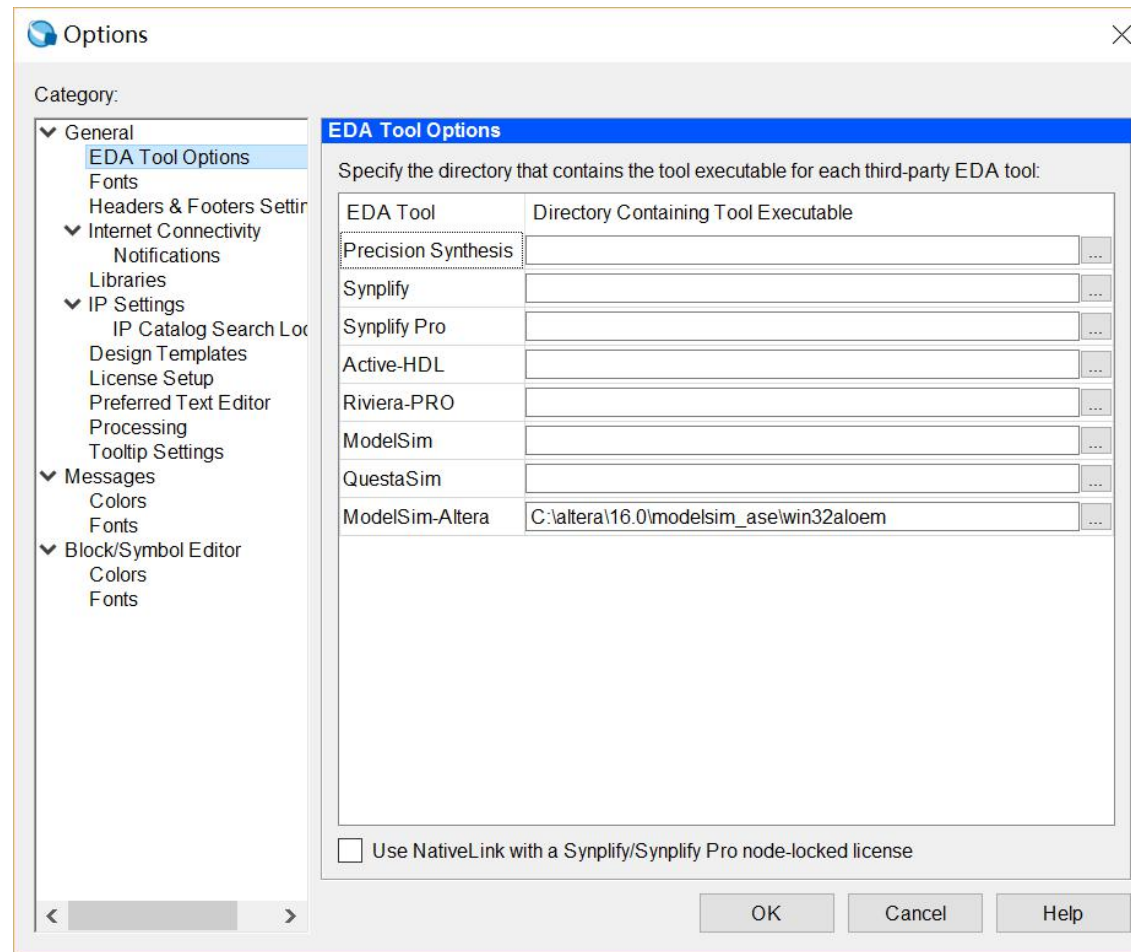
网表文件提取（**EDA Netlist Writer**）。

3.1.3 1位全加器的编译

Flow Summary	
Flow Status	Successful - Tue Jun 28 23:27:48 2016
Quartus Prime Version	16.0.1 Build 218 06/01/2016 SJ Standard Edition
Revision Name	adder1
Top-level Entity Name	fulladder
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	2 / 114,480 (< 1 %)
Total combinational functions	2 / 114,480 (< 1 %)
Dedicated logic registers	0 / 114,480 (0 %)
Total registers	0
Total pins	5 / 529 (< 1 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

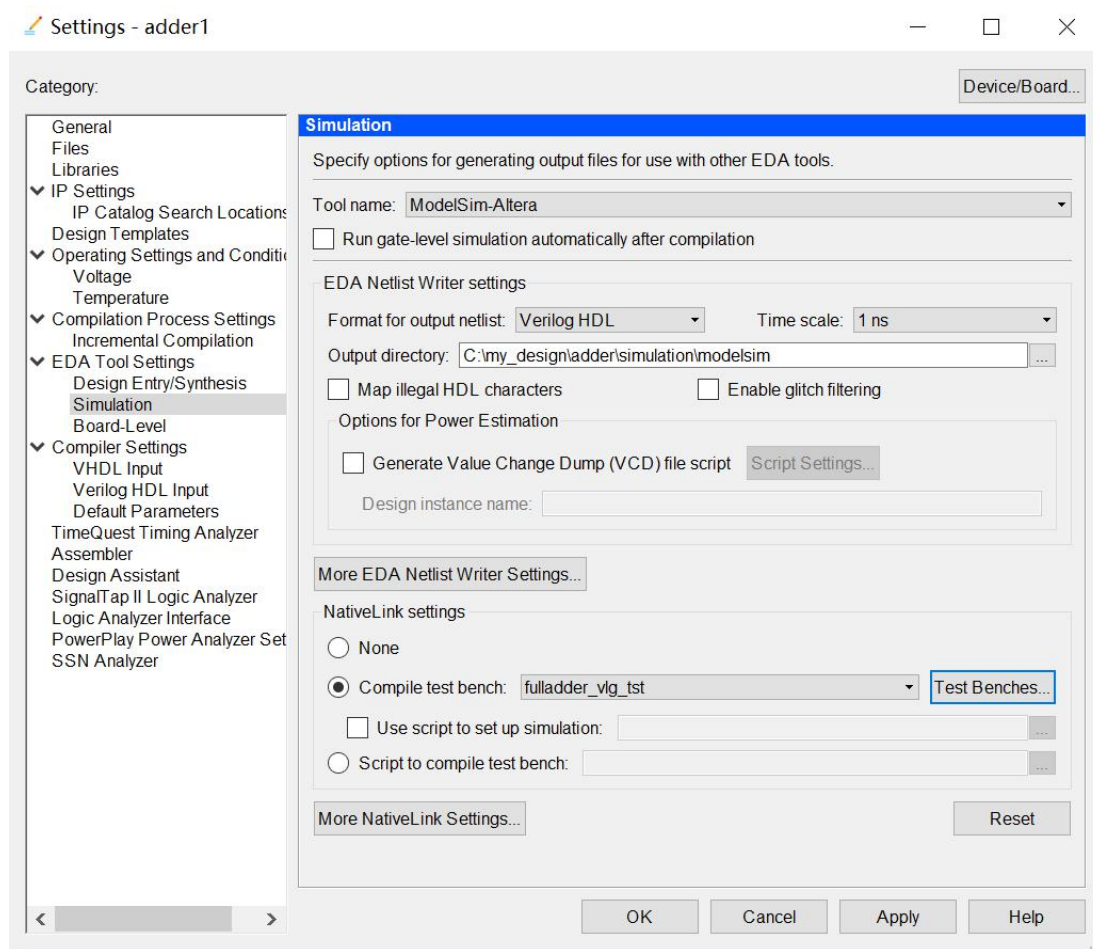
编译信息汇总

3.1.4 1位全加器的仿真



建立Quartus Prime和Modelsim的链接

3.1.4 1位全加器的仿真



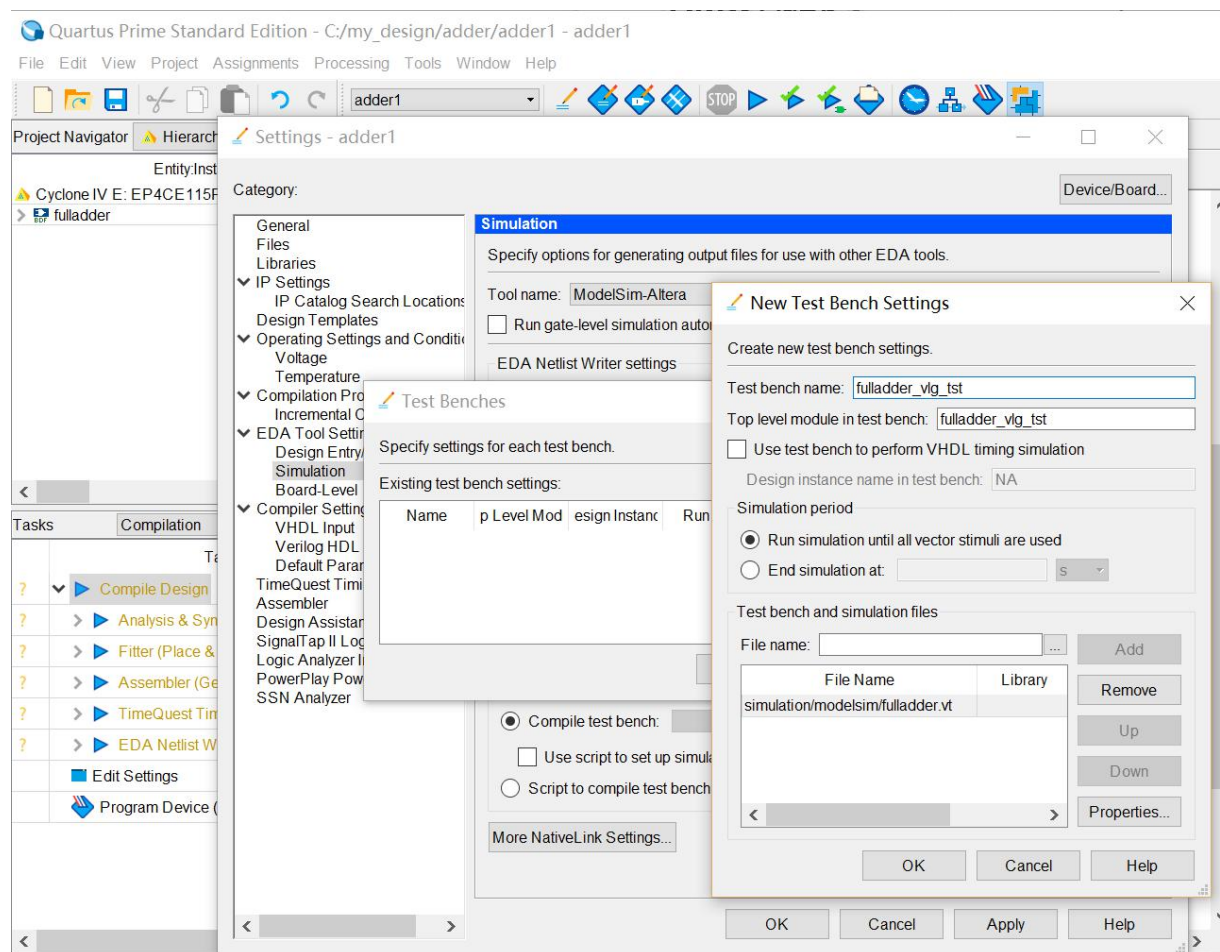
设置仿真文件的格式和目录

3.1.4 1位全加器的仿真

```
27
28 `timescale 1 ps/ 1 ps
29 module fulladder_vlg_tst();
30 // constants
31 // general purpose registers
32 reg eachvec;
33 // test vector input registers
34 reg A;
35 reg B;
36 reg CIN;
37 // wires
38 wire COUT;
39 wire SUM;
40
41 // assign statements (if any)
42 fulladder i1 (
43 // port map - connection between master ports and signals/registers
44 .A(A),
45 .B(B),
46 .CIN(CIN),
47 .COUT(COUT),
48 .SUM(SUM)
49 );
50 initial
51 begin
52 // code that executes only once
53 // insert code here --> begin
54
55 // --> end
56 $display("Running testbench");
57 end
58 always
59 // optional sensitivity list
60 // @(event1 or event2 or .... eventn)
61 begin
62 // code executes for every event on sensitivity list
63 // insert code here --> begin
64
65 @eachvec;
66 // --> end
67 end
68 endmodule
69
```

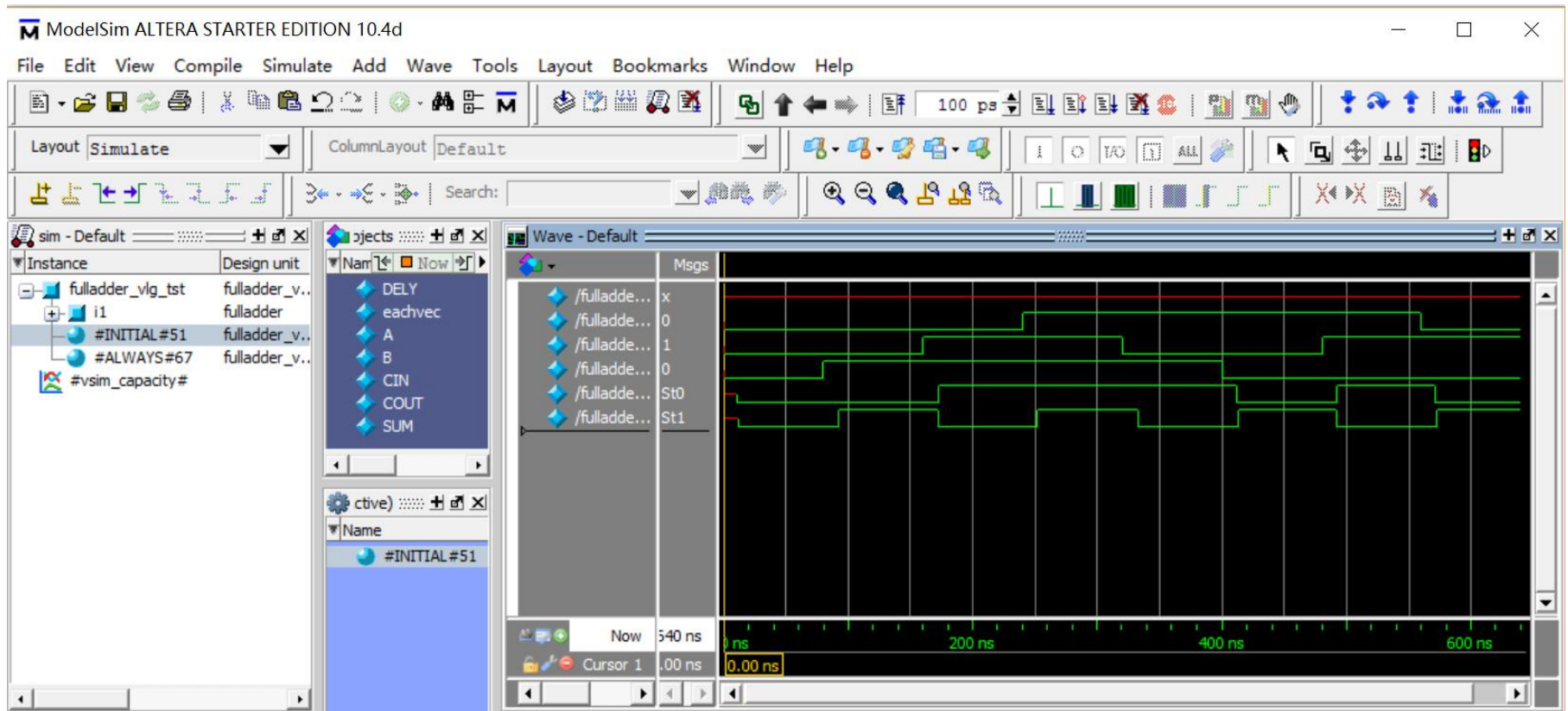
自动生成的Test Bench模板文件

3.1.4 1位全加器的仿真



对Test Bench进一步设置

3.1.4 1位全加器的仿真



1位全加器时序仿真波形图

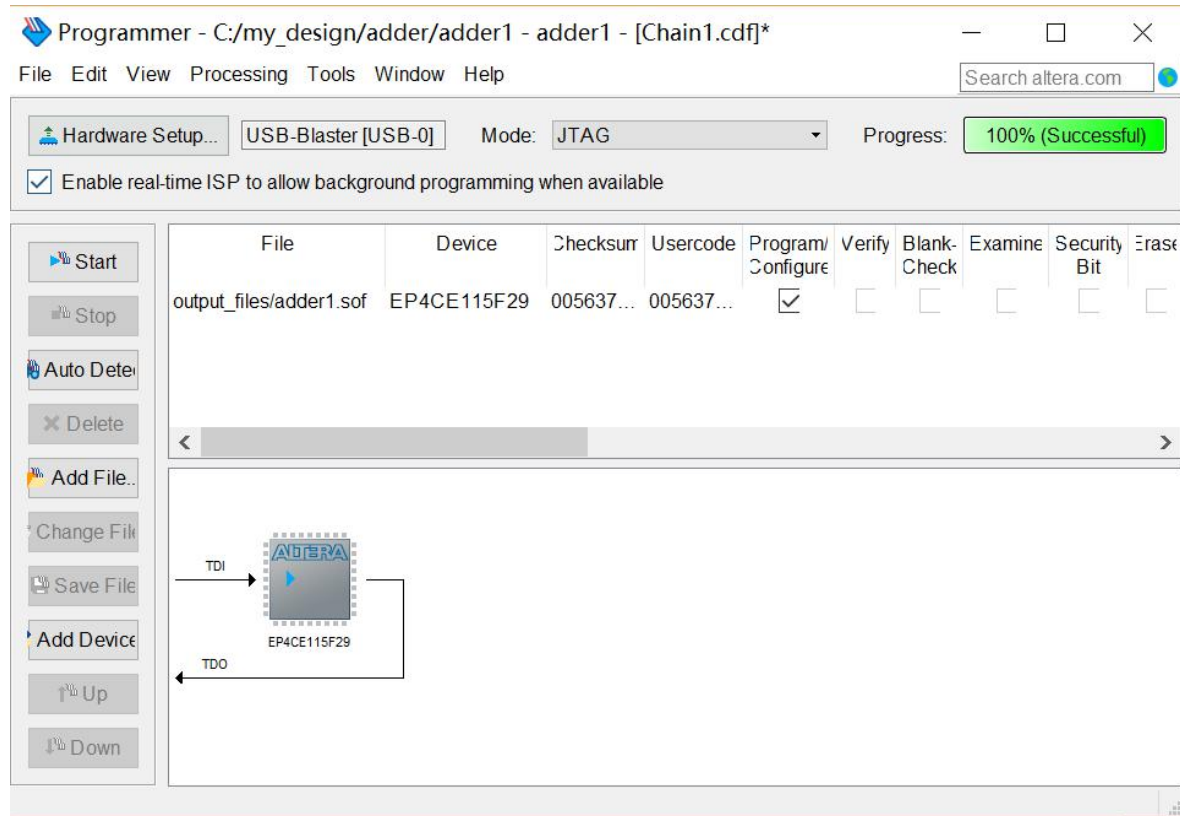
3.1.5 1位全加器的下载

本例针对的下载板为DE2-115，故目标器件应为：EP4CE115F29C7。

选择菜单Assignments→Pin Planner，在Pin Planner对话框中，进行引脚的锁定。

A	→PIN_AB28	SW0（拨动开关）
B	→PIN_AC28	SW1（拨动开关）
CIN	→PIN_AC27	SW2（拨动开关）
SUM	→PIN_E21	LEDG0（LED灯）
COUT	→PIN_AB28	LEDG1（LED灯）

3.1.5 1位全加器的下载



编程下载窗口

第3章 Quartus Prime使用指南

3.1 Quartus Prime原理图设计

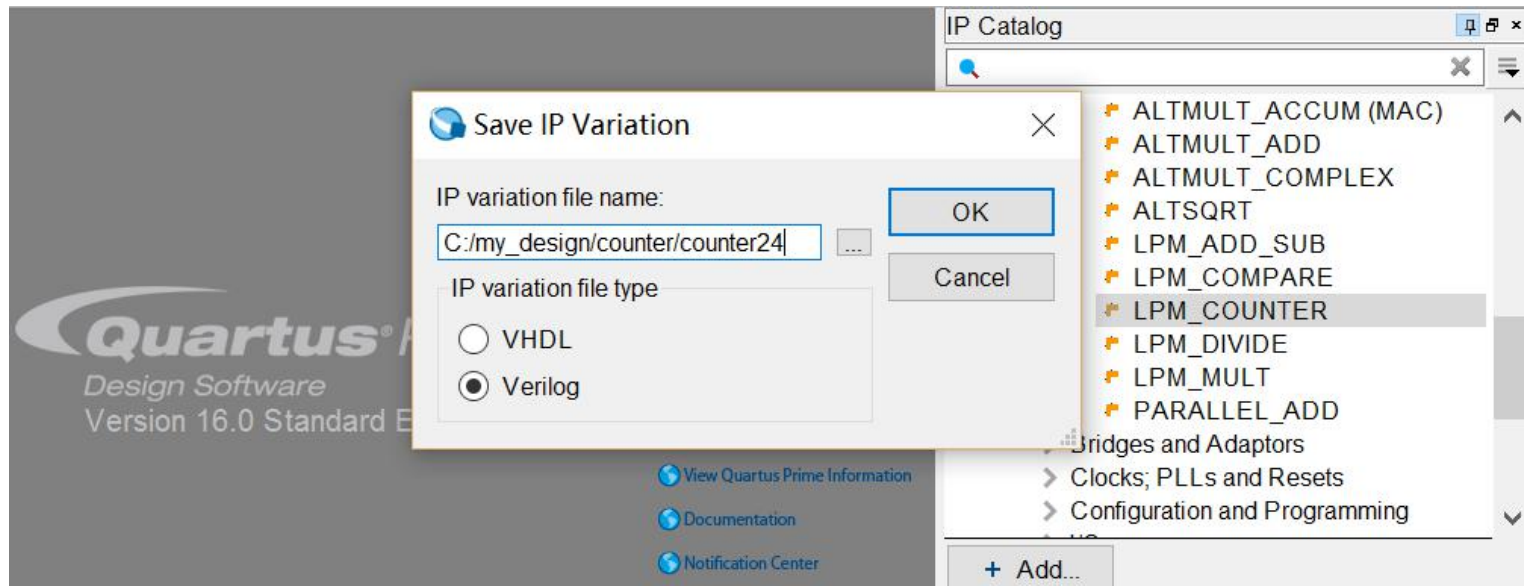
3.2 基于IP核的设计

3.3 SignalTap II的使用方法

3.4 Quartus Prime的优化设置与时序分析

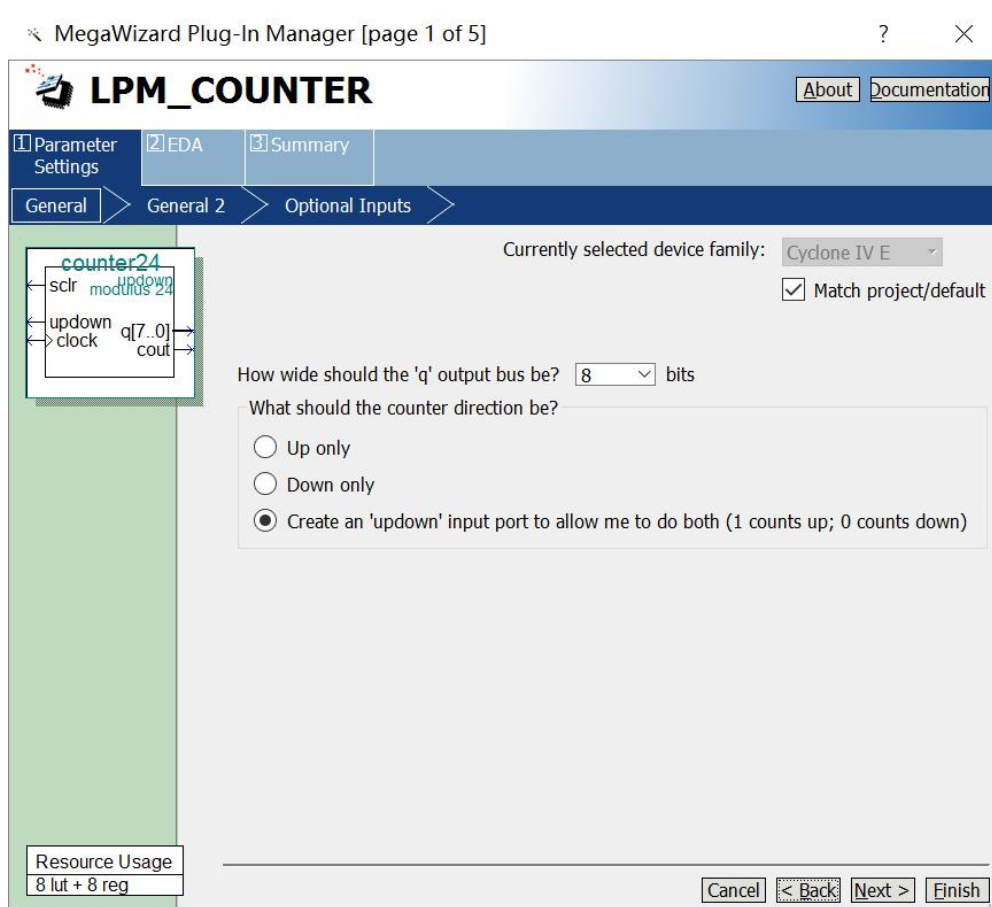
3.2 基于IP核的设计

3.2.1 用LPM_COUNTER设计模24方向可控计数器



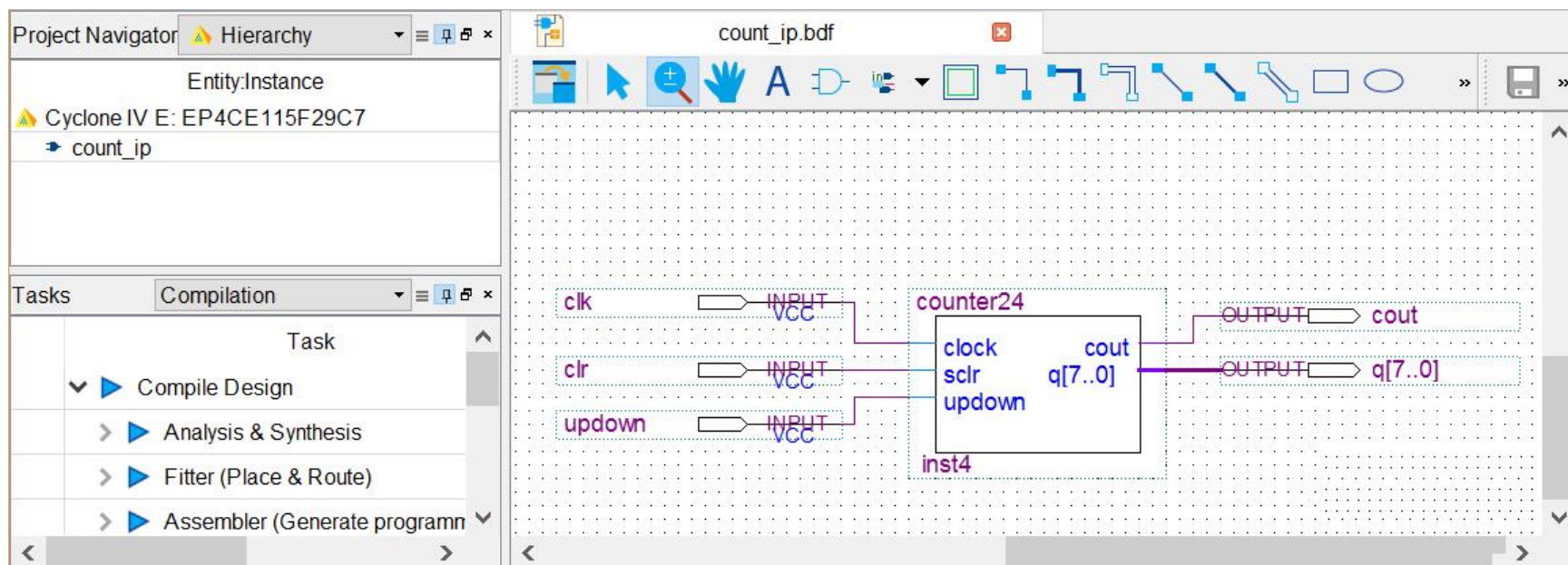
LPM_COUNTER模块命名

3.2.1 用LPM_COUNTER设计模24方向可控计数器



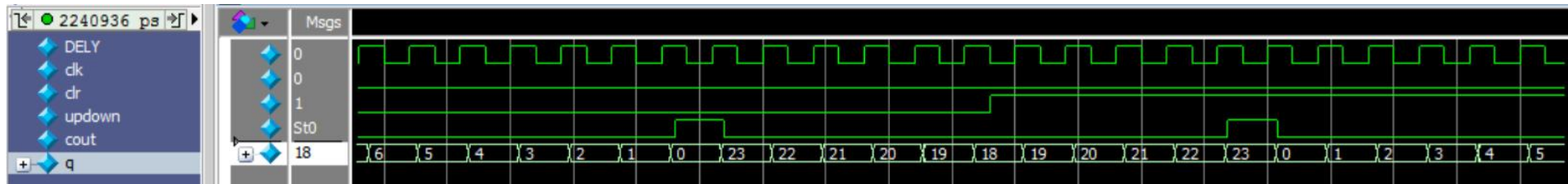
启动MegaWizard Plug-In Manager，对LPM_COUNTER模块进行参数设置

3.2.1 用LPM_COUNTER设计模24方向可控计数器



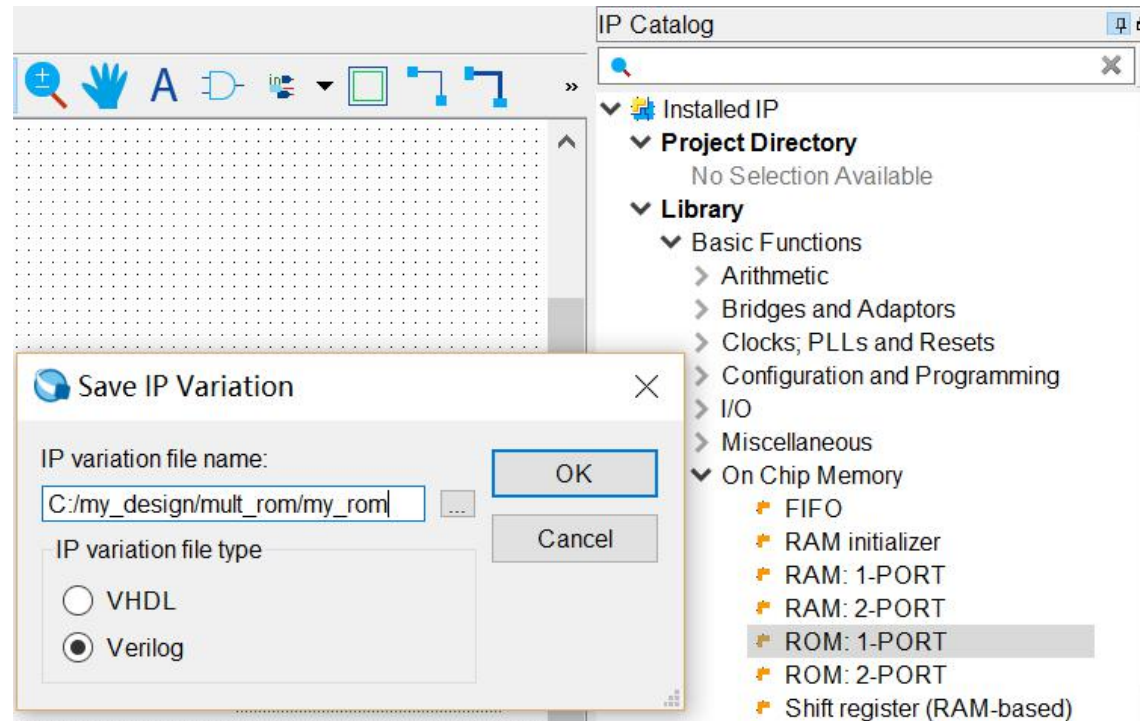
模24方向可控计数器原理图

3.2.1 用LPM_COUNTER设计模24方向可控计数器



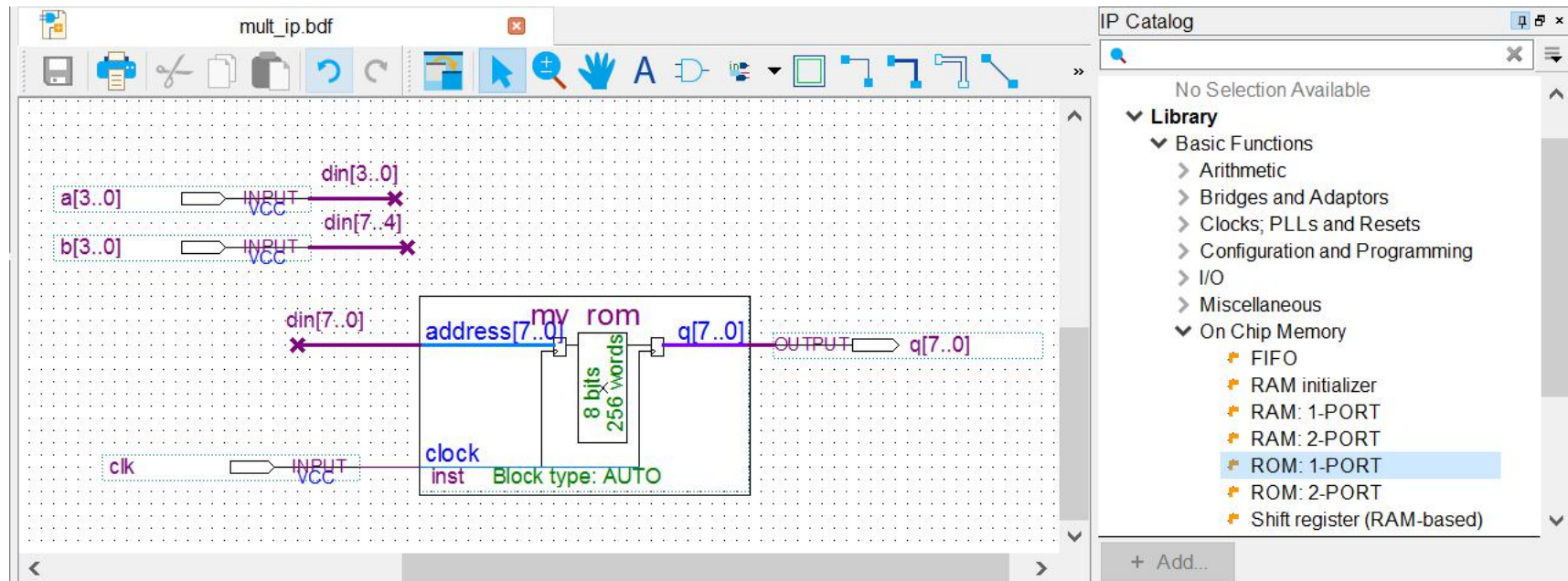
模24方向可控计数器门级仿真波形图

3.2.2 用LPM_ROM模块实现 4×4 无符号数乘法器



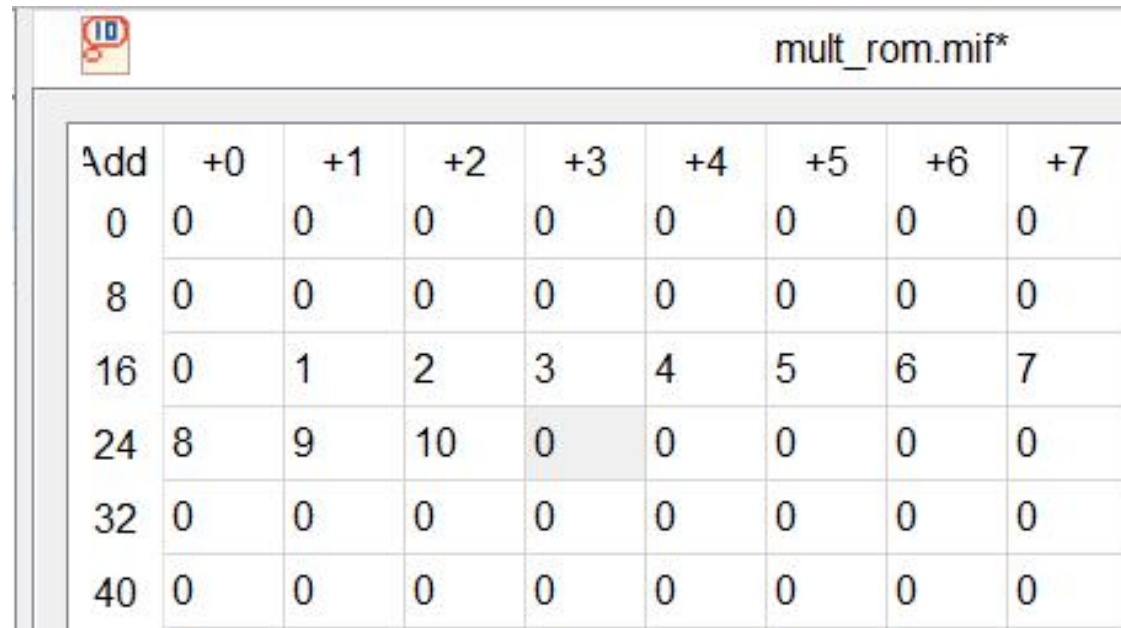
Save IP Variation对话框

3.2.2 用LPM_ROM模块实现 4×4 无符号数乘法器



基于lpm_rom实现的 4×4 无符号数乘法器原理图

3.2.2 用LPM_ROM模块实现4×4无符号数乘法器

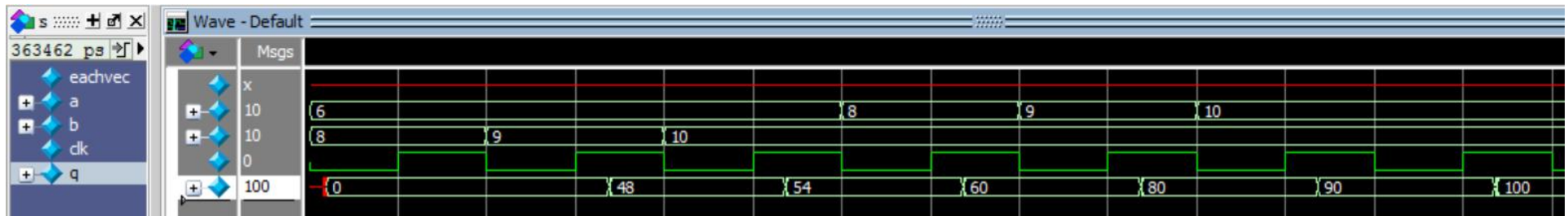


The image shows a screenshot of a Quartus II ROM editor window titled "mult_rom.mif*". The window displays a 4x4 ROM configuration table. The table has 8 columns labeled "Add", "+0", "+1", "+2", "+3", "+4", "+5", "+6", and "+7". The rows are labeled with addresses: 0, 8, 16, 24, 32, and 40. The data values are as follows:

Add	+0	+1	+2	+3	+4	+5	+6	+7
0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0
16	0	1	2	3	4	5	6	7
24	8	9	10	0	0	0	0	0
32	0	0	0	0	0	0	0	0
40	0	0	0	0	0	0	0	0

ROM存储器的内容存储在*.mif文件中

3.2.2 用LPM_ROM模块实现 4×4 无符号数乘法器



4×4 无符号数乘法器波形仿真结果

第3章 Quartus Prime使用指南

3.1 Quartus Prime原理图设计

3.2 基于IP核的设计

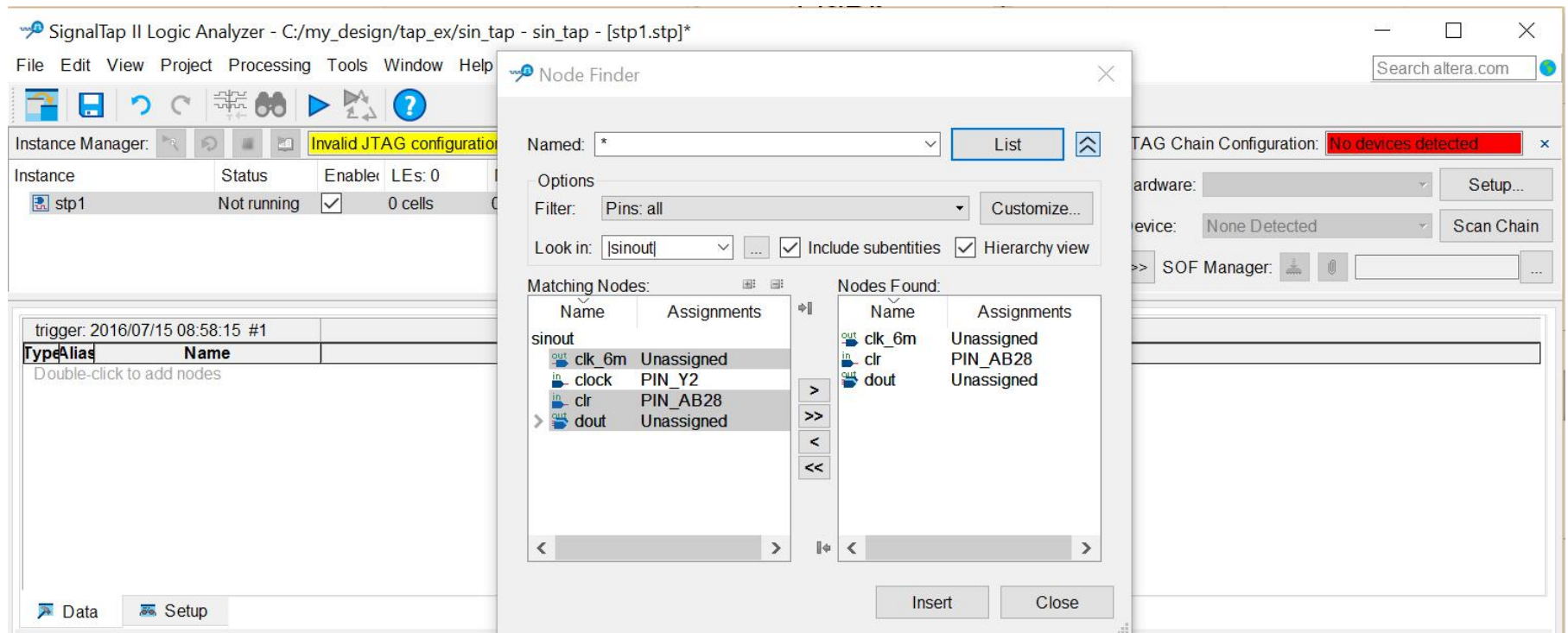
3.3 SignalTap II的使用方法

3.4 Quartus Prime的优化设置与时序分析

3.3 SignalTap II的使用方法

Quartus Prime的嵌入式逻辑分析仪**SignalTap II**为设计者提供了一种方便高效的硬件测试手段，它可以随设计文件一起下载到目标芯片中，捕捉目标芯片内信号节点或总线上的数据，将这些数据暂存于目标芯片的嵌入式**RAM**中，然后通过器件的**JTAG**端口将采到的信息和数据送到计算机进行显示，供用户分析。

3.3 SignalTap II的使用方法



调入待测信号

3.3 SignalTap II的使用方法

The screenshot displays the SignalTap II Logic Analyzer software interface. The main window title is "SignalTap II Logic Analyzer - C:/my_design/tap_ex/sin_tap - sin_tap - [stp1.stp]*". The menu bar includes File, Edit, View, Project, Processing, Tools, Window, and Help. The toolbar contains icons for file operations, logic analysis, and help.

The **Instance Manager** window shows a table of instances:

Instance	Status	Enabler	LEs: 633	Memory: 4096	Small: 0/0
stp1	Not running	<input checked="" type="checkbox"/>	633 cells	40960 bits	0 blocks

The **JTAG Chain Configuration** window shows the JTAG chain is ready. The hardware is set to "USB-Blaster [USB-0]". The device is "@1: EP3C120/EP4CE115 (0x020F70DD)". The SOF Manager shows the file "C:/my_design/tap_ex/output_files/sin_tap.sof".

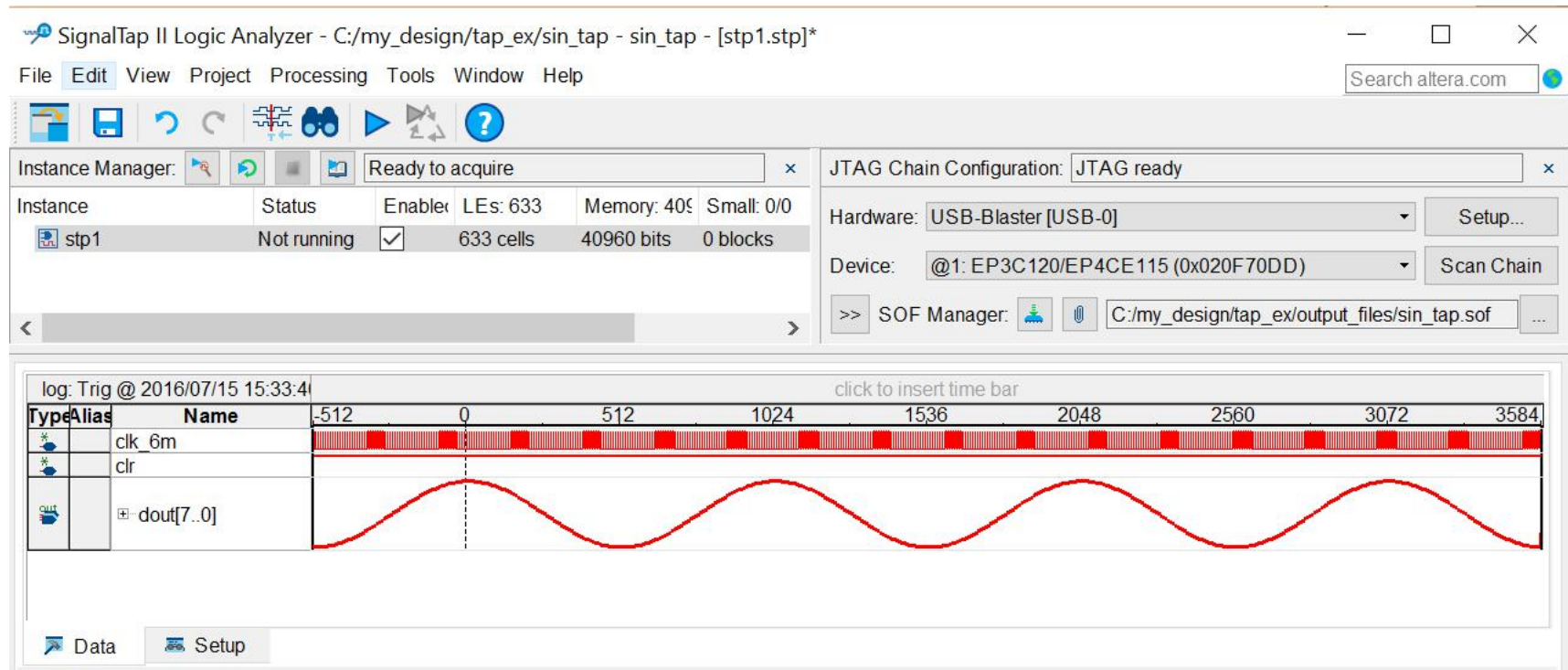
The **Signal Configuration** window shows the clock set to "clock". The data configuration includes a sample depth of 4 K, RAM type set to Auto, and segmented data with 2 K sample segments. The nodes allocated are set to Auto, and the pipeline factor is 0. The storage qualifier is set to Continuous.

The **Signal Configuration** window also displays a table of nodes:

Type	Alias	Node Name	Data Enable	Trigger Enable	Trigger Conditions
		clk_6m	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> Basic AND
		clr	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/> 1
		dout[7..0]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	XXXXXXXXb

SignalTap II参数设置窗口

3.3 SignalTap II的使用方法



SignalTap II数据窗口显示的实时采样的信号波形

第3章 Quartus Prime使用指南

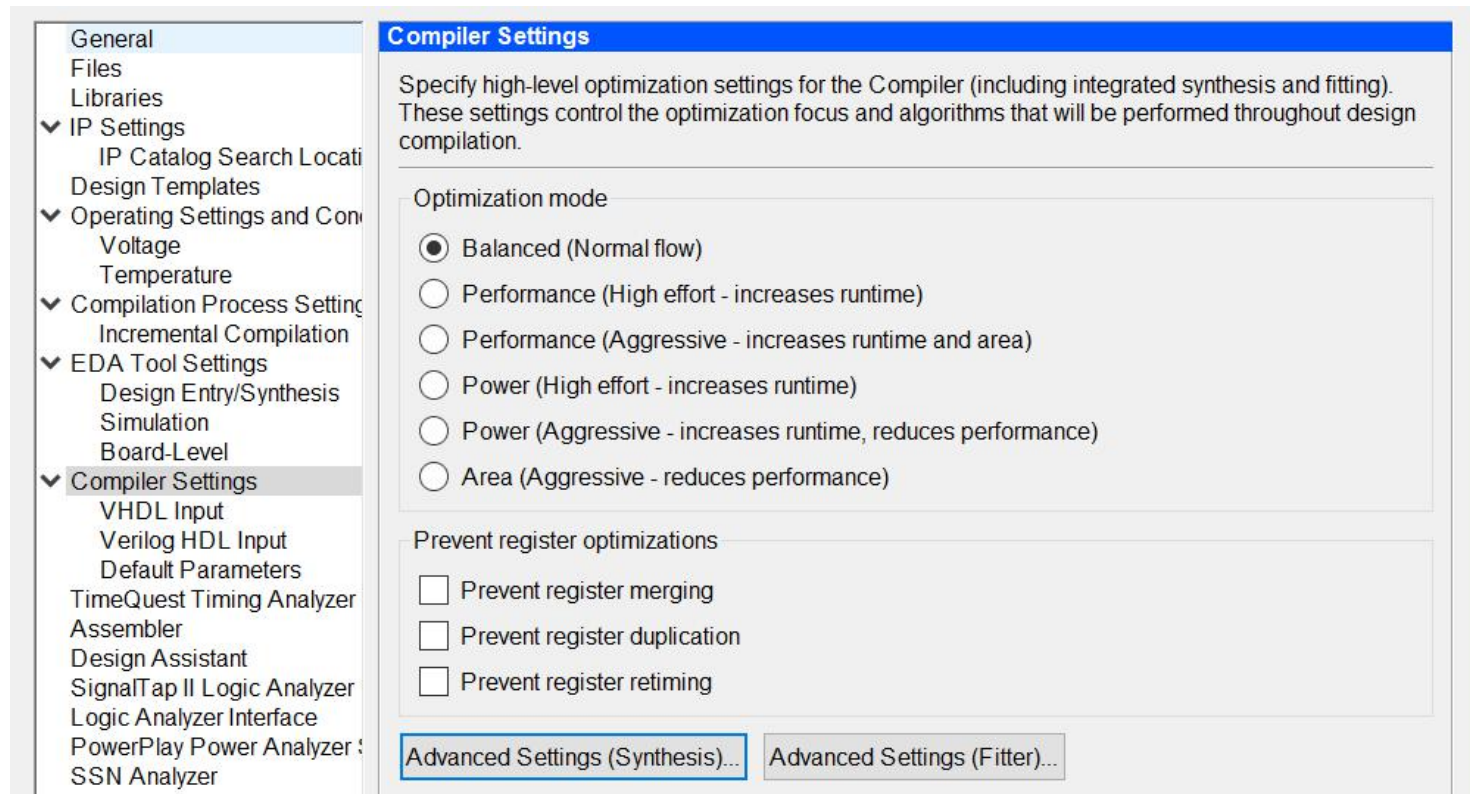
3.1 Quartus Prime原理图设计

3.2 基于IP核的设计

3.3 SignalTap II的使用方法

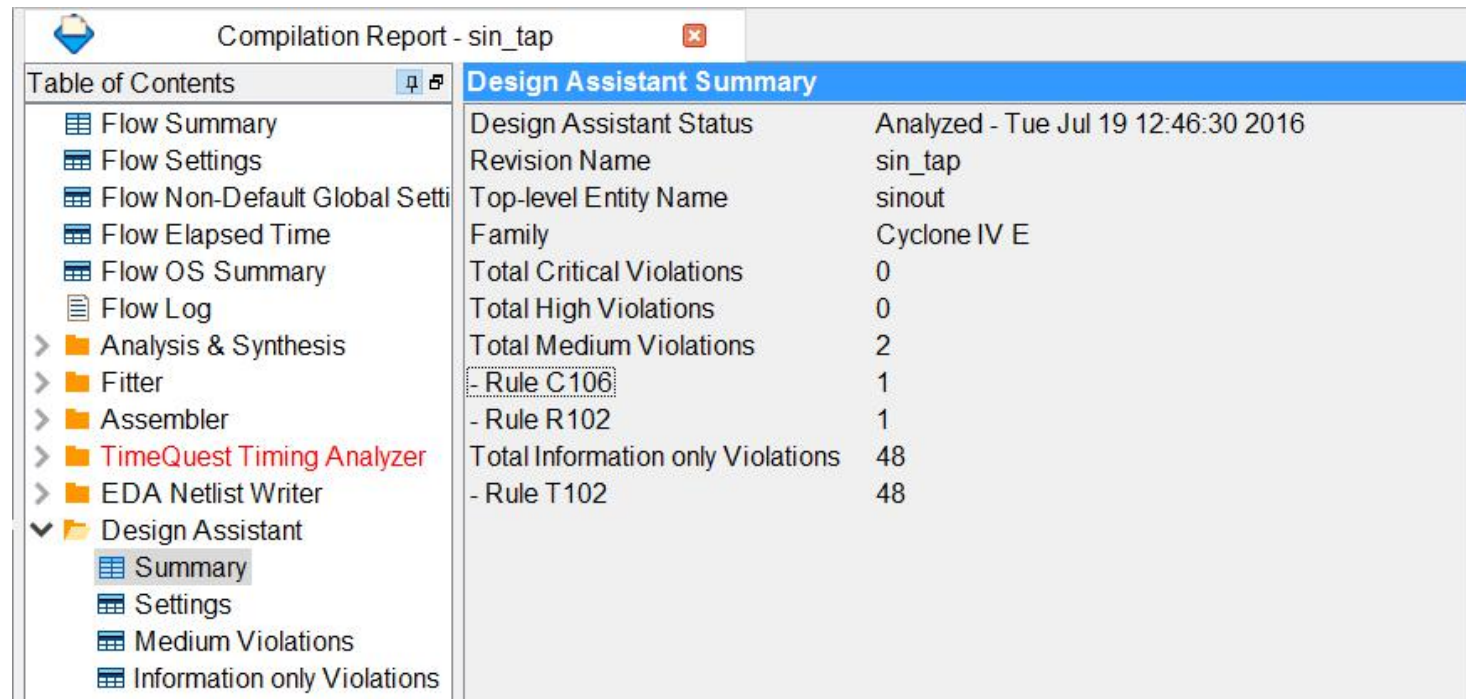
3.4 Quartus Prime的优化设置与时序分析

3.4 Quartus Prime的优化设置与时序分析



编译器设置

3.4 Quartus Prime的优化设置与时序分析



The screenshot shows the 'Compilation Report - sin_tap' window. The left pane displays a 'Table of Contents' with a tree structure. The right pane shows the 'Design Assistant Summary' table.

Table of Contents	
Flow Summary	
Flow Settings	
Flow Non-Default Global Settings	
Flow Elapsed Time	
Flow OS Summary	
Flow Log	
> Analysis & Synthesis	
> Fitter	
> Assembler	
> TimeQuest Timing Analyzer	
> EDA Netlist Writer	
▼ Design Assistant	
Summary	
Settings	
Medium Violations	
Information only Violations	

Design Assistant Summary	
Design Assistant Status	Analyzed - Tue Jul 19 12:46:30 2016
Revision Name	sin_tap
Top-level Entity Name	sinout
Family	Cyclone IV E
Total Critical Violations	0
Total High Violations	0
Total Medium Violations	2
Rule C106	1
- Rule R102	1
Total Information only Violations	48
- Rule T102	48

查看Design Assistant报告

3.4 Quartus Prime的优化设置与时序分析

Project Navigator | Hierarchy | Entity:Instance

▲ Cyclone IV E: EP4CE6E22C8

> DDS_PLL

Tasks | Compilation

Task

- ✓ > Compile Design
- ✓ > Analysis & Synthesis
- ✓ > Fitter (Place & Route)
- ✓ > Assembler (Generate programming)
- ✓ > TimeQuest Timing Analysis
- > EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Resource Optimization Advisor

- ▲ Use smart compilation
- ✓ Use the auto fit feature
- ✓ Logic Element Usage (6%)
- ▼ ▲ Stage 1
 - ▲ Optimize for area
 - ▲ Perform WYSIWYG primitive resynthesis
 - ▲ Turn on auto ROM/RAM/DSP/Shift Register Replacement
 - ✓ Use register packing
 - ✓ Remove location/LogicLock region assignments
- ▼ ▲ Stage 2
 - ▲ Change synthesis options
 - ✓ Turn off Physical Synthesis for Performance
 - ▲ Restructure multiplexers
 - ▲ Turn on Allow any size for ROM/RAM/Shift Register Recognition.
 - ▲ Turn on Allow Shift Register Merging across Hierarchies
 - ▲ Turn on Fast Input/Output Registers
- > ▲ Stage 3
- ✓ Memory Block Usage (0%)
 - ① Retarget memory blocks
 - ▲ Remove automatic inferencing of memory blocks
 - ✓ Remove location/LogicLock region assignments
 - ▲ Turn on Allow Shift Register Merging across Hierarchies
 - ① Optimize source code
- ✓ DSP Block Usage (N/A)
 - ▲ Remove automatic inferencing of DSP blocks
 - ✓ Balance DSP blocks
 - ① Optimize source code
- > ✓ I/O Usage (18%)
- ✓ Routing Resource Usage
 - ✓ Remove location/LogicLock region assignments
 - ① Verify hold timing constraints
 - ▲ Use the standard fit feature
 - ▲ Increase placement effort
 - ✓ Set Auto Packed Registers to Auto
 - ▲ Enable clocking topology analysis during routing
 - ▲ Turn on Aggressive Routability Optimizations
 - ▲ Turn off Optimize Timing
 - ✓ Remove Maximum Fan-Out assignment

Resource Summary

Flow Status	✓	Successful - Mon Aug 08 23:19:22 2016
Logic Element Usage	✓	375 / 6,272 (6%)
Memory Block Usage	✓	0 / 276,480 (0%)
DSP Block Usage	✓	Not available
I/O Usage	✓	17 / 92 (18%)

[Open Flow Summary \(Compilation Report\)](#)

资源优化指导 (Resource Optimization Advisor)

习 题 3

3.1 基于Quartus Prime软件，用D触发器设计一个2分频电路，并做波形仿真，在此基础上，设计一个4分频和8分频电路，做波形仿真。**1.4** 数字系统的实现方式有哪些？各有什么优缺点？

3.2 基于Quartus Prime软件，用74161设计一个模10计数器，并进行编译和仿真。

3.3 基于Quartus Prime软件，用74161设计一个模99的计数器，个位和十位都采用8421BCD码的编码方式设计，分别用置0和置1两种方法实现，完成原理图设计输入、编译、仿真和下载整个过程。

3.5 基于Quartus Prime软件，用74283（4位二进制全加器）设计实现一个8位全加器，并进行综合和仿真，查看综合结果和仿真结果。