SoC 的管脚约束表（信号与管脚对应表）

Name	Direction	Package Pin
Ports (47)		
clk	IN	W5
cs[3]	OUT	W4
cs[2]	OUT	V4
cs[1]	OUT	U4
cs[0]	OUT	U2
digit[7]	OUT	W7
digit[6]	OUT	W6
digit[5]	OUT	U8
digit[4]	OUT	V8
digit[3]	OUT	U5
digit[2]	OUT	V5
digit[1]	OUT	U7
digit[0]	OUT	V7
btn_c	IN	U18
btn_r	IN	T17
btn_l	IN	W19
Btn-d(reset)	IN	T18
sw[15]	IN	R2
sw[14]	IN	T1
sw[13]	IN	U1
sw[12]	IN	W2
sw[11]	IN	R3
sw[10]	IN	T2
sw[9]	IN	T3
sw[8]	IN	V2
sw[7]	IN	W13
sw[6]	IN	W14
sw[5]	IN	V15
Sw[4]	IN	W15
sw[3]	IN	W17
sw[2]	IN	W16
sw[1]	IN	V16
sw[0]	IN	V17