1 GHz Instantaneous Bandwidth Digital Pre-Distortion for Multi-Concurrent Channel Wideband Power Amplifiers

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Abstract — This paper presents an extremely broadband digital predistortion linearization (DPD) technique that uses an adaptive Volterra-based model of the nonlinear distortion transfer function. The model is parameterized to accommodate higher order terms as necessary to accurately approximate the actual broadband nonlinear transfer function. The algorithm uses matrix and tensor factorizations to significantly simplify the complexity of the hardware implementation by identifying and removing mathematical redundancy and ignoring the components of the model that have negligible impact on the performance. This results in fewer multiplications and allows the addition of higher order terms to the model without the exponential growth in complexity. Polyphase filtering techniques are also used to run these operations in parallel which allows very broadband operation using signal processing operating at much lower data rate commensurate with the capabilities of off-the-shelf FPGAs. Measured results of the linearization technique are presented for multi-carrier concurrent waveforms into a 100 W GaN power amplifier showing an improvement in intermodulation products of more than 30 dB over an instantaneous bandwidth of 1 GHz. To our knowledge, this is far higher instantaneous bandwidth than other wideband DPD linearization techniques published in the literature.

Index Terms — Digital predistortion (DPD), linearization, multi-channel, Volterra series, power amplifiers.

I. INTRODUCTION

Modern communications utilize complex varying envelope waveforms with high peak-to-average power ratio (PAPR) that induce phase and amplitude errors when amplified by power amplifiers due to the latter's nonlinearity. The distortion of the amplifier is not fixed but can change slowly due to temperature or other environmental effects, which are denoted as memory effects. A broadband multi-octave power amplifier especially faces additional challenges when amplifying single or multiple signals across its broad bandwidth. Not only does a broadband amplifier produce Error Vector Magnitude (EVM) and spectral re-growth distortion of the input waveforms, but it also generates harmonics of the intended signals that can appear within the RF bandwidth of the amplifier and cannot be filtered as in the case of a narrow band amplifier.

Digital Predistortion has been a popular linearization technique used in abundance for communication transmitters, especially in conjunction with Doherty power amplifiers to maintain high efficiency when backed off. However, the technique has been limited for relatively narrow bandwidths, although indeed Doherty power amplifiers have been demonstrated recently with near octave bandwidth.

Several wideband DPD linearization techniques have been proposed in the literature, covering long-term evolution (LTE) and LTE-advanced bandwidth requirements up to 100 MHz, e.g. [1-4]. In [1], a pruned Volterra model was proposed to take into account the impact of phase distortion observed in multi-band PAs as well as the compound amplitude distortion over a wide bandwidth. In [2], an under-sampled analog-to-digital converter (ADC) technique obviates the need for a high-speed ADC in the feedback path for wide bandwidth processing. In [3], a baseband equivalent Volterra series is proposed for the behavioral modeling and linearization of wideband RF power amplifiers. And in [4], a band limited Volterra series-based DPD technique is proposed for the linearization of wideband power amplifiers.

Similar to the above papers, the technique described in this paper is also based on a Volterra series model of the non-linear transfer function of the power amplifier. The model is parameterized to accommodate higher order terms, such as fifth-order or seventh-order components, and therefore can more accurately approximate the actual, broadband non-linear transfer function. In addition, increasing the memory of the model is akin to adding coefficients to an FIR filter for more accurate frequency response. Traditionally, however, augmenting the model in this way exponentially increases the complexity of the hardware implementation of the digital signal processing. To date, these practicalities have limited the bandwidth of DPD techniques to 100 MHz or less.

Our technique achieves 1 GHz instantaneous bandwidth by using matrix and tensor factorization to significantly simplify the complexity of the hardware implementation by identifying and removing mathematical redundancy and ignoring components of the model that have negligible impact on the performance. Polyphase filtering techniques are also used to run these operations in parallel to allow very broadband operation using signal processing operating at a much lower data rate commensurate with the capabilities of standard commercial FPGAs. For example, for 1 GHz instantaneous bandwidth, a data rate of 3.04 GHz is used; the data is demultiplexed to provide sixteen parallel channels each with a data rate of 190 MHz, which is then suitable for implementation in a standard FPGA.

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II. Overview of the Technique

As depicted in Figs. 1-4, the wideband Volterra nonlinear model is used to digitally process the raw (i.e, not linearized) input signal, $x[n]$ (Fig. 1), to generate the pre-distorted input to the amplifier, $y[n]$ (Fig. 2), such that the output of the amplifier represents an accurate, amplified version of the raw input (Fig. 4). Harmonic and intermodulation distortion is reduced by more than 30 dB. The raw, uncompensated output of the amplifier is also shown (Fig. 3).

A. Wideband Volterra Nonlinear Model

The pre-distorted system output, $y[n]$, is generated by an M^{th} order Volterra model that is comprised of the summation of M Volterra operations on the input signal, $x[n]$, given by

$$y[n] = \sum_{m=1}^{M} y_m[n] = \sum_{m=1}^{M} \langle H_m, x[n] \rangle \tag{1}$$

where the m^{th} order term is the tensor inner product between the m^{th} order Volterra kernel, h_m, and the m^{th} order tensor outer product of the input signal, $x[n]$, given by

$$\langle H_m, x[n] \rangle = \sum_{k_1=1}^{K} \sum_{k_2=1}^{K} \cdots \sum_{k_M=1}^{K} h_m[k_1, k_2, \cdots, k_M] \prod_{l=1}^{M} x[n - k_l - 1] \tag{2}$$

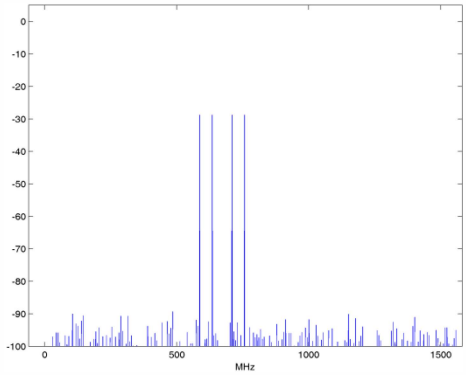

Fig. 1. Raw (not linearized) digital input signal. Amplitude [dB] corresponds to +42 dBm power amplifier output.

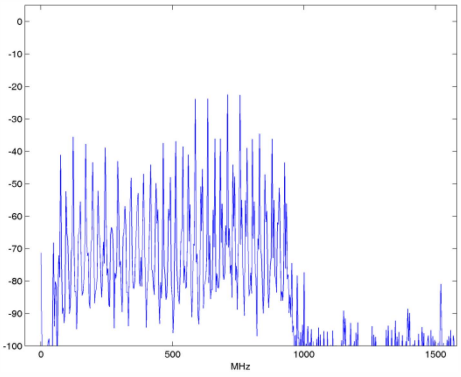

Fig. 2. Pre-distorted digital input signal to the power amplifier signal using broadband nonlinear model.

where K represents the memory of the system. The order M is chosen based on the observed order of nonlinearity in the RF power amplifier being pre-distorted. Generally an $M = 5^{th}$ order model is sufficient for a wide range of RF power amplifier architectures over a wide bandwidth (e.g., 1 GHz), but the linearizer is parameterized to support higher orders. During factory calibration, the Volterra kernels, h_m, are estimated via harmonic probing [5], by injecting multi-tone test calibration signals, evaluating the resulting harmonic and intermodulation signal levels, and using LMS and MINIMAX algorithms to estimate the coefficients of the Volterra kernels, h_m.

The nonlinear transfer function of the RF power amplifier exhibits fading memory, so initially, the Volterra memory, K, is chosen to be conservatively large to accurately gauge the memory required to accurately represent the system. The initial, raw Volterra kernels are therefore unnecessarily large and can first be truncated or windowed to discard negligible contributions.

B. Low-Rank Volterra Approximation

The Volterra kernels, h_m, are matrices or tensors that can be further simplified via factorization with techniques such as Singular Value Decomposition (SVD), Tucker Decomposition, and parallel factors (PARAFAC / CANDECOMP) [5-6] to identify and rank the level of the primary modes of the kernel. The low-ranking components

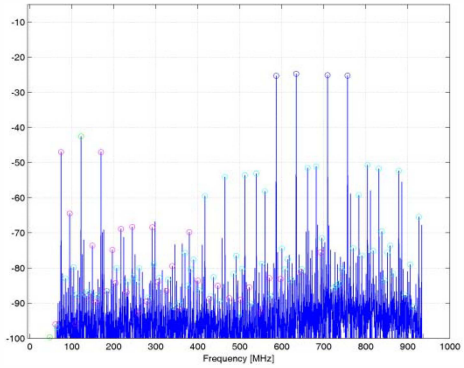

Fig. 3. Raw (not linearized) power amplifier output.

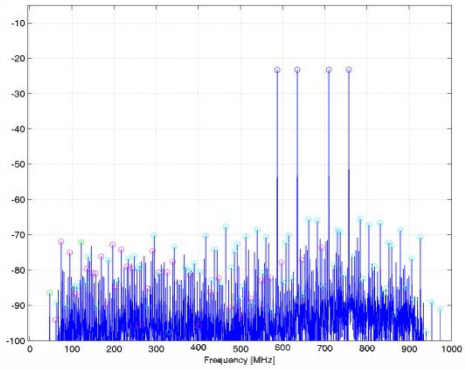

Fig. 4. Linearized power amplifier output. Amplitude [dB] corresponds to +42 dBm amplifier output.

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(i.e., modes with level below a prescribed threshold) can safely be discarded without appreciable loss of accuracy.

For example, the second-order Volterra kernel, the SVD factorization is given by

$$H_2 = U\Sigma V^T \tag{3}$$

where Σ is a diagonal matrix comprising the M singular values in descending level. Due to the inherent symmetry of the Volterra kernels, the matrices $U = V^T$. By discarding negligible contributions from singular values below the prescribed threshold to form the reduced rank diagonal matrix $\hat{\Sigma}$ and its corresponding reduced rank matrix $\hat{U}$, a reduced rank approximation of the Volterra can be formed as follows

$$H_2 \approx \hat{H}_2 = \hat{U}\hat{\Sigma}\hat{U} \tag{4}$$

Similarly, reduced rank approximations of the higher order Volterra kernels can be derived using Tucker or PARAFAC / CANDECOMP decompositions to factor the kernel into its primary modes and discard its negligible components.

Another key to significantly reducing the complexity of implementing the Volterra filtering is to exploit the extreme symmetry inherent in the Volterra kernels, namely, $h_m[k_1, k_2, \cdots, k_m]$ are identically equal for all permutations of $[k_1, k_2, \cdots, k_m]$. This dramatically reduces the implementation complexity from K^m total coefficients to $\binom{K+m-1}{m}$ unique coefficients. For example, a fifth-order Volterra kernel ($m = 5$) with memory $K = 8$ has 32,768 total coefficients, of which 792 are unique (a reduction of over 97%).

C. Fast FIR Filter Implementation

The unique Volterra coefficients of the reduced rank approximation of the kernel, $\hat{H}_m$, are implemented in P parallel FIR filters, $f_{m,p}[r]$,

$$\langle \hat{H}_m, x[n] \rangle = \sum_{p=1}^{P} \left(\prod_{l=1}^{M} x[n - k_l - 1] \right) * f_{m,p}[r] \tag{5}$$

(where $*$ denotes convolution). The FIR filters, $f_{m,p}[r]$, represent the main and offset diagonal coefficients of the Volterra kernel matrix ($m = 2$) or tensor ($m \geq 3$).

For applications such as this with extremely wide bandwidth, each of the FIR filters can be implemented as parallel polyphase filters at a lower data rate commensurate with the capabilities of commercial off-the-shelf FPGAs.

An FIR filter $F(z)$ can be implemented in an L-way polyphase filter structure at $1/L$ the effective data rate by demultiplexing the input, $X(z)$, by a factor of L (i.e., $X_0(z), X_1(z), \cdots, X_{L-1}(z)$) and filtering such that

$$\begin{aligned} Y_d(z) = &\left(\sum_{i=0}^{d} F_i(z)\ X_{d-i}(z) \right) \\ &+ z^{-L} \left(\sum_{i=d+1}^{L-1} F_i(z)\ X_{L+d+i}(z) \right), \\ &0 \leq d \leq L-2 \\ Y_{L-1}(z) = &\left(\sum_{i=0}^{L-1} F_i(z)\ X_{L-1-i}(z) \right) \end{aligned} \tag{6}$$

where $F_i(z)$ are the polyphase components of the filter $F(z)$, and $Y_d(z)$ represent the demultiplexed output, $Y(z)$.

The approach also adaptively monitors the error signal (i.e., the difference between the power amplifier's output and its raw input). When the error signal exceeds a defined threshold (for example, due to drift over temperature, change in operating conditions, change in signal conditions, etc.), the algorithm will update the model coefficients to bring the error below the threshold, thereby insuring optimal performance in changing conditions.

III. Experimental Setup

The approach has been demonstrated in realtime hardware by linearizing a 100W GaN solid-state power amplifier from Aethercomm, Inc. over the frequency range of 20 MHz to 1000 MHz.

As shown in Fig 5., a custom-built system includes a Xilinx Virtex-6 (XC6VSX475T) FPGA, a MAXIM (MAX19693) 12-bit digital-to-analog converter running at 3 GSPS to generate the pre-distorted signals, an RF coupler and Texas Instruments (ADC12D1800RF) 12-bit analog-to-digital converter running at 3 GSPS to monitor the amplifier output. A laptop computer is used for data capture and analysis.

IV. Test Results

A series of arbitrary test signals was digitally generated to characterize the performance of the system in various operating conditions over its 1 GHz instantaneous bandwidth, including single and multi-tone CW signals and multiple

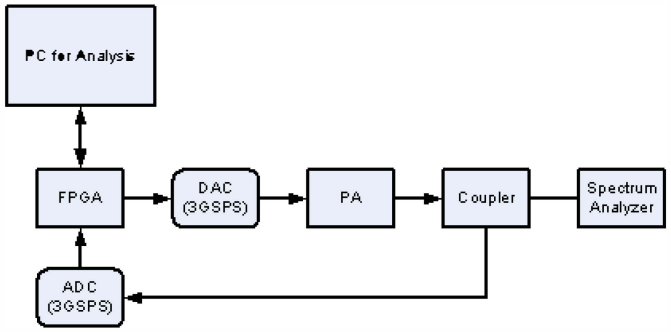

Fig. 5. Realtime Hardware Experimental Setup for 1 GHz DPD

simultaneous passband signals, as shown below. For the performance analysis, data was captured both by the feedback ADC and with a spectrum analyzer connected to the power amplifier output. The multi-tone CW test results are shown in Figs. 1-4.

To demonstrate the amelioration of spectral regrowth, a signal was designed with two wideband passband signals, as shown in Fig. 6 and Fig. 7. The spectral regrowth from both signals bleeds into the band between the two signals and to higher frequencies, thereby degrading the adjacent channel leakage ratio (ACLR). The nonlinearity also affects the spectral shape of the bandpass signals themselves. The linearizer effectively removes these distortion components and corrects the original spectral shape of the signals.

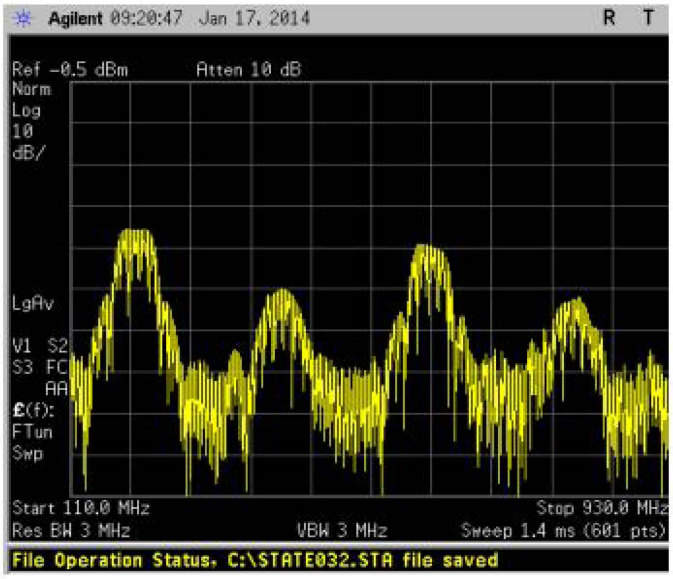

Fig. 6. Spectrum analyzer display of dual passband waveforms without linearization.

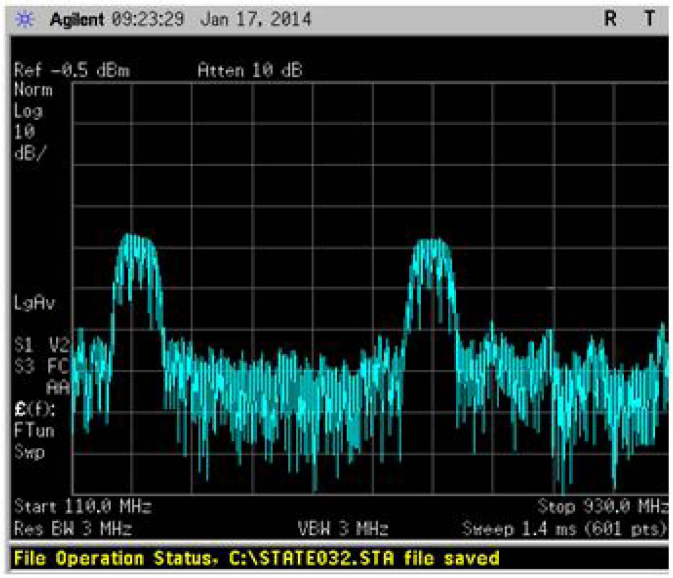

Fig. 7. Spectrum analyzer display of linearization of the dual passband waveforms.

V. Conclusion

An extremely broadband power amplifier pre-distortion linearizer with over 1 GHz instantaneous bandwidth has been demonstrated in realtime hardware with a variety of waveforms. This represents an order of magnitude bandwidth improvement compared to traditional pre-distortion techniques. The approach takes advantage of extremely computationally-efficient digital signal processing to accurately model the very wideband nonlinear transfer function of power amplifiers. The processing can be implemented in standard commercial off-the-shelf FPGA hardware, and is highly parameterized so that it can be easily customized for different applications (e.g., bandwidths, frequency ranges, power outputs, size, cost, etc.). Experimental results using a 100W GaN solid-state power amplifier over the frequency range of 20 MHz to 1000 MHz demonstrate greater than 30 dB improvement in harmonic and intermodulation distortion. This represents a significant improvement in amplifier efficiency because, without linearization, a much higher power amplifier would have to be used in a severely backed-off condition (e.g., input reduced by more than 15 dB) to achieve the same power output and linearity.

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