0.6-V 2.1-mW RF receiver based on passive mixing and master–slave common-mode rejection technique in 65 nm CMOS

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A 0.6-V 2.1-mW RF receiver with regular threshold transistors is presented. A passive mixer which is built on low-power current-buffer is designed to build the RF front-end. A master–slave operational transconductance amplifier (OTA) structure which provides sufficient common-mode rejection ratio (CMRR) by auto-adjusting the gate of the triode-region biased tail current source is proposed as the building block of the intermediate-frequency (IF) modules. The proto-type of the RF receiver is designed and fabricated in Semiconductor Manufacturing International Corporation (SMIC) 65 nm CMOS process. The measurement indicates that the receiver covers a bandwidth from 1 to 1.5 GHz, achieving a voltage gain of 32 dB and a noise figure (NF) of 10 dB.

Introduction: For the application of portable wireless consumer electronics, low power consumption is especially crucial to prolong the lasting time of the battery powered devices. Current reusing techniques which share the static current of several current-hungry modules, reduces the total power dissipation dramatically [1–3]. However, the inter-module crosstalk cannot be completely avoided in the current reusing structures. Besides the current-reducing approaches, another intuitive idea to cut down the total power consumption is reducing the supply voltage. Designing circuits under a supply voltage as low as 0.6 V makes it possible to be powered by a single solar-cell. However, the 0.6 V inter-space between vdd and gnd can only accommodates two transistors working in saturated region, leading to voltage headroom issues. Circuit with cascode structure such as a Gilbert mixer has to be avoided in the RF front-end design. For the IF modules in RF receivers, the OTA is an important building block to make up filters and programmable-gain amplifiers (PGAs). However, the classic OTA structure cannot be directly transplanted into the 0.6 V design because of the insufficient voltage headroom [4, 5]. Receivers using low threshold transistors have been introduced by previous works, but it faces leaking current issues.

In this Letter, a prototype of the 0.6 V receiver with regular threshold transistors is designed and fabricated in SMIC 65 nm CMOS process. A passive mixer based on low-voltage current-buffer is proposed to form the RF front-end of the receiver. The current-buffer is designed to have only two stacked transistors between vdd and gnd. As the fundamental block of the IF modules such as filters and PGAs, a master–slave OTA structure which can realise sufficient common-mode rejection under low supply voltage is also proposed.

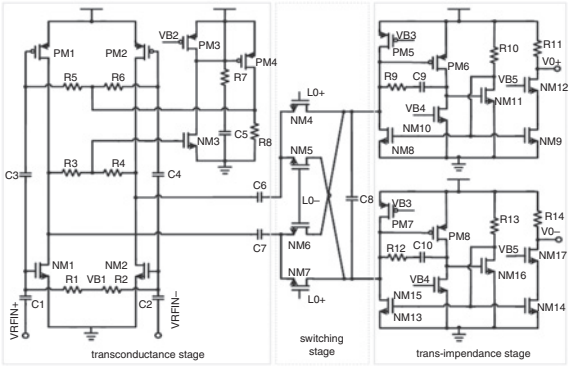

Fig. 1 *Circuit schematic of proposed 0.6 V passive mixer*

Circuit design: Fig. 1 shows the circuit schematic of the proposed passive mixer. The V_{GS} of the transistors in the CMOS transconductance (gm) stage are set close to the supply voltage to obtain adequate bandwidth. The dc bias voltage at the output node of the gm stage is set equal to the V_{GS} of NM3 by the low-voltage common-mode feedback circuit. With the low input impedance of the current-buffer, the passive mixing core makes the output of the gm stage a virtual ground at the local oscillator (LO) frequency. The RF current is down-converted into IF band, which is converted into IF voltage by the current-buffer. The current-buffer is based on negative feedback which turns the input current into the V_{GS} variations of NM8. The current of NM9 is mirrored from NM8, copying the IF current and converts it into output voltage on the load resistors R11/R14. The feedback loop in the current-buffer is constituted by three common-source amplifier stages. For the ease of stability design, the value of R10 is minimised to limit the loop gain. There are at most two transistors stacked between vdd and gnd, which makes it suitable for the 0.6 V supply voltage.

Fig. 2 shows the circuit schematic of the proposed two-stage OTA. To be used in the receiver IF circuits, single-output (MS-SOTA) and differential-output (MS-DOTA) structures are both proposed. The first stage is a master–slave structure which provides input common-mode rejection. The second stage is a common-source amplifier with current-source-load. The transistors in the master stage are the proportional duplications of those in the slave stage. The sizes of P5, P6 and P7 are half of P2, P3 and P4, respectively. P2 and P5 are biased in triode region to spare voltage headroom. In the master stage, the gate of P5 is connected to the drain of N4, forming a negative feedback loop which sets the current of P5 equal to that of N4 under the voltage fluctuations at the gates of P6 and P7. The current source N4 is biased in saturated region to provide a stable current. The V_{GS} of N2, N3 is designed to be close to the V_{DS} of N4. The gates of P2, P3 and P4 are connected to P5, P6 and P7, respectively. Ignoring the channel modulation effect of the input transistors which are biased in saturated region, the V_{DS} of P5 tracks the V_{DS} of P2. So the total current in the slave stage is identical with the current in the master stage and is fixed by N4. Sufficient CMRR can thus be achieved in the slave stage.

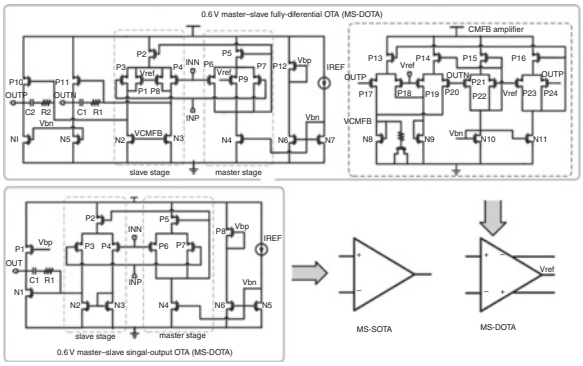

Fig. 2 *Circuit schematic of proposed 0.6 V master–slave OTA*

The expression of the low-frequency CMRR of the proposed near-threshold OTA is given by the following equation:

$$\mathrm{CMRR}_{ms} = 2g_{\mathrm{mN3}}\left(r_{\mathrm{oP2}} + \frac{1}{2g_{\mathrm{mP3}}}\right)\left(1 + \frac{g_{\mathrm{mp2}}r_{\mathrm{oN4}}}{2}\right)g_{\mathrm{mP3}}r_{\mathrm{oN3}} \parallel r_{\mathrm{oP3}} \quad (1)$$

For a traditional OTA without the master–slave structure, the CMRR expression is indicated in the following equation:

$$\mathrm{CMRR}_{\mathrm{tr}} = 2g_{\mathrm{mN3}}\left(r_{\mathrm{oP2}} + \frac{1}{2g_{\mathrm{mP3}}}\right)g_{\mathrm{mP3}}r_{\mathrm{oN3}} \parallel r_{\mathrm{oP3}} \quad (2)$$

For the traditional OTA structure working under a supply voltage of 0.6 V, the limited r_{oP2} leads to a dramatic degradation of CMRR. As for the proposed OTA, the CMRR is boosted by $1 + g_{\mathrm{mp2}}r_{\mathrm{oN4}}/2$ which is about 20–30 dB since N4 is biased in saturated region. Therefore, even though P2 is biased in triode region, sufficient CMRR can still be guaranteed.

In a fully-differential OTA, output common-mode feedback circuit is indispensable. As indicated in Fig. 2, the master–slave structure is also used in the common-mode feedback amplifier within the MS-DOTA.

Using MS-SOTA and MS-DOTA as building blocks, the traditional topology of IF modules based on OTAs [6] can be transplanted directly into the 0.6 V design. Fig. 3 gives the topologies of the IF blocks in the 0.6 V receiver. The input of the filter is AC coupled with an off-chip capacitor to remove the DC offset from the mixer.

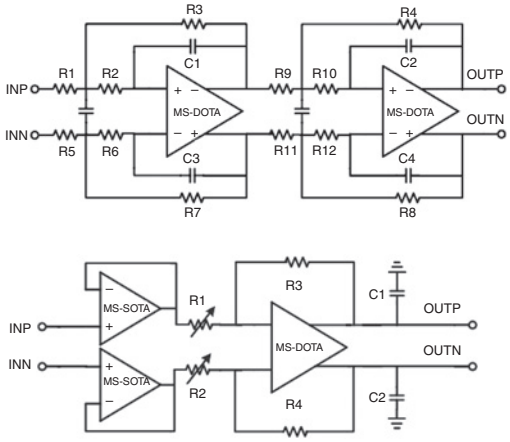

Fig. 3 *Circuit structure of 0.6 V low-pass filter and PGA using MS-DOTA and MS-SOTA as building blocks*

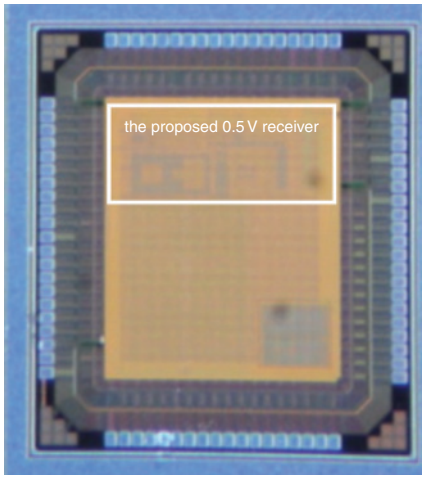

Fig. 4 *Chip micrograph*

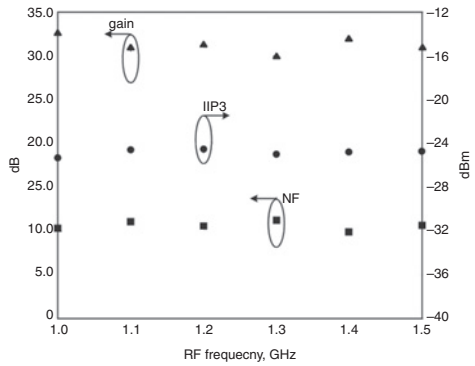

Fig. 5 *Measured gain, NF and IIP3 against RF with a fixed 2 MHz IF*

Table 1: Comparison with other designs

	[1]	[3]	This work
Frequency band, GHz	1.6	0.91	1–1.5
IF −3 dB bandwidth, MHz	5	6	4
Gain, dB	36	44.5	33
DSB NF, dB	4.8	4.3	10
IIP3, dBm	−19	−14.5	−25
Power dissipation (PLL excluded), mW	5.4	8	2.1
Supply voltage, V	1.2	1.8	0.6
CMOS technology, nm	130	180	65

Measurement results: Fig. 4 shows the micrograph of the proposed receiver prototype. The active area is 0.8 mm × 0.4 mm and the total power consumption is 2.1 mW under a 0.6 V supply voltage. Fig. 5 indicates the measured gain, NF and IIP3 against RF of the proposed receiver. The maximum and minimum conversion gains are 33 and 30 dB, respectively. The measured minimum IIP3 is −25 dBm and the NF is about 10 dB. Table 1 compares the measured results with two other previous published works. With supply voltage cut down, the proposed receiver is superior to others in power consumption with the slight degradation of linearity performance.

Conclusion: This Letter proposes a 0.6-V 2.1-mW RF receiver in 65 nm CMOS. A low-voltage current-buffer is designed to build the passive mixer. A master–slave OTA, which can provide sufficient CMRR with triode-region biased tail current source, is proposed as the building block to form the IF modules. The receiver covers a bandwidth from 1 to 1.5 GHz, achieving a voltage gain of 32 dB and a NF of 10 dB.

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One or more of the Figures in this Letter are available in colour online.

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