G_m-Boosted Complementary Current-Reuse Colpitts VCO With Low Power and Low Phase Noise

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***Abstract*—In this letter, a transformer-based current-reuse Colpitts voltage controlled oscillator (VCO) is proposed, which combines a N-type and P-type Colpitts oscillators using a 5-port transformer in a complementary form to provide the differential outputs. The proposed VCO has low phase noise due to the low noise Colpitts oscillator topology and the negative-Gm boosting technique with half of the DC-current consumption using the current-reusing method. The proposed VCO has the frequency tuning range from 8.57 to 10.21 GHz, and shows low phase noise of $-110.6\ \mathrm{dBc/Hz}$ at 1 MHz offset frequency at 9.41 GHz and high figure of merit with tuning range (FoM^T) of $-191.8\ \mathrm{dBc/Hz}$. The power consumption is 2.1 mW from 1.2 V supply voltage. The VCO is implemented using 0.13 μm CMOS process with chip area of 0.45 mm^2.**

***Index Terms*—G_m boosted, CMOS, Colpitts, complementary, current-reuse, voltage controlled oscillator (VCO).**

I. Introduction

THE demand on the low power voltage controlled oscillator (VCO) is being increased for the wireless sensor applications, since the local oscillator still makes a significant portion of the current consumption in the battery-driven system. Several circuit techniques for reducing the current consumption of the VCO are reported including the current-reuse technique [1], [2]. Another stringent requirement for the VCO is to achieve low phase noise. The Colpitts oscillator is well known for having low phase noise characteristic due to the inherent immunity to the flicker and thermal noise of the active devices [3]. However, the Colpitts oscillator requires relatively more current in generating the same negative-G_m than that of a differential cross-coupled oscillator. To achieve low phase noise performance and low power characteristics simultaneously, a novel circuit technique is needed for the conventional Colpitts oscillator. Additionally, since the inductors occupy a large portion of the VCO chip, a single inductor or a single transformer configuration is recommended.

In this letter, a complementary current-reuse Colpitts VCO (CRC-VCO) is proposed, which combines a single transistor-based N-type and P-type Colpitts VCOs using a 5-port transformer in a complementary form. The proposed VCO exhibits low phase noise due to the inherent low phase noise characteristic of the Colpitts oscillator topology and draws low dc current due to the current-reuse configuration. The 5-port transformer is used to enhance the negative-G_m of the VCO, which results in lowering phase noise and power consumption, and also reducing chip area.

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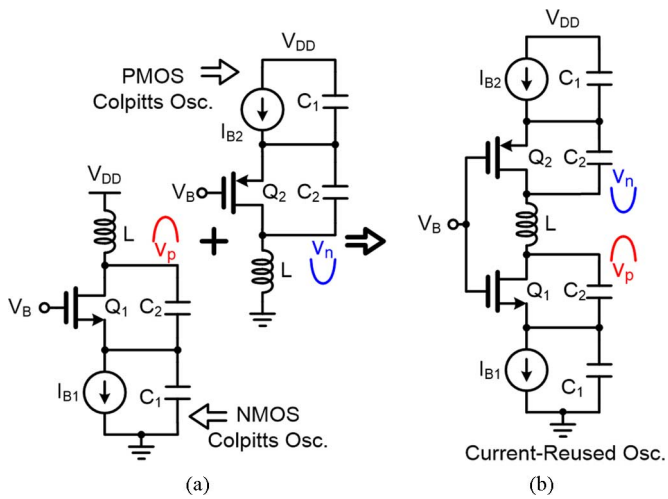

Fig. 1. (a) Schematic diagrams of the single-transistor based NMOS and PMOS Colpitts oscillators and (b) the complementary Colpitts oscillator using current-reuse technique.

II. Current Reuse Colpitts VCO Design

Fig. 1(a) shows a NMOS and PMOS Colpitts oscillators using drain to source capacitive feedback with a single transistor. If the drain voltages of the two oscillators have opposite polarities, the two Colpitts oscillators can be combined as one complementary Colpitts oscillator by sharing the inductor L and connecting the gate bias nodes V_B. Fig. 1(b) shows the conceptual complementary Colpitts oscillator, which can provide the differential voltages v_p and v_n. The gate dc bias V_B is set to a voltage that provides equal transconductance $g_{m1,m2}$ for Q_1 and Q_2, and the bias currents I_{B1} and I_{B2} are set to match each other.

The negative-G_m of the above Colpitts oscillator is given as $-n \cdot g_m$, where n is the capacitive feedback ratio $\mathrm{C}_2/(\mathrm{C}_1 + C_2)$ and g_m is the transconductance of the transistor. To enhance the negative-G_m, a drain to gate voltage feedback using a transformer is employed as shown in Fig. 2(a). The transformer also provides a means of the self DC-biasing by connecting the center-tap node A between the gate inductor L_1 and the drain inductor L_2. This connection simplifies the dc bias circuit. Since

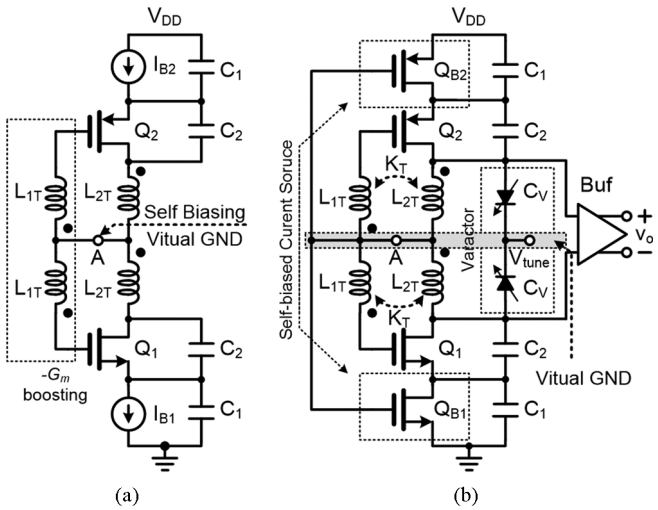

Fig. 2. (a) Schematics of the CRC oscillator using a transformer and (b) the CRC-VCO including the self-biased current sources, the varactors for frequency tuning, and the output buffer.

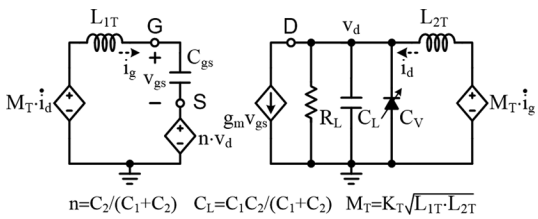

Fig. 3. Half equivalent circuit of the CRC-VCO.

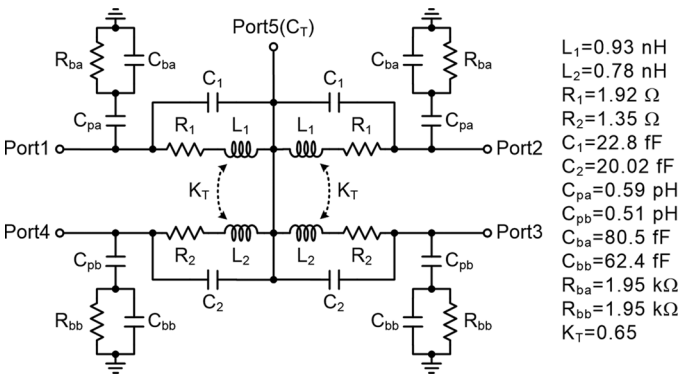

Fig. 4. Equivalent circuit of the 5-port transformer.

the PMOS and NMOS work differentially, the center nodes is virtually grounded. Fig. 2(b) shows the proposed complementary current-reuse VCO, where the bias currents I_{B1} and I_{B2} are also realized by connecting the gate nodes to the center tap voltage. This connection automatically matches two currents. For the frequency tuning, the accumulation NMOS varactors are used. And the self biased inverter-type output buffers are employed with high resistance feedback.

The small signal half equivalent circuit of the proposed VCO using the virtual ground is illustrated in Fig. 3, where the output impedance of the transistor is assumed as infinite. The negative-G_m in the proposed VCO is generated by two feedbacks: one is the capacitive feedback through C_1 and C_2, and the other is the magnetic coupling through the transformer. The v_{gs} is determined by impedance dividing ratio of the feedback voltage and feedback current as $v_{gs} = -\mathrm{n} \cdot \mathrm{v}_d + \mathrm{M}_T \cdot \dot{i}_d$, because the impedance of C_{gs} is much higher than that of L_{2T}. Since the

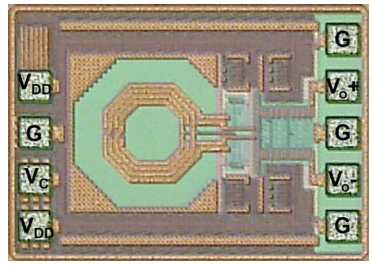

Fig. 5. Micro-photograph of the proposed CRC-VCO.

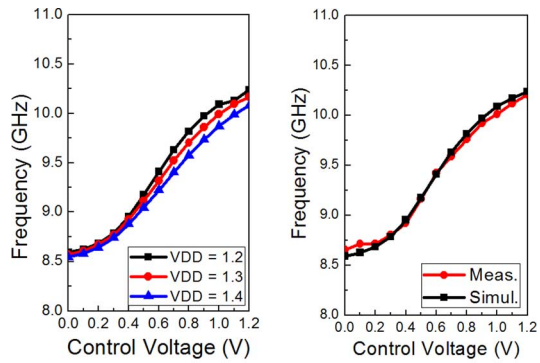

Fig. 6. (a) Measured VCO frequencies with V_{DD} variations and (b) the oscillation frequency comparison of the measurement and simulation.

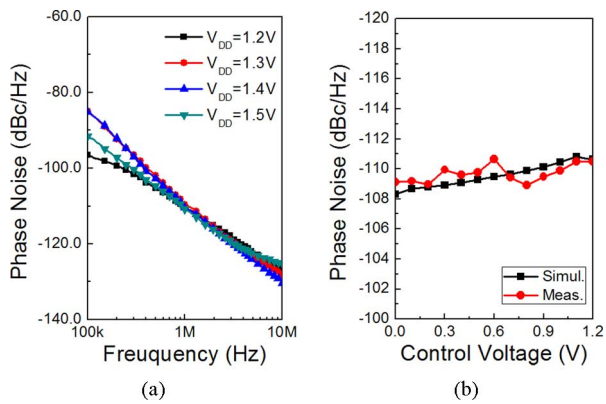

Fig. 7. (a) Measured phase noise at 9.41 GHz with $V_{DD} = 1.2 - 1.5$ V and (b) the measured phase noises vs. the varactor control voltages.

gate current i_g is very small, the total negative-G_m of the half VCO is simplified as

$$G_{m,T} = -g_m \left(n + K_T \sqrt{\frac{L_{1T}}{L_{2T}}} \right), \quad g_m = g_{m,n} = g_{m,p}. \quad (1)$$

The negative-G_m is boosted by the mutual coupling factor of the transformer. The gate inductance is designed to be higher than the drain inductance to maximize the negative-G_m. The enhanced negative-G_m reduces the current consumption of the proposed VCO. The oscillation frequency is mainly determined by the resonance frequency at the drain as

$$f_{osc} \simeq \frac{1}{2\pi \sqrt{L_{2T} \cdot (C_L + C_V)}}. \quad (2)$$

The gate widths of the core NMOS transistors (Q_1 and Q_{B1}) are 36 μm and 108 μm, respectively, and the gate widths of the PMOS transistors (Q_2 and Q_{B2}) are 2 times larger than that of

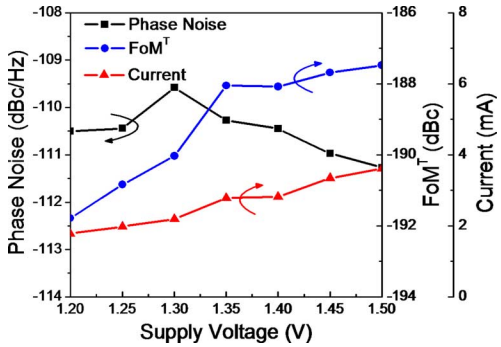

Fig. 8. Measured phase noises, current consumptions, and FoM^T vs. V_{DD}.

TABLE I
COMPARISONS OF THE EVER-REPORTED VCOS WITH THE CRC-VCO

	This	[3]	[5]	[6]	[7]	[8]	Unit
Tech.	0.13	HBT	0.13	0.18	0.18	0.18	μm
Config.	CR-Colpitts	Colpitts	Armstrong	Colpitts	CR-Colpitts	Hartley	-
Freq.	8.57-10.21	12.7-13.5	13-14.8	7.4-7.9	5.23-5.27	5.48-5.63	GHz
FTR	17.4	3.16	13.3	7	0.84	2.7	%
L(1MHz)	-110.6	-113.8	-100.6	-108.3	-117.6	-122.7	dBc/Hz
FoM	-186.9	-180.7	-186	-179.3	-191.8	-189.6	dBc/Hz
FoM^T	-191.8	-169.3	-189	-176.2	-170.3	-178.2	dBc/Hz
V_{DD}	1.2	3	0.4	1.8	1	1.4	V
I_{DC}	1.75	16	1.5	2.72	1.05	4.6	mA
Area	0.45	0.574	0.455	0.552	0.99	0.59	mm^2

the NMOS. The capacitances of C_1 and C_2 are 25 and 65 fF with the associated capacitance ratio n of 0.28. The oscillation frequency range is set to be 8.57–10.21 GHz. The transformer employed in the VCO was simulated using 2.5D EM simulator, *Sonnet*, and the S-parameter was included in the circuit simulation as well as the interconnection lines. The equivalent circuit of the 5-port transformer is described with the circuit parameters in Fig. 4 [4].

III. EXPERIMENT RESULTS

The proposed transformer-based complementary CRC-VCO is implemented using a 1P8M 0.13 μm TSMC CMOS process. Fig. 5 shows the photograph of the fabricated VCO. The chip size is 0.56×0.8 mm^2 including all pads. The output frequency and the phase noise performances are obtained by Agilent E4440A spectrum analyzer. Fig. 6(a) shows the oscillation frequencies as a function of the varactor control voltage, in which the supply voltage varies from 1.2 to 1.4 V in 0.1 V step. The oscillation frequency at $V_{DD} = 1.2$ V is 8.57–10.21 GHz with the tuning range of 1.64 GHz (17.4%). The frequency discrepancy between the simulated and measured frequencies in Fig. 6(b) is very small in all the control voltage range. The measured phase noise performance at 9.41 GHz is shown in Fig. 7(a). The measured phase noises are -96 and -110.6 dBc/Hz at 100 kHz and 1 MHz offset, respectively at 1.2 V supply voltage. The phase noise variations with the control voltage change are less than 2 dB as shown in Fig. 7(b). Fig. 8 shows the measured phase noise, current consumption, the figure of merit with tuning range (FoM^T) at the center frequency versus the supply voltage. The phase noise is from -111 to -109 dBc/Hz and the FoM^T is from -187.5 to -191.8 dBc with the supply voltage variations from 1.2 to 1.5 V, where the equation for (FoM^T) is as follows:

$$FoM^T = L(\Delta f) + 10\log\left(\frac{P_{diss}}{1\ \mathrm{mW}}\right) - 20\log\left(\frac{f_{osc}}{\Delta f}\right) - 20\log\left(\frac{FTR}{10\%}\right) \quad (3)$$

where L is the measured phase noise at the frequency of f_{osc} with the offset frequency of Δf, *FTR* is the frequency tuning range in %, and P_{diss} is the power consumption of the VCO core in milliwatt. The proposed CRC-VCO shows comparable phase noise, low power consumption, lowest FoM^T, and smallest chip area as summarized in Table I [3], [5]–[8].

IV. CONCLUSION

In this letter, a new complementary current-reuse Colpitts VCO is proposed. The proposed VCO achieves low phase noise and low power consumption, simultaneously by using the current-reuse technique and the Colpitts configuration. The two single transistor-based Colpitts oscillators are combined using a five-port transformer in a small chip area. The proposed VCO shows low phase noise of -110.6 dBc/Hz at 1 MHz offset frequency at 9.41 GHz with high FoM^T of -191.8 dBc/Hz. The VCO consumes low dc power of 2.1 mW. And the frequency tuning range is about 17.4% from 8.57 to 10.21 GHz. The VCO is implemented using 0.13 μm CMOS process with chip area of 0.57×0.8 mm^2.

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