G_m-Boosted Differential Drain-to-Source Feedback Colpitts CMOS VCO

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***Abstract*—This paper proposes a g_m-boosted differential drain-to-source feedback Colpitts voltage-controlled oscillator (VCO) that allows larger output oscillation amplitude while keeping the switching transistor from triode-mode operation such that lower optimal close-in phase noise can be obtained by delaying the AM-to-FM conversion by the switching transistors. The phase-noise behavior of the proposed VCO is analyzed and compared with previously reported g_m-boosted Colpitts and conventional NMOS-only *LC*-VCOs, and it is demonstrated in comparison that the proposed VCO can provide 2- and 4-dB lower optimum figure of merit, respectively. The feedback capacitor ratio effect of the proposed VCO is also explored and shown the directions of the capacitor ratio for better phase noise. The proposed VCO is implemented in 0.18-μm CMOS for 1.76–1.93-GHz operation. Measurement shows, at 1.84 GHz, the phase noise of -104 and -126 dBc/Hz (FOM $=$ 190 dBc/Hz) at 100-kHz and 1-MHz offset, respectively, while dissipating 1.5 mA from 0.9-V supply.**

***Index Terms*—AM-to-FM conversion, CMOS, Colpitts, flicker noise, phase noise, voltage-controlled oscillator (VCO).**

I. Introduction

DEEP-SUBMICROMETER CMOS processes are attractive for future RF technology since convergence of the multistandard and multiband wireless systems requires low power, small area, and low-cost design. However, the increasing flicker noise by decreasing the size of the MOS transistor and the hot carrier effect degrades the noise performance of the analog and RF circuits [1], [2]. In addition, the downscaling of channel length reduces the supply voltage. With an integrated voltage-controlled oscillator (VCO), those technical issues lead to phase-noise degradation due to the flicker-noise upconversion and the reduction of output oscillation amplitude, respectively.

The conventional NMOS-only cross-coupled differential VCO is widely used for its easy startup and implementation. On the contrary, the Colpitts oscillator can potentially achieve good phase noise due to its class-C operation, which has a short amount of the switching transistor on time and large oscillation amplitude at the peak. However, the Colpitts architecture was rarely adopted until a couple of years ago, due to its nondifferential output, poor startup, and relatively small oscillation amplitude, i.e., it requires higher power dissipation [3]–[6]. Lately, several g_m-boosted differential Colpitts architectures have been reported that overcome those shortcomings [3]–[10]. Furthermore, the recently reported g_m-boosted gate-to-source feedback Colpitts (GS-Colpitts) VCO has shown the reduction of the flicker-noise contribution in the close-in phase noise by suppressing the AM-to-FM conversion through the switching transistor capacitance nonlinearity [4]. Therefore, the g_m-boosted Colpitts is getting attention as an attractive oscillator topology in the deep-submicrometer CMOS technology.

Among the previously reported g_m-boosted drain-to-source feedback Colpitts (DS-Colpitts) VCOs, the one reported in [7] is not suitable for low supply design due to the limited voltage headroom, and of the two VCOs reported in [8], one of them is not fully differential, and the other one, which has two feedback paths, is susceptible to the AM-to-FM conversion by the switching transistors. This paper presents a differential Colpitts VCO architecture that improves startup condition and oscillation amplitude by a newly proposed drain-to-source (DS) feedback based g_m-boosting technique and shows lower optimal phase noise by keeping the switching transistor in the saturation region at the largest oscillation amplitude. In this paper, the close-in phase-noise behavior of the NMOS-only, the conventional Colpitts, and the proposed g_m-boosted DS-Colpitts VCOs are analyzed and compared, providing information that can be useful in design guidelines.

In Section II, the topology and g_m-boosting effect of the proposed DS-Colpitts VCO are described. The startup current and oscillation amplitude of the proposed VCO are compared with those of the previously reported oscillators. In Section III, the phase-noise characteristics of the proposed topology is analyzed and verified with simulation results. In Section IV, the analysis and simulation results are verified based on the measurement results of both proposed and conventional cross-coupled VCO prototypes and Section V concludes.

II. G_m-Boosted Differential DS-Colpitts CMOS VCO

There are three types of conventional single-ended, Colpitts oscillator topologies: gate-to-drain (GD), gate-to-source (GS), and DS capacitor feedback topologies [11]. The recently reported differential GD-Colpitts VCOs [9], [10] still show poor startup characteristics that result in high power consumption, while the g_m-boosted differential GS-Colpitts VCO [4] achieves lower startup current and good phase-noise characteristics. The majority of the reported g_m-boosting differential Colpitts VCOs are the DS capacitor feedback based [3], [7], [8].

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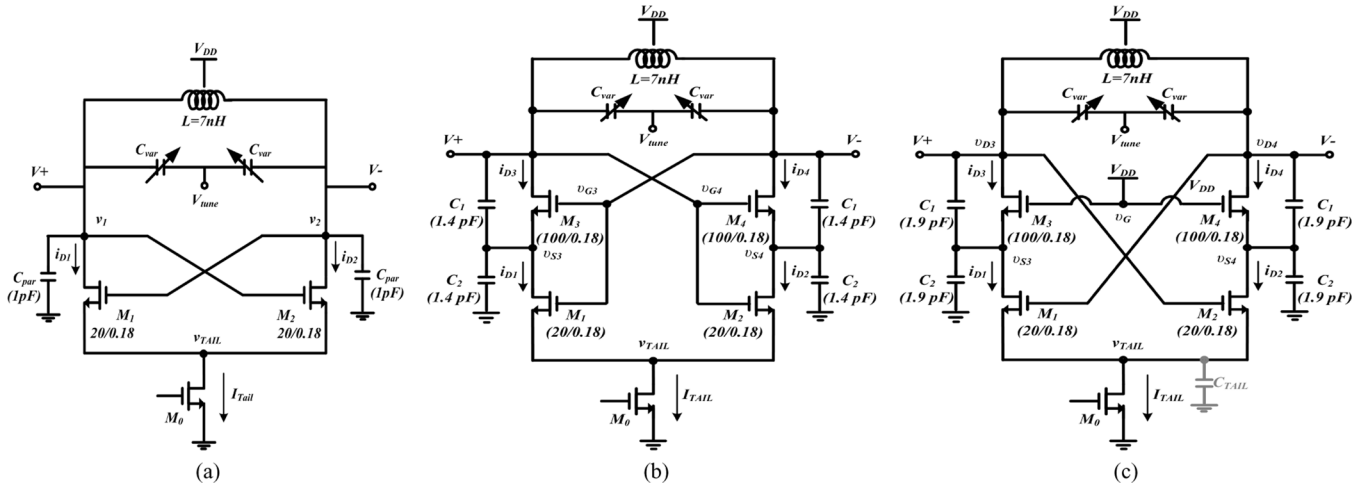


Fig. 1. Schematic of: (a) conventional NMOS-only, (b) Li *et al.*'s, and (c) proposed g_m-boosted differential DS-Colpitts VCOs.

Fig. 1 shows the schematics of three VCOs: the conventional NMOS-only cross-coupled, Li *et al.*'s DS-Colpitts [8], and the proposed g_m-boosted differential DS-Colpitts. In the newly proposed DS-Colpitts VCO shown in Fig. 1(c), the differential operation is obtained by adopting the tail current source M_0 and the startup condition is improved by the addition of the g_m-boosting transistor $M_{1,2}$. From Fig. 1(c), the gates of $M_{1,2}$ in the proposed DS-Colpitts VCO are connected to the drains of the opposite switching transistors $M_{3,4}$, while in Fig. 1(b), the gates of $M_{1,2}$ are tied together with $M_{3,4}$ for additional positive feedback. In Fig. 1(c), the drain terminal of the main positive feedback transistor $(M_{3,4})$ instead of the source is selected for the feedback signal sampling, which allows lower supply voltage operation. In the g_m-boosted DS-Colpitts VCOs shown in Fig. 1(b) and (c), the transistor size of $M_{3,4}$ are much larger than that of $M_{1,2}$ since the transistors (M_0, $M_{1,2}$, and $M_{3,4}$) must be biased in the saturation region to start oscillation.

The small-signal conductance seen by the *LC*-tank of the proposed DS-Colpitts [see Fig. 1(c)] VCOs is given by

$$\mathrm{Re}[Y_{\text{IN-DS}}] = -\frac{g_{m3}\omega^2 C_1 C_2}{{g_{m3}}^2 + \omega^2(C_1+C_2)^2} \cdot\frac{1}{2}\left[1 + \frac{{g_{m1}}^2}{\omega^2 C_1 C_2} + \frac{g_{m1}}{g_{m3}}\left(1+\frac{C_1}{C_2}\right)\right] \quad (1)$$

where g_{m1} and g_{m3} are the transconductance of the g_m-boosting $(M_{1,2})$ and switching transistors $(M_{3,4})$, respectively. The small-signal negative conductance of the conventional DS-Colpitts oscillator is given by [11]

$$\mathrm{Re}[Y_{\text{IN-CONV}}] = -\frac{g_{m3}\omega^2 C_1 C_2}{{g_{m3}}^2 + \omega^2(C_1+C_2)^2}. \quad (2)$$

Likewise, the small-signal negative conductance of the NMOS-only oscillator shown in Fig. 1(a) is given by

$$\mathrm{Re}[Y_{\text{IN}}] = -\frac{g_{m1}}{2} \quad (3)$$

It can be seen from (1)–(3) that the proposed g_m-boosted DS-Colpitts oscillators can provide higher small-signal negative conductance compared to those of the conventional Colpitts and NMOS-only cross-coupled oscillators. Therefore, the g_m-boosting transistors $M_{1,2}$ enhance the overall small-signal loop gain of the proposed DS-Colpitts oscillator, increasing the negative conductance and thus reducing the startup current. In the case of the g_m-boosted Li *et al.*'s Colpitts oscillator, its negative conductance can be more negative than that of the proposed oscillator due to the additional feedback generated by $M_{3,4}$. This means that the startup of Li *et al.*'s Colpitts oscillator can outperform that of the proposed DS-Colpitts oscillator.

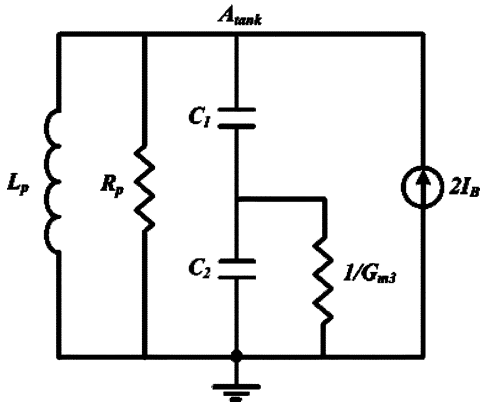


Fig. 2. Equivalent functional model of Colpitts oscillator.

Fig. 2 represents the equivalent large-signal model for the g_m-boosted DS-Colpitts VCOs shown in Fig. 1(b) and (c) to estimate the oscillation amplitude [12]. In Fig. 2, $1/G_{m3}$ represents the large-signal source–gate resistance of the transistor M_3 and the bias current $2I_B$ is twice the amount of the conventional Colpitts oscillator [6] since the g_m-boosting transistors M_1 generate a common source node for fully differential operation. Assuming a first harmonic current $2I_1$ generated by the transistor M_3 [6], the peak voltage amplitude generated by $2I_1$ is given by

$$V_{\text{peak}} = 2I_1\left(\frac{R_p}{n^2 G_{m3} R_p + 1}\right) = 4I_B\left(1-\frac{\Phi^2}{14}\right)\left(\frac{R_p}{n^2 G_{m3} R_p + 1}\right). \quad (4)$$

where $n \equiv C_1/(C_1+C_2)$, I_B, and Φ are the capacitive voltage divide factor, bias current, and conduction angle, respectively

[6]. In (4), for Li *et al.*'s DS-Colpitts oscillator [see Fig. 1(b)], the large-signal transconductance G_{m3} is given by

$$G_{m3\text{-Li}} \approx \frac{2I_1}{v_{\text{GS}} - V_{\text{th}}} \approx \frac{2I_1}{(1-n)V_{\text{peak-Li}}} \tag{5}$$

From (4) and (5), the peak amplitude of Li *et al.*'s DS-Colpitts $V_{\text{peak-Li}}$ is given by

$$V_{\text{peak-Li}} = 4I_{\text{bias}}\, R_p \left(1 - \frac{n^2}{1+n}\right)\left(1 - \frac{\Phi^2}{14}\right). \tag{6}$$

where the large-signal transconductance G_{m3} for the proposed DS-Colpitts oscillator is given by

$$G_{m3\text{-proposed}} \approx \frac{2I_1}{v_{\text{GS}} - V_{\text{th}}} \approx \frac{2I_1}{nV_{\text{peak-proposed}}}. \tag{7}$$

From (4)–(7), the peak amplitude of the proposed g_m-boosted DS-Colpitts $V_{\text{peak-proposed}}$ is given by

$$V_{\text{peak-proposed}} = 4I_{\text{bias}}\, R_p\,(1-n)\left(1 - \frac{\Phi^2}{14}\right). \tag{8}$$

From (6) and (8), when n and Φ are identical, the peak amplitude of the proposed g_m-boosted DS-Colpitts oscillator is double that of the conventional DS-Colpitts oscillator [6] and slightly smaller than that of Li *et al.*'s oscillator at the same I_B and Φ due to $G_{m3\text{-Li}} < G_{m3\text{-proposed}}$.

Fig. 3 shows the electrically simulated output oscillation amplitude of the three VCOs shown in Fig. 1 as a function of tail current, each under the same frequency of oscillation, tuning range, and quality factor of the *LC* resonator while adopting $n = 0.5$ for the Colpitts VCOs [see Fig. 1(b) and (c)]. The insert in Fig. 3 shows the zoom-in plot at low tail current. Overall from Fig. 3, it can be said that the three VCOs shows no major difference in oscillation amplitude. From the insert in Fig. 3, when the three VCOs operate in the saturation region, Li *et al.*'s DS-Colpitts VCO shows the largest oscillation amplitude at the same bias current. For the tail current range of 1.2–5 mA, the proposed g_m-boosted DS-Colpitts VCO has the largest output oscillation amplitude as the corresponding switching transistors can stay in saturation-mode operation for larger values of tail current, which is explained in Section III.

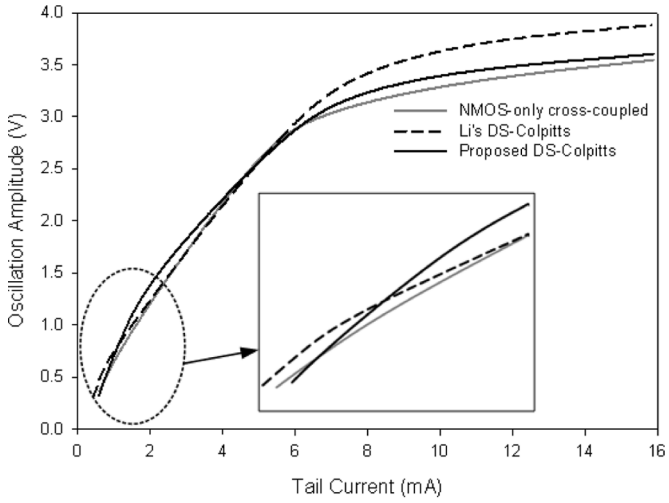


Fig. 3. Simulated output oscillation amplitude versus tail bias current of three VCOs with 1.8-V supply.

III. Phase-Noise Analysis of Proposed DS-Colpitts VCO

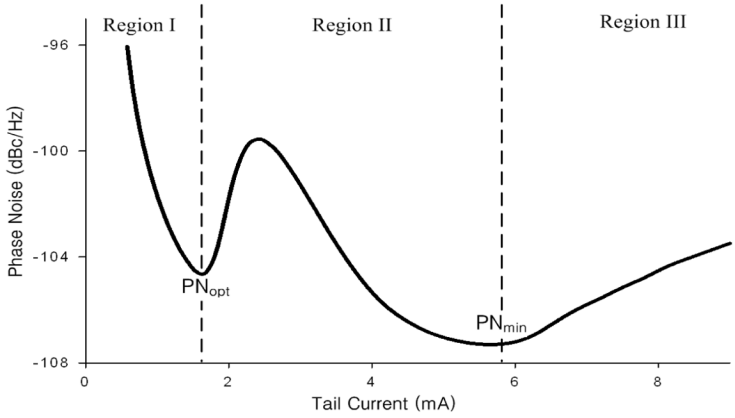
Table I summarizes the dominant noise sources, mechanisms, and solutions for close-in phase-noise behavior with respect to the oscillation amplitude [4]. When the current source transistor operates in the current limited regime, the close-in phase noise is generated mainly from the flicker noise in the current source transistor by the AM-to-FM conversion mechanism [4], [13], [14]. In the voltage-limited regime, the flicker noise in the switching transistor becomes the dominant noise source for the phase-noise degradation by the second harmonic current modulation. In general, both the minimum close-in and the far-out phase noise (PN_{min}) can be obtained from the boundary between the current and the voltage-limited regime. On the contrary, the optimum phase noise (PN_{opt}) where the VCO operates at its lowest figure of merit (FOM_{min}) is shown in the maximum saturation operation point of the switching transistor. With regard to the output voltage swing, the capacitance nonlinearity of the switching transistors changes the oscillation frequency of the VCO, which increases the frequency variation sensitivity to the voltage swing. In particular, when the switching transistor operation includes the triode mode, the frequency sensitivity as a function of output oscillation amplitude increases significantly, so does the close-in phase noise [4], [14]. In addition, as the switching transistor operates in the triode-mode region, the $1/f^2$ region of the phase noise is also degraded due to the increased switching transistor noise and reduced oscillation amplitude [3], [15]. However, both the $1/f^3$ and $1/f^2$ regions of the optimum phase noise can be improved by delaying the starting point of triode-mode operation with an increase in the voltage swing.

Compared to the conventional NMOS-only and Li *et al.*'s oscillator, the proposed g_m-boosted DS-Colpitts oscillator can achieve lower optimal phase noise by delaying the switching transistor's entry into triode-mode operation. Furthermore, the bias current (1.6 mA) for the lowest far-out phase-noise oscillator compared to that (6 mA) of the other two oscillators. The proposed g_m-boosted DS-Colpitts topology can be adopted for the VCO with low power and low phase noise simultaneously.

A. AM-to-FM Conversion by the Switching Transistor

Fig. 4 shows the node voltage and current waveforms of the conventional NMOS-only cross-coupled [see Fig. 1(a)], Li *et al.*'s [see Fig. 1(b)], and the proposed DS-Colpitts [see Fig. 1(c)] VCOs for the tail current and capacitive voltage divider factor n of 1.3 mA and 0.5, respectively. For the same output oscillation amplitude v_o of the three VCOs, the gate–source voltage v_{GS} of the switching transistors for the proposed DS-Colpitts VCO is smaller than those of other two VCOs. Furthermore, the gate–drain voltage v_{DS} of the

TABLE I
SUMMARY OF THE CLOSE-IN PHASE NOISE (100-kHz OFFSET) BEHAVIOR

	Region I	Region II	Region III
Close-In Phase Noise Curve			
peration of Switch & Current Source Tr.	Sat. & Current Limited	Triode & Current Limited	Triode & Voltage Limited
Dominant 1/f Noise Source	Current Source Tr.	Current Source Tr.	Switching Tr.
Dominant Mechanism	AM-FM by Varactor	AM-FM by Switching Tr.	2nd Harmonic Modulation
Solution	$V_O \uparrow$ & $K_{VCO} \downarrow$	Delay ($V_O \uparrow$@ $I_{max.sat}$) Suppress ($C_1/C_2 \uparrow$)	Suppress 1/f Noise ($\upsilon_{DS} \downarrow$) High Impedance @ $2\omega_0$ $C_1/C_2 \downarrow$
Common Solution	$V_O \uparrow$ & LC-tank Q $\uparrow$		

proposed DS-Colpitts VCO is larger than the other two VCOs at the peak gate–source voltage, as can be seen in Fig. 4. For the given output swing υ_o, the switching transistors of the proposed g_m-boosted DS-Colpitts VCO can operate in saturation mode while those of Li *et al.*'s and conventional NMOS-only VCOs may enter into triode mode, as can be seen from current waveform shown in Fig. 4. The gate voltage of $M_{3,4}$ in the proposed VCO [see Fig. 4(c)] is fixed at a supply voltage V_{DD}, while those of Li *et al.*'s [$M_{3,4}$ in Fig. 4(b)] and conventional NMOS-only [$M_{1,2}$ in Fig. 4(a)] VCOs is superpositioned by the output swing $(V_{DD} + \upsilon_o)$. The drain voltage of the three VCOs are the same as $V_{DD} - \upsilon_o$. Therefore, from the equation for the saturation-mode operation, $\upsilon_{\rm GS} - V_{\rm TH} \leq_{\rm DS}$, if the source bias voltages of switching transistors V's are the same in the three VCOs, the maximum output oscillation amplitude $(V_{\rm TH})$ of the proposed DS-Colpitts VCO can be double that $(V_{\rm TH}/2)$ of Li *et al.*'s DS-Colpitts and conventional NMOS-only VCO while the transistors stay in saturation. The larger output oscillation amplitude while abstaining from triode-mode operation leads to improvement of the optimum phase noise in the proposed DS-Colpitts VCO by delaying the AM-to-FM conversion and noise increase by the switching transistors.

Fig. 5 shows schematics and the equivalent capacitance seen by the *LC*-tank of the three VCOs shown in Fig. 1 at the peak of differential output swing. From the NMOS-only cross-coupled oscillator shown in Fig. 5(a), the effective capacitance seen by the *LC*-tank can be given by

$$C_{\rm eff,sat} = \frac{C_{\rm gs2,sat} \cdot C_{\rm gs1,off}}{C_{\rm gs2,sat} + C_{\rm gs1,off}} + \frac{C_{\rm par}}{2} + C_{\rm gd1,off} + C_{\rm gd2,sat}. \tag{9}$$

when M_2 is in saturation-mode operation, and

$$C_{\rm eff,triode} = \frac{C_{\rm gs2,triode} \cdot C_{\rm gs1,off}}{C_{\rm gs2,triode} + C_{\rm gs1,off}} + \frac{C_{\rm par}}{2} + C_{\rm gd1,off} + C_{\rm gd2,triode} \tag{10}$$

when M_2 is in triode-mode operation, respectively, where the subscript $\rm off$, $\rm triode$, and $\rm sat$ represents the corresponding transistor parasitic capacitance in its cutoff, and saturation-mode operation, respectively. When the MOS transistor enters into triode mode from saturation, its parasitic capacitance $C_{\rm gs}$ approximately decreases from $2/3WLC_{\rm ox} + WC_{\rm ov}$ to $0.5WLC_{\rm ox} + WC_{\rm ov}$, while $C_{\rm gd}$ increases from $WC_{\rm ov}$ to $0.5WLC_{\rm ox} + WC_{\rm ov}$, where W and L are the transistor dimension, $C_{\rm ox}$ is the oxide capacitance, and $C_{\rm ov}$ is the overlap capacitance, respectively. From (9) and (10) and the above discussion, as the switching transistor enters into the triode from saturation, the variation of the effective capacitance $C_{\rm eff,triode}$ is mainly caused by $C_{\rm gd}$ variation. As can be seen from Fig. 5(a), since $C_{\rm gs2}$ is in series with $C_{\rm gs1,off}$, the variation in $C_{\rm gs2}$ has little effect, but the variation in $C_{\rm gd2}$ dominates the increase in time-averaged effective capacitance $C_{\rm eff}$, which leads to the decrease in output oscillation frequency.

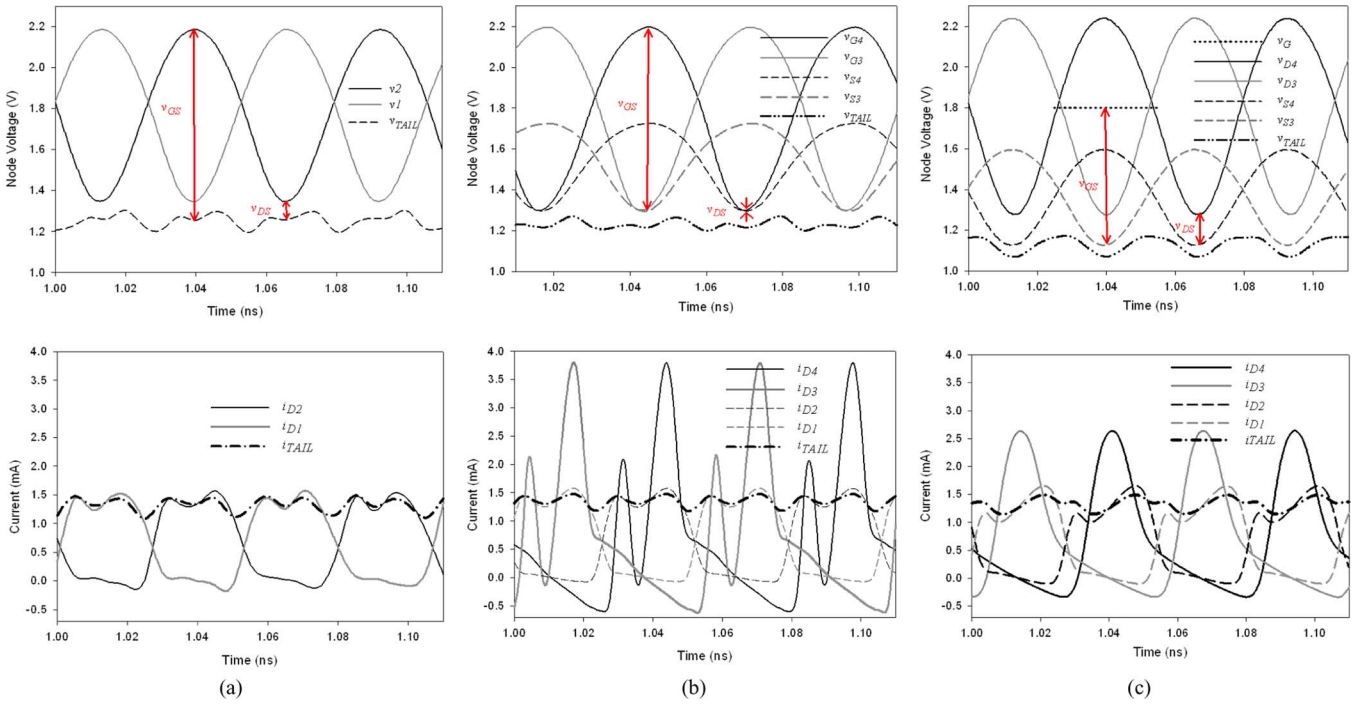


Fig. 4. Simulated node voltage and current waveforms. (a) Conventional NMOS-only. (b) Li *et al.*'s. (c) Proposed g_m-boosted differential DS-Colpitts VCOs.

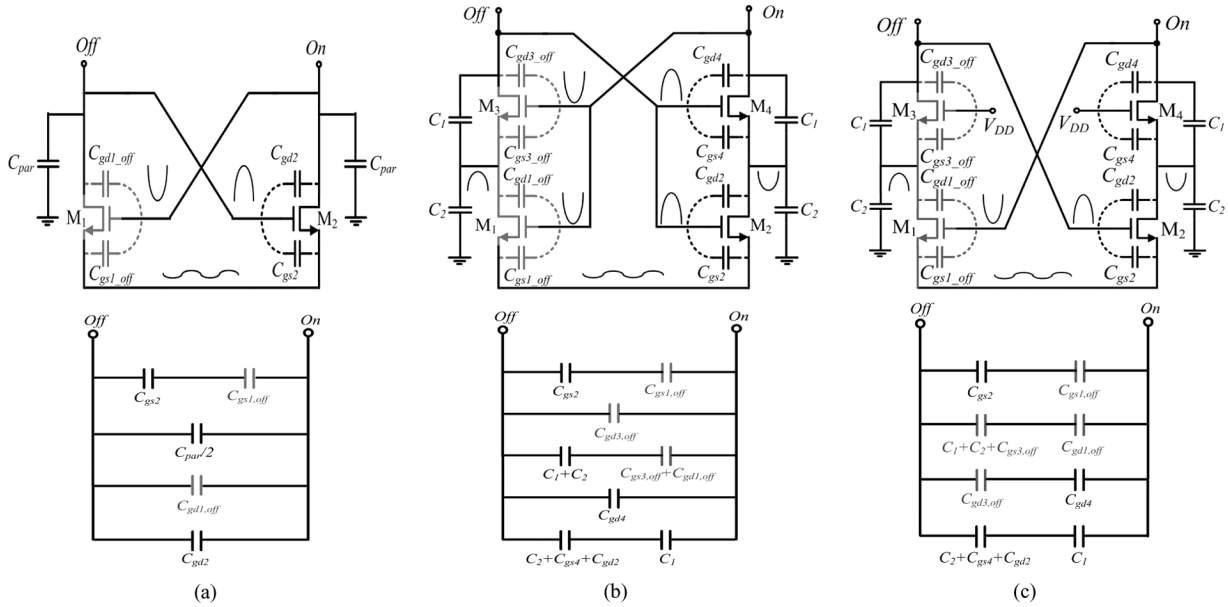


Fig. 5. Schematics and the equivalent capacitance seen by the *LC*-tank of the three VCOs. (a) NMOS-only. (b) Li *et al.*'s. (c) Proposed DS-Colpitts oscillators.

Similarly, for the Li *et al.*'s DS-Colpitts oscillator shown in Fig. 5(b), the effective capacitance can be given by

$$C_{\text{eff,sat}} = \frac{C_{\text{gs2,sat}} \cdot C_{\text{gs1,off}}}{C_{\text{gs2,sat}} + C_{\text{gs1,off}}} + C_{\text{gd3,off}} + C_{\text{off}} + C_{\text{gd4,sat}} + C_{\text{sat}} \quad (11)$$

when M_2 and M_4 are in saturation-mode operation, where

$$C_{\text{off}} = (C_{\text{gs3,off}} + C_{\text{gd1,off}}) // (C_1 + C_2)$$
$$C_{\text{sat}} = \frac{C_1 \cdot (C_2 + C_{\text{gs4,sat}} + C_{\text{gd2,sat}})}{C_1 + C_2 + C_{\text{gs4,sat}} + C_{\text{gd2,sat}}} \quad (12)$$

and, when M_2 and M_4 are in triode-mode operation,

$$C_{\text{eff,triode}} = \frac{C_{\text{gs2,triode}} \cdot C_{\text{gs1,off}}}{C_{\text{gs2,triode}} + C_{\text{gs1,off}}} + C_{\text{gd3,off}} + C_{\text{off}} + C_{\text{gd4,triode}} + C_{\text{triode}} \quad (13)$$

where

$$C_{\text{triode}} = \frac{C_1 \cdot (C_2 + C_{\text{gs4,triode}} + C_{\text{gd2,triode}})}{C_1 + C_2 + C_{\text{gs4,triode}} + C_{\text{gd2,triode}}} \quad (14)$$

where C_1 and C_2 are the feedback capacitances for the Li *et al.*'s DS-Colpitts oscillator. Comparing (11) and (13), the variation of C_{eff} from saturation to triode is caused by the change

in $C_{\rm gs2}$, $C_{\rm gd2}$, $C_{\rm gs4}$, and $C_{\rm gd4,triode}$. From (9)–(14), assuming that $C_{\rm eff,sat}$ are the same in both the NMOS-only and Li *et al.*'s DS-Colpitts oscillator, the $C_{\rm eff,triode}$, of Li *et al.*'s Colpitts oscillator changes more than the case of the NMOS-only oscillator since the dominant variation capacitance $C_{\rm gd4,triode}$ in (13) (finger width is 100 μm) increases five times larger than that $C_{\rm gd2,triode}$ in (10) (finger width is 20 μm).

From Fig. 5(c), $C_{\rm eff}$ of the proposed DS-Colpitts oscillator can be given by

$$C_{\rm eff,sat} = \frac{C_{\rm gs2,sat}\cdot C_{\rm gs1,off}}{C_{\rm gs2,sat}+C_{g1,\rm off}} + C_{\rm off} + \frac{C_{\rm gd4,sat}\cdot C_{\rm gd3,off}}{C_{\rm gd4,sat}+C_{\rm gd3,off}} + C_{\rm sat} \quad (15)$$

with M_2 and M_4 in saturation-mode operation, where

$$C_{\rm off} = C_{\rm gd1,off}//(C_1+C_2+C_{\rm gs3,off})$$
$$C_{\rm sat} = \frac{C_1\cdot(C_2+C_{\rm gs4,sat}+C_{\rm gd2,sat})}{C_1+C_2+C_{\rm gs4,sat}+C_{\rm gd2,sat}} \quad (16)$$

while with M_2 and M_4 operating in triode mode,

$$C_{\rm eff,triode} = \frac{C_{\rm gs2,triode}\cdot C_{\rm gs1,off}}{C_{\rm gs2,triode}+C_{\rm gs1,off}} + C_{\rm off} + \frac{C_{\rm gd4,triode}\cdot C_{\rm gd3,off}}{C_{\rm gd4,triode}+C_{\rm gd3,off}} + C_{\rm triode} \quad (17)$$

where

$$C_{\rm triode} = \frac{C_1\cdot(C_2+C_{\rm gs4,triode}+C_{\rm gd2,triode})}{C_1+C_2+C_{\rm gs4,triode}+C_{\rm gd2,triode}}. \quad (18)$$

From (11)–(18), when the $C_{\rm eff,sat}$ of both Li *et al.*'s and the proposed DS-Colpitts oscillators are the same, the capacitance change from $C_{\rm eff,sat}$ to $C_{\rm eff,triode}$ is smaller in the proposed DS-Colpitts oscillator. This is because the $C_{\rm gd4,triode}$ of the proposed oscillator is in series with $C_{\rm gd3,off}$, while in Li *et al.*'s oscillator it is in parallel. However, the capacitance variation from $C_{\rm eff,sat}$ to $C_{\rm eff,triode}$ of the proposed DS-Colpitts oscillator is larger than that of the NMOS-only VCO due to larger $C_{\rm gd4,triode}$. Therefore, the AM-to-FM conversion by the switching transistors is most significant in Li *et al.*'s DS-Colpitts oscillator among the three VCOs, which leads to higher close-in phase noise as the switching transistors enter into triode region operation.

The three VCOs shown in Fig. 1 are designed to operate from 1.79 to 1.97 GHz with 1.8-V supply when the switching transistors operate in the saturation region. The same value of the varactors and center-tapped inductor are adopted for the same frequency tuning range, $K_{\rm VCO}$, and quality factor of the *LC*-tank. For the Li *et al.*'s and the proposed DS-Colpitts VCO, the feedback capacitor ratio of $C_1/C_2 = 1$ is selected. The value of C_1, C_2, and $C_{\rm par}$ of the three VCOs in Fig. 1 are selected for the same value of $C_{\rm eff,sat}$ shown in (9), (11), and (15), which leads to the same output oscillation frequency (1.79–1.97 GHz). Fig. 6 shows the output oscillation frequency [see Fig. 6(a)] and the derivative (slope) [see Fig. 6(b)] versus tail current of the three VCOs at the center frequency of 1.88 GHz. In Fig. 6(b), at low tail current (below 2 mA), the frequency variation slope initially decreases, and then after passing the maximum saturation point, starts to increase sharply. The maximum saturation point is the maximum tail current (or the output voltage swing) point where the switching transistors operate without entering in triode mode.

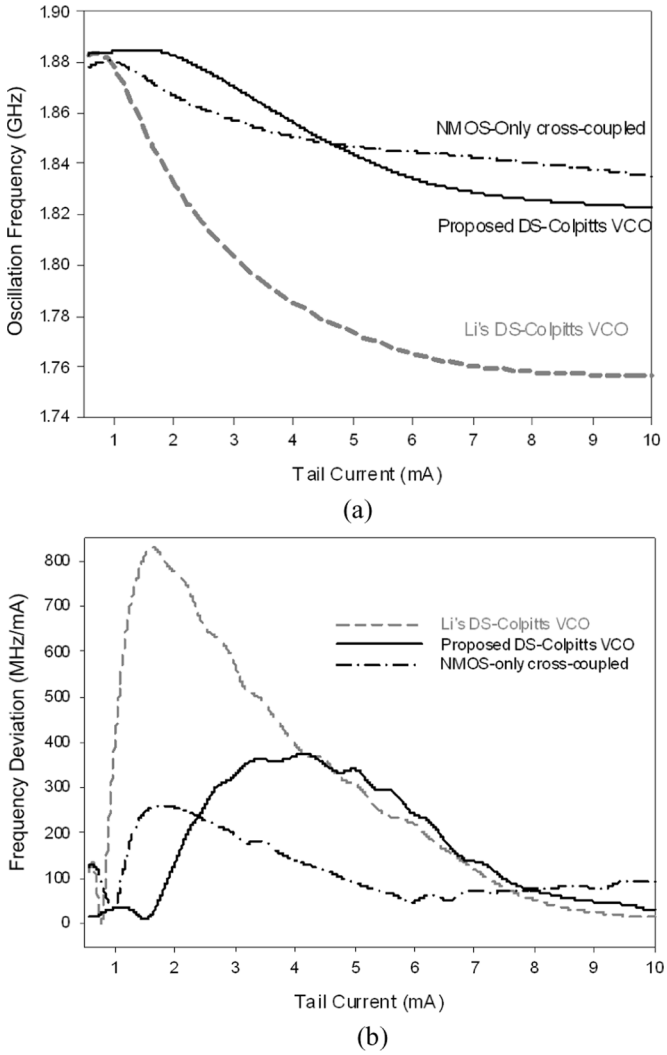


Fig. 6. Simulated: (a) output oscillation frequency and (b) derivative versus tail current of NMOS-only, Li *et al.*'s, and proposed Colpitts VCOs at the center frequency of 1.88 GHz.

The sharp increase in the frequency variation slope is caused by the change of $C_{\rm eff,sat}$ to $C_{\rm eff,triode}$. In Fig. 6(b), the maximum saturation point occurs at 0.73, 0.9, and 1.5 mA for the Li *et al.*'s DS-Colpitts, conventional NMOS-only, and proposed DS-Colpitts VCOs, respectively, and the corresponding output amplitudes are 0.57, 0.57, and 1.2 V, respectively, which can be seen from Fig. 3. These simulation results are in good agreement with the predictions that the output amplitude $(V_{\rm TH})$ of the proposed VCO at the peak saturation point is twice the amount of the other two VCOs. As expected from equations (9)–(18), in Fig. 6(b), the smallest variation of the effective capacitance from saturation to triode in the conventional NMOS-only VCO leads to the lowest peak frequency slope (250 MHz/mA), while that of Li *et al.*'s DS-Colpitts VCO shows the largest (800 MHz/mA) amount.

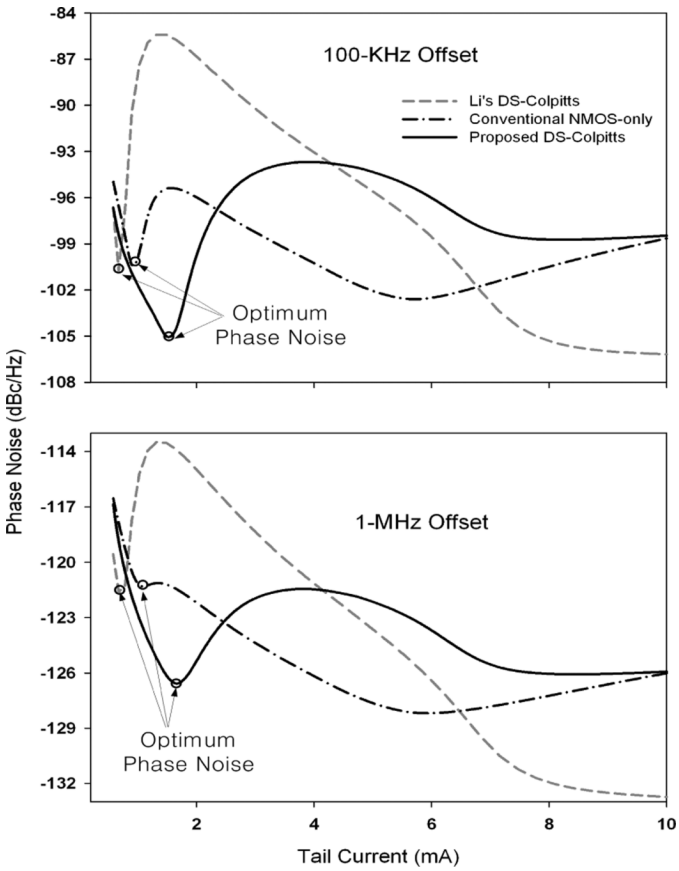


Fig. 7. Simulated phase noise versus tail current of NMOS-only, Li *et al.*'s, and proposed DS-Colpitts VCOs with 1.8-V supply.

Fig. 7 shows the simulation results of the phase noise versus tail bias current for the three VCOs at 100-kHz and 1-MHz offset frequency. The simulations are done at the center frequency of 1.88 GHz where the effect of the AM-to-FM conversion by the varactors is negligible, i.e., $V_{\rm tune}$ in Fig. 1 is set at the middle point of $V_{\rm tune}$ versus $C_{\rm var}$. As can be seen in Fig. 7, the close-in phase-noise (100 kHz) curves of the three VCOs show similar behavior as the frequency sensitivity curves shown in Fig. 6(b). The Li *et al.*'s DS-Colpitts VCO shows the lowest phase noise at low tail current due to the largest oscillation amplitude (see Fig. 3). However, the lowest optimum close-in phase noise is achieved from the proposed DS-Colpitts VCO (solid black) due to the delay into the triode-mode operation of the switching transistors, suppressing the AM-to-FM conversion by the switching transistors. As the switching transistors enter triode-mode operation, with an increase in the tail current, the increase of oscillation amplitude becomes less steep while the thermal noise increases. This mitigates the phase-noise improvement ratio with respect to the increase in tail current [3], [15]. Therefore, the delay of the switching transistor operation into the triode mode at higher tail current also improves the optimum far-out phase noise (1-MHz offset). It can be seen from Fig. 7 that the optimum phase noise of the proposed DS-Colpitts VCO is lower by 5 dB compared to those of Li *et al.*'s DS-Colpitts and NMOS-only VCOs.

In Fig. 7, due to the high frequency sensitivity caused by the high nonlinearity of the effective switch transistor capacitance

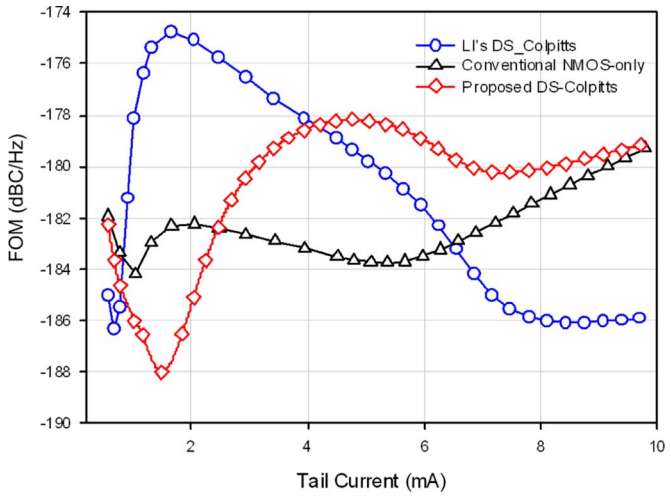


Fig. 8. Simulated FOM at 1-MHz offset over tail current for NMOS-only, Li *et al.*'s, and proposed Colpitts VCOs.

(large change from $C_{\rm eff,sat}$ to $C_{\rm eff,triode}$), the Li *et al.*'s DS-Colpitts VCO shows the worst close-in phase-noise (-85 dBc/Hz) performance. The simulated phase-noise behaviors shown in Fig. 7 are in agreement with the analytical predictions. Fig. 8 shows the FOM versus the tail bias current of the three VCOs based on the simulation results of Fig. 7 at 1-MHz offset [8], [14]. As can be seen in Fig. 8, the proposed DS-Colpitts VCO (diamond) shows the best FOM of -188 dBc/Hz at 1-MHz offset among the three VCOs.

In the proposed DS-Colpitts VCO, the gate voltage $(V_{DD+\upsilon_O})$ of the g_m-boosting $(M_{1,2})$ transistors is larger than that (V_{DD}) of the switching $(M_{3,4})$ transistors. As a result, the g_m-boosting transistors $(M_{1,2})$ enter into the triode region earlier, such that the effective capacitance of the g_m-boosting transistors increases with an increase in the tail current. However, during this time, since the switching transistors $M_{3,4}$ still operate in the saturation or cutoff region, their effective capacitance decreases with an increase in tail current. Therefore, the sum of the effective capacitances provided by the switching and g_m-boosting transistors remains nearly constant with an increase in tail current, such that the AM-to-FM conversion is suppressed in this region. In addition, since the output oscillation amplitude is determined by the operating conditions of the switching transistor $M_{3,4}$, even though $M_{1,2}$ quickly enters into triode, it does not significantly affect the oscillation amplitude when $M_{3,4}$ still operates in the saturation region. Therefore, in the current limited regime, the operation of the switching transistor $M_{3,4}$ mainly determines the phase noise of the proposed Colpitts oscillator. The transistors $M_{1,2}$ contribute to improving the startup condition by boosting the small-signal negative conductance and increase the bias current $(I_B \rightarrow 2I_B)$ by generating a common source node for fully differential operation.

B. Performance Comparison Between Gm-Boosted GS and DS-Colpitts VCOs

The g_m-boosted GS-Colpitts VCO shows good phase-noise characteristics based on the same principle of keeping MOS switches out of the triode region [4]. The oscillation amplitude

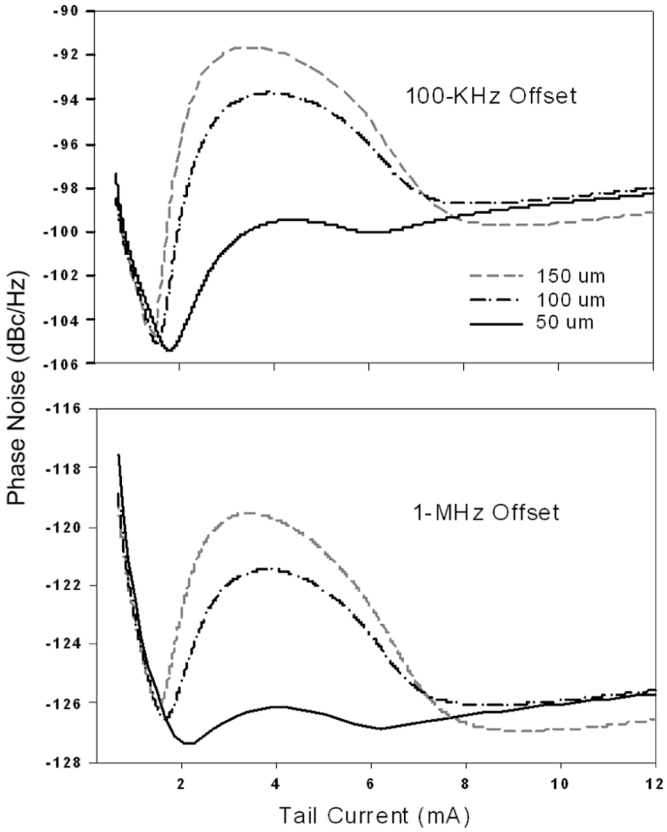


Fig. 9. Simulated phase noise versus tail bias current for different values of switching transistor size of the proposed DS-Colpitts VCO.

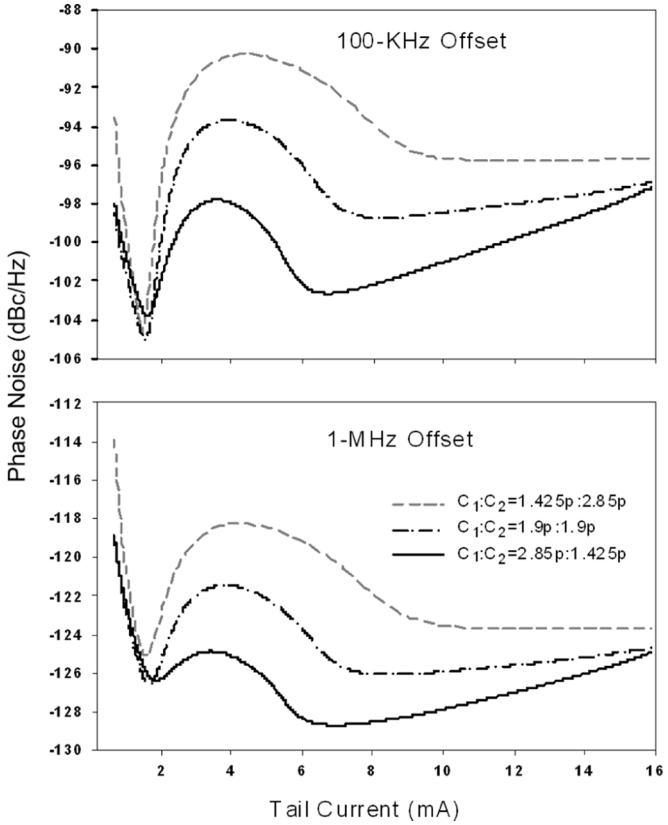


Fig. 10. Simulated phase noise versus tail bias current of the proposed DS-Colpitts VCO for different values of feedback capacitor ratio.

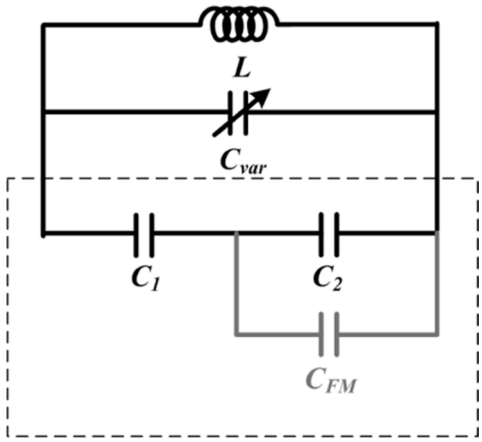
of both g_m-boosted GS and DS-Colpitts VCOs can be double that of the conventional VCO at the maximum saturation operation point since the gate and drain are fixed at V_{DD}, respectively. In the proposed g_m-boosted DS-Colpitts VCO, both M_1 and M_3 turn on at the same time during the half period, while the two transistors operate in a complementary manner in the GS-Colpitts VCO. As a result, when the switching transistor M_3 enters into triode operation, the oscillation frequency of the proposed DS-Colpitts VCO significantly decreases by adding the two parasitic capacitances of the switching transistors M_1 and M_3, while increasing slightly in the GS-Colpitts VCO by subtracting the two parasitic capacitances. Therefore, for the g_m-boosted GS-Colpitts VCO, the phase-noise degradation in the triode region (Region II) is much less than that of the proposed DS-Colpitts and conventional NMOS-only VCOs because it suppresses the AM-to-FM conversion by the switching transistor.

C. Effect of Transistor Size and Feedback Capacitor Ratio

Fig. 9 shows the simulated phase noise versus tail bias current for different values of switching transistor size of the proposed DS-Colpitts VCO. In Fig. 9, larger switching transistor size, and therefore, higher $g_{m3,4}$ leads to lower phase noise at low current (below 1.5 mA) due to the larger oscillation amplitude. On the contrary, the smaller switching transistor size has better phase noise at high currents (2–7 mA), where the switching transistor operation is dominated by the triode mode, as the switching transistor capacitance contributes a smaller amount of the total capacitance variations.

The simulated phase noise versus tail bias current of the proposed DS-Colpitts VCO for different values of feedback capacitor ratio is shown in Fig. 10. In Fig. 10, the three different feedback capacitor ratioed VCOs are designed to oscillate at the same frequency. From (15)–(18), the feedback capacitors C_1 and C_2 affect the variation of $C_{\text{eff,sat}}$ to $C_{\text{eff,triode}}$ by affecting the values of C_{triode}. From (18), as the switching transistor enters from saturation into triode mode, C_{triode} decreases due to a decrease of C_{gs4}. Since the larger C_1 leads to more decrease in C_{triode} and it cancels out the increase in the C_{gd4} in (17), therefore, the total effective capacitance shown in (17) is reduced, which leads to the decrease in frequency sensitivity. Therefore, in the proposed DS-Colpitts VCO, the larger feedback capacitor ratio $(C_1/C_2 = 2)$ helps to improve the phase-noise performance by suppressing switching transistors AM-to-FM conversion. The same mechanism can be applied to Li *et al.*'s DS-Colpitts VCO, as can be seen from (11)–(14).

The flicker noise of the switching transistors modulates the second harmonic current at the common source node (C_{TAIL}). After mixing operation by the switching transistors, the modulated second harmonic current downconverts to the fundamental oscillation frequency and flows into the *LC*-tank. As a result, the effective capacitance of the *LC*-tank fluctuates and this FM upconverts the flicker noise into close-in phase noise [4], [16], [17]. In the current limited regime, the close-in phase noise is dominated by the flicker noise of the current source transistor (M_0) through the AM-to-FM conversion. However, in the voltage-limited regime, where the current source transistor enters into the triode region and the output oscillation amplitude



$$C_{eff} = \frac{C_1 \cdot (C_2 + C_{FM})}{C_1 + C_2 + C_{FM}}$$

Fig. 11. Equivalent circuit of the proposed VCO modeling the capacitance modulation by the second harmonic.

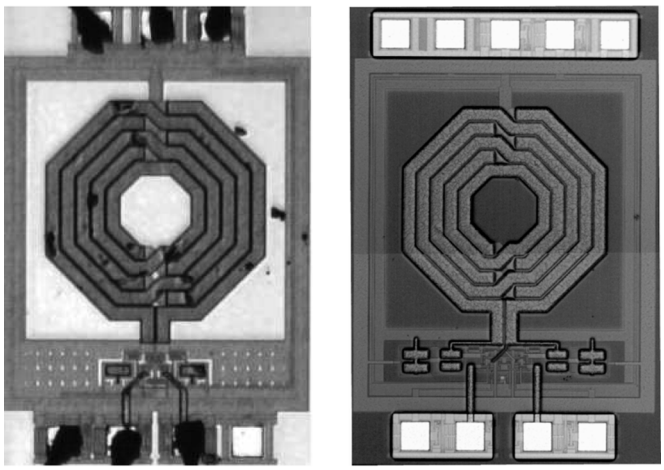


Fig. 12. Fabricated chip photograph. (a) Conventional NMOS-only cross-coupled VCO. (b) Proposed g_m-boosted DS-Colpitts VCO.

is limited, the flicker noise of the switching transistors becomes the dominant noise source for the phase-noise degradation by the second-order harmonic-modulation mechanism.

In the proposed DS-Colpitts VCO shown in Fig. 1(c), since the flicker noise of $M_{3,4}$ is filtered out at the *LC*-tank, the flicker noise of $M_{1,2}$ is the dominant source for the close-in phase-noise degradation in the voltage-limited regime, by the second-order harmonic modulation mechanism. Fig. 11 shows the equivalent circuit of the proposed VCO modeling the capacitance modulation by the second harmonic [16]. In Fig. 11, the contribution of $M_{1,2}$'s flicker-noise current $(C_{\rm FM})$ to the effective capacitance of the *LC*-tank $(C_{\rm eff})$ can be reduced by decreasing C_1. Therefore, the close-in phase noise of the smaller feedback capacitor ratio $(C_1/C_2 = 0.5)$ does not degrade in the voltage-limited region (higher than 9 mA), while that of the large $C_1/C_2(= 2)$ increases, as can be seen in Fig. 10.

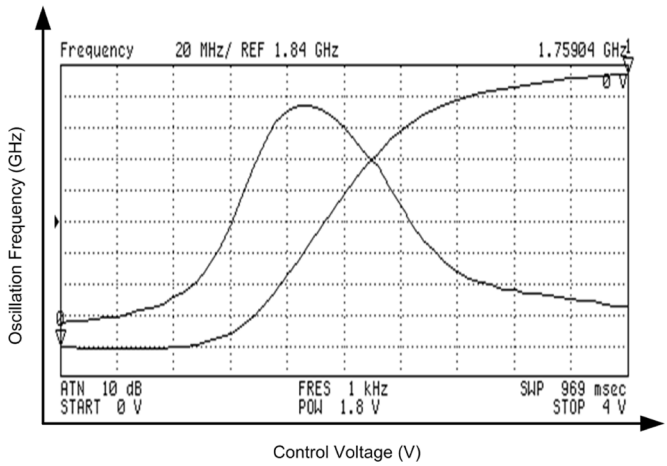


Fig. 13. Measured oscillation frequency and its gain $(K_{\rm VCO})$ versus the control voltage of the proposed GS-Colpitts VCO.

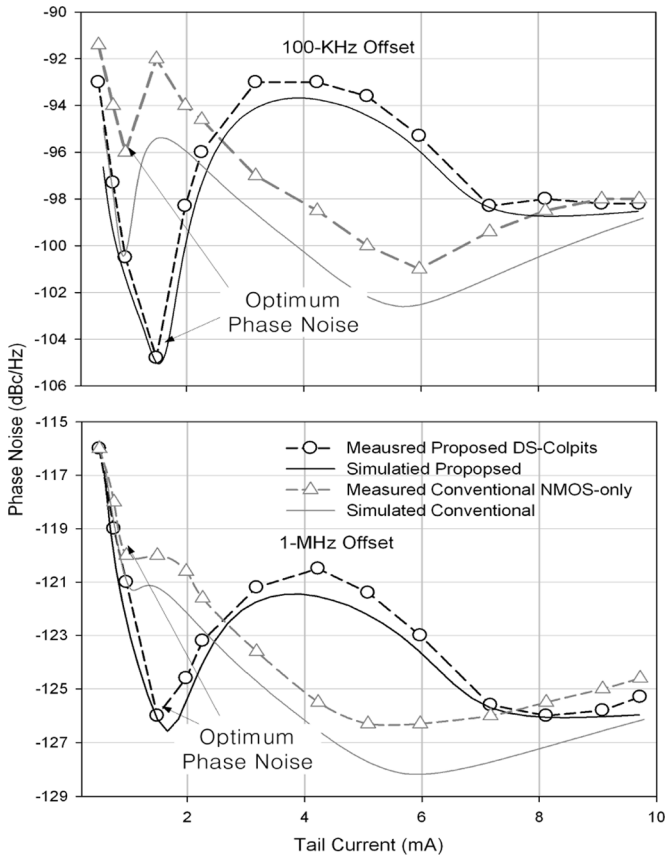


Fig. 14. Measured phase noise versus tail current of conventional NMOS-only and proposed VCO at 1.84 GHz from 1.8-V supply.

IV. Measurement Results

The proposed g_m-boosted differential DS-Colpitts shown in Fig. 1(c) and conventional NMOS-only cross-coupled LC-VCO shown in Fig. 1(a) are fabricated in a 0.18-μm CMOS technology. Fig. 12 shows the implemented chip photograph of the two VCOs with a size of 800 $\times$ 680 μm^2 each excluding the pads. To deliver output power of the oscillator to a 50-Ω load, the open drain transistor is used as a buffer. Fig. 13 shows the measured oscillation frequency and its gain $(K_{\rm VCO})$ versus the

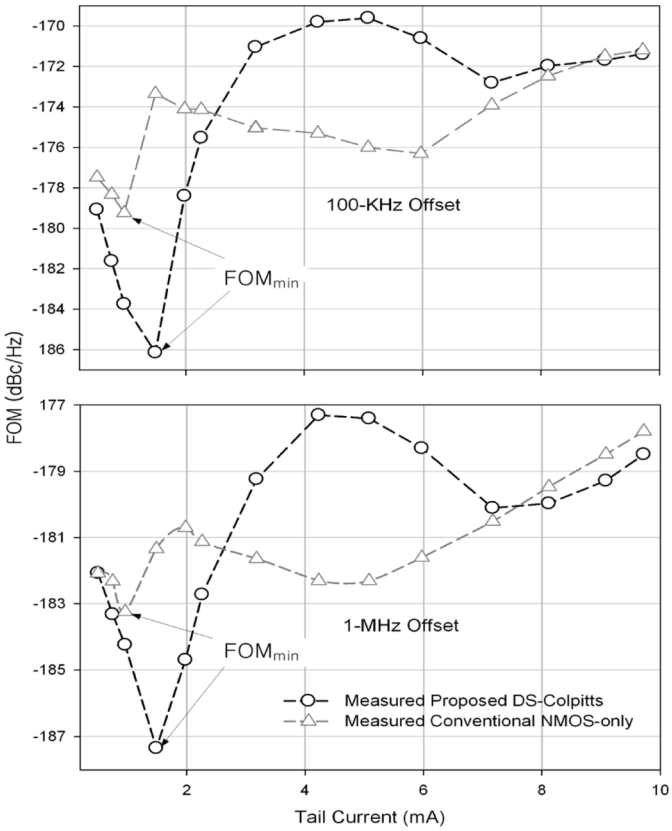


Fig. 15. Measured FOM versus tail current of conventional NMOS-only and proposed VCO at 1.84 GHz from 1.8-V supply.

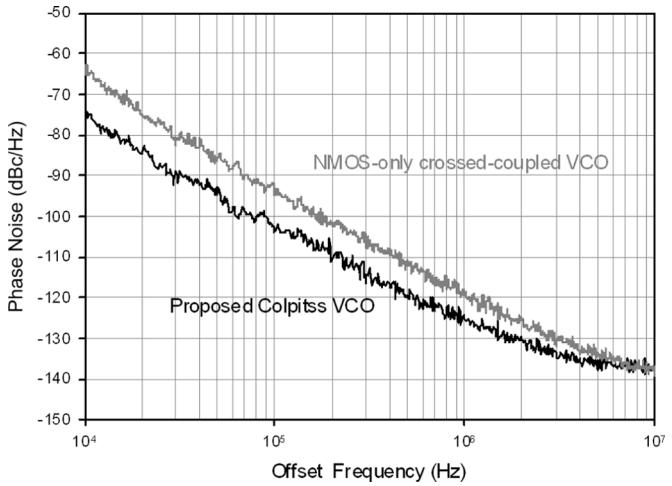


Fig. 16. Measured optimum phase noise of the two VCOs at 1.84 GHz with 0.9-V supply.

control voltage of the proposed DS-Colpitts VCO, showing an operating frequency range of 1.76 to 1.93 GHz over control voltage of 1.1–2.8 V. The conventional cross-coupled LC-VCO has a similar frequency behavior. Figs. 14 and 15 show the measured phase noise and FOM (100-kHz and 1-MHz offset of the two VCOs) with 1.8-V supply as a function of the tail bias current at the center frequency of 1.84 GHz, respectively. In Fig. 14, the control voltage $V_{\rm tune}$ is set at 1.9 V, where the contribution of the varactor AM-to-FM conversion is negligible, as shown in Fig. 13. It can be seen that the measured results shown in Figs. 14 and 15 are well matched with the analytical predictions and the simulation results shown in Figs. 7 and 8. Fig. 16 shows the measured optimum phase noise of the NMOS-only cross-coupled and the proposed DS-Colpitts VCOs at 0.9 and 1.5-mA tail current, respectively. Fig. 17 shows the measured output spectrum of the proposed VCO at a 1.84-GHz carrier frequency with a −4.6-dBm output power. In Fig. 16, to obtain the optimum FOM, the phase noise is measured with 0.9-V supply and the center frequency of 1.84 GHz is selected where the contribution of the varactor AM-to-FM conversion is negligible. In Fig. 16, the measured optimum phase noise of the proposed g_m-boosted differential Colpitts VCO is −104 and −126 dBc/Hz at 100-kHz and 1-MHz offset, respectively, while those of the conventional NMOS-only VCO is −95 and −120 dBc/Hz. The FOM of the proposed g_m-boosted differential DS-Colpitts VCO is 190 dBc/Hz, while that of the conventional NMOS-only VCO is −185 dBc/Hz at 1-MHz offset.

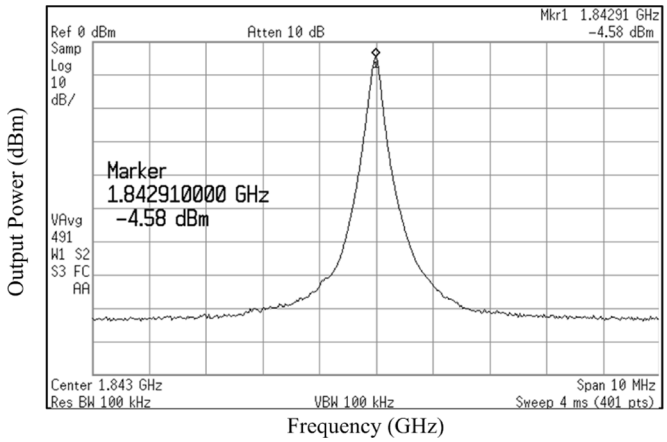


Fig. 17. Measured output spectrum of the proposed VCO at 1.84 GHz.

TABLE II
PERFORMANCE COMPARISON

VCO	Power [mW]	Freq. [GHz]	Phase Noise [dBc/Hz]	FOM [dBc/Hz]	Tech. [μm]
[4]	1.6	1.86	-128@1MHz	-191.2	0.18
[7]	10	1.8	-127@1MHz	-182.1	0.18
[8]	7.2	1.8	-128@1MHz	-184.5	0.18
[9]	15.8	1.8	-135@1MHz	-188	0.18
[15]	4.9	2	-103@100kHz	-182.3	0.18
[18]	36	2	-117@1MHz -135@1MHz	-168(VCO) -185(QVCO)	0.18
[19]	0.36	2.4	-117@1MHz	-197	0.18
[20]	1.7	3.6	-122@1MHz	-190.8	0.18
[21]	6.7	2	-121.6@500KHz	-186	0.35
[22]	7.5	3	-128.5@1MHz	189.2	0.25
This work	1.35	1.84	-126@1MHz	-190	0.18

As can be seen in Fig. 16, the proposed g_m-boosted DS-Colpitts VCO shows significant improvement in phase noise at low offset frequencies compared to the conventional cross-coupled VCO. Table II summarizes the performances of the proposed DS-Colpitts VCO compared to those of previously reported CMOS *LC*-VCOs. The proposed g_m-boosted GS-Colpitts VCO shows good performance in all parameters.

V. Conclusion

A g_m-boosted differential DS-Colpitts VCO that reduces startup current has been reported. The behavior of the proposed topology is analyzed and demonstrated by simulations and measurements in comparison with the previously reported Li *et al.*'s DS-Colpitts and conventional NMOS-only VCOs. The proposed topology shows better optimum phase noise compared to the other two VCOs by keeping the switching transistor operation in the saturation region at larger output oscillation amplitude. In the proposed DS-Colpitts VCO, the larger capacitor feedback ratio and smaller switching transistor width helps to reduce phase noise over the tail bias current variation. The proposed g_m-boosted differential DS-Colpitts VCO, which is implemented in 0.18-μm CMOS for 1.76–1.93-GHz operation, shows the phase noise of -104 and -126 dBc/Hz (corresponds to a FOM of -190 dBc/Hz) at 100 kHz and 1 MHz, respectively, at 1.84 GHz while dissipating 1.5 mA from a 0.9-V supply.

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