Hardware-Based Cascaded Topology and Modulation Strategy With Leakage Current Reduction for Transformerless PV Systems

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***Abstract*—Leakage current reduction of the single-phase transformerless cascaded H-bridge PV inverter is investigated in this paper. The high-frequency common-mode loop model of a typical single-phase cascaded H-bridge PV system is established. Based on the model, the main factors that affect the leakage current are discussed. The reason why the typical single-phase cascaded H-bridge inverter fails to reduce the leakage current is explained. In order to solve the problem, a cascaded topology based on the H5 inverter is presented, along with a new modulation strategy, which can ensure that the stray capacitor voltage is free of high-frequency components. In this way, the leakage current can be effectively reduced. Finally, a prototype with TMS320F28335DSP + XC3S400FPGA digital control is built. The performance tests of cascaded H-bridge and the proposed topologies are carried out. The experimental results verify the effectiveness of the proposed solution.**

***Index Terms*—Cascaded H-bridge inverter, leakage current, pulse width modulation, transformerless photovoltaic system.**

I. Introduction

THE transformerless photovoltaic (PV) inverters have the advantages of low cost, small size, light weight, and high efficiency [1]. However, the leakage current will arise due to lack of galvanic isolation. The undesirable leakage current may lead to electromagnetic inferences, current harmonic distortion, and safety concerns. VDE 0126-1-1 specifies that the PV systems should be disconnected from the grid within 0.3 s, if the leakage current rms is beyond 30 mA or the peak value of leakage current is more than 300 mA [2]. Therefore, it is crucial to eliminate the leakage current in transformerless PV systems.

Many interesting solutions have been reported. They can be classified into two categories. One is modulation-based solutions, and the other is topology-based solutions. In [3], an improved modulation technique to keep the common-mode voltage constant for the leakage current reduction is proposed. In [4], another space vector modulation is presented to eliminate the leakage current for neutral-point-clamped inverters. In [5], an interesting space vector modulation to reduce the leakage current for three-phase T-type inverters is proposed. The above-mentioned methods are modulation-based solutions. On the other hand, the leakage current can be reduced by introducing new topologies. Many interesting single-phase topologies have been reported such as Heric, H5, H6, and so on [6]–[13]. Recently, in order to further increase the efficiency, the soft-switching transformerless PV inverters are proposed in [14]. It can achieve the higher efficiency with the leakage current suppression capability. However, these single-phase topologies are limited to three-level inverters. In PV grid-connected system, the panels need to reach the required power levels. This encourages the possibility to use multilevel inverters for high-power applications. Multilevel inverters have an advantage over two- and three-level inverters in high-power and low-power system [15], which can decrease the total harmonic distortion, voltage stress of *dv/dt* on switches, and electromagnetic interference, and can increase the output waveform quality [16]–[19]. There are different studies on single-phase five-level cascaded inverters [20], [21]. However, few papers have been reported regarding eliminating the leakage current for the single-phase cascaded multilevel inverters. A significant contribution in [22] is the filter-based leakage current suppression solution for the single-phase cascaded multilevel PV inverter. In [23] and [24], the improved modulation techniques are presented to reduce leakage current in the cascaded H4 topology. However, the leakage current cannot be effectively suppressed due to the high-frequency components on the stray capacitors. So far, the topology-based solution has not been discussed in the literature, and needs further investigation.

The main contribution of this paper is to present the theoretical analysis and experimental verification of a cascaded topology based on the H5 inverter to reduce the leakage current for single-phase transformerless PV systems. The paper is organized as follows. In Section II, the high-frequency common-mode loop model of a typical single-phase cascaded H-bridge PV system is established. The main factors that affect the leakage current are discussed. The reason why the typical single-phase cascaded H-bridge inverter fails to reduce the leakage current is explained. Section III presents the proposed topology and new modulation strategy to reduce the leakage current. Also, both the high-frequency and the low-frequency common-mode models are established to figure out the stray capacitor voltage, which explains why the leakage current of the upper cell is a little bit higher than that of the lower cell. The experimental results of the conventional and proposed solutions are presented in Section IV. Finally, the conclusion is provided in Section V.

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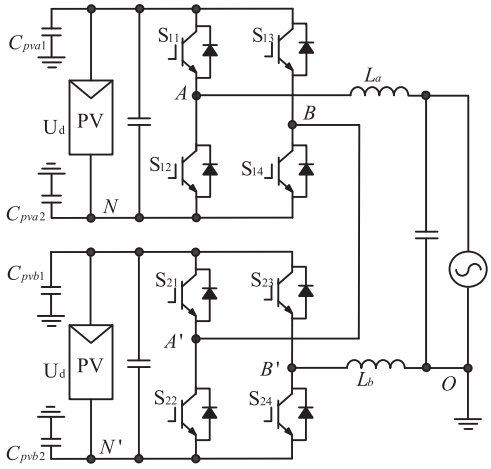

Fig. 1. Schematic diagram of a conventional single-phase cascaded H-bridge inverter.

II. Conventional Cascaded H-Bridge Topology

The schematic diagram of a conventional single-phase cascaded H-bridge inverter for the transformerless PV system is shown in Fig. 1. Note that each cell of the cascaded H-bridge topology requires an independent dc input source. Therefore, the multiple common-mode paths and loops make it more complicated than the noncascaded topologies [22]. It is necessary to consider the all stray capacitors of C_{pvx} $(x = a1, a2, b1, b2)$ between PV panels and ground.

The common-mode voltage (CMV) and differential mode voltage (DMV) of the upper cell in the cascaded topology can be expressed as follows [25]:

$$U_{cma} = (U_{AN} + U_{BN})/2 \tag{1}$$

$$U_{dma} = U_{AN} - U_{BN}. \tag{2}$$

Similarly, the CMV and DMV of the lower cell in the cascaded topology can be expressed as follows:

$$U_{cmb} = (U_{A'N'} + U_{B'N'})/2 \tag{3}$$

$$U_{dmb} = U_{A'N'} - U_{B'N'}. \tag{4}$$

Using (1)–(4), the following equations can be obtained:

$$\begin{cases} U_{AN} = U_{cma} + 0.5U_{dma} \\ U_{BN} = U_{cma} - 0.5U_{dma} \\ U_{A'N'} = U_{cmb} + 0.5U_{dmb} \\ U_{B'N'} = U_{cmb} - 0.5U_{dmb}. \end{cases} \tag{5}$$

Fig. 2 shows the high-frequency common-mode model for single-phase cascaded H-bridge topology, where $C_{pva} = C_{pva1}//C_{pva2}$, $C_{pvb} = C_{pvb1}//C_{pvb2}$, and the low frequency grid voltage is neglected due to small influence on the high frequency leakage current [26].

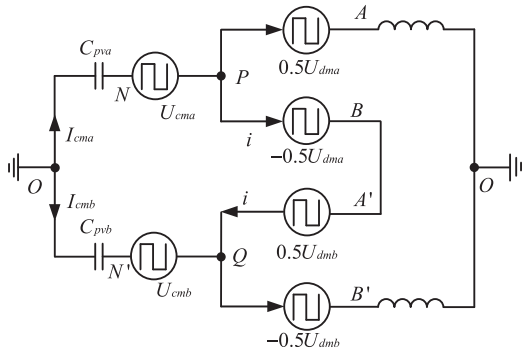

Fig. 2. Common-mode model of the single-phase cascaded H-bridge topology.

Based on the common-mode model in Fig. 2, the following equations can be obtained:

$$\begin{cases} -\dfrac{U_{PO} - U_{cma}}{Z_{cpva}} = i + \dfrac{U_{PO} + 0.5U_{dma}}{Z_{La}} \\ -\dfrac{U_{QO} - U_{cmb}}{Z_{cpvb}} = -i + \dfrac{U_{QO} - 0.5U_{dmb}}{Z_{Lb}} \\ U_{PQ} = 0.5U_{dma} + 0.5U_{dmb} \\ I_{cma} = \dfrac{U_{OP} + U_{cma}}{Z_{cpva}} \\ I_{cmb} = \dfrac{U_{OQ} + U_{cmb}}{Z_{cpvb}} \end{cases} \tag{6}$$

where $Z_{cpva} = 1/(sC_{pva})$, $Z_{cpvb} = 1/(sC_{pvb})$, $Z_{La} = sL_a$, $Z_{Lb} = sL_b$, I_{cma} is the leakage current of upper unit, I_{cmb} is the leakage current of lower unit, i is the current flowing through differential voltage source. From (6), the leakage current of the single-phase cascaded H-bridge topology can be derived as (7), shown at the bottom of the page, where

$$A = Z_{cpva}(Z_{La}Z_{Lb} + Z_{cpvb}Z_{Lb} + Z_{cpvb}Z_{La}),$$

$$B = -0.5\, Z_{cpva}(Z_{La}Z_{Lb} - Z_{cpvb}Z_{Lb} + Z_{cpvb}Z_{La}),$$

$$C = -Z_{cpva}Z_{La}Z_{Lb}, D = -0.5\, Z_{cpva}Z_{La}(Z_{Lb} + Z_{cpvb})$$

$$A' = -Z_{cpvb}Z_{La}Z_{Lb}, B' = Z_{cpvb}Z_{Lb}(0.5\, Z_{La} + Z_{cpva}),$$

$$C' = Z_{cpvb}(Z_{La}Z_{Lb} + Z_{cpva}Z_{Lb} + Z_{cpva}Z_{La}),$$

$$D' = 0.5\, Z_{cpvb}(Z_{La}Z_{Lb} + Z_{cpva}Z_{Lb} - Z_{cpva}Z_{La}).$$

From (7), it can be concluded that the leakage current is dependent on many factors, e.g., the CMV and DMV of each H-bridge cell. The relationship between switching states and their corresponding CMV and DMV is illustrated in Table I, where

$$\begin{cases} I_{cma} = \dfrac{AU_{cma} + BU_{dma} + CU_{cmb} + DU_{dmb}}{Z_{cpva}[(Z_{cpva} + Z_{cpvb})Z_{La}Z_{Lb} + (Z_{La} + Z_{Lb})Z_{cpva}Z_{cpvb}]} \\ I_{cmb} = \dfrac{A'U_{cma} + B'U_{dma} + C'U_{cmb} + D'U_{dmb}}{Z_{cpvb}[(Z_{cpva} + Z_{cpvb})Z_{La}Z_{Lb} + (Z_{La} + Z_{Lb})Z_{cpva}Z_{cpvb}]} \end{cases} \tag{7}$$

TABLE I
CMV/DMV IN CASE OF DIFFERENT SWITCHING STATES

	1	2	3	4	5	6	7	8
S_{11}	1	1	1	1	0	0	0	0
S_{12}	0	0	0	0	1	1	1	1
S_{13}	0	0	1	1	1	1	0	0
S_{14}	1	1	0	0	0	0	1	1
S_{21}	1	1	1	1	0	0	0	0
S_{22}	0	0	0	0	1	1	1	1
S_{23}	0	1	0	1	1	0	1	0
S_{24}	1	0	1	0	0	1	0	1
U_{cma}	$U_d/2$	$U_d/2$	U_d	U_d	$U_d/2$	$U_d/2$	0	0
U_{dma}	U_d	U_d	0	0	$-U_d$	$-U_d$	0	0
U_{cmb}	$U_d/2$	U_d	$U_d/2$	U_d	$U_d/2$	0	$U_d/2$	0
U_{dmb}	U_d	0	U_d	0	$-U_d$	0	$-U_d$	0

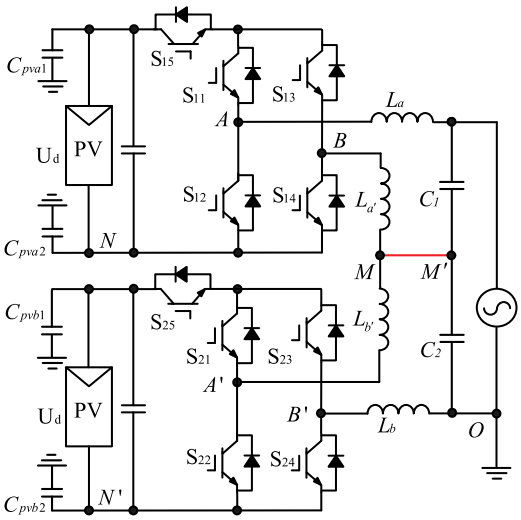

Fig. 3. Schematic diagram of the proposed single-phase cascaded topology.

U_d is the dc-link voltage. It can be observed that the CMV and DMV vary in a high-frequency manner as the switching states vary. Therefore, it is difficult to eliminate the leakage current of the conventional single-phase cascaded H-bridge topology in an effective way.

III. PROPOSED SINGLE-PHASE CASCADED TOPOLOGY

A. Proposed Topology and Modulation Strategy

In order to solve the abovementioned problem, based on an H5 inverter [27], a cascaded topology is proposed. Similar with the H5 inverter operating principle, the proposed cascaded inverter disconnects PV panel and grid connection in the freewheeling period, avoiding the voltage between PV array and ground fluctuating with the switching state variation. The schematic diagram of the proposed cascaded topology is shown in Fig. 3. It can be seen that there are two additional power switches in the proposed cascaded topology, compared with a conventional single-phase cascaded H-bridge inverter.

The common-mode model of the proposed topology is shown in Fig. 4. With Thevenin's theorem, the common-mode model

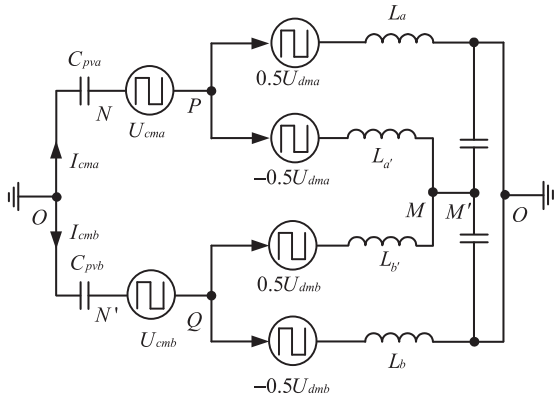

Fig. 4. High-frequency common-mode model of the proposed topology.

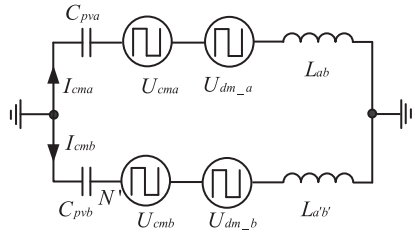

Fig. 5. Simplified common-mode model of the proposed topology.

in Fig. 4 can be simplified, as shown in Fig. 5, where

$$U_{dm\_a} = U_{dma}\frac{L_b - L_a}{2(L_a + L_b)} \tag{8}$$

$$U_{dm\_b} = U_{dmb}\frac{L_{b'} - L_{a'}}{2(L_{a'} + L_{b'})} \tag{9}$$

$$L_{ab} = L_a // L_b, L_{a'b'} = L_{a'} // L_{b'}. \tag{10}$$

From Fig. 5, the following equation can be derived:

$$\begin{cases} I_{cma}Z_{cpva} - U_{cma} - U_{dm\_a} + I_{cma}Z_{Lab} = 0 \\ I_{cmb}Z_{cpvb} - U_{cmb} - U_{dm\_b} + I_{cmb}Z_{La'b'} = 0 \end{cases} \tag{11}$$

where $Z_{Lab} = sL_{ab}$ and $Z_{La'b'} = sL_{a'b'}$. The leakage current can be derived from (11) as follows:

$$\begin{cases} I_{cma} = \dfrac{U_{cma} + U_{dm\_a}}{Z_{cpva} + Z_{Lab}} \\ I_{cmb} = \dfrac{U_{cmb} + U_{dm\_b}}{Z_{cpvb} + Z_{La'b'}} \end{cases}. \tag{12}$$

From (12), it can be concluded that leakage current is dependent on each cell's CMV and DMV, which are defined in (8) and (9). In practice, the filter inductances are generally designed as the same size, i.e., $L_a = L_b = L_{a'} = L_{b'}$. That is, $U_{dm\_a} = U_{dm\_b} = 0$. In this way, (12) can be simplified as follows:

$$\begin{cases} I_{cma} = \dfrac{U_{cma}}{Z_{cpva} + Z_{Lab}} \\ I_{cmb} = \dfrac{U_{cmb}}{Z_{cpvb} + Z_{La'b'}} \end{cases}. \tag{13}$$

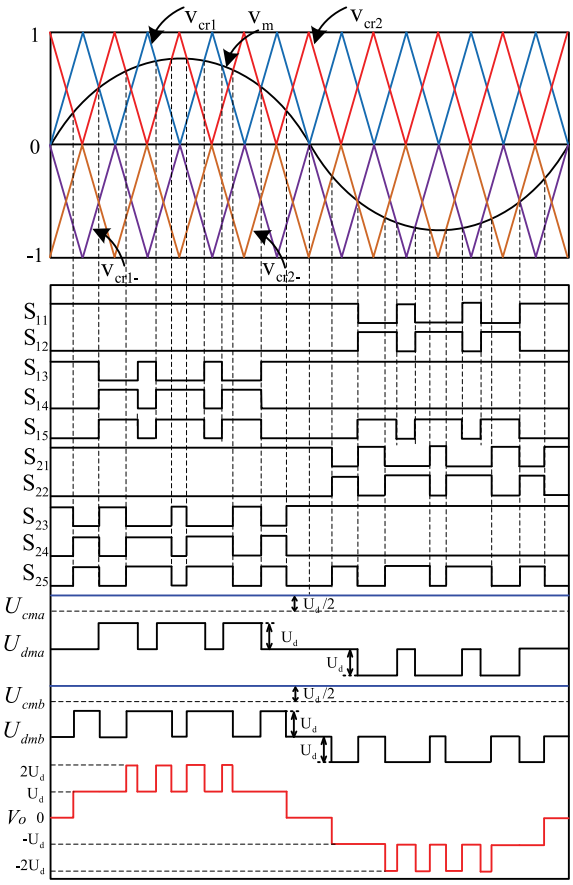

Fig. 6. Proposed modulation strategy.

From (13), it can be observed that the leakage current can be eliminated on condition that each cell's CMV is constant. In this case, the stray capacitor voltage is

$$\begin{cases} U_{cpva\_hf} = -U_{cma} = -U_d/2 \\ U_{cpvb\_hf} = -U_{cmb} = -U_d/2 \end{cases} \tag{14}$$

where U_{cpva_hf} and $U_{cpvb-hf}$ are stray capacitor C_{pva}, C_{pvb} voltage in high-frequency domain.

Fig. 6 shows the proposed modulation strategy for the cascaded topology based on the H5 topology. Due to two additional power switches in the proposed topology, the modulation is a little more complicated. But both the five-level output voltage and constant CMV can be achieved, which means the high quality output waveforms with the leakage current reduction.

Since the proposed topologies are five-level structure, four carriers of equal frequency and peak-to-peak amplitude are required, i.e., $v_{\rm cr1}$, $v_{\rm cr1-}$, $v_{\rm cr2}$, and $v_{\rm cr2-}$. The gate signals $\rm S_{11}$–$\rm S_{15}$ are generated by comparing the modulating wave v_m with the carrier waves ($v_{\rm cr1}$, $v_{\rm cr1-}$), which are symmetrically distribute on both sides of the X-axis. The gate signals $\rm S_{21}$–$\rm S_{25}$ are generated by comparing the modulating wave v_m with the carrier waves ($v_{\rm cr2}$, $v_{\rm cr2-}$), which are 180° out of phase with $v_{\rm cr1}$ and $v_{\rm cr1-}$, as shown in Fig. 6. The switching states of $\rm S_{12}$, $\rm S_{14}$, $\rm S_{22}$, and $\rm S_{24}$ are, respectively, in contrast to the signal of $\rm S_{11}$, $\rm S_{13}$, $\rm S_{21}$, and $\rm S_{23}$.

When the modulating wave is on positive half-cycle, the switches $\rm S_{11}$, $\rm S_{21}$ are turned ON and the switches $\rm S_{12}$, $\rm S_{22}$ are turned OFF. When the modulating wave v_m is greater than the carriers $v_{\rm cr1}$ and $v_{\rm cr2}$, the switches $\rm S_{14}$, $\rm S_{15}$, $\rm S_{24}$, and $\rm S_{25}$ are turned ON and the switches $\rm S_{13}$ and $\rm S_{23}$ are turned OFF. In this case, the output voltage is $2U_d$. When the modulating wave v_m is greater than the the carrier $v_{\rm cr1}$ and smaller than the carrier $v_{\rm cr2}$, the switches $\rm S_{14}$, $\rm S_{15}$, and $\rm S_{23}$ are turned ON and the switches $\rm S_{13}$, $\rm S_{24}$, and $\rm S_{25}$ are turned OFF. In this case, the output voltage is U_d. When the modulating wave v_m is smaller than the carrier $v_{\rm cr1}$ and greater than the carrier $v_{\rm cr2}$, the switches $\rm S_{13}$, $\rm S_{24}$, and $\rm S_{25}$ are turned ON and the switches $\rm S_{14}$, $\rm S_{15}$, and $\rm S_{23}$ are turned OFF. In this case, the output voltage is U_d. When the modulating wave v_m is smaller than the carrier $v_{\rm cr1}$ and smaller than the carrier $v_{\rm cr2}$, the switches $\rm S_{13}$ and $\rm S_{23}$ are turned ON and the switches $\rm S_{14}$, $\rm S_{15}$, $\rm S_{24}$, and $\rm S_{25}$ are turned OFF. In this case, the output voltage is 0.

When the modulating wave is on negative half-cycle, the switches $\rm S_{13}$ and $\rm S_{23}$ are turned ON and the switches $\rm S_{14}$ and $\rm S_{24}$ are turned OFF. When the modulating wave v_m is greater than the carrier $v_{\rm cr1-}$ and greater than the carrier $v_{\rm cr2-}$, the switches $\rm S_{11}$ and $\rm S_{21}$ are turned ON and the switches $\rm S_{12}$, $\rm S_{15}$, $\rm S_{22}$, and $\rm S_{25}$ are turned OFF. In this case, the output voltage is 0. When the modulating wave v_m is greater than the carrier $v_{\rm cr1-}$ and smaller than the carrier $v_{\rm cr2-}$, the switches $\rm S_{11}$, $\rm S_{22}$, and $\rm S_{25}$ are turned ON and the switches $\rm S_{12}$, $\rm S_{15}$, and $\rm S_{21}$ are turned OFF. In this case, the output voltage is $-U_d$. When the modulating wave v_m is smaller than the carrier $v_{\rm cr1-}$ and greater than the carrier $v_{\rm cr2-}$, the switches $\rm S_{12}$, $\rm S_{15}$, and $\rm S_{21}$ are turned ON and the switches $\rm S_{11}$, $\rm S_{22}$, and $\rm S_{25}$ are turned OFF. In this case, the output voltage is $-U_d$. When the modulating wave v_m is smaller than the carrier $v_{\rm cr1-}$ and smaller than the carrier $v_{\rm cr2-}$, the switches $\rm S_{12}$, $\rm S_{15}$, $\rm S_{22}$, and $\rm S_{25}$ are turned ON and the switches $\rm S_{11}$ and $\rm S_{21}$ are turned OFF. In this case, the output voltage is $-2U_d$. Table II shows the different switching states and their corresponding CMV and DMV.

It should be noted that in the above theoretical analysis, the effect of the grid voltage on the leakage current is neglected. In order to clarify this point, the low-frequency common-mode model of the proposed topology of Fig. 3 is established in Fig. 7, where the grid voltage V_o is split due to the filter capacitor divider. It is assumed that $L_a = L_b = L_{a'} = L_{b'} = L$ for simplicity of analysis.

Take "O" in Fig. 7 as a reference node, with the node voltage method, the following equations can be obtained, where u_{n1}, u_{n2}, u_{n3}, and u_{n4} are four node voltages, as shown in Fig. 7. $Z_{cpva} = 1/(sC_{pva})$, $Z_{cpvb} = 1/(sC_{pvb})$, and $Z_L = sL$

$$\begin{cases} \left(\dfrac{1}{Z_{cpva}} + \dfrac{1}{Z_L} + \dfrac{1}{Z_L}\right) u_{n1} - \dfrac{1}{Z_L} u_{n3} - \dfrac{1}{Z_L} u_{n4} = 0 \\ \left(\dfrac{1}{Z_{cpvb}} + \dfrac{1}{Z_L} + \dfrac{1}{Z_L}\right) u_{n2} - \dfrac{1}{Z_L} u_{n3} = 0 \\ u_{n3} = V_o/2 \\ u_{n4} = V_o. \end{cases} \tag{15}$$

TABLE II
SWITCHING STATES OF THE PROPOSED CASCADED INVERTER

v_m		Switches of upper H5 unit			Switches of lower H5 unit			CMV		DMV	
		S_{11}	S_{13}	S_{15}	S_{21}	S_{23}	S_{25}	U_{cma}	U_{cmb}	U_{dma}	U_{dmb}
$v_m > 0$	$v_{cr1} < v_m > v_{cr2}$	1	0	1	1	0	1	$U_d/2$	$U_d/2$	U_d	U_d
	$v_{cr1} < v_m < v_{cr2}$	1	0	1	1	1	0	$U_d/2$	$U_d/2$	U_d	0
	$v_{cr1} > v_m > v_{cr2}$	1	1	0	1	0	1	$U_d/2$	$U_d/2$	0	U_d
	$v_{cr1} > v_m < v_{cr2}$	1	1	0	1	1	0	$U_d/2$	$U_d/2$	0	0
$v_m < 0$	$v_{cr1-} < v_m > v_{cr2-}$	1	1	0	1	1	0	$U_d/2$	$U_d/2$	0	0
	$v_{cr1-} < v_m < v_{cr2-}$	1	1	0	0	1	1	$U_d/2$	$U_d/2$	0	$-U_d$
	$v_{cr1-} > v_m > v_{cr2-}$	0	1	1	1	1	0	$U_d/2$	$U_d/2$	$-U_d$	0
	$v_{cr1-} > v_m < v_{cr2-}$	0	1	1	0	1	1	$U_d/2$	$U_d/2$	$-U_d$	$-U_d$

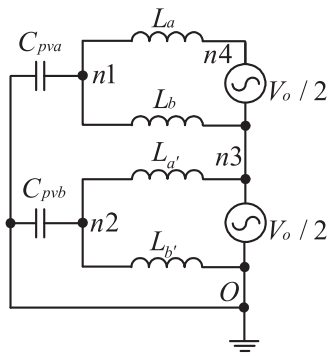

Fig. 7. Low-frequency common-mode model of the proposed topology.

TABLE III
PARAMETERS OF THE CASCADED INVERTER

Parameter	Value
Input voltage	120 V_{DC} for each bridge
Output voltage	180 V_{AC}/50 Hz
Rated power	500 W
Switching frequency	10 kHz
Insulated gate bipolar transistor	IKW40T120
L_a, L_b (conventional circuit) L_a, L_b, $L_{a'}$, $L_{b'}$ (new circuit)	Core: A60-572A
	5 Mh 2.5 mH
Filter capacitor	9.4 μF
PV parasitic capacitor	150 nF
Rated power	500 W
Gate driver	DCP020515DB+ HCPL-J312

The low frequency voltage across the stray capacitor can be derived from (15) as follows:

$$\begin{cases} U_{cpva-lf} = u_{n1} = \dfrac{3Z_{cpva}}{Z_L + 2Z_{cpva}} \dfrac{V_o}{2} \\ U_{cpvb-lf} = u_{n2} = \dfrac{Z_{cpvb}}{Z_L + 2Z_{cpvb}} \dfrac{V_o}{2} \end{cases} \tag{16}$$

where $U_{cpva-lf}$ is the voltage of stray capacitor C_{pva} in low-frequency model, $U_{cpvb-lf}$ is the voltage of stray capacitor C_{pvb} in low-frequency model. In the low-frequency domain, there is $Z_{cpva} \gg Z_L$ and $Z_{cpvb} \gg Z_L$. Therefore, (16) can be simplified as

$$\begin{cases} U_{cpva-lf} = \dfrac{3}{2} \dfrac{V_o}{2} \\ U_{cpvb-lf} = \dfrac{1}{2} \dfrac{V_o}{2}. \end{cases} \tag{17}$$

The stray capacitor voltage is the sum of low-frequency and high-frequency components. Based on the analysis of high-frequency models in Fig. 4 and low-frequency models in Fig. 7, the full expression of the stray capacitor voltage can be obtained

$$U_{cpva} = U_{cpva-lf} + U_{cpva-hf} = \frac{3}{2}\frac{V_o}{2} - U_d/2 \tag{18}$$

$$U_{cpvb} = U_{cpvb-lf} + U_{cpvb-hf} = \frac{1}{2}\frac{V_o}{2} - U_d/2 \tag{19}$$

where U_{cpva} and U_{cpvb} are the voltage of stray capacitors C_{pva} and C_{pvb}, respectively. From (18) and (19), it can be observed that the stray capacitor voltage of the upper cell is different from that of the lower cell. The amplitude ratio of their low-frequency components is 3:1, which means the leakage current of the upper cell will be a little bit higher than that of the lower cell. On the other hand, it should be noted that the stray capacitor voltage is free of any high-frequency components. Therefore, the high frequency leakage current can be effectively eliminated, which will be experimentally verified in the following section.

B. Asymmetric Cascaded Inverters

The proposed cascaded inverter is composed of two single-phase H5 inverters and can be classified into symmetric and asymmetric groups based on the magnitude of dc voltage sources. In the symmetric types, the magnitudes of the dc voltage sources of two H5 are equal, whereas in the asymmetric types, the values of the dc voltage sources of two H5 are different. The performance of the symmetric types has been illustrated above. In the asymmetric types, when the voltage ratio is 1:2 for the upper and lower H5 unit, it will generate seven-level output voltage. When the voltage ratio is not 1:2 for the upper and lower H5 unit, it will generate nine-level output voltage theoretically. However, it can only generate seven-level output voltage using the proposed reducing CMV modulation strategy. The reason is that the redundancy of switching states is decreasing with the number of levels increasing. Moreover, there are only

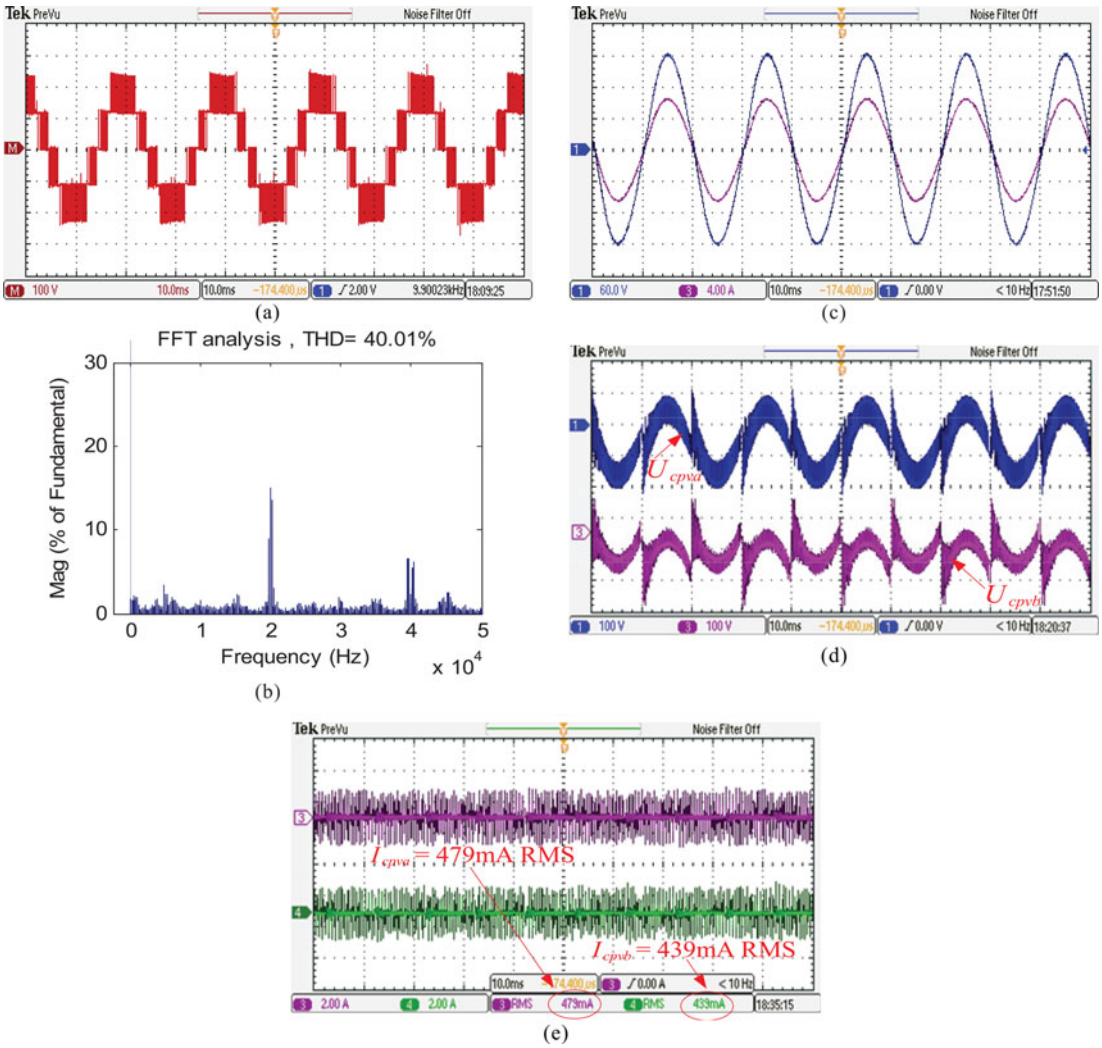

Fig. 8. Experimental results of the conventional topology: (a) output voltage, (b) FFT analysis, (c) voltage and current after the filter, (d) stray capacitor voltage, and (e) leakage current.

seven switching states in the proposed modulation strategy. In summary, it will generate seven-level output voltage in the asymmetric types. The output waveform quality will be improved. The high-frequency and low-frequency common-mode models for asymmetric types are equivalent to symmetric types', as shown in Figs. 5 and 7. The leakage current is influenced by the sum of U_{cma} and U_{cmb}. When the dc supply voltage for upper H5 unit is aU_d, and the dc supply voltage for lower H5 unit is bU_d, in this case, the CMV $U_{cma} = aU_d/2$, and $U_{cmb} = bU_d/2$. Thus, due to the constant CMV, the leakage current can be reduced effectively in an asymmetric cascaded inverter. The derivation process of the stray capacitor voltage is similar to formula (18) and (19). The stray capacitor voltage is expressed as follows:

$$\begin{cases} U_{cpva} = \dfrac{a+2b}{a+b} \cdot V_o - \dfrac{a}{2}U_d \\ U_{cpvb} = \dfrac{b}{a+b} \cdot V_o - \dfrac{b}{2}U_d. \end{cases} \tag{20}$$

It can be seen that the stray capacitor voltage is free of any high-frequency components, and only a dc and low-frequency ac components exist. Because of constant CMV in the proposed modulation strategy, the leakage current will be suppressed effectively.

For symmetrical topology, $a = 1$, $b = 1$ in (20), the variety value of stray capacitor voltage is

$$\begin{cases} \Delta U_{cpva} = \left(\dfrac{a+2b}{a+b} \cdot V_{o\max} - \dfrac{a}{2}U_d\right) \\ \qquad -\left(\dfrac{a+2b}{a+b} \cdot V_{o\min} - \dfrac{a}{2}U_d\right) = \dfrac{3}{2}\left(V_{o\max} - V_{o\min}\right) \\ \Delta U_{cpvb} = \left(\dfrac{b}{a+b} \cdot V_{o\max} - \dfrac{b}{2}U_d\right) \\ \qquad -\left(\dfrac{b}{a+b} \cdot V_{o\min} - \dfrac{b}{2}U_d\right) = \dfrac{1}{2}\left(V_{o\max} - V_{o\min}\right) \end{cases} \tag{21}$$

where ΔU_{cpva} and ΔU_{cpvb} are the variety value of stray capacitor voltage C_{pva}, C_{pvb}, respectively. $V_{o\max}$ and $V_{o\min}$, respectively, are the maximum and minimum value of output voltage.

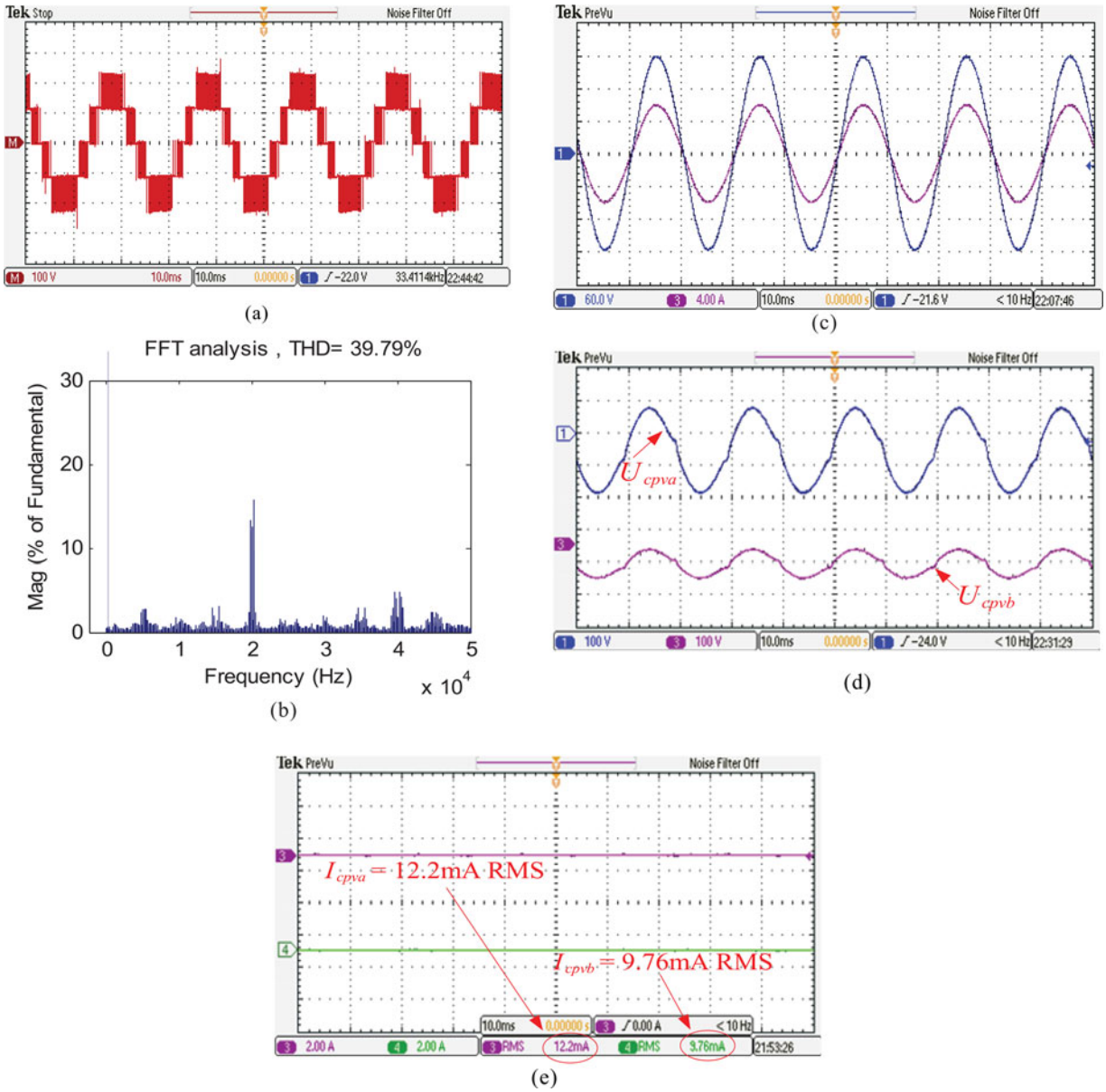

Fig. 9. Experimental results of the proposed topology: (a) output voltage, (b) FFT analysis, (c) voltage and current after the filter, (d) stray capacitor voltage, and (e) leakage current.

For asymmetrical topology, e.g., $a = 1$, $b = 2$ in (20), the variety value of stray capacitor voltage is

$$\begin{cases} \Delta U_{cpva} = \left(\dfrac{a+2b}{a+b} \cdot V_{o\max} - \dfrac{a}{2}U_d\right) \\ \qquad - \left(\dfrac{a+2b}{a+b} \cdot V_{o\min} - \dfrac{a}{2}U_d\right) = \dfrac{5}{3}\left(V_{o\max} - V_{o\min}\right) \\ \Delta U_{cpvb} = \left(\dfrac{b}{a+b} \cdot V_{o\max} - \dfrac{b}{2}U_d\right) \\ \qquad - \left(\dfrac{b}{a+b} \cdot V_{o\min} - \dfrac{b}{2}U_d\right) = \dfrac{2}{3}\left(V_{o\max} - V_{o\min}\right). \end{cases} \tag{22}$$

From (21) and (22), it can be seen that the variety value of stray capacitor voltage of the asymmetrical topology is larger than that of the symmetrical topology. Therefore, the symmetrical topology is better from the leakage current point of view.

When the number of output voltage levels is more than seven, it needs three or more H5 units to be cascaded. The proposed topology and modulation strategy can be extended to a general multilevel converter. If n H5 units are cascaded, it needs $2n$ carriers to modulate and the maximum number of output voltage levels is

$$N = 2(C_n^0 + C_n^1 + \cdots + C_n^{n-1} + C_n^n) - 1 = 2^{n+1} - 1 \tag{23}$$

where N is the maximum number of output voltage levels. When the dc supply voltage is equal for every H5 unit, the level of output voltage is

$$N = 2n + 1. \tag{24}$$

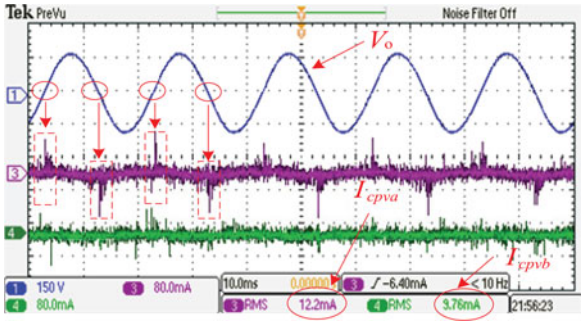

Fig. 10. Zoomed experimental results of Fig. 9(d).

The paper mainly focuses on two cascaded H5 units, three or more H5 units cascaded are out of the scope of this paper.

IV. Experimental Results

This section presents the performance test of the conventional cascaded H-bridge and the proposed topologies. The control and modulation strategies are implemented in the TMS320F28335 DSP + XC3S400 FPGA digital control platform. The specifications of the converter are listed in Table III.

Fig. 8 shows the experimental results of the conventional cascaded H-bridge topology. It can be observed that the output voltage waveform is five-level as 240 V, 120 V, 0, –120 V, and –240 V. The harmonics in output voltage appear as sidebands centered around $2f_c$ and its multiples such as $4f_c$, where f_c is the carrier frequency. The first-harmonic cluster of switching ripples appears at $2f_c$. In agreement with the theoretical analysis, the stray capacitor voltage is full of high-frequency components. Consequently, the leakage currents are very high, and in experiment their rms values of the upper and lower cells are 479 mA and 439 mA, respectively, which are far beyond 30 mA, as specified in the VDE0126-1-1.

Fig. 9 shows the experimental results of the proposed topology. It can be observed that the output voltage waveform is five-level as 240 V, 120 V, 0, –120 V and –240 V. The harmonics in output voltage appear as sidebands centered around $2f_c$ and its multiples such as $4f_c$, where f_c is the carrier frequency. The first harmonic cluster of switching ripples appears at $2f_c$. In agreement with the theoretical analysis of (17) and (18), the stray capacitor voltage is free of any high-frequency components, and only a dc and low-frequency ac components exist. The amplitude ratio of low-frequency ac components in the upper and lower cells is 3:1. That is the reason why the leakage current of the upper cell is larger than that of the lower cell. Their rms values of upper and lower cells are 12.2 mA and 9.76 mA, respectively, which are well below 30 mA and meet the requirement of the VDE0126-1-1 standard.

Fig. 10 shows the zoomed experimental results of Fig. 9(d). In agreement with the theoretical analysis of (17) and (18), the instantaneous leakage current of the upper cell reaches the maximum value at the zero crossing point of V_o, due to the fact that $i = C(du/dt)$. On the other hand, the instantaneous leakage current of the lower cell has no significant spikes, which is mainly due to the fact that the stray capacitor voltage of the lower cell is much smaller than that of the upper cell.

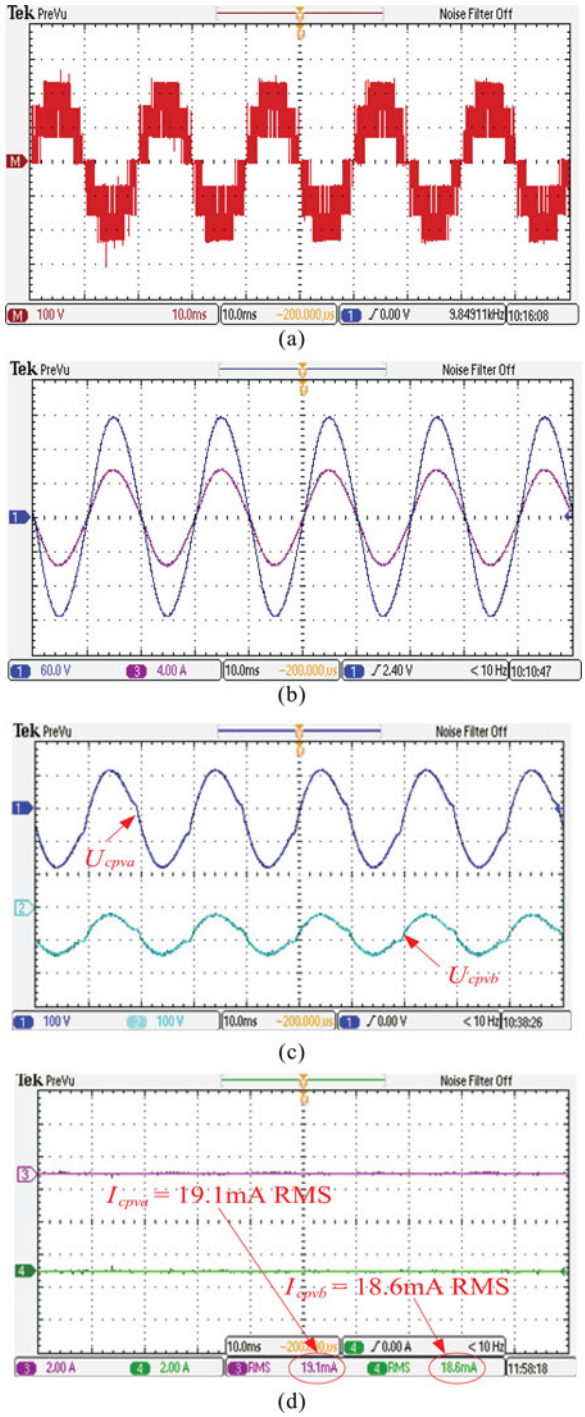

Fig. 11. Experimental results of the proposed topology for voltage ratio 1:2: (a) output voltage, (b) voltage and current after the filter, (c) stray capacitor voltage, and (d) leakage current.

Further experimental tests regarding the proposed asymmetric cascaded topologies are carried out. The dc supply voltages of the upper and lower H5 units are different in this case. Take the voltage ratio 1:2 for instance. The experiment results are illustrated in Fig. 11. The dc input voltage of upper cell is 80 V, the

TABLE IV
EXPERIMENTAL RESULTS OF THE LEAKAGE CURRENT

		I_{cpva}	I_{cpvb}
Conventional topology		479 mA	439 mA
Proposed topology	Symmetric type	12.2 mA	9.76 mA
	Asymmetric type	19.1 mA	18.6 mA

dc input voltage of lower cell is 160 V, which means the equivalent input voltage is 240 V. The ac voltage is 180 V/50 Hz. The switching frequency is 10 kHz. The filter inductor and capacitor are 5 mH and 9.4 μF, respectively. The stray capacitance is 150 nF. Fig. 11 shows the experimental results of the asymmetric proposed topology. It can be observed that the output voltage waveform is seven-level as 240 V, 160 V, 80 V, 0, –80 V, –160 V and –240 V. The stray capacitor voltage is free of any high-frequency components, and only a dc and low-frequency ac components exist. Their rms values of upper and lower cells are 19.1 and 18.6 mA, respectively, which are well below 30 mA and meet the requirement of the VDE0126-1-1 standard.

The summary of the leakage currents is shown in Table IV. It can be observed that the conventional single-phase cascaded H-bridge topology fails to reduce the leakage current. While, with the proposed topology and modulation strategy, the leakage current can be effectively reduce below 30 mA, which complies with the VDE0126-1-1 standard. It can be observed when the output voltage is equal, the leakage current of the asymmetrical topology is larger than that of the symmetrical topology, which is in good agreement with the theoretical analysis of (21) and (22).

V. CONCLUSION

This paper has presented the theoretical analysis and experimental verification of a cascaded topology based on the H5 inverter and modulation strategy to reduce the leakage current for single-phase transformerless PV systems. Compared with the filter-based solution, the proposed topology-based solution needs to add small active switching devices instead of bulky passive components. There is no need to design the parameter of bulky and heavy filters. The experimental results indicate that the conventional single-phase cascaded H-bridge topology fails to reduce the leakage current. On the other hand, the proposed topology and new modulation strategy can ensure that the stray capacitor voltage is free of any high-frequency components. Therefore, the leakage current can be significantly suppressed well below 30 mA, as specified in the standard VDE-0126-1-1. Therefore, it is attractive for single-phase transformerless PV systems.

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