0.8/2.2-GHz Programmable Active Bandpass Filters in InP/Si BiCMOS Technology

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***Abstract*—Programmable active bandpass filters (BPFs) have been designed in a chip-scale heterogeneous integration technology, which intimately integrates InP HBTs on a deep scaled CMOS technology. Therefore, the active BPF can leverage both high performance of InP HBT and high density and programmability of CMOS. Two BPF prototypes, consisting of a programmable gain amplifier (PGA), a fifth- or third-order BPF core, and a buffer, have been designed and fabricated. The BPF center frequency can be switched from 0.8 to 2.2 GHz with 150-MHz passband and delivers >55-dB out-of-band (OOB) rejection for the fifth-order one. Four gain steps: 0, 6, 12, and 16 dB, are enabled by the front PGA to trade off noise and linearity performances. Due to the >300-GHz f_T of InP HBTs, the BPF cores can leverage active-*RC* architecture for high linearity owing to the close-loop implementation. The fifth-order BPF prototype occupies a 1.5×1.02 mm^2 area together with pads and draws 106/121 mA from a 3.3-V power supply for 0.8/2.2-GHz bands, respectively, which demonstrates OOB output third-order intercept points (OIP3s) of 22.69/21.25 dBm for 0.8/2.2-GHz bands at the high gain mode. The measurement results suggest the fifth-order BPF core achieves 36.69/35.25-dBm OOB OIP3s. In addition, the designed third-order programmable BPF has been successfully used as a technology yield vehicle to assist the BiCMOS technology development.**

***Index Terms*—Bandpass filter (BPF), BiCMOS integrated circuit, heterojunction bipolar transistor (HBT), indium phosphide (InP), wafer-scale integration.**

I. Introduction

A VARIETY of technologies have been developed so far to push performance envelops of electronic systems. For example, silicon CMOS technologies have the unparalleled integration capability and dominate system-on-a-chip (SoC) implementations in a variety of applications, such as TV tuners [1], wireless local area network (WLAN) [2], mobile communications [3], and even millimeter-wave applications like car radar applications at 24- and 77-GHz bands [4]. In contrast, III–V compound semiconductors featuring much higher f_T, f_{MAX}, and breakdown voltage than those of CMOS [5], such as GaAs or InP. Hence, GaAs dominates power amplifier (PA) markets, and InP starts to penetrate into terahertz electronics [6], where CMOS has yet limited presence. Moreover, wideband compound semiconductor technologies, such as GaN or SiC, can readily support an over 10-V breakdown voltage with high device f_T and f_{MAX} [7], which render GaN a good candidate to deliver an extreme high-power PA [8]. Additionally, zero bandgap semiconductors, such as graphene, feature ultra-thin layer with high mobility and demonstrate potentials for high-speed analog circuits [9]. Though with lots of technology options, there is no single technology delivering all the desired features that electronic systems demand. To create a new device to offer all desired features concurrently may be far fetched or prohibitively expensive. A possible approach could be integrating several technologies together intimately [10].

Heterogeneous technologies can benefit electronics systems through a variety of high-performance function blocks. Analog-to-digital converters and digital-to-analog converters (DACs) can fully leverage the advantages of the heterogeneous integration technologies due to the benefits from both device speed/dynamic range and sophisticated calibration [11]. In contrast, RF circuits tend to be small-scale, e.g., low-noise amplifiers (LNAs) [12] and mixers, and only demand several high-performance transistors. Such configuration seems not being able to fully exploiting performance advantages from the heterogeneous integration other than a small form factor. This perception may not be accurate when we design an integrated RF transceiver, which consists of many RF blocks and demands extremely tight matching, fine frequency tuning, and ultra-low transmitter local oscillator (LO) leakage. Calibration and self-healing algorithms are usually employed to enhance these performances [13], which are hard to be achieved by only relying on open-loop operations. One additional advantage with these embedded-calibration functions is to enable the optimization of RF circuits with the alleviation of transistor matching concern, which otherwise results in large device sizes and inferior performance in speed and power consumption. Furthermore, heterogeneous integration technologies also enable RF functions that are not available otherwise, such as a highly linear and programmable bandpass filter (BPF) over an octave band.

There are several approaches to realize a programmable active BPF. Reference [14] used CMOS varactors and on-board

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passive components to implement a second-order discrete BPF, which is large and has a poor linearity due to the nonlinear varactors. Reference [15] leveraged a microelectromechanical system (MEMS) technology to implement a third-order integrated BPF at 1 GHz, which is bulky and not compatible with chip integration. Q boosted inductor-based BPFs are often used to emulate passive BPFs and allow a low power implementation [16], [17]. However, the Q boosted inductor is essentially an active component that leverages positive feedback and suffers from both poor linearity and noise performance. A G_m-C filter is often used to realize an integrated, high-frequency, and tunable BPF. However, they also demonstrate poor linearity. Though a switched G_m-C BPF can provide good performance [18], it mandates an extra LO and increases design complexity and system form factor. In addition, the long LO switching time constrains the system adaptation speed, and shares the identical problem of conventional RF transceivers. Active-*RC* filters have been employed at low frequencies and promise excellent linearity due to their closed-loop operations [19], [20]. However, they mandate op-amps with an extremely high gain-bandwidth (GBW) product, which cannot be easily achieved by current technologies. In this paper, we present a programmable active-*RC* BPF based on HRL's InP/Si BiCMOS technology, enabled by the op-amp with >100-GHz GBW and CMOS programmability.

This paper introduces a fifth-order active BPF [21] based upon an InP/Si BiCMOS technology. The active-*RC* BPF can switch its center frequency from 0.8 to 2.2 GHz, and has the potential to continuously cover the entire band for software-defined radio (SDR) applications. Simultaneously, a developed third-order active BPF has been developed early to served as an excellent test vehicle to evaluate the technology yield and diagnose the developed technology defects during processing. This paper is arranged as follows. In Section II, we briefly introduce the InP/Si heterogeneous integration technology. Section III presents the active programmable filter design and simulation results. Section IV shows the measurement results, and Section V describes how we leverage the third-order BPF to diagnose the technology yield, followed by a conclusion in Section VI.

II. InP/Si BiCMOS Integration Technology

HRL has developed an intimate heterogeneous integration technology vertically integrating InP HBTs with CMOS technology. The interconnect via between the CMOS tier and the InP tier features only 1×1 μm^2 size with negligible parasitic. Compared with lateral integration technologies, e.g., SiGe technologies, this approach enables a technology agnostic integration in a silicon platform and features a low processing cost. The integration starts with a fabricated unfinished CMOS wafer and a fully grown epitaxial InP HBT wafer. The CMOS wafer has full thickness and stops at one planarized metal layer. The InP double heterojunction bipolar transistor (DHBT) epitaxial layer is then transferred from its growth substrate to a temporary handle wafer, and subsequently bonded to the silicon CMOS wafer. Once bonded, the handle wafer is removed and subsequent InP DHBT and heterogeneous interconnect processing starts. There are several technology aspects requiring special attention, which are: 1) the heat sink of the InP DHBT to ensure the operating temperature of the HBT; 2) the yield impact of the epitaxial layer transfer and the additional topography due to the head spreader and adhesion layer; and 3) the heterogeneous connection via between the InP DHBT and the bottom CMOS metal. Fig. 1(a) presents a cross section of the integration technology and Fig. 1(b) shows a scanning electron microscope (SEM) image of a heterogeneously integrated 250-nm InP DHBT on top of a 90-nm silicon CMOS technology. The technology development is detailed in [10].

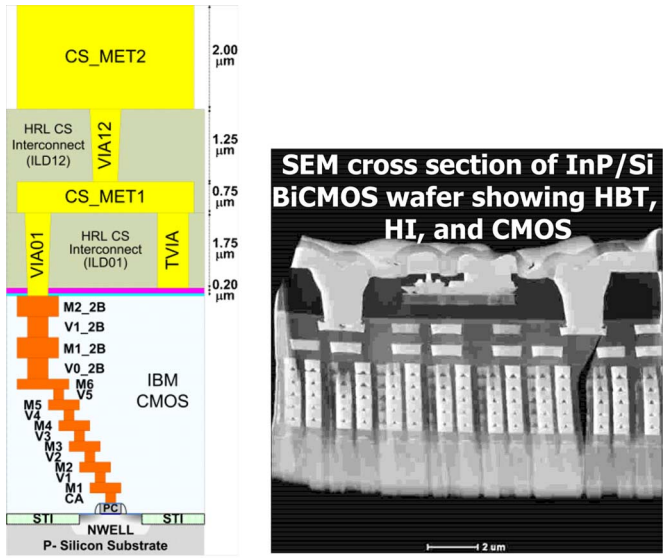


Fig. 1. (a) Cross section of HRL InP/Si BiCMOS technology shows the InP DHBT tier is intimately integrated on a CMOS tier vertically. M1 to M2-2B are the metal interconnects layers fabricated with the CMOS, and CS_MET1 represents the global interconnect layer fabricated during heterogeneous integration. VIA01 and TVIA are the heterogeneous connection via and thermal via. (b) TEM image of the cross section of a fabricated chip showing DHBT and CMOS devices.

From design perspectives, the developed integration technology offers designers more options with devices that excel in different aspects, such as high speed, low power, high breakdown voltage, and efficient light emission. HRL also provides a complete set of process design kits to facilitate the design, including the Cadence design kit, Spectre model, layout verification rules, and layout *RC* parasitic extraction rules.

III. Programmable BPF Circuit Design

Conventional radio transceivers tend to use low-pass filters to attenuate out-of-band (OOB) jammers, which features low power consumption and simple design such as a direct conversion RF transceiver [22]. This approach works well when the radios do not need to adapt and dwell rapidly between frequency channels. However, it constrains the system frequency-hopping speed because the system relies on LOs to switch between frequency channels, where a frequency synthesizer is often used, and demonstrates tens of microsecond settling time. In order to reduce channel settling time and boost RF system hopping speed, a programmable BPF may be used together with direct RF-to-digital or digital-to-RF converters (DRCs). Fig. 2 shows

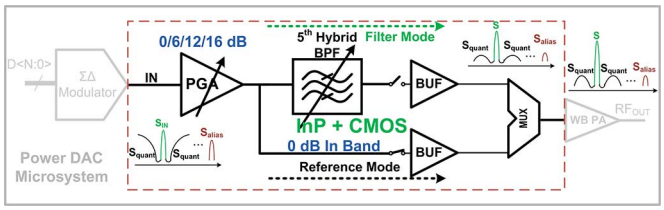


Fig. 2. Diagram of a direct digital-to-RF signal generator.

a diagram of a direct digital-to-RF signal generator, i.e., power DAC [23], where a BPF is required to filter out the images generated by the DRC. This BPF must deliver high linearity, wideband programmability, and fast frequency switching concurrently.

Passive BPFs are often used in the radio front end due to their high linearity and power-handling capability, which, however, have limited frequency tunability. A solution with multiple BPFs and single-port multiple-throw switches renders a bulky system and is not preferred. Therefore, active BPFs are seriously considered due to their excellent configurability and compact implementation. However, they demonstrate poor linearity that hinders their deployment in the radio front end. On the other hand, the intended DRC imposes reduced requirement on the BPF bandwidth and stopband rejection due to a high-frequency operation, whose aliases are several hundred megahertz away from the center frequency. This greatly relaxes the design complexity due to a lower Q requirement. In this project, we target to deliver a BPF function with programmable center frequencies, 150-MHz passband, >50-dB rejection at 300 MHz away, <25-dB noise figure (NF), and >30-dBm OOB output third-order intercept point (OIP3).

A fifth-order 0.8–2.2-GHz programmable BPF has been designed to achieve 150-MHz passband with >50-dB OOB attenuation based upon a fifth-order *LC* passive BPF prototype, as shown in Fig. 3(a). The BPF programmability is achieved by switchable resistor and capacitor banks, as exemplified in Fig. 3(b), and covers two 0.8- and 2.2-GHz bands. To achieve high OOB rejection and relax the Q requirement of each biquad concurrently, we adopt a hybrid filter architecture. The BPF is partitioned into a third-order BPF with the an elliptic architecture, and a second-order BPF with a Chebyshev architecture. The hybrid BPF demonstrates sharp transition bands with design flexibility to position OOB zeros at the alternative adjacent channel for a large attenuation. The third-order elliptic BPF has also been built into an individual test chip. To maintain a modest NF, we use a filter characteristic impedance of 100 Ω with 200 Ω differentially. We then construct the active BPF based on a programmable passive *LC* BPF prototype, as shown in Fig. 3(a). Since the BPF performs at high frequencies, it has a small group delay that does not distort the transmission signal significantly. In essence, the active BPF synthesizes the high Q, programmable tanks through active *RC* implementations, and achieve the similar filtering function by using a much smaller area than the passive realizations. The quality factor of each active tank is determined by the gain of the op-amp at the operating frequencies, which is proportional to the GBW of the op-amp.

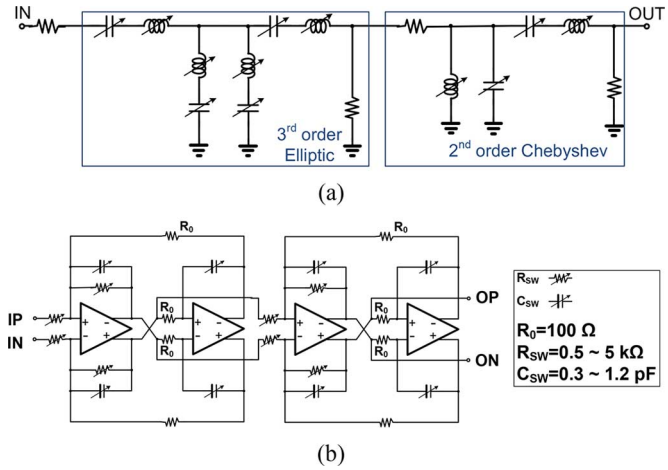


Fig. 3. (a) *LC* representation of a fifth-order BPF. (b) Diagram of the second-order BPF in the fifth-order programmable BPF, whose Q can be as high as 57 for the biquad stages at 2.4 GHz.

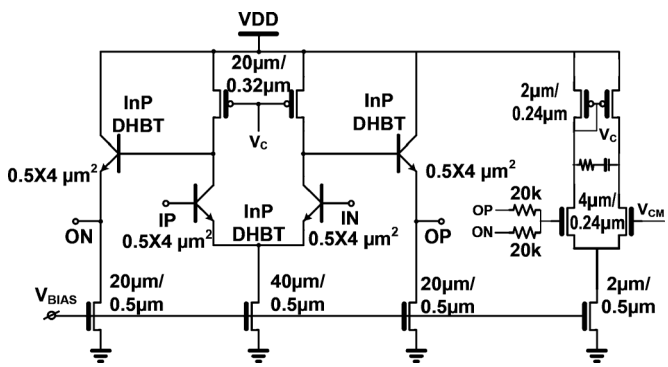
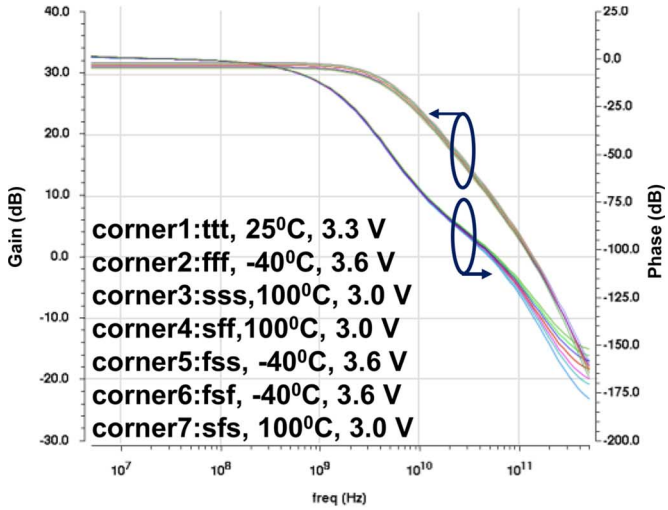


Fig. 4. Schematic of the two-stage op-amp, which features fully differential implementation with CMFB circuit and strong drivability.

In order to achieve a high-Q tank mandated by the BPF, the op-amp must deliver a >8/24-GHz GBW for the 0.8/2.4-GHz operation to ensure a larger than 20-dB gain. Simultaneously, the op-amp needs to drive the associated loads, including the load resistors and capacitors, which are around 1.4/0.3 pF for the 0.8/2.4-GHz frequency bands. We adopt a two-stage op-amp architecture to leverage the high-speed InP DHBT to deliver a high gain for the first stage and a strong drivability for the second stage, as sketched in Fig. 4. The op-amp uses differential implementation with a common-mode feedback (CMFB) circuit to ensure the output common mode at the half of the supply voltage. Post-layout simulation verifies that the op-amp provides a >20/34-GHz GBW across process corners with the corresponding loads at 0.8/2.2 GHz. The GBW even exceeds 150 GHz when without external loads, as summarized in Fig. 5.

The programmable BPF core is shown in Fig. 3. To alleviate the noise and linearity performance tradeoff, a preceding PGA is applied in the front of the BPF to offer four gain options: 0, 6, 12, and 16 dB, by using the identical op-amp. To facilitate characterization, we have designed a unity gain output buffer to drive a 250-Ω load, which consists of a 200-Ω on-chip resistor and an off-chip 50-Ω load of the instrument. The resistor divider imposes 14-dB loss to the BPF. In addition, an extra through path has been designed to bypass the BPF core and connect the PGA



(a)

	Gain Bandwidth	Phase Margin
corner1	164.8 GHz	51.47
corner2	172.7 GHz	53.71
corner3	157.9 GHz	49.41
corner4	158.2 GHz	54.29
corner5	171.5 GHz	48.54
corner6	178.0 GHz	54.91
corner7	152.5 GHz	47.99

(b)

Fig. 5. (a) Simulated gain and phase of the two-stage InP/Si BiCMOS opamp with extracted parasitic resistance and capacitance. (b) Simulated GBW product and phase margin at seven process, voltage, and temperature corners.

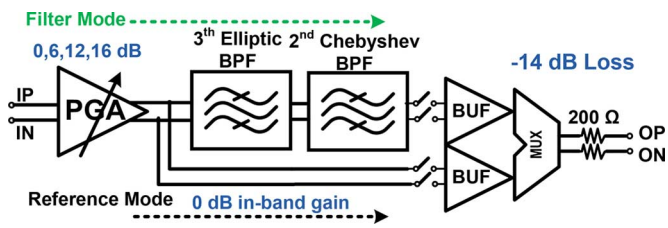


Fig. 6. Diagram of the test chip with a PGA, a fifth-order hybrid BPF, and the buffers.

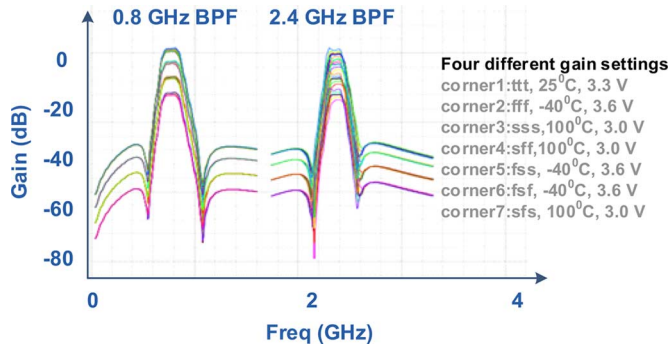


Fig. 7. Simulated third-order elliptic BPF filtering function with four programmable gains and two tuning frequencies across seven process, voltage, and temperature corners.

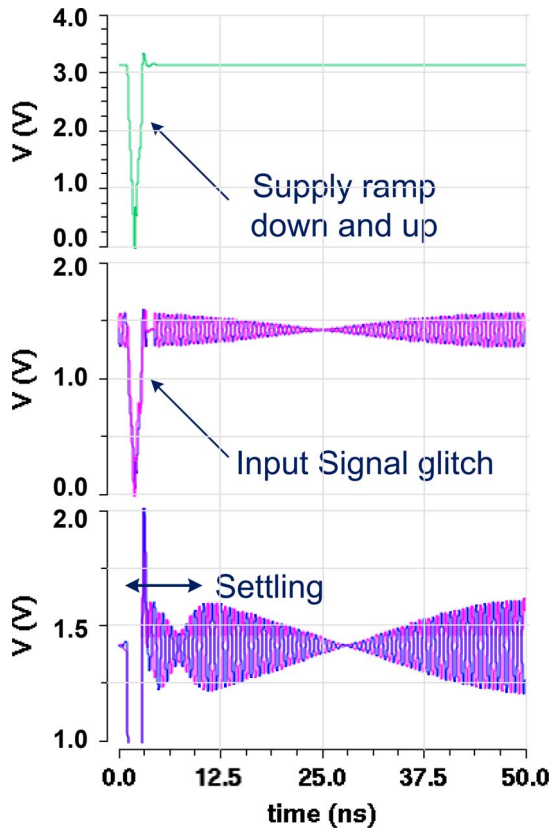


Fig. 8. Simulated BPF transient waveform with supply ramp down/up and input signal glitch.

directly to the output buffer for de-embedding. Fig. 6 presents the BPF test chip configuration.

Fig. 7 gives the filtering function of the first third-order elliptic BPF of the test chip in post-layout simulation. Simulation results suggest the BPF can reliably deliver the desired filtering functions at both 0.8 and 2.4 GHz across all seven simulated process/voltage/temperature corners.

The BPF stability is always a concern due to its high-Q operation. We have verified that in both linear and transient simulations. When evaluating the filter stability in linear analysis, we usually simulate each individual loop to ensure enough phase margin together with other circuits in active conditions. When evaluating the filter stability in transient analysis, we apply an input signal spike and quickly ramp the supply voltage down and up to simulate the circuit. When there is instability, an oscillation can be built up to indicate that. Fig. 8 shows the input signal spike and supply ramping, together with the simulated BPF outputs under two-tone simulations. The outputs quickly settle into normal operation without significant ringing, which suggests the BPF is reliably stable at the simulation corners.

Compared with the traditional LO-based transmitter, one advantage of the proposed direct digital-to-RF signal generator is the fast channel switching. In order to realize such an architecture, the BPF must demonstrate similar or shorter settling time than the target channel switching time, which could be around tens of nanoseconds. We have conducted a post-layout simulation to verify this. A single-tone signal at 850 MHz is fed into

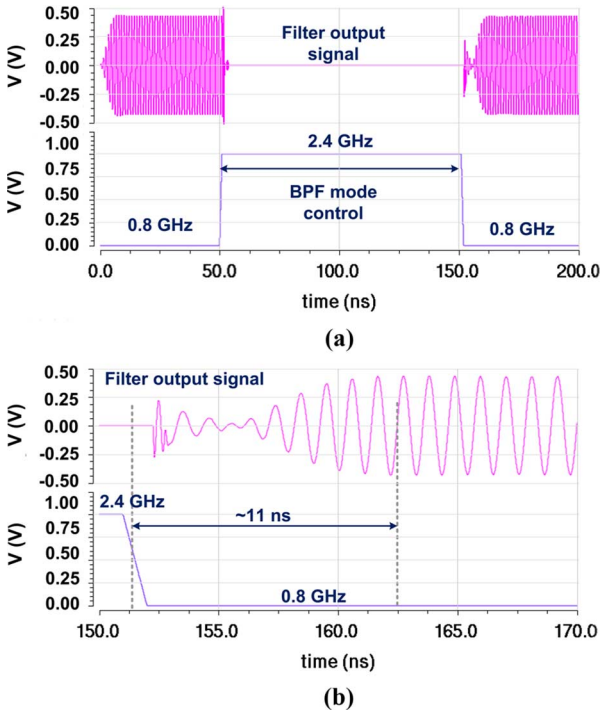


Fig. 9. (a) Simulated BPF output signals with 0.85-GHz input when the BPF mode switches from 0.8 to 2.4 GHz then back to 0.8 GHz. (b) Zoom-in picture of the output signal and band switch signal during the BPF mode switching, indicating the BPF channel settling time is around 11 ns.

the BPF. When the BPF is set in 850-MHz filter mode, the BPF outputs the corresponding signals in a large output swing as the purple curve (in online version) in Fig. 9(a). When the BPF is set in 2.4-GHz filter mode, the 850-MHz input signals are filtered out and significantly attenuated. When the BPF transitions from 800- to 2.4-GHz mode or vice versa, the output signals need time to settle, which directly determines the channel switching time. Fig. 9 shows the simulation results that suggest the BPF channel switching time can be as short as 11 ns to settle within 5% of the final outputs, where the BPF is in the 0.8-GHz mode when the band is equal to 0 and in the 2.4-GHz mode when the band is equal to 1.

IV. Measurement Results

We have designed and fabricated fifth- and third-order programmable BPFs in HRL InP/Si BiCMOS technology with an HRL 250-nm InP DHBT and IBM 90-nm 1-poly 8-metal CMOS technology. The fifth-order BPF test chip occupies 0.6×0.25 mm^2 and 1.5×1.02 mm^2 without and with pads, respectively. Fig. 10 presents the fabricated die photograph. The BPF draws 106/121-mA current from a 3.3-V power supply for the 0.8/2.2-GHz bands. A 6-GHz network analyzer is used to characterize the filtering function. Two RF signal generators, e.g., Agilent E4438C, and HP spectrum analyzer 8653E, are used to characterize the BPF's linearity performance. A noise source NC346KA from Noise Com Inc. is used to characterize the BPF noise performance in the Y-factor method. Fig. 11 sketches the test setup.

We first characterized the BPF filtering function. Fig. 12 presents the measured S_{21}, which shows the fifth-order

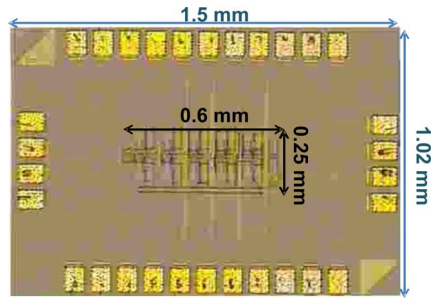


Fig. 10. Die photograph of the programmable active BPF.

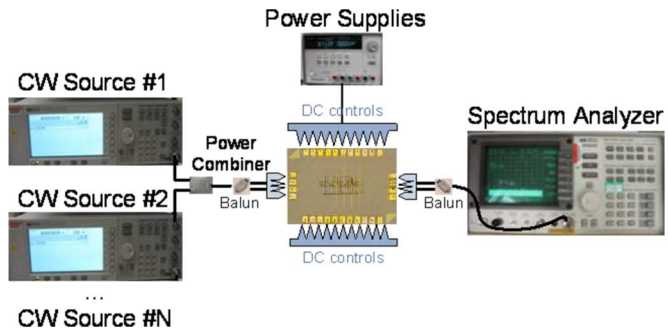


Fig. 11. Test setup for the BPF.

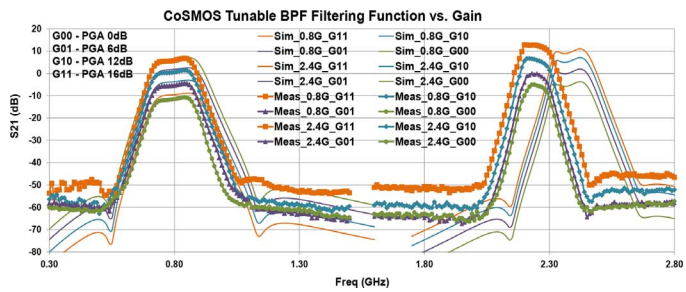
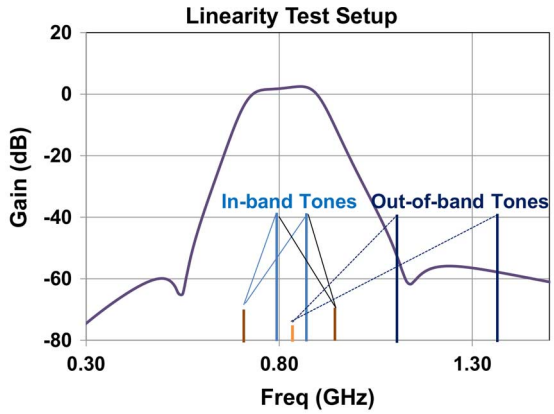


Fig. 12. Measured BPF filtering functions at 0.8- and 2.4-GHz modes with four gain settings.

BPF can be programmed from 0.8 to 2.2 GHz. The figure also compares the measured data with simulated ones. The measured BPF center frequency at 0.8 GHz agrees well with the simulation one, while the center frequency at the 2.4-GHz mode shifts low mainly because the post layout simulation did not take into account the parasitic capacitance of DHBT interconnects. A positive in-band (IB) gain is expected because the PGA gain negates the buffer loss. During measurements, we observe extra parasitics in the layout that have not been taken into account during simulation, which is manifested by the reduced BPF center frequency to 2.2 GHz at 2.4-GHz mode. We often characterize filter's linearity by measuring both IB and OOB linearities. To facilitate the characterization, we use a four-tone test to derive the IB and OOB linearities concurrently. Fig. 13 illustrates the test tone locations and gives the tone frequencies we used for both bands.

Figs. 14 and 15 shows the measured IB and OOB linearities of the programmble BPF test chip at both 0.8 and 2.2 GHz, which demonstrates 18.29/16.95- and $-1.12/-4.3$-dBm OOB and IB third-order input intercept points (IIP3s) for the two bands. The corresponding OIP3s are 22.69/21.25 and 2.51/0.43 dBm for



(a)

	In-band Two Tones (GHz)	Out-of-band Two Tones (GHz)
0.8 GHz	0.78	1.1
	0.82	1.4
2.2 GHz	2.2	2.52
	2.24	2.82

(b)

Fig. 13. (a) Four-tone test to characterize the filter's IB and OOB linearity at 0.8 GHz. (b) Tone frequencies used to test the BPF.

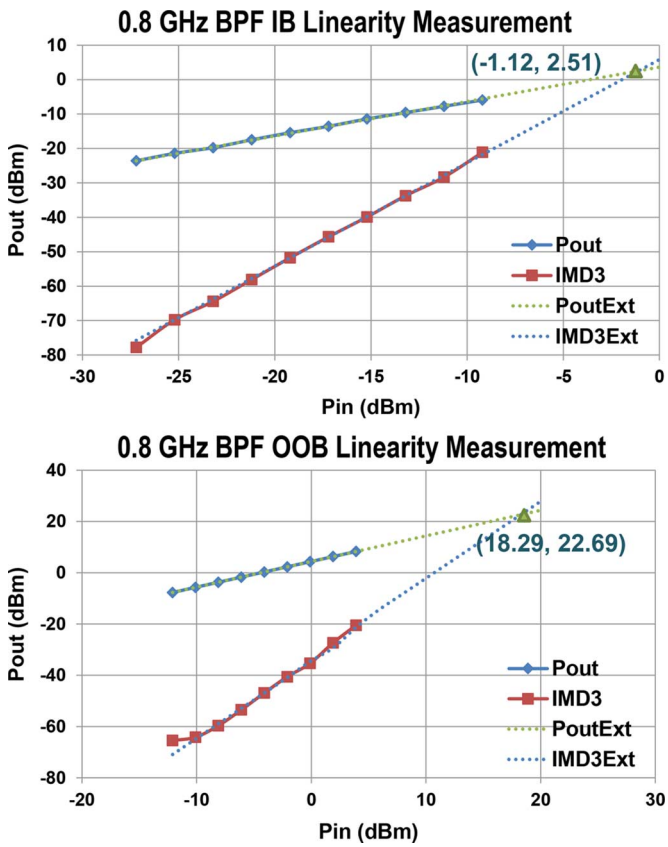


Fig. 14. Measured IB linearity and OOB linearity of the BPF at 0.8-GHz bands with output power Pout and third-order intermodulation distortion (IMD3).

OOB and IB at the two bands. The measured IB output 1-dB (OP1dB) intercept points are $-7.03/-9.34$ dBm at 0.8/2.2-GHz

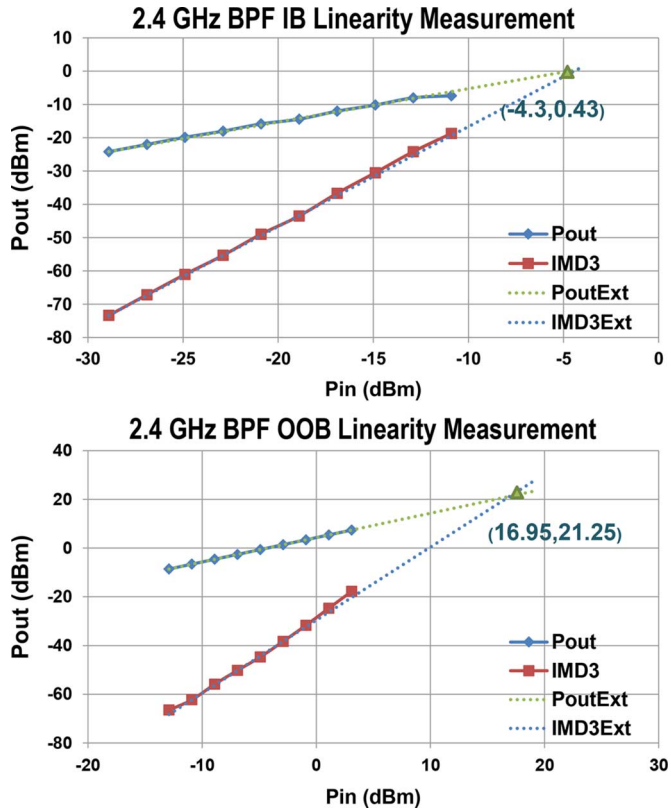


Fig. 15. Measured IB linearity and OOB linearity of the BPF at 2.2-GHz bands.

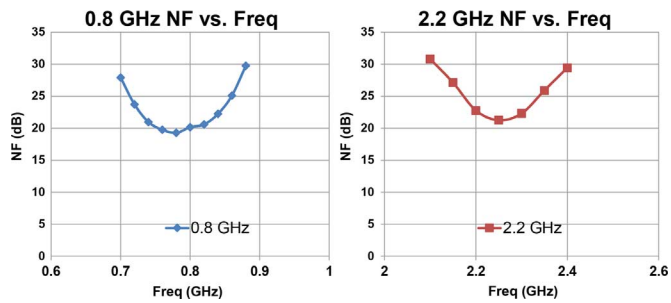


Fig. 16. Measured BPF NF at 0.8- and 2.4-GHz bands.

bands with the 14-dB loss at the output. The measured NFs are 19.26/21.24 dB at the center frequency for 0.8/2.2-GHz bands, respectively, as shown in Fig. 16, which are consistent with simulations. The high NF is mainly due to high noise contributions from resistors and transistors of the active *RC* implementation, which is insufficient for receiver applications. However, it can meet power DAC application requirements with an around 3-octave frequency tuning range. By configuring the switchable resistors and capacitors with a finer step, the active BPF can potentially cover 0.8–2.2-GHz band in a small frequency resolution, e.g., 100 MHz. Compared with other BPFs, this BPF has a wider tuning range with better OOB rejection. Its linearities are also better than other active implementations owing to the closed-loop realization. Table I summarizes its performances.

V. Excellent Test Vehicle

HRL has also utilized the designed third-order BPF to evaluate the heterogeneous integration technology yield during

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	ref [14]	ref [15]	ref [16]	ref [18]	*This work (BPF Test Chip)*	*This work(BPF Core)*
Type	PCB+CMOS varactors	MEMs	Active IND	G_m-C	*Active RC*	*Active RC*
Center Frequency (GHz)	0.68~1.011	0.602~1.011	2.14	0.048-0.78	*0.8/2.4*	*0.8/2.4*
Order of filter	2	3	3	8	*5*	*5*
BW (MHz)	60~120	78~145	60	15-60	*150*	*150*
Gain (dB)	-1.5 ~ -1.1	-3.6 ~ -3	0	4.7	*0/6/12/16*	*0*
Rejection (dB)	N/A	~30 dB	N/A	39	*>55*	*>55*
IIP3 (In-band) (dBm)	13	20	-4.9	N/A	*-1.12/-4.3 @ 16 dB*	*14.68/10.9*
IIP3 (out-of-band) (dBm)	N/A	N/A	N/A	3.8	*18.29/16.95 @ 16 dB*	*34.09/32.15*
NF (dB)	N/A	N/A	19	24	*19.26/21.24*	*N/A*
Core Active Area (mm^2)	900	165	3.51	N/A	*0.15*	*0.1*
Current Cons. (mA)	N/A	N/A	7	30	*106/121*	*76/87*

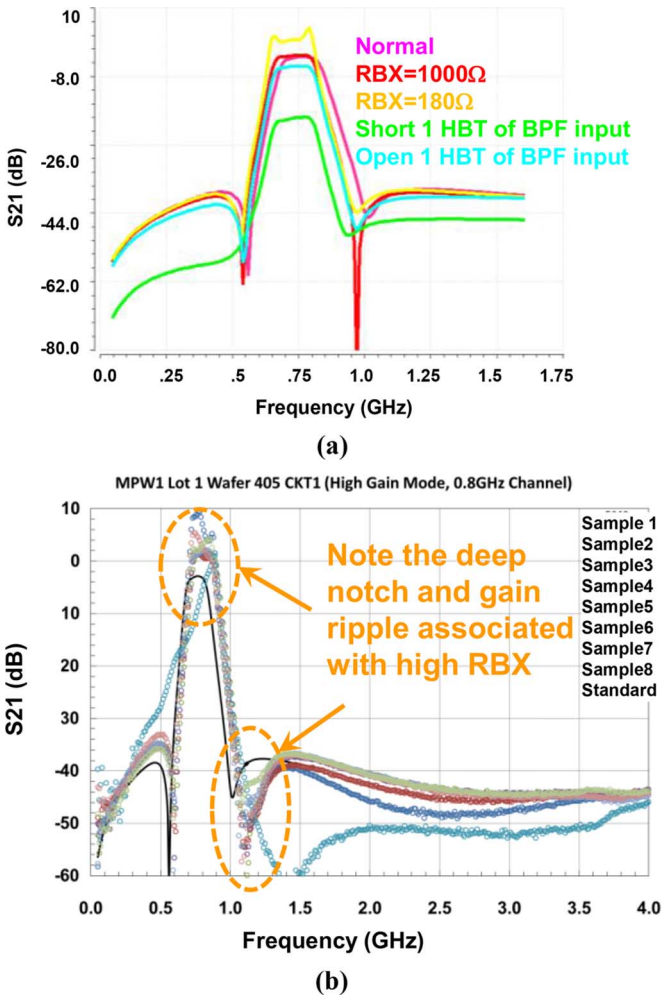


Fig. 17. (a) Simulated third-order BPF filtering functions with different technology failure assumptions. (b) Measured third BPF filtering functions at 0.8 GHz during technology development.

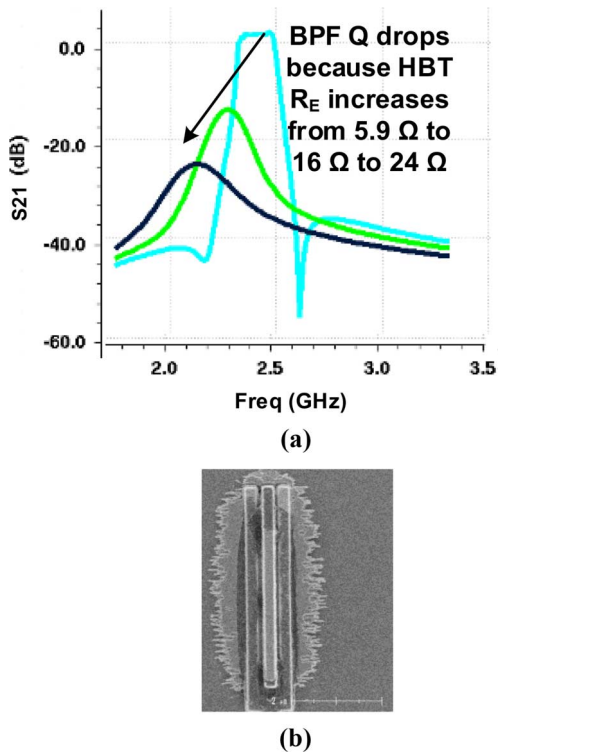


Fig. 18. (a) Simulated third-order 2.4-GHz BPF filtering functions with low-Q biquad due to large emitter resistance. (b) SEM image of one transistor suggests over-etching of the emitter connection introducing large emitter resistance.

development and assist the failure diagnosis. Compared with a traditional ring oscillator [24] that mainly tests the device speed, the BPF provides more information to diagnose the technology problems of the process. For instance, simulation results show a large base resistor distorts the filtering function by deepening the filter OOB notch and narrowing the passband. An electrical short of one input HBT of the op-amp due to interconnect process failure induces significant loss of the filter. Fig. 17(a) summarizes the simulated filtering functions at 0.8 GHz under several technology failures we have met during the technology development. Fig. 17(b) compares a normal filtering function with several measured filtering functions at 0.8 GHz with high base resistance, which agrees well with the simulations.

At high frequencies, BPFs often suffer from a low gain op-amp, which effectively reduces the biquad Q and corrupts the filtering function. Fig. 18(a) shows simulation results proving that the filtering function has been degraded by a low-Q biquad associated with a low op-amp gain at 2.2 GHz, which

is introduced by excessive emitter connection resistance of InP HBT. We have found one malfunction BPF and successfully identified the root cause of the malfunction BPF during technology development, which was introduced by a large emitter resistance due to over-etching, as shown in Fig. 18(b). During the technology development, the BPF characterization results have assisted the technology failure diagnosis and helped us to improve the technology yield.

VI. Conclusion

A fifth-order programmable BPF with four gain options, operating from 0.8 to 2.2 GHz for SDR applications, has been designed to demonstrate HRL InP/Si BiCMOS technology. Measurements of the BPF suggest proper function and good performance. It indicates that the InP/Si BiCMOS technology provides a potential integration platform to leverage good features of different technologies and delivers the capabilities that cannot be achieved by a single technology. Additionally, a third-order programmble BPF has been successfully used to diagnose several technology failures during our development and serves as a technology yield vehicle.

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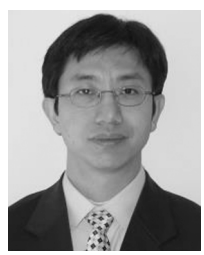

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