

„2nd Generation” SiC Schottky diodes: A new benchmark in SiC device ruggedness.

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Abstract: A new commercially available SiC Diode is reported and key features like widely improved surge current capability and avalanche ruggedness are described and related to the merged pn/Schottky device structure. The clearly positive temperature coefficient of the avalanche allows high avalanche power dissipation in the range of 20W/mm² even in the frame of long term (1000h) testing. Additionally the device has the same excellent dynamic properties as already known from pure SiC Schottky diodes. The dV/dt ruggedness of the device was also proven with a long term test (3.6E11 cycles with > 90V/ns). No noticeable difference in switching losses occur when the device is switched off from nominal current at room temperature or from 10x nominal current at 150°C. The long term stability of the device under bipolar operation at high current densities (> 2kA/cm²) at the p-areas was proven over a stress time of 1h.

I. INTRODUCTION

SiC Schottky diodes are available in the market since 2001 and show unrivalled performance concerning virtually lossless switching (besides capacitive switching losses). This property makes them especially attractive for applications like SMPS (Switch Mode Power Supply) Power Factor Correction under CCM (Continuous Current Mode) operation, by allowing switching frequencies in the >100kHz range without efficiency trade off [1].

However, SiC devices are still very expensive compared to their Si counterparts mainly due to the costly base material. At the same time the today available SiC Schottky diodes show the typical characteristic of any majority carrier device: a strong positive temperature coefficient of the device resistivity. As a consequence, surge current stress can lead to thermal runaway and device destruction due to the strong coupling between power dissipation and resistivity increase [2].

With respect to the application this means, that the current rating of the SiC diode mainly has to be chosen according to the surge current requirements (e.g. start up or AC drop out conditions), what usually leads to a large over-dimensioning for regular operation. Together with the cost issue mentioned above, this makes the SiC diode solution less suited for cost sensitive applications.

In this paper we want to introduce an alternative device concept, which integrates the very attractive switching behaviour with a strong surge current capability. The device is a combination of a pn-diode and a Schottky diode (MPS: Merged pn Schottky). This is not a new approach, but so far in the medium voltage range (< 1800V) only employed to

reduce the field stress at the Schottky interface and therefore allowing higher blocking voltage at low thermionic field emission and tunnelling leakage current in SiC [3].

Furthermore we also focused on rugged avalanche capability when designing the pn cell structure of the device, because this addresses another important drawback of today's SiC Schottky diode technology: Due to the lack of a stable avalanche a large safety margin between rated voltage and breakdown voltage was necessary in the past, not allowing to make full use of the superior breakdown field strength of SiC.

II. DEVICE STRUCTURE AND STATIC PROPERTIES

In Fig. 1 the structure of a SiC Schottky diode is compared with the merged pn-Schottky concept. We optimized the p-areas with respect to emitter efficiency and conductivity, so that they can serve as a kind of surge current bypass in the case of forward voltage exceeding ~4V. This superior forward behaviour is shown in Fig. 2 (top) in comparison to a standard SiC Schottky diode. In the minority carrier injection mode (high current density), the remaining drift layer resistivity can be neglected compared to the substrate resistivity, what leads to a nearly temperature independent forward characteristic as also shown in Fig. 2 (bottom).

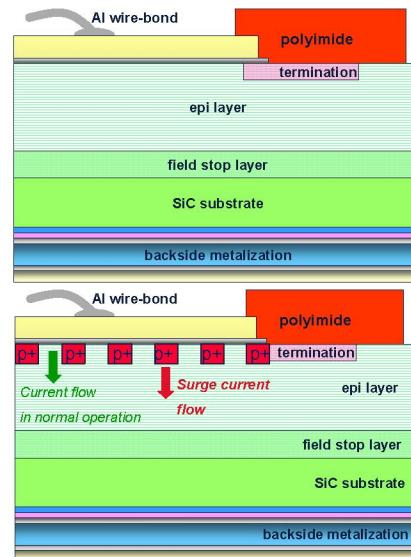


Fig. 1.
 Top:
 Schematic cross section
 of conventional SiC
 Schottky diode

Bottom: 2nd Generation
 SiC diode with merged p-
 doped islands (MPS
 diode).
 The termination area is a
 p⁻ implanted ring with a
 doping concentration
 optimized for surface
 field reduction

With the chosen design (Schottky vs pn area trade off, cell structure geometry) the MPS forward behaviour allows a 2-3 times higher surge current density rating than a pure Schottky diode, leading to a I_{FSM} value (surge non-repetitive forward

current, sine halfwave, 10 ms) of ~8-9x rated nominal current. Accordingly the I^t rating can be increased by roughly a factor of 5. In case of the 10 μ s surge current rating (I_{Fmax}) the new device offers stability beyond 35 x rated current.

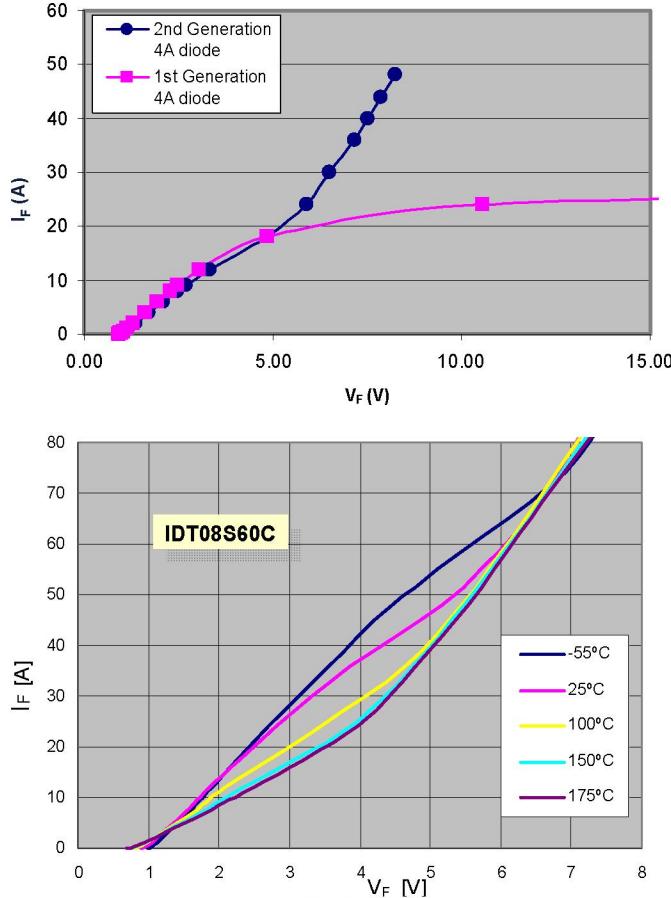


Fig. 2.
Top: Comparison between first (Standard Schottky) and second generation (MPS) SiC diodes at room temperature.

Bottom: Current-voltage characteristics for different temperatures of an 8A/600V MPS SiC diode. The various temperature curves all merge in one straight line corresponding to the nearly temperature independent substrate resistivity.

All measurement performed with 400 μ s pulses.

To investigate, whether the stacking fault related bipolar V_F -drift issue well known for high voltage SiC pn diodes [4] may also degrade the surge current capability of the MPS diode after a longer accumulated operation time under surge current condition we carried out the following experiment:

Wafers with the same pn-Schottky cell structure as for our new product have been processed with a thick oxide layer covering the Schottky areas but having openings at the position of the p^+ -wells. With this structure high current densities can be achieved in a pure bipolar operation mode without thermal management problems. A high current density stress test was carried out on 36 devices (soldered on DCB) with the following parameters and results:

- Current density 2.3 kA/cm² /1h → no noticeable V_F drift ($\Delta V_F < 20$ mV @ 2.3 kA/cm²)

- Current density 4.6 kA/cm² /1h: no noticeable V_F drift on chip level again. Metal surfaces already showed clear signs of oxidation due to the high stationary power dissipation of ~40-50kW/cm².

Typically the V_F degradation for high voltage pn diodes (> 3kV blocking capability) can be easily revealed within a 30min forward stress test with 50 A/cm² [5]. The superior behaviour of our 600V MPS diodes is explainable by the quite small thickness of the drift layer used in these 600V diodes (only ~4 μ m) compared to high voltage (> 3 kV) SiC pn diodes. The volume available for stacking fault formation and growth is therefore pretty small, moreover due to the cellular structure with p -wells of only some μ m lateral extension the available volume for stacking fault growth is also laterally limited.

The surge current stress test time is equivalent to 3.6*10⁵ cycles with 10 ms duration as specified in the datasheet as I_{FSM} (current density at $I_{FSM} \sim 4$ kA/cm²). This is an excellent stability with respect to typical application situations and also in comparison to the drift behaviour of high voltage SiC pn diodes [4; 5].

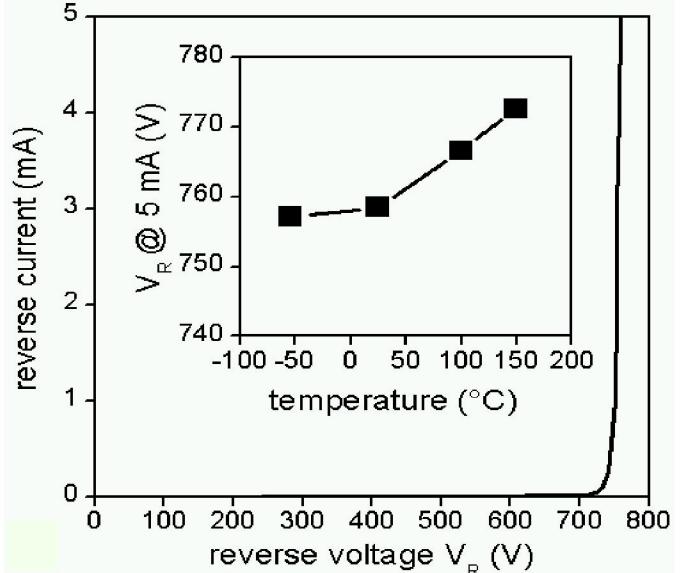
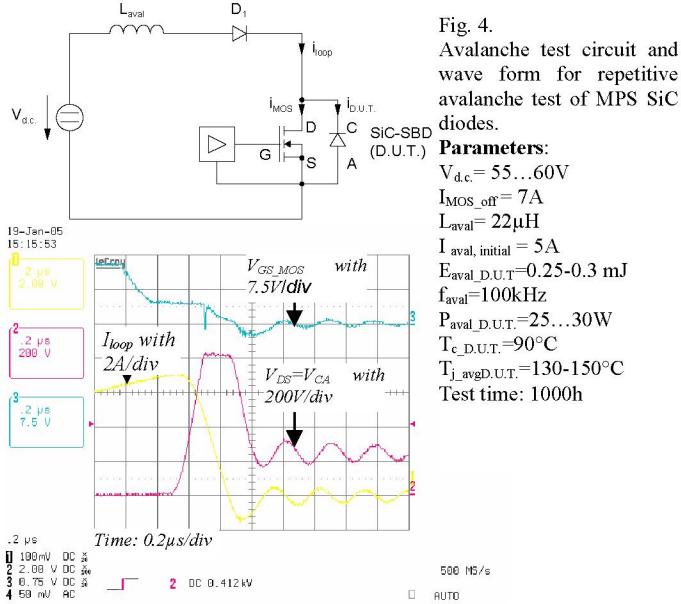


Fig. 3.
Typical reverse current-voltage relation of a 2nd Generation SiC diode. The onset of the avalanche is at about 750V. The inset shows the typical temperature dependence of the breakdown voltage at a reverse current of 5 mA.

In addition to the surge current capability also the reverse behaviour of the diodes is significantly improved by the MPS structure. Besides the field reduction at the Schottky interface due to the space charge region of the p^+ -wells a stable avalanche is enabled by the fact that the highest electric field appears at the edges of the periodic p^+ -wells. This is achieved by a larger implantation depth of the p^+ compared to the p -guard ring area. Thereby it is the first avalanche rugged SiC device available in the market.

Due to unavoidable variations of epi-layer doping and thickness the avalanche starts locally on one cell of the device,

but due to the positive temperature coefficient of the avalanche voltage (Fig. 3) it spreads out over the whole device area when increasing the avalanche energy. This leads to a quite homogenous distribution of the avalanche energy dissipation over the whole active area allowing the device to withstand quite high reverse energy spikes. To prove the stability of the device under such conditions we carried out a repetitive avalanche testing of 2 lots with 40 devices each (8A current rating, active area 1.95 mm^2). During this test an average power of 30W was dissipated in the chip solely in avalanche mode for 1000h (for test details see Fig. 4). No degradation or parameter drift could be detected for all devices under test.



III. PROPERTIES UNDER DYNAMIC OPERATION

The properties of the new diodes have been investigated both under high dI/dt and dV/dt stress conditions.

Compared to a pure SiC Schottky diode the new device can easily be operated at pulsed high surge current conditions. For a PFC like application this means that it might be switched off from very high current densities, i.e. operating in the bipolar regime (minority carrier injection by the p-wells). An obvious question in this case is, whether the device will experience a dynamic avalanche as known from Si pn diodes and whether a noticeable Q_{tr}/t_{tr} will show up when the device is switched off from those high current densities. A clear answer to this question is given in Fig. 5, where the switching wave form of a 5A diode is shown for room temperature & nominal current (pure unipolar operation) and at $150^\circ C$ and 10x rated current (bipolar operation).

The switching waveform for both conditions is identical within the test accuracy. The diode only shows a very small displacement current peak in reverse direction, which is related to the junction capacitance of the device. The related Q_C of this 5A diode is as small as 12 nC and completely independent of I_F , T , dI/dt . This behaviour is true even under bipolar operation due to the short minority carrier lifetime (\ll

$1 \mu s$) and the thin drift layer required ($\sim 4 \mu m$). For the same reason a dynamic avalanche can not occur.

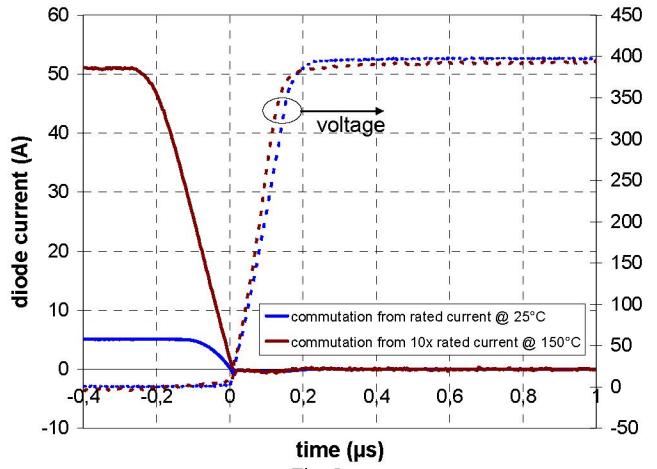


Fig. 5. Switching wave form comparison of the MPS diode: normal operation vs. surge current switching at elevated temperature.

In the past there have been some concerns about reduced blocking capability of SiC diodes under high dV/dt -stress [6]. The new Infineon SiC diodes analyzed in this study are especially designed for a fast response to external dV/dt stress. A key issue in this concern is an optimization of post implant annealing process of the implanted acceptors. By that means not only the emitter efficiency responsible for the surge current capability but also the hole mobility in the bipolar edge termination area was improved significantly. In case of large voltage turn off gradients the displacement current necessary to form the space charge region in the edge termination area can therefore instantaneously follow the external dV/dt , reducing the amount of power dissipation in the edge termination area and avoiding dynamic lateral field crowding. This was again proven in a long term stability study. 10 devices have been stressed with voltage gradients of $90\ldots95V/\text{ns}$ over $3.6E11$ cycles (1000h @ 100kHz) showing no electrical or physical degradation (details of this test are given in Fig. 6).

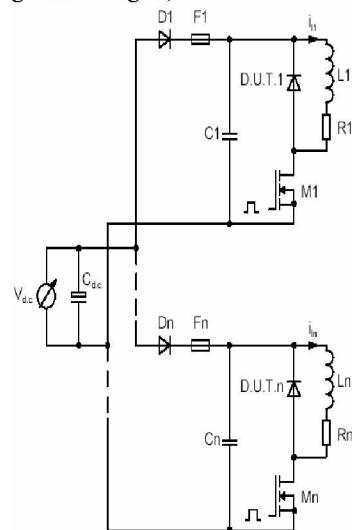


Fig. 6a:
High turn off voltage transient test circuit topology (10 devices to be stressed in parallel)
Device under Test: 16A SiC MPS Diode (IDT16S60C)

Circuit parameters:
 $V_{dc} = 400V$;
 $M1 = SPP07N60C3$ ($V_{gs} = 13V/0V$); $I_L = 1A$;
duty cycle = 0.5;
 $R1 = 200\Omega$ (200W);
 $f = 100\text{kHz}$;

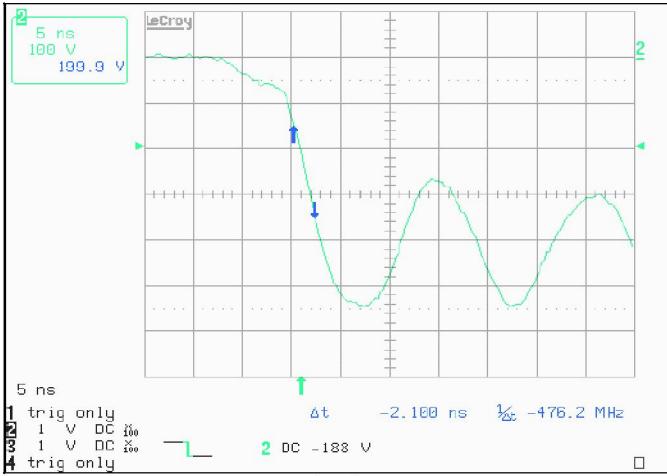


Fig. 6b.
High turn off voltage transient test wave form
($dV/dt=95V/ns$; 100V/div; 5ns/div)

IV. APPLICATION RESULTS

The new diode has been used in a state of the art power supply as PFC boost diode (130 kHz, wide input range, 300W output power, CoolMOS® IPP60R199CP as PFC switch). In this application other fast diodes including our 1st Gen SiC Schottky diodes have been used for comparison (see Fig. 7).

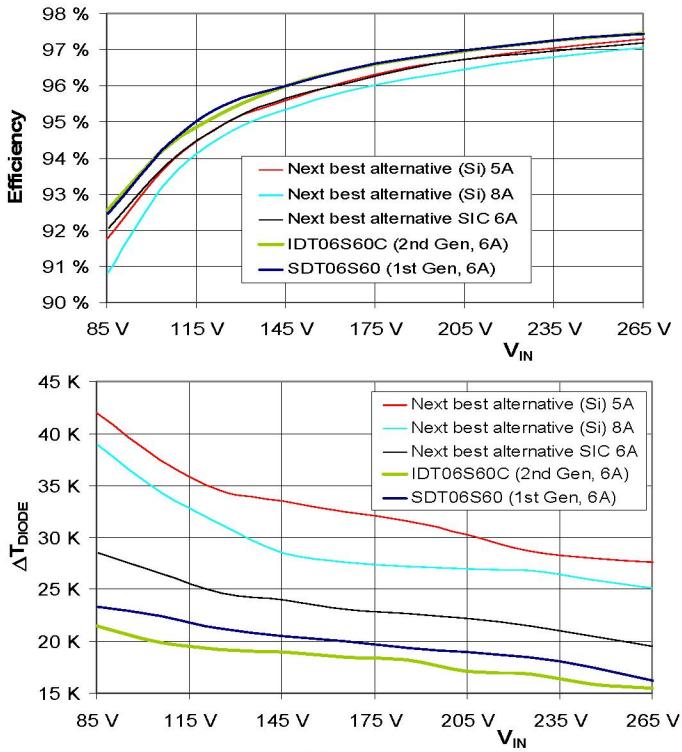


Fig. 7.

PFC efficiency (top) and diode case temperature (bottom) for various PFC diodes used ($T_{\text{ambient}} = 22^\circ\text{C}$, full load) in a 300 W PFC demo board. The Si diodes used for comparison are Tandem pn diodes.

It is clearly visible from this comparison, that the SiC diodes are advantageous with respect to both efficiency and

temperature (directly translate in cooling requirements/heat sink size). When comparing 1st Gen with 2nd Gen SiC Diodes from Infineon no difference is visible which cannot be explained by individual parameter variations of the devices. In Fig. 7 only 6A SiC diodes have been compared, but also when using a 4A 2nd Gen diode in this 300W application the efficiency penalty is less than 0.2% and the additional increase of the case temperature is smaller than 5K.

On the other hand, the cost saving when using a 4A diode instead of a 6A diode is quite significant due to the high cost/A for SiC devices compared to Si pn diodes (due to large SiC wafer costs). This move to lower current rating is now possible due to the widely improved surge current capability as explained in chapter I.

Additionally the use of a SiC diode has a very strong impact on the T_c of the PFC transistor. Under worst case conditions (low input voltage) this transistor T_c is 40K-60K lower in combination with a SiC boost diode and independent of the current rating of this SiC diode.

V. DISCUSSION

The new SiC diode presented in this paper was extensively tested under severe stress conditions like high current density (4.6 kA/cm²), repetitive avalanche with an average avalanche power dissipation of 1.5 kW/cm², repetitive dV/dt-stress with > 90V/ns and switching off from 5kA/cm² @ 150°C. None of those stress conditions, as well as the standard reliability tests, resulted in a device degradation. Based on these results the new SiC diode is a benchmark in SiC device ruggedness addressing potential application failure modes like inductive overvoltage spikes and excessive surge current stress due to positive feedback between resistivity and power dissipation.

Therefore circuit designers get additional safety margins on device level, which significantly reduce failure risks in case of unforeseen operation conditions. Smaller and cheaper devices can be used compared to 1st Gen SiC Schottky devices, making the use of this nearly ideal diode being virtually free of switching losses very attractive for all 600V applications where switching speed, efficiency and power density are key features.

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