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Deliverable / Lab 7 - ENG PHYS 2E04

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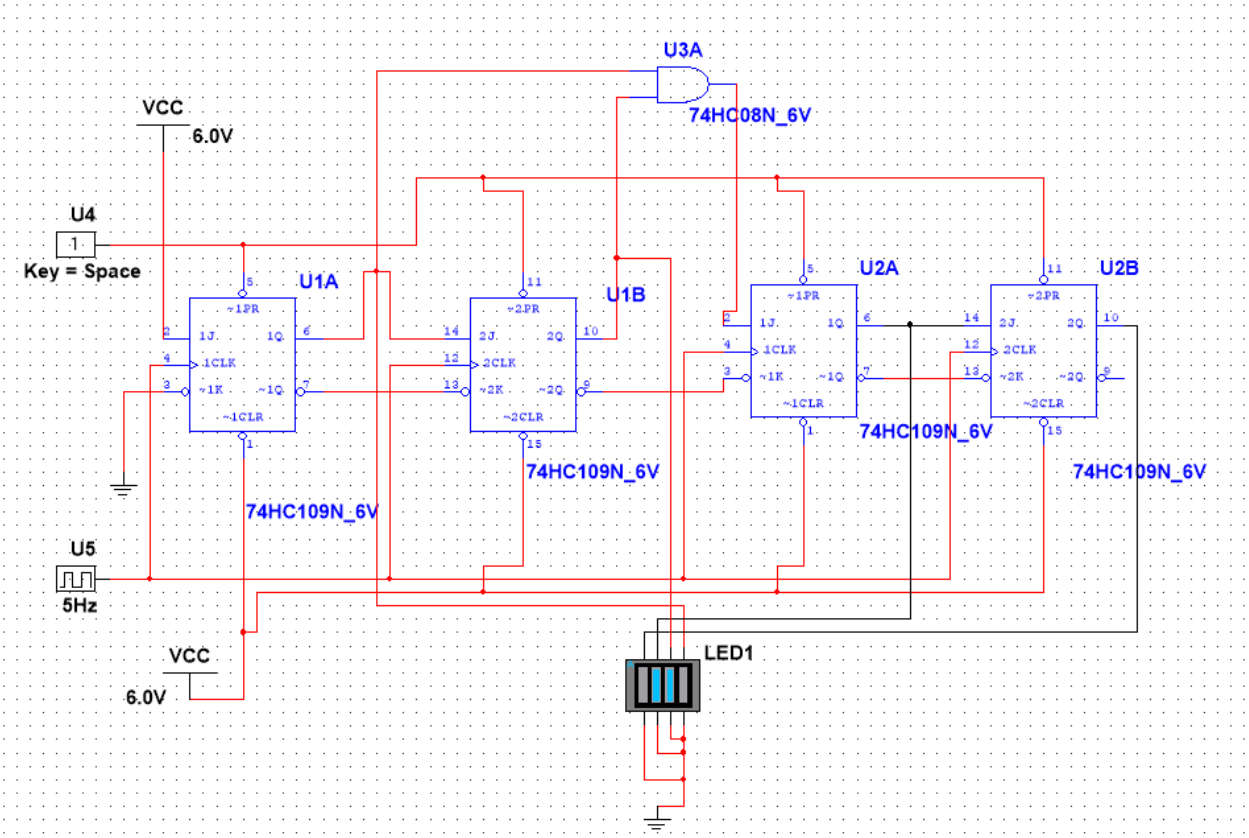

Fig 7.1

- Step 1: Draw the timing diagram and state diagram for the circuit in Figure 1 for varying Q values on the outputs of the four flip flops.

- Step 2: Simulate the circuit in Figure 1 using Multisim and confirm the functionality of the circuit.

- Step 3: Build the circuit in Figure 1 on the breadboard and confirm the functionality is correct.

- Step 4: Vary the clock frequency and see how it affects the output. At what frequency does the circuit stop functioning correctly and why?

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Analytical Method

- The circuit shown in Figure 7.1, consists of 4 JK flip-flops connected and one AND gate. It also consists of a clock that is responsible for timing the flip-flops and a LED that allows the output to be seen.

Flip-Flop 1:

- J1 = 1.
  K1 = 0, therefore, !K1 = 1. As both J1 and! K1 are equal to 1 the flip flop is in **toggle mode** meaning the Q1 would be switching between 1 and 0.

Flip-Flop 2:

- J2 = Q1
  !K2 = !!Q1 which means that J2 and !K2 are both equal to Q1.

- This means that the Flip-Flop inputs are both **toggling**. The latch only works when the clock is high due to the rising clock edge. Therefore, when the values of both J2 and! K2 are high, the value of the output Q2 is high and when the value of both the inputs are low the output stays the same (set), and when the value of both outputs is high again the output toggles to low.

Flip-Flop 3:

- The input J3 is obtained by AND of the outputs Q1 and Q2 and therefore can be written as the following in Boolean algebra:

$$J_3 = Q_1 * Q_2$$

- !K3 = !!Q2 = Q2, this shows that the input K3 is just equal to the output Q2

Flip-Flop 4:

- The input J4 is obtained by the output of the third flip-flop which is Q3.
- Therefore, J4 = Q3.
  The input, !K4 = !!Q3 = Q3. Therefore, both inputs are equal to Q3

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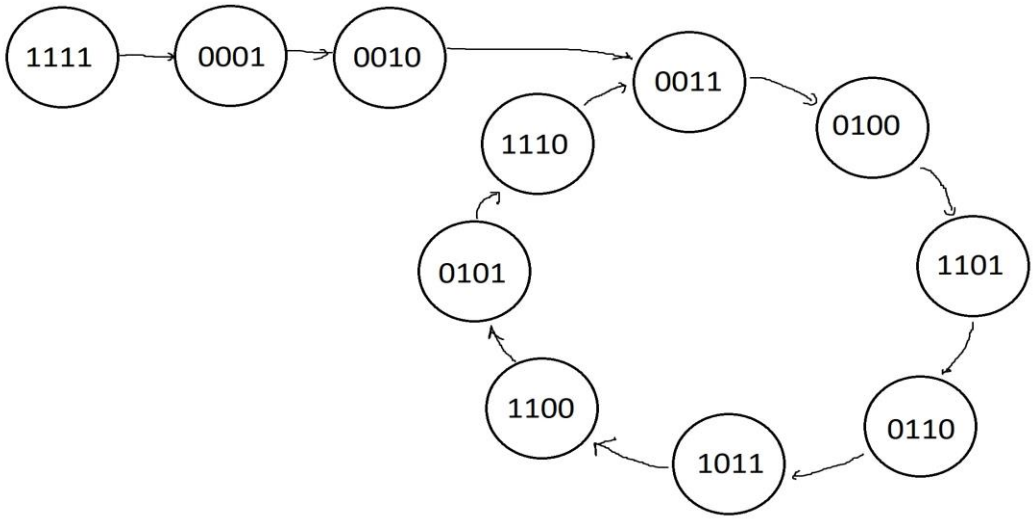
State-transition table & State-transition diagram

Q4 output is obtained and shown below. The finite state machine has **11 possible states and loops between 8 of those states.**

Q4 (initial)	Q3 (initial)	Q2 (initial)	Q1 (initial)	J2	K2	J3	K3	J4	K4	Q4	Q3	Q2	Q1
1	1	1	1	1	0	1	0	1	0	0	0	0	1
0	0	0	1	1	0	0	1	0	1	0	0	1	0
0	0	1	0	0	1	0	0	0	1	0	0	1	1
0	0	1	1	1	0	1	0	0	1	0	1	0	0
0	1	0	0	0	1	0	1	1	0	1	1	0	1
1	1	0	1	1	0	0	1	1	0	0	1	1	0
0	1	1	0	0	1	0	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0	0	1	1	1	0	0
1	1	0	0	0	1	0	1	1	0	0	1	0	1
0	1	0	1	1	0	0	1	1	0	1	1	1	0
1	1	1	0	0	1	0	0	1	0	0	0	1	1



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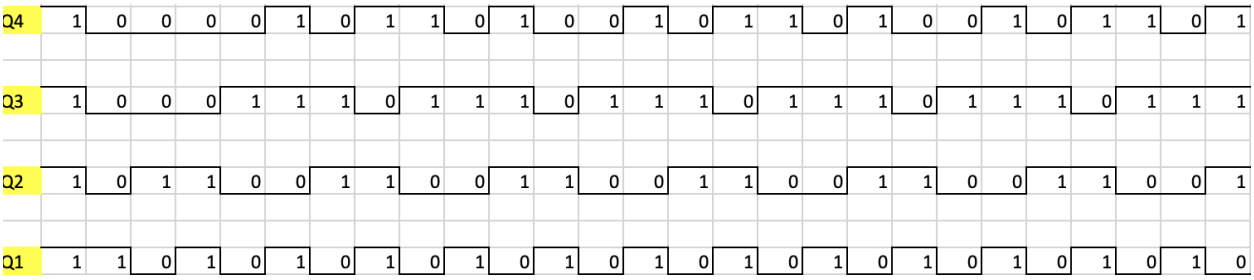
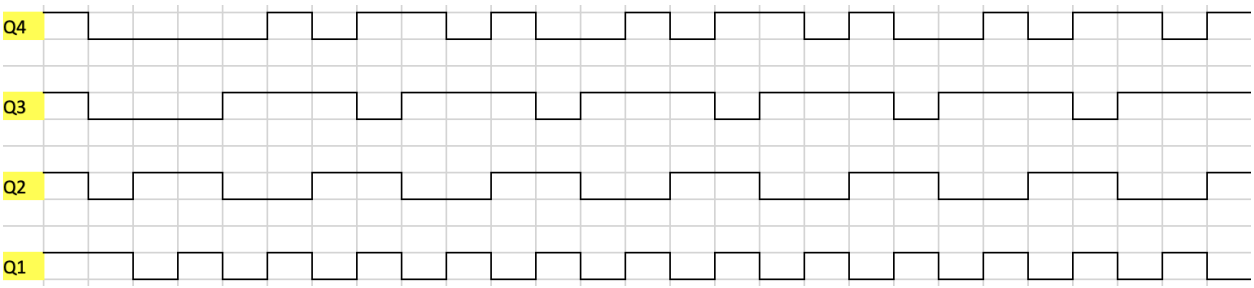
Timing Diagrams

The timing diagrams can be acquired for each of the outputs based on the transition table shown above:



- The above figure shows the timing diagrams with the 0 and 1 values and the below figure shows it without the 0 and 1 values to understand the way the values change for each output as time goes on.



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Multisim Method

The circuit is set up in Multisim as shown above in Fig 7.1, the circuit consists of 4 74HC109N JK Flip-flops. Each Flip-flop has two individual inputs and a third for the clock; the clock input is provided by a digital clock which is common for all four flip-flops. The inputs for each flip flop are varied and are directly or indirectly dependent on the output of the previous JK flip-flop. The third input J is given by a combination of AND of the inputs Q1 and Q2 and shown above, the output for the circuit are 4 LEDs which are connected to each of the outputs of the Flip-flop with Q4 being the left most and the right most being Q1.

The demonstration of the circuit can be seen in the video below:

https://drive.google.com/file/d/1J0Ffx22-EwmiXjsc7Qi7zbQXa_w48Avw/view?usp=sharing

The states of the FSM can be acquired by seeing the LED lights up and by seeing which led light up and this gives us the following transition table.

Q4	Q3	Q2	Q1
1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
1	1	0	1
0	1	1	0
1	0	1	1
1	1	0	0
0	1	0	1
1	1	1	0
0	0	1	1

The finite state machine transition table is the same as the one obtained using the analytical method. This can therefore lead to the conclusion that the calculations done using the analytical method is correct.

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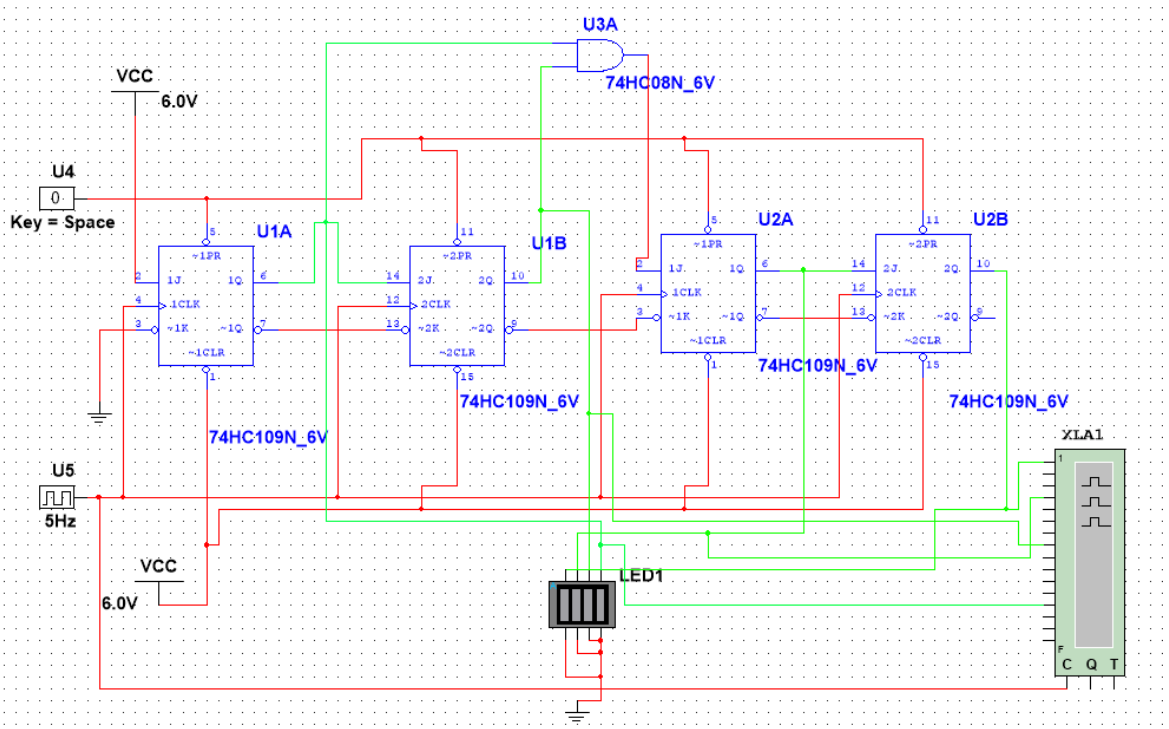
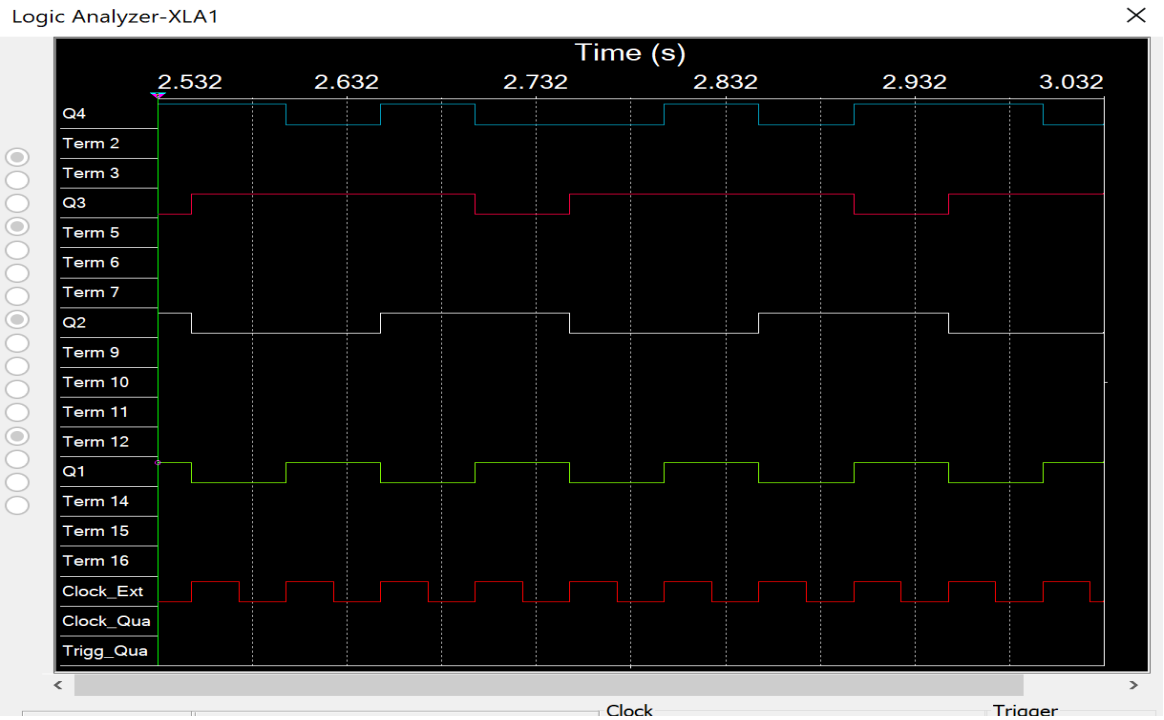
Furthermore, the timing diagrams obtained in the analytical method can also be compared to the timing diagrams obtained using the logic analyzer function in Multisim.



The logic analyzer is set up as shown above. The graphs obtained from the logic analyzer are shown below:



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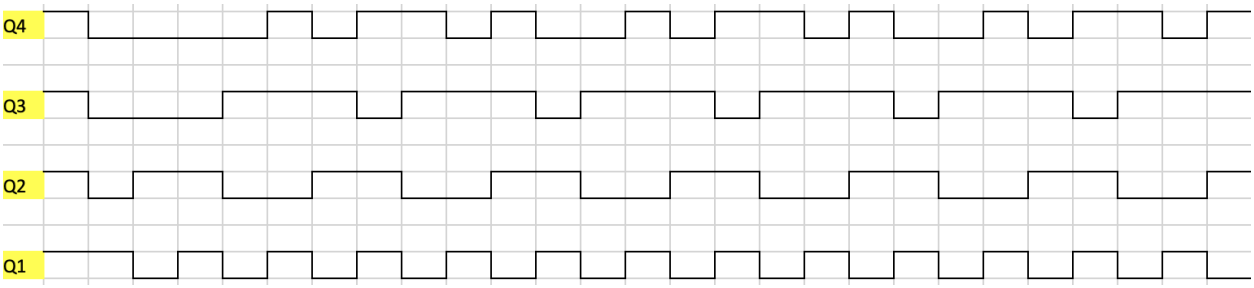
The timing diagram from the analytical part is shown below:



When comparing both timing diagrams, we can deduce that both the timing diagrams are identical to each other such as the timing diagram for Q1 has regular toggles between high and low, this can also be seen in the timing diagram obtained from Multisim.

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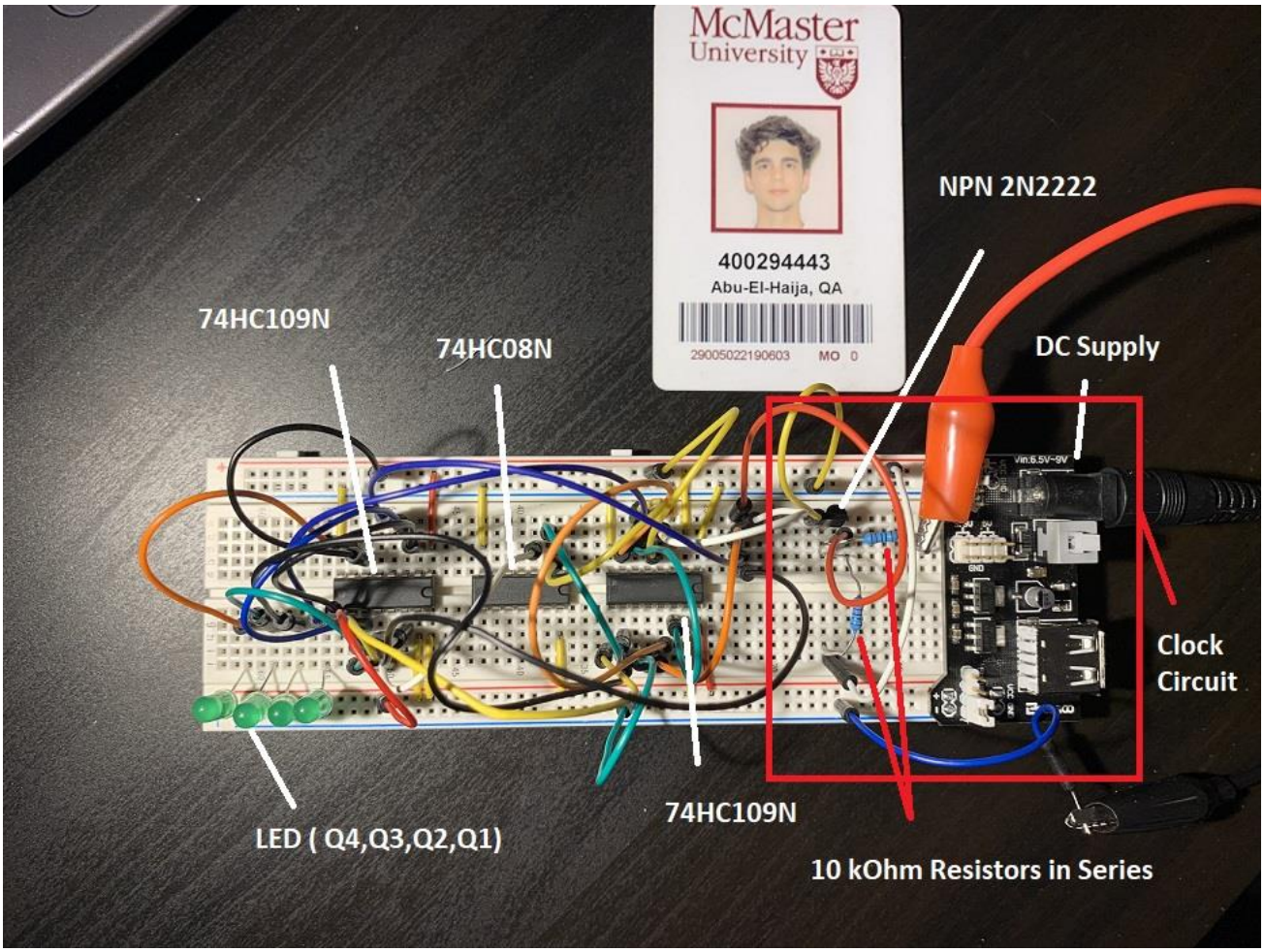
Experimental Method

The circuit was set up using the Take Home kit and the Hantek. The Soul-bay was used as the power supply. The Soul-bay power supply was required for powering up the IC. The 1 value for the presets and clears and for the value of J1. The Hantek circuit was used in the clock circuit to modify the signal. The clock circuit was set up using an NPN 2N2222 transistor which consists of three inputs. The first input (from the left) was connected to the ground, the second input was the input of the square wave of 1V from the Hantek which had a 10kohm resistor in series. The third input was the input of 5V from the Soul-bay into the transistor which gave the clock, which was used in the JK Flip-flops, a square wave with rising from 0 to 5V. The circuit was made up of three IC's, 2 74HC109 and 1 74HC08 (AND). The circuit was set up as shown below:



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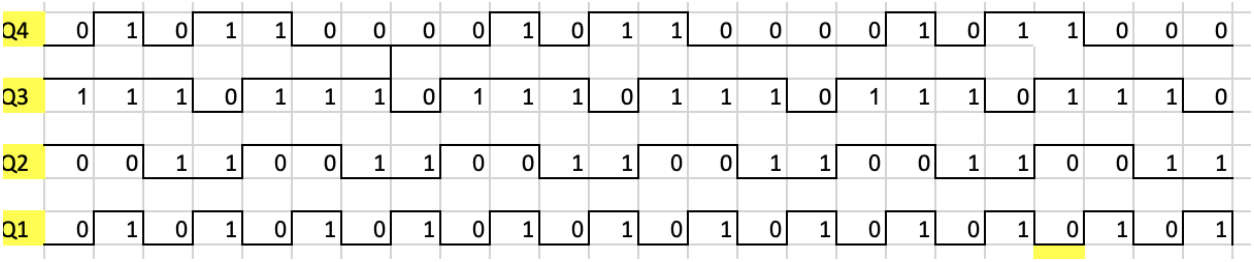
The demonstration of the circuit can be seen in the video below:

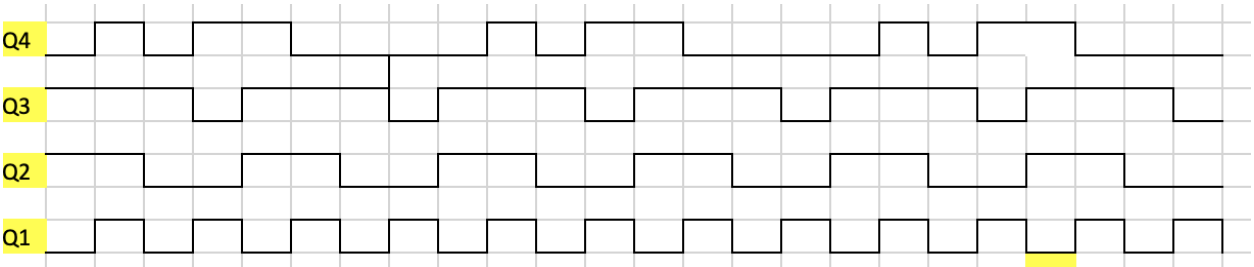
https://drive.google.com/file/d/1jjXzNbpcaus8AgTzb2v-_Ut3PTvhPu4S/view?usp=sharing

In the video above that the circuit starts from the 0000, and then follows a steady transition into 8 states which can be shown in the transition table below:

Q4	Q3	Q2	Q1
0	1	0	0
1	1	0	1
0	1	1	0
1	0	1	1
1	1	0	0
0	1	0	1
1	1	1	0
0	0	1	1
0	1	0	0

The transition table above can be used to create a timing diagram for each of the outputs and the following output is obtained:





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Discussion

The results from the three methods are compared and it is found that the result obtained from all three methods is similar but there are some differences in the experimental results. All three methods have a finite state machine which loops in 8 states which are

Q4	Q3	Q2	Q1
0	1	0	0
1	1	0	1
0	1	1	0
1	0	1	1
1	1	0	0
0	1	0	1
1	1	1	0
0	0	1	1

The difference is seen only in the experimental method where the finite state machine does not go through the initial state of 0001 but follows the above sequence which can be confirmed by seeing the Multisim simulation and the experimental video. This can also be compared by viewing the timing diagrams obtained from each of the methods. All are the same and follow the same pattern in terms of rising and falling. The analytical method was done by inspecting the inputs and by comparing it to the clock and understanding what states the finite state machine goes in using Boolean algebra laws for the and gate and the JK flip-flop truth table for the understanding each of the outputs was used to construct the transition table and the diagram of the finite state machine. The circuit was simulated in Multisim and the finite state was first set by setting all the presets to 0, to allow all outputs to be 1 and then was allowed to enter its states to make it easier as seen in the video shown. The experimental part was complex since it required creating a timing circuit using the 2N222 transistor and was integral since all the Flip-Flops were required. A total of 3 ICs were required. There were 2 for the flip-flops and one for the AND gate. The frequency of the square wave was changed to see what difference would occur, it was observed as the frequency of the square wave was increased, the states of the FSM would change faster which would cause the led to change much quicker. Furthermore, it was observed that at a very high frequency such as 1000Hz the LED seemed to not change state at all, this was because it was changing states so fast that it was difficult to understand which state it was in as all 4 LEDs seemed to be lit up.

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Reflection

This topic was very interesting as I learned about different types of latches that can be used which are the basics of memory such as the SR latch which can be made of NOR or NAND gates and only changes state under certain conditions and how it can hold its state. Furthermore, I got to learn about D latches, JK flip-flops, and T flip-flops and how to make a timing diagram for each of these components. The timing diagrams are useful for understanding how inputs change with time and how this affects the output. Moreover, I got to learn about rising edges which means that the latch only works when the clock signal goes from 0 to a +ve value. I also learned about finite state machines which are machines that are only able to change state if certain conditions are met and understood how to implement them in a practical aspect. There are various uses for latches such as D latches and JK flip flops. They are used in computing as the basics of storing data since they can keep their state until changed, they are also used in encoding binary numbers since they can have conditions.