UNIVERSITY OF WALES, ABERYSTWYTH
Department of Computer Science

CS25510 - COMPUTER HARDWARE
EXAMINATION REVISION QUESTIONS

The following questions are for revision purposes only, and serve to direct a student's study to relevant areas of the CS25510 syllabus. Some questions are indicative of the type of section question that may be found on an examination paper.

NOTE: Students are recommended to revise ALL the material covered during the CS25510 module lectures, as well as ALL the material that was covered during the hardware (NAND gate and 6802 microprocessor) and software (THR68HC11 Simulator) practicals.

1. What are the differences between an analogue and a digital system?
2. What is a digital waveform and what are their characteristics?
3. What are the differences between DIP, SOIC, PLCC, LCCC and Flat Pack IC packages?
4. What are the truth tables for the following gates: AND, NAND, OR, NOR, NOT, EX-OR and EX-NOR?
5. Explain the operation of the following logic devices: the Half Adder, a 4-bit comparator, a decimal to BCD encoder and a MUX.
6. What are the laws and theorems of Boolean algebra?
7. Draw the equivalent logic circuit for the following Boolean expression:
   $$(\neg ABC) + (A\neg B\neg C) + (\neg A\neg B\neg C) + (A\neg BC) + (ABC)$$
8. Simplify the previous Boolean expression and draw the resultant equivalent logic circuit. (Soln. $(BC) + (A\neg B) + (\neg B\neg C)$)
9. Why are NAND and NOR gates universally applicable?
10. How does an S-R latch operate and what applications are there for this device?
11. What are the differences between an S-R type, a D type and a J-K flip-flop?
12. For two input waveforms (J and K) to an edge-triggered J-K flip-flop, how would you determine the output (Q and NOTQ) waveforms?
13. How could you use a flip-flop for a) parallel data storage, b) frequency division and c) counting applications?
14. A Motorola 68HC11 microcontroller has a number of on-chip capabilities. What are they?
15. What modes does a 68HC11 possess and how do these differ?
16. What registers does a 68HC11's CPU possess, and how are they used during the fetch/ execute cycle?
17. What is a memory map and why is an address decoding circuit required when a 68HC11 is in expanded mode?
18. Four $1K \times 8$ bit external RAM chips are required to occupy address 0000 to 0FFF. Using a 74HC138 decoder, design a schematic diagram for the required address decoding circuit.
19. What is partial address decoding and how does it differ from full address decoding?
20. What 68HC11 assembly language instructions have been introduced during practicals and what operation does each instruction perform?