CS25410

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Objectives

- Introduction to an HDL
- Simple system descriptions
- Test Benches
- Design Approach
- Simulators
- Simulation

Design Units

- ***The Entity***
- Contains information on all inputs and outputs. This includes details on propagation delays and bus widths.
- But NO information on how the unit behaves

Example description

- Example a general purpose 2 input AND gate
  - entity AND is
  - generic (DELAY : time := 10ns)
  - port (A, B : in bit;
  - Y : out bit)
  - end AND
- Described the detail of all connections to the AND but not how the AND works

The Architecture

- Describes how the AND works
-
  - architecture BEHAVE of AND is
  - begin
  - Y <= A and B after DELAY;
  - end BEHAVE;

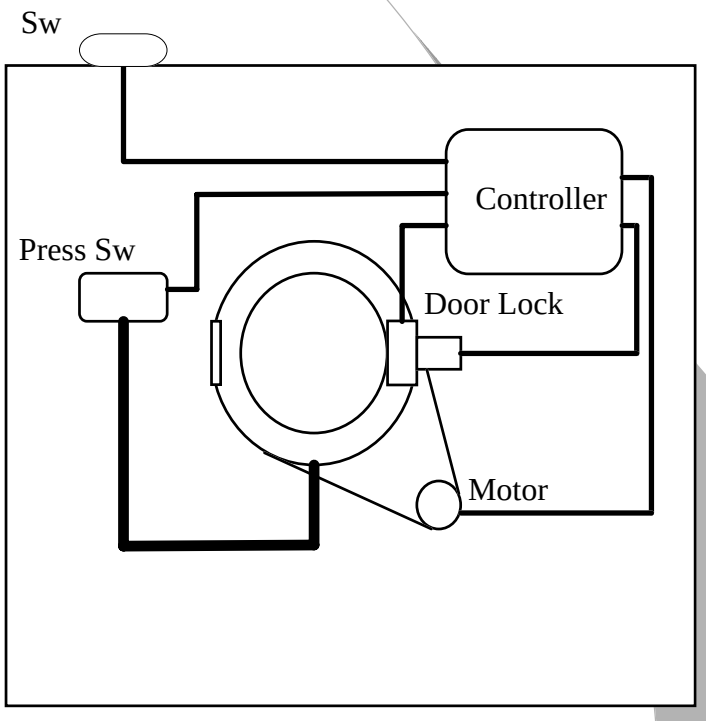
Entity + Architecture

- Together the entity and associated architecture of the AND function can now be used to describe a 2 input AND with any propagation delay by simply replacing the value of the generic DELAY.
- NOTE architectures can contain other components, in other words, other ENTITIES. See then example of making a 3 input AND gate from two input AND gates on page 2-5.

Entity design.

- Use top down approach
  - Implement at high level
  - Then test
  - Then describe precise implementation
  - See example

A Washing Machine



Design Entity

- Define entity Controller
- Entity CONTROLLER is
  - port(PRESS : in bit:
  - ON: in bit:
  - DOOR_SHUT: in bit:
  - MOTOR_ON: out bit:
  - DOOR_RELEASE: out bit:)

end

Behaviour

- architecture BEHAVE of CONTROLLER is

begin

  - MOTOR_ON <= ON and PRESS;
  - DOOR_RELEASE <= not MOTOR_ON after 30s:

end

NOTE

NO idea how to produce 30s delay but it must be feasible.

Libraries

- There are standard libraries available
- Store all your work in your own libraries.
- Use a different library for each assignment

Packages

- Packages provide a place to store frequently used definitions enabling them to be shared by multiple Design Units.

- Typically a package may be used declare constants, types, sub-types and sub-programs. Entities themselves may not be declared as a package.

The Package

- A package is split into two parts, a package declaration which defines the interface and a package body which defines the deferred details. See Appendix A in the Training Manual. In a Library called IEEE a package Std_Logic_1164 is defined (pages A-1 A-3).The associated Package body is defined on pages A-4 A-20.

The Configuration

- You may well have different implementations of the same design. You will need the same Test bench, whatever the implementation. The Configuration statement allows you to select which implementation you wish to test.