ES7243 User Guide

(Rev.1.00)

ES7243 User Guide

ES7243 is a high performance stereo audio ADC, and it supports LRCK frequency range from 8 kHz to 192 kHz. It has two differential inputs, AINLP-AINLN and AINRP-AINRN, followed by a stereo microphone amplifier with programmable gain. Also, it has TDM mode to cascade multiple ES7243 devices. Its TDM cascading mode makes it easy to connect with DSP.

ES7243 is easy to use, utilizing the differential inputs and the internal PGA to interface with microphone and boost the microphone signal level. One ES7243 can interface with two microphones. It also can be interfaced with line input if the internal PGA gain is +1dB.

ES7243 supports standard audio clocks (256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (25 MHz, 26 MHz, etc). According to the serial audio data sampling frequency (Fs), the device can work in three speed modes: single speed mode, double speed mode and Quad Speed mode. In single speed mode, Fs normally range from 8 kHz to 48 kHz, and in double speed mode, Fs normally ranges from 64 kHz to 96 kHz. In quad speed mode, Fs normally range from 96 kHz to 192 kHz.

ES7243 can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

ES7243 is very suitable for music and voice application, such as Microphone Array, Conference system, Sound bar, Audio Interface, DVR, NVR, etc. Its input circuit and TDM mode makes it ideal for microphone array application.

Features

1. Supports I2S, Left Justified and DSP-A/B digital format, supports Master or Slave mode.
2. Supports 256 or 384 LRCK ratio. Also, it supports non standard LRCK ratio without obvious performance degraded.
3. Has one stereo differential line input or microphone input, followed by a stereo PGA with gain range from +1dB to +27dB.
4. Has I2C controls port to read/write internal register.
5. Has TDM mode to cascade multiple ES7243 for microphone array application or conference system.
6. Has standby capability to save power consumption.

ADC Performance

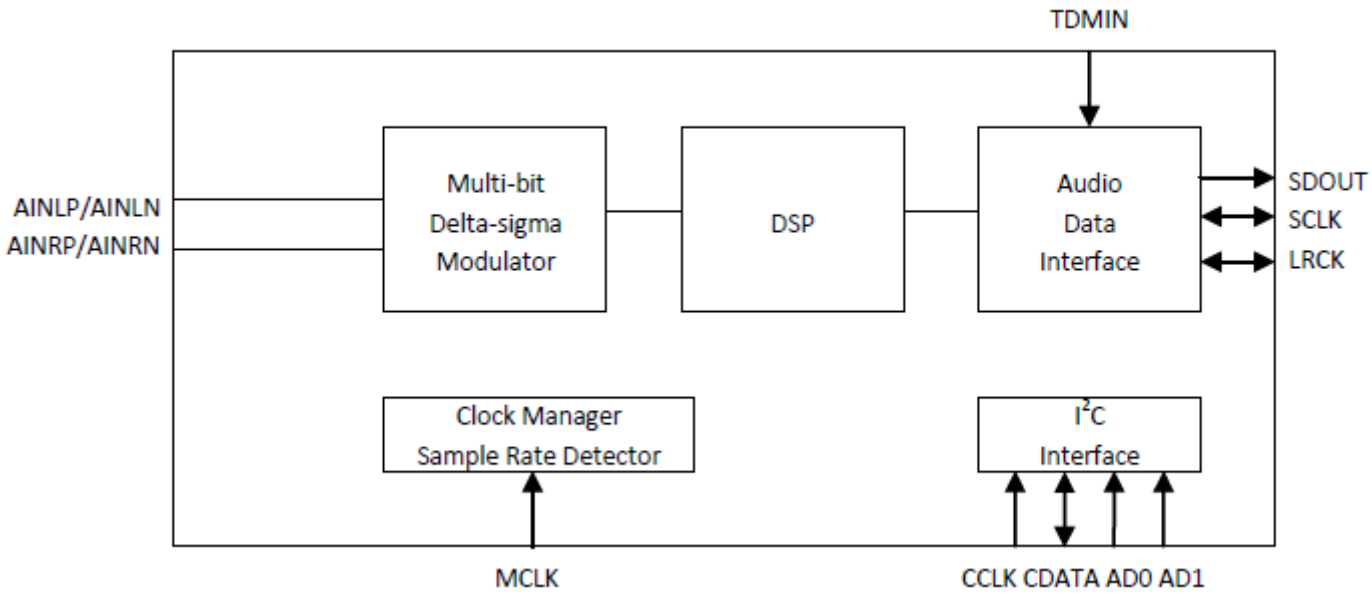
1. -88dB THD+N
2. 103dB SNR @ +1dB PGA gain, 92dB SNR @ +27dB PGA gain
3. 24-bit, 8 to 200 kHz sampling frequency
4. Stereo differential line inputs or microphone inputs

Package Outline

1. ES7241 QFN-20, 3mm × 3mm

ES7243 User Guide

1 BLOCK DIAGRAM



ES7243 Block Diagram

SIGNAL PATH

ES7243 has stereo differential inputs, AINLP-AINLN and AINRP-AINRN, followed by a stereo PGA with gain range from +1dB to +27dB. Then, the internal high performance multi-bit delta-sigma audio ADC does analog to digital converting. At last digital signal should be outputted on ASDOUT pin.

The maximum input level of these line inputs is 1Vrms.

2 Recommended Operating Condition and Power Consumption

The following Table shows the recommended operating condition of ES7243.

PARAMETER	MIN	TYP	MAX	UNIT
VDDA	3.0	3.3	3.6	V
VDDD	3.0	3.3	3.6	V
VDDP	1.6	3.3	3.6	V

Below Table lists power consumption in normal mode and standby mode.

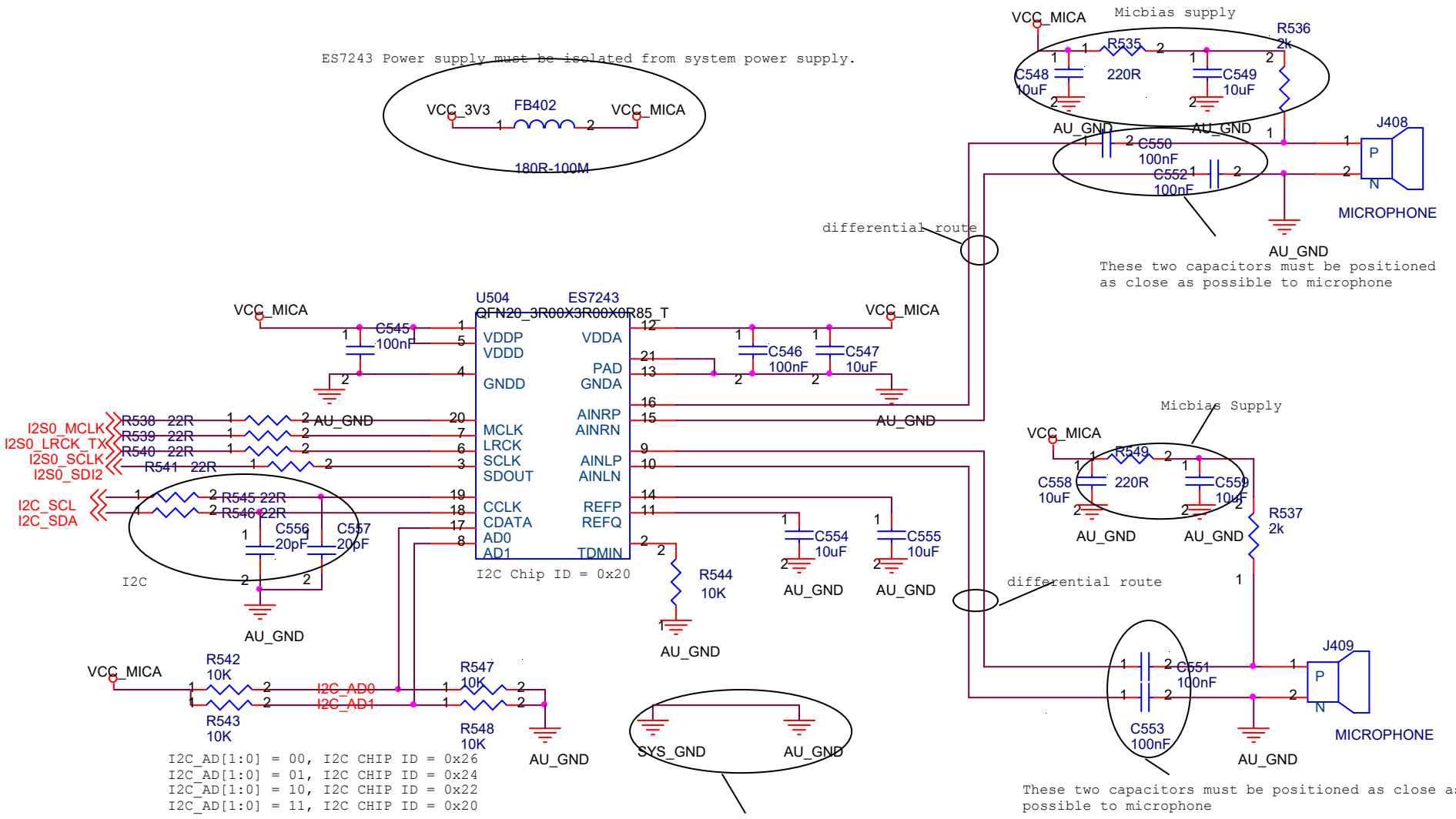
	Clock Condition	Ivddp(mA) (VDDP = 3.3V)	Ivddd(mA) (VDDD = 3.3V)	Ivdda(mA) (VDDA = 3.3V)
Normal Mode	MCLK=12.288MHZ LRCK = 48KHZ	0.00	10.88	10.08
	MCLK=6.144MHZ LRCK = 48KHZ	0.00	5.77	10.08
	MCLK=6.144MHZ LRCK = 24KHZ	0.00	5.79	10.08
	MCLK=4.096MHZ LRCK = 16KHZ	0.00	3.99	10.08
	MCLK=2.048MHZ LRCK = 16KHZ	0.00	2.38	10.08
Standby Mode	Standby Mode 1: R6=0x5C R7=0xFF R8=0x4B R9=0x9F	0.00	0.68	0.67
	Standby Mode 2: R6=0x5C R7=0x3F R8=0x4B R9=0x9F	0.00	0.68	0.01
	Standby Mode 3: Stop MCLK and I2S CLK, R6=0x5C,R7=0x3F,R8=0x4B, R9=0x9F	0.00	0.09	0.01

3 Application Circuit and PCB Layout Guide

This section provides some guideline about circuit schematic and PCB layout.

3.1 ES7243 Application Circuit

Below circuit schematic shows the details about microphone interface, I2C, ground and power supply.

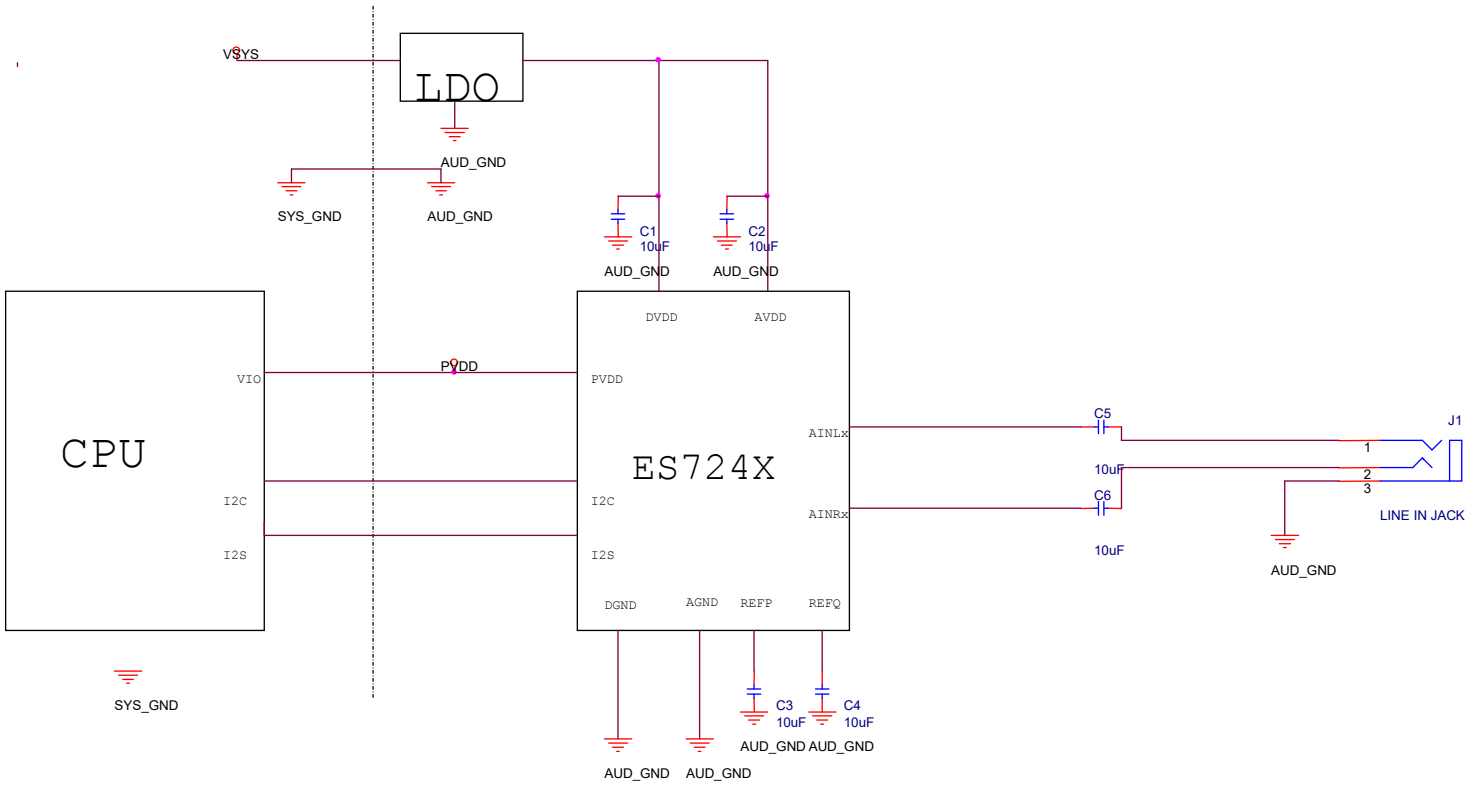


3.2 PCB Layout Guide

As with any high-resolution audio converter, designing with ES7243 requires careful attention to PCB layout if its potential performance is to be realized.

3.2.1 The Power supply, Grounding, Decoupling and Filters

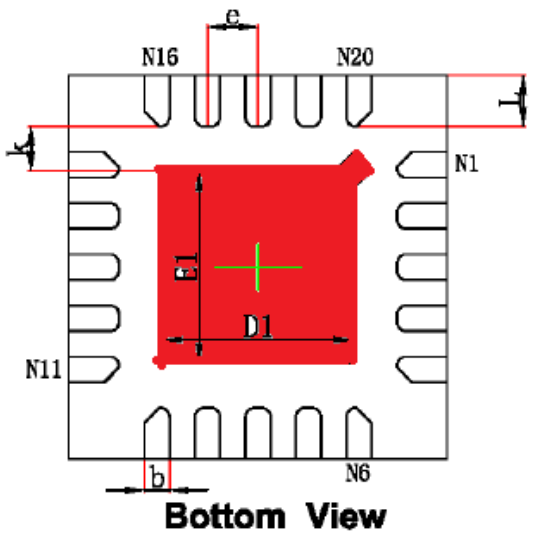
The power supply of ES7243 must be isolate from system power supply. A LDO specified for ES7243 is recommended in order to get the best audio performance. Usually, GNDD and GNDA must be connect to the same analog ground plane, and then join into system ground at a single point nearby the power supply. It is important to prevent high frequency noise or high current noise from going into audio ground plane. Below diagram illustrates ES7243 power supply and grounding.



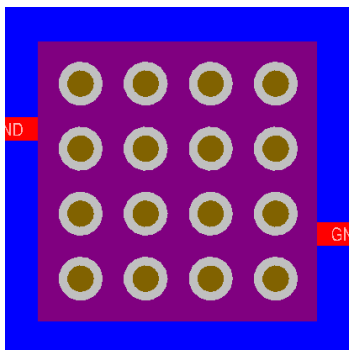
There need some decoupling and filter capacitors on VDDD, VDDA, REFP and REFQ pins. These decoupling and filter capacitors must be as near to ES7243 package as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from REFP and REFQ in order to avoid unwanted coupling to ADC modulators. The filter capacitors on REFP and REFQ pins, especially 0.1uF capacitor, must be positioned to minimize the electronic path from these reference pins to GND.

3.2.2 The Thermal Pad of ES7243

There is a thermal pad on the bottom of ES7243 package. The following drawing shows this thermal pad.

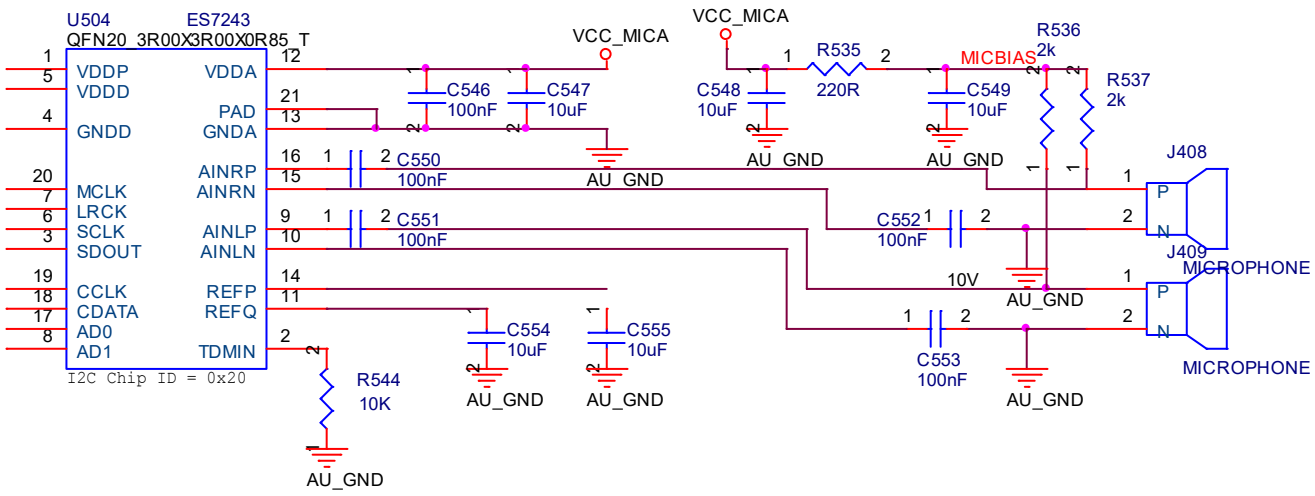


In practical system, the thermal pad must be connected to ground plane by via. The following picture illustrates how the thermal pad is connected to ground plane.

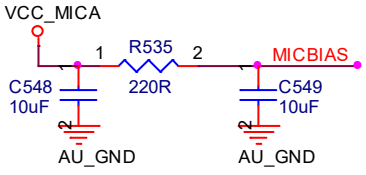


3.3 Microphone Circuit

ES7243 has two differential inputs, AINLP-AINLN and AINRP-AINRN, which can be used as microphone interface. Usually, AINLP and AINLN is a differential route. AINRP and AINRN is another differential route. It is important note here that the analog input capacitors, such as C550, C551, C552 and C553, must be near to the microphone.

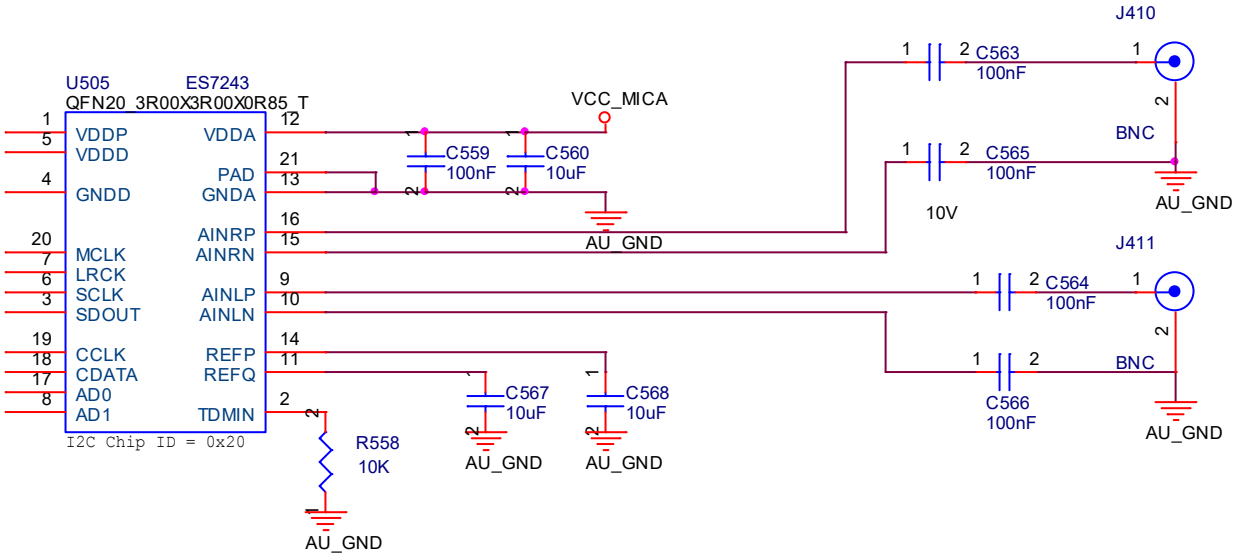


ES7243 doesn't have microphone bias voltage, so an external microphone bias circuit is used to supply for microphones. Usually, an R-C filter, for example 220Ω and 10uF, is used to generate microphone bias voltage from ES7243 power supply. Below picture shows how to generate MICBIAS voltage from ES7243 power supply.



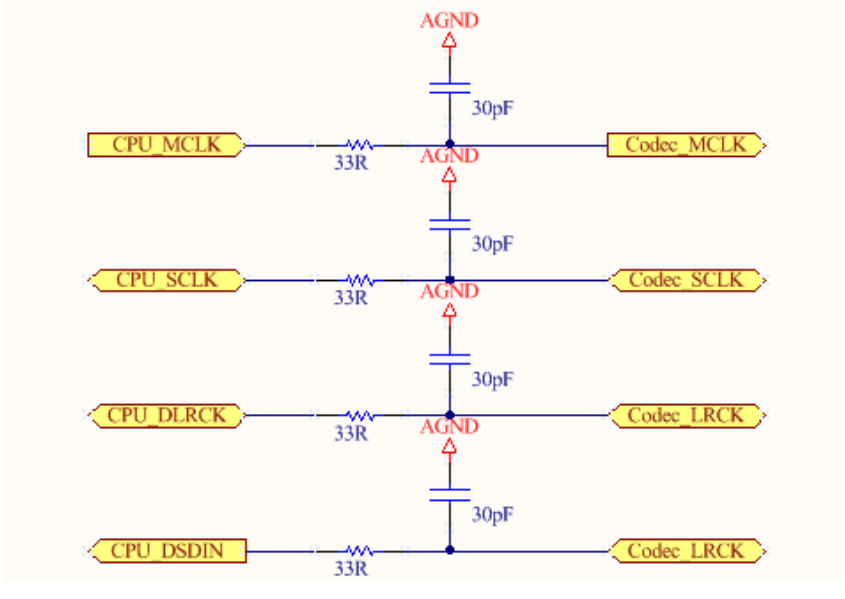
3.4 Line input

If the internal PGA gain is 1dB, the differential inputs of ES7243 can also be used as line inputs. Following circuit schematic illustrates the line input of ES7243. It is important note here that the analog input capacitors, such as C563, C565, C564 and C566, must be near to the line input jack.



3.5 The Circuit Schematic for I2S

If the length of I2S clock is larger than 10cm, please use 30pF capacitors between I2S clock route and ground. For example,

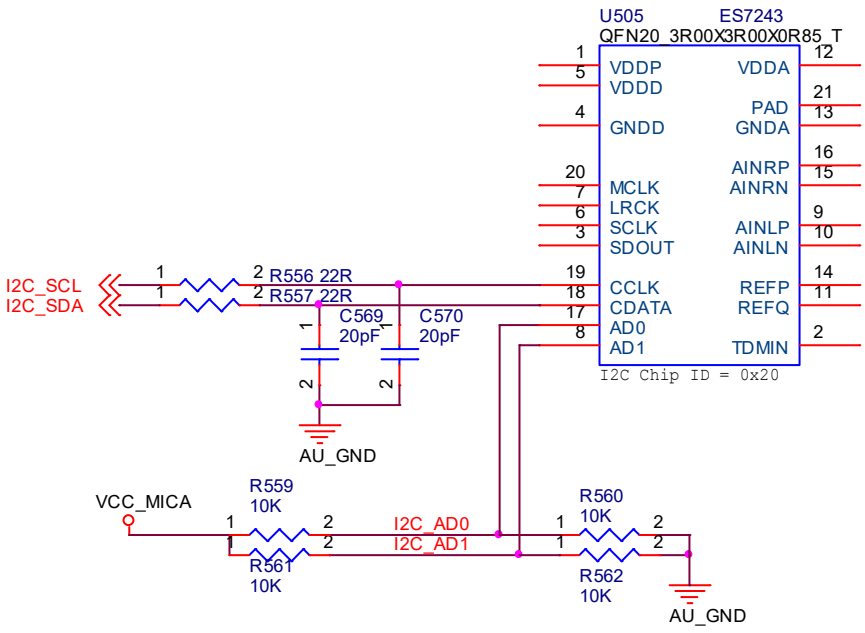


3.6 The Circuit Schematic of I2C

ES7243 has I2C control port to read / write internal register. Below schematic shows the circuit of I2C port. The R-C low pass filter is generally recommended for I2C bus to avoid high frequency noise. The I2C route must be shielded by ground.

Pin17 (AD0) and Pin8 (AD1) are used to select the I2C chip address of ES7243. Following Table shows the definition of I2C chip address.

ES7243 I2C Chip Address	The Level of AD[1:0] pin
0x20 (8bit) / 0x10 (7bit)	AD1 =1, AD0 = 1
0x22 (8bit) / 0x11(7bit)	AD1 = 1, AD0 = 0
0x24 (8bit) / 0x12 (7bit)	AD1 =0, AD0 = 1
0x26(8bit) / 0x13(7bit)	AD1 = 0, AD0 = 0



3.7 TDMIN pin

ES7243 has TDM mode to cascade multiple ES7243 devices. The TDMIN pin of ES7243 device must be pulled down to GND by 10kΩ resister whether TDM mode enabled or not.

4 ES7243 Application

ES7243 operates in software mode, and it communicates with host device by I2C port. In ES7243, some internal registers

are used for power control, PGA gain control, serial digital audio format selection, master or slave mode selection, TDM mode enable/disable and LRCK ratio selection, etc.

Multiple ES7243 can be cascaded for microphone array application. This TDM cascading mode is very useful in speech recognition, speech localization and conference system. It is important note here that the TDMIN pin must be pulled down to GND by 10KΩ resister even if TDM mode is disabled.

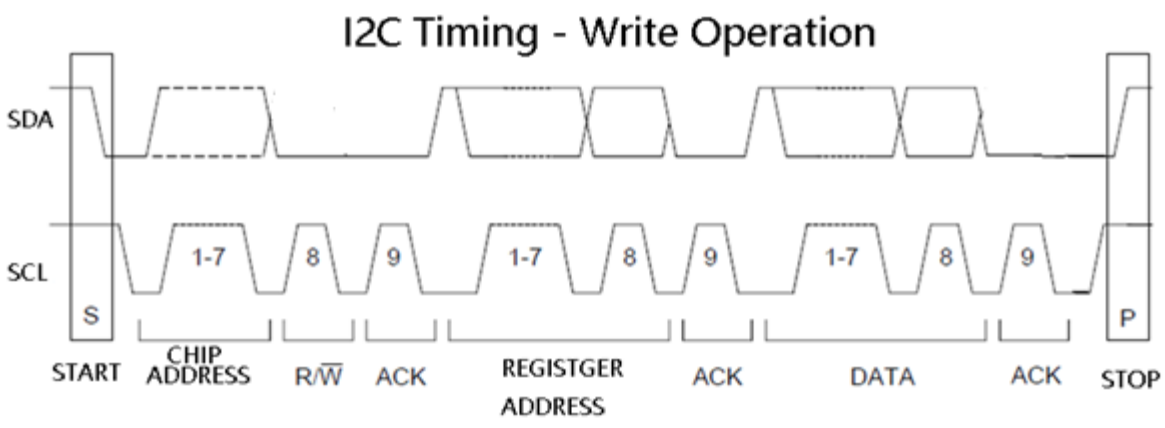
4.1 Register Map

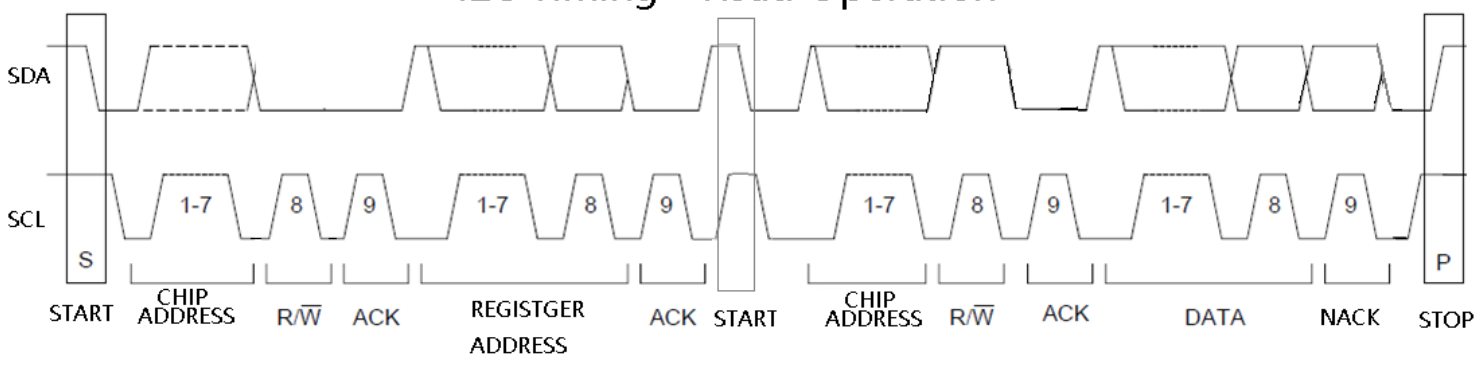
	Register Addr	B7	B6	B5	B4	B3	B2	B1	B0	default
Reg.00	**0x00**	//////////////////	MCLK_DIV		ADC_HPF_DIS	SPEED_MODE		MS_MODE	WORK_MODE	0x00
Reg.01	**0x01**	TDM_ENA	SP_BCLKINV	SP_LRP	SP_WL			SP_PROTOCAL		0x00
Reg.02	**0x02**	LRCKDIV								0x10
Reg.03	**0x03**	//////////////////	//////////////////	BCLKDIV						0x04
Reg.04	**0x04**	//////////////////	//////////////////	//////////////////	//////////////////	CLK_ADC_DIV				0x02
Reg.05	**0x05**	//////////////////	//////////////////	AUTOMUTE_DETED	ADC_MUTE_SIZE	ADC_SDP_MUTE	ADC_NOISETHD		ADC_AUTOMUTE	0x13
Reg.06	**0x06**	SP_TRI	MCLK_DIS	SEQ_DIS	RST_DIG	RST_ADCDIG	FORCE_CSM			0x00
Reg.07	**0x07**	VMIDSEL		PDN_ADCVREFGEN	MODTOP_RST	PDN_MODL	PDN_MODR	PDN_PGAL	PDN_PGAR	0x3F
Reg.08	**0x08**	//////////////////	GAIN_SW[4:2]			INPUT_SEL2	GAIN_SW[1:0]		INPUT_SEL	0x11
Reg.09	**0x09**	ANA_PDN	VMIDLOW		ADC_LP_VRP	ADC_LP_VCMMOD	ADC_LP_PGA	ADC_LP_INT1	ADC_LP_FLASH	0x80
Reg.10	**0x0A**	CHIPINI_CON								0xC0
Reg.11	**0x0B**	POWERUP_CON								0xC0
Reg.12	**0x0C**	//////////////////	//////////////////	ADCBIAS_SWH		SRATIO_DIV				0x12
Reg.13	**0x0D**	ADC_CSM		ADC_OSR						0xA0
Reg.14	**0x0E**	CHIP_ID								0x40

4.2 I2C Control Port

ES7243 supports standard I2C interface with maximum 400kbps rate. External host device can completely configure this device through writing to internal registers. The transfer rate of I2C can be up to 400kbps.

The following drawing illustrates the timing of I2C.





ES7243 has two chip address pins, AD1 and AD0, to set I2C chip address. The following table shows the chip address definition,

State of AD[1:0] pins	Chip Address
00	0x13(7bit) / 0x26 (8bit)
01	0x12(7bit) / 0x24 (8bit)
10	0x11(7bit) / 0x22 (8bit)
11	0x10(7bit) / 0x20 (8bit)

4.3 Software Mode

ES7243 operates in software mode. WORK_MODE (bit0 of register 0x00) must be set to 1 to enable software mode.

WORK_MODE = 0	ES7243 In Hardware Mode
WORK_MODE = 1	ES7243 In Software Mode

4.4 Master or Slave mode

ES7243 can operate in master mode or slave mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock. In slave mode, ES7243 detects MCLK/LRCK ratio automatically. In master mode, ES7243 generates LRCK and SCLK from MCLK according to the setting of LRCKDIV and BCLKDIV.

MS_MODE (Bit1 of register 0x00) is used to select master or slave mode.

MS_MODE = 0	ES7243 In Slave Mode
MS _MODE = 1	ES7243 In Master Mode

4.5 Speed Mode

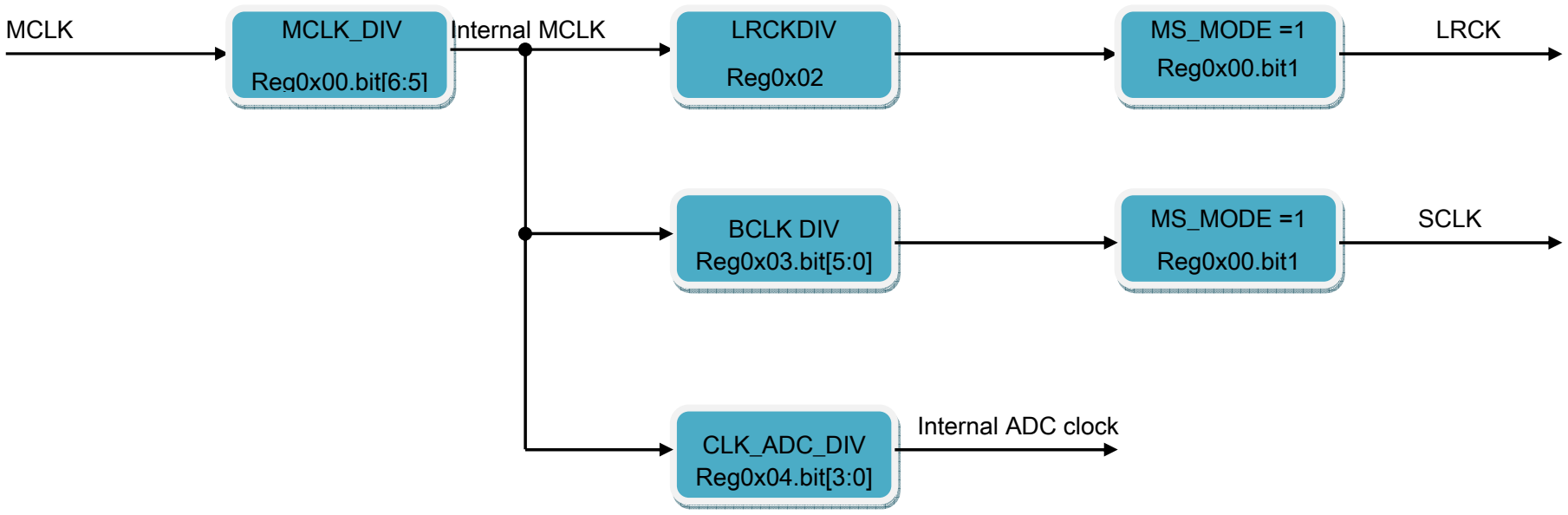
ES7243 supports three speed modes: single speed mode, double speed mode and quad speed mode. In single speed mode, LRCK frequency normally ranges from 8kHz to 48kHz; In double speed mode, LRCK frequency normally ranges from 64kHz to 96kHz; In quad speed mode, LRCK frequency normally ranges from 96kHz to 192kHz.

In slave mode, ES7243 detects speed mode automatically. In master mode, Bit[3:2] of register 0x00 is used to select proper speed mode.

SPEED_MODE	3:2	Set output sampling frequence for chip 00 – single speed 01 – double speed 10 – quad speed 11 – not allowed

4.6 Internal clock diagram

The following diagram illustrates internal clock diagram in master mode. It is important note here that ES7243 can detect LRCK ratio automatically in slave mode



Following is the register definition for internal clock management.

	B7	B6	B5	B4	B3	B2	B1	B0	default
Reg0x00	////////////////////	MCLK_DIV		ADC_HPF_DIS	SPEED_MODE		MS_MODE	WORK_MODE	0x00
Reg0x02	LRCKDIV								0x10
Reg0x03	////////////////////	////////////////////	BCLKDIV						0x04
Reg0x04	////////////////////	////////////////////	////////////////////	////////////////////	CLK_ADC_DIV				0x02
Reg0x0D	ADC_CSM		ADC_OSR						0xA0

1. MCLK_DIV definition

MCLK_DIV = 00	Internal MCLK = MCLK /1
MCLK_DIV = 01	Internal MCLK = MCLK /2
MCLK_DIV = 10	Internal MCLK = MCLK /3
MCLK_DIV = 11	Internal MCLK = MCLK /4

2. LRCKDIV definition

	LRCK	ratio	LRCK_DIV	CLK_ADC_DIV	CYCLES	ADC_OSR
ADC MCLK 12M288	96k	128	0x08	0x02	256	0X20
	64k	192	0x0C	0x03	256	0X20
	48k	256	0x10	0x02	256	0X20
	32k	384	0x18	0x03	256	0X20
	24k	512	0x20	0x04	256	0X20
	16k	768	0x30	0x06	256	0X20
	12k	1024	0x40	0x08	256	0X20
	8k	1536	0x60	0x0C	256	0X20
ADC MCLK 12M	96k	125	0X85	0x02	250	0X1F
	88k2	136				
	48k	250	0X85	0x02	250	0X1F
	44k1	272	0X11	0x02	272	0X22
	32k	375	0X8A	0x03	250	0X1F
	24k	500	0X94	0x04	250	0X1F
	22k05	544	0X22	0x04	272	0X22
	16k	750	0X9E	0x06	250	0X1F
	12k	1000	0XAA	0x08	250	0X1F
	11.025k	1088	0X44	0x08	272	0X22
	8k	1500	0XBC	0x0C	250	0X1F

ADC MCLK 11M 2896	LRCK	ratio	LRCK_DIV	CLK_ADC_DIV	CYCLES	ADC_OSR
	88k2	128	0x08	2	256	0X20
	44k1	256	0x10	2	256	0X20
	22k05	512	0x20	4	256	0X20
	11k025	1024	0x40	8	256	0X20
ADC MCLK 25M	96k	260				
	88k2	283				
	48k	521		4	260	32
	44k1	567		4	283	33
	32k	781		6	260	32
	24k	1042				
	22k05	1134				
	16k	1563				
	12k	2083				
	8k	3125				

3. BCLKDIV definition

BCLKDIV	4:0	00000 – master mode BCLK generated automatically based on the clock table (default) 00001 – MCLK/1 00010 – MCLK/2 00011 – MCLK/3 00100 – MCLK/4 00101 – MCLK/6 00110 – MCLK/8 00111 – MCLK/9 01000 – MCLK/11 01001 – MCLK/12 01010 – MCLK/16 01011 – MCLK/18 01100 – MCLK/22 01101 – MCLK/24 01110 – MCLK/33	01111 – MCLK/36 10000 – MCLK/44 10001 – MCLK/48 10010 – MCLK/66 10011 – MCLK/72 10100 – MCLK/5 10101 – MCLK/10 10110 – MCLK/15 10111 – MCLK/17 11000 – MCLK/20 11001 – MCLK/25 11010 – MCLK/30 11011 – MCLK/32 11100 – MCLK/34 Others – MCLK/4

4.7 Serial Digital Audio Format

ES7243 supports I2S, Left Justified, DSP-A and DSP-B serial digital audio format with resolution from 16bits to 32bits. Only DSP-A or DSP-B format is supported in TDM cascading mode.

The following is the register definition of serial digital audio format,

	B7	B6	B5	B4	B3	B2	B1	B0	default
Reg0x01	TDM_ENA	SP_BCLKINV	SP_LRP	SP_WL			SP_PROTOCAL		
	1. Enable TDMIN for Cascading mode 0. Disable TDMIN	SP_BCLKINV = 0, normal mode, SP_BCLKINV=1, BCLK Inverted	LRC polarity For I2S/Left Justify: 0 – L/R normal polarity 1 – L/R invert polarity For DSP mode case: 0 – Mode A, 1 – Mode B,	The data format of serial data port 000 – 24-bit 001 – 20-bit 010 – 18-bit 011 – 16-bit 100 – 32-bit			The protocol of serial data port 00 – I2S 01 – LJ 10 – not allowed 11 – DSP		0x00

The following diagram illustrates the timing of serial digital audio format.

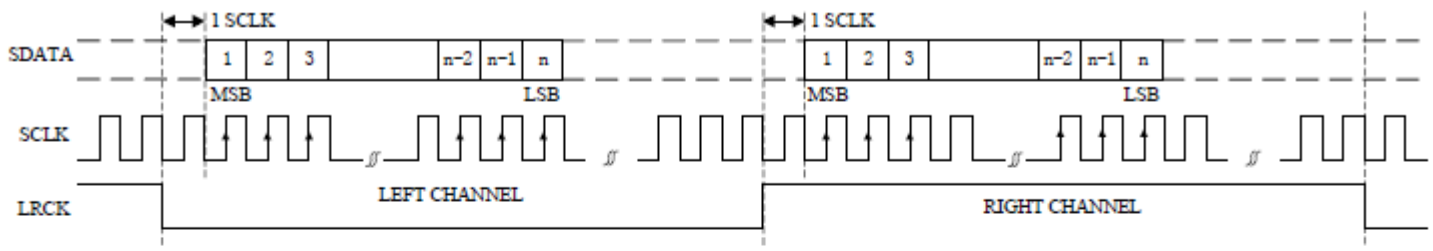


Figure 2 I²S Serial Audio Data Format Up To 24-bit

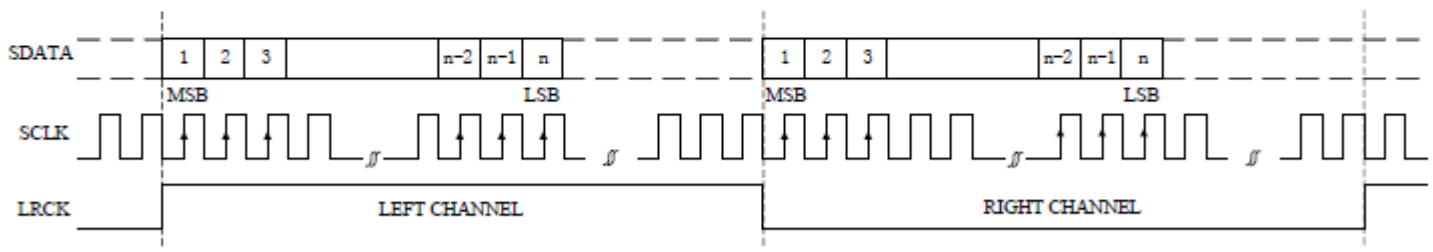


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

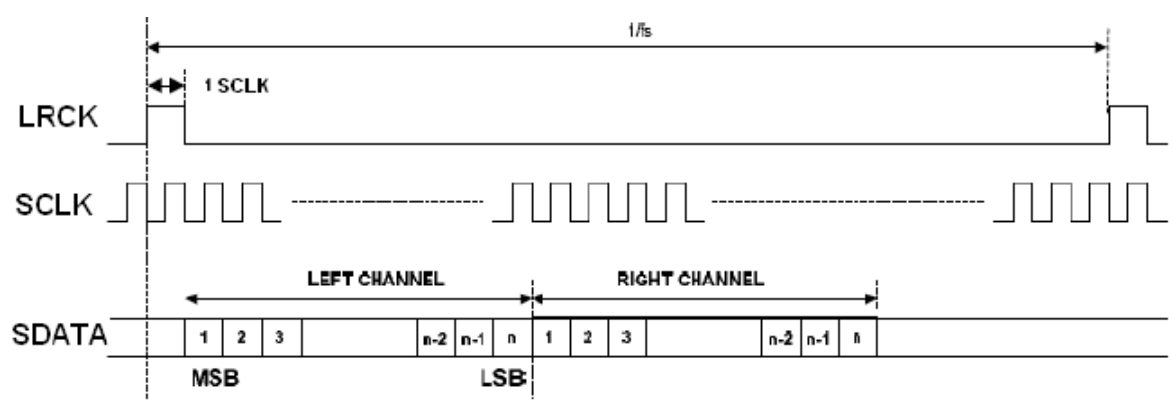


Figure 4 DSP/PCM Mode A

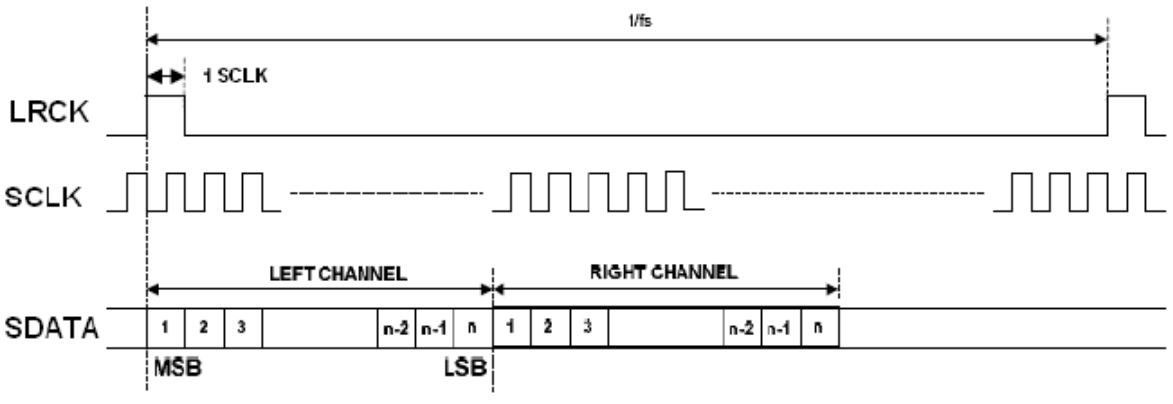


Figure 5 DSP/PCM Mode B

4.8 TDM Mode

ES7243 supports TDM mode to cascade multiple ES7243 devices. In TDM mode, up to 4 ES7243 devices can be cascaded, and up to 8 channels ADC data will be presented in one LRCK cycle. No Phase difference exists between these ADC data.

Its TDM mode makes it ideal for microphone array application. Two critical issues must be considered in microphone array application. One is the number of microphone. Another is the phase difference between ADC data .Usually more than one microphone will be used to form a microphone array. Ideally, all ADCs in microphone array do analog-to-digital conversion at the same time, so that there isn't phase difference between ADC data.

If this microphone array consists of two microphones, there only needs one ES7243 device. If the array is made by more than two microphones, there should need two or more ES7243 devices, and these ES7243 devices should be cascaded.

In TDM mode, the serial digital audio format must be DSP-A or DSP-B. CPU will get incorrect data if I2S or Left justified format is used in TDM mode.

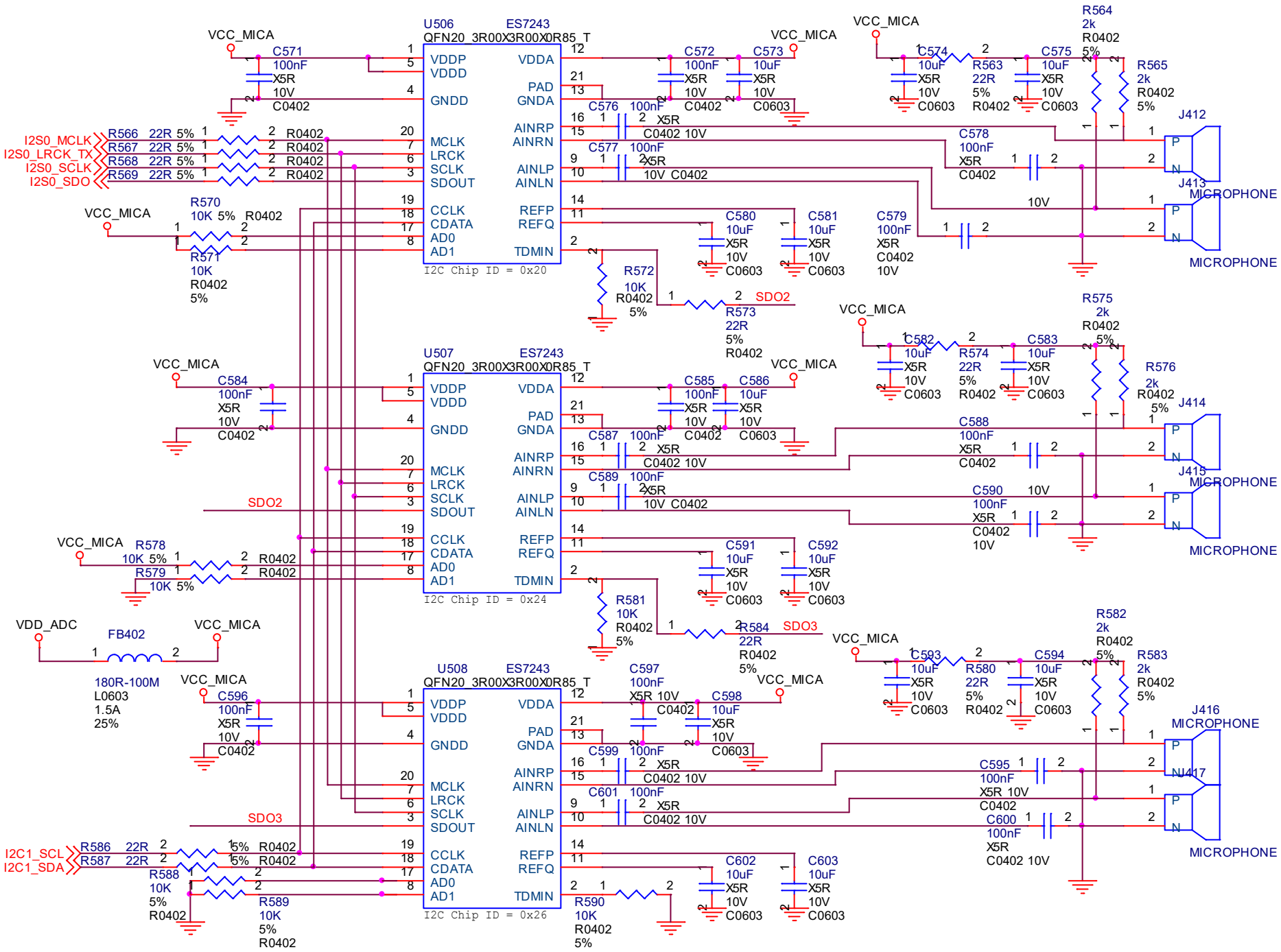
TDM_ENA (Bit7 of Register 0x01) is used to enable or disable TDM mode.

TDM_ENA = 0	TDM Mode Disable
TDM_ENA = 1	TDM Mode Enable

It is important note here that the TDMIN pin of ES7243 must be pulled down to ground by 10kΩ even if TDM mode is disabled.

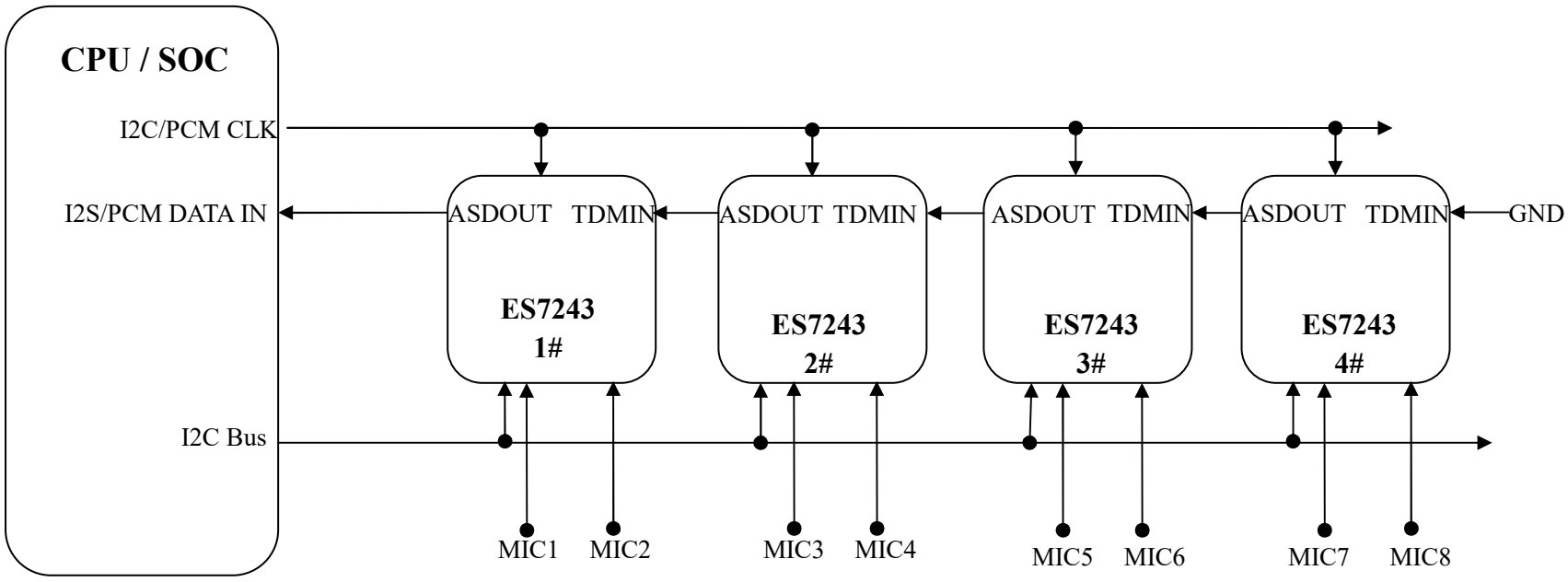
4.8.1 Application circuit of TDM Mode

Below schematic shows three ES7243 devices cascaded in TDM mode.

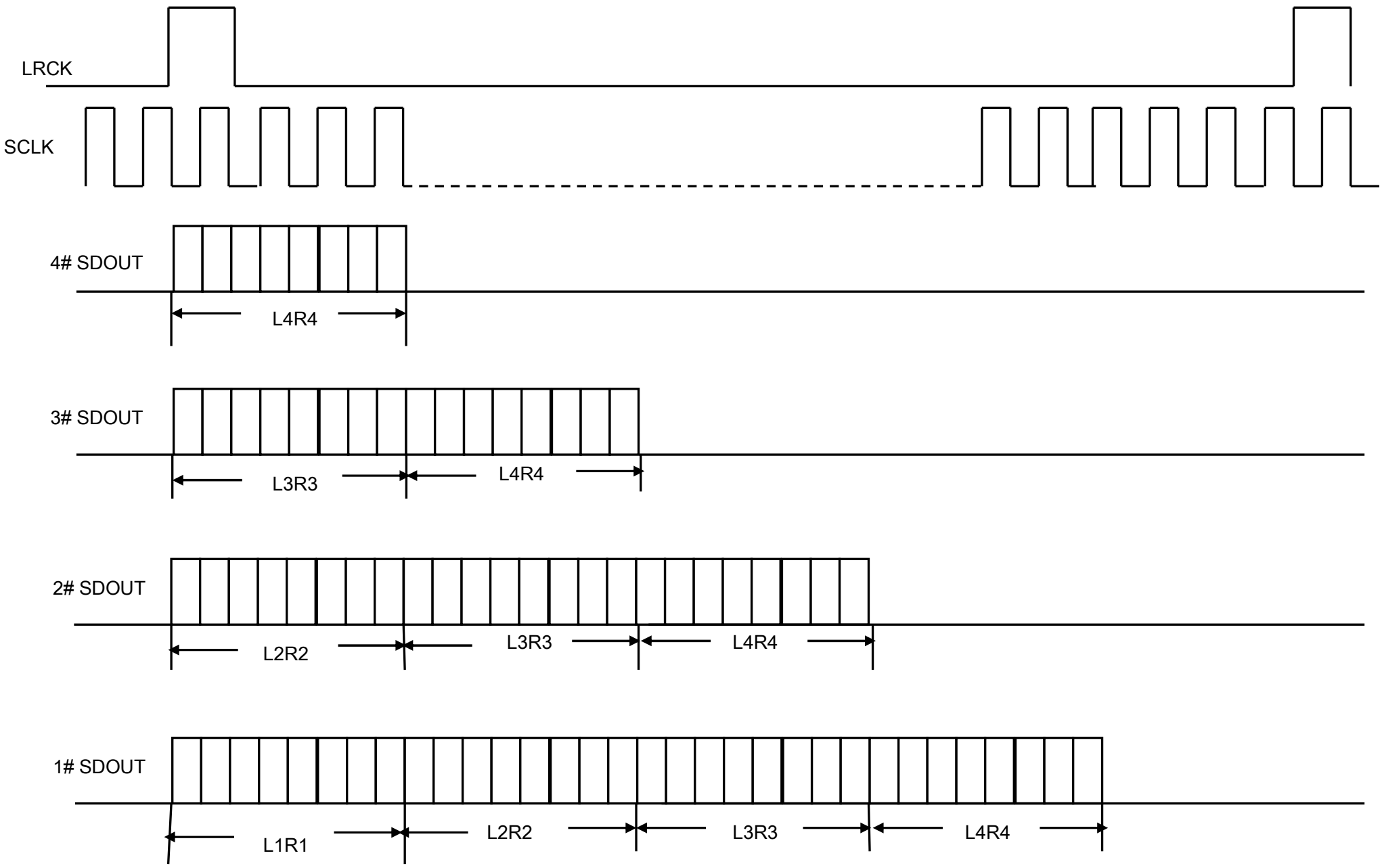


4.8.2 Diagram and Timing of TDM Cascading Mode

Below diagram illustrates the TDM cascading mode of ES7243.

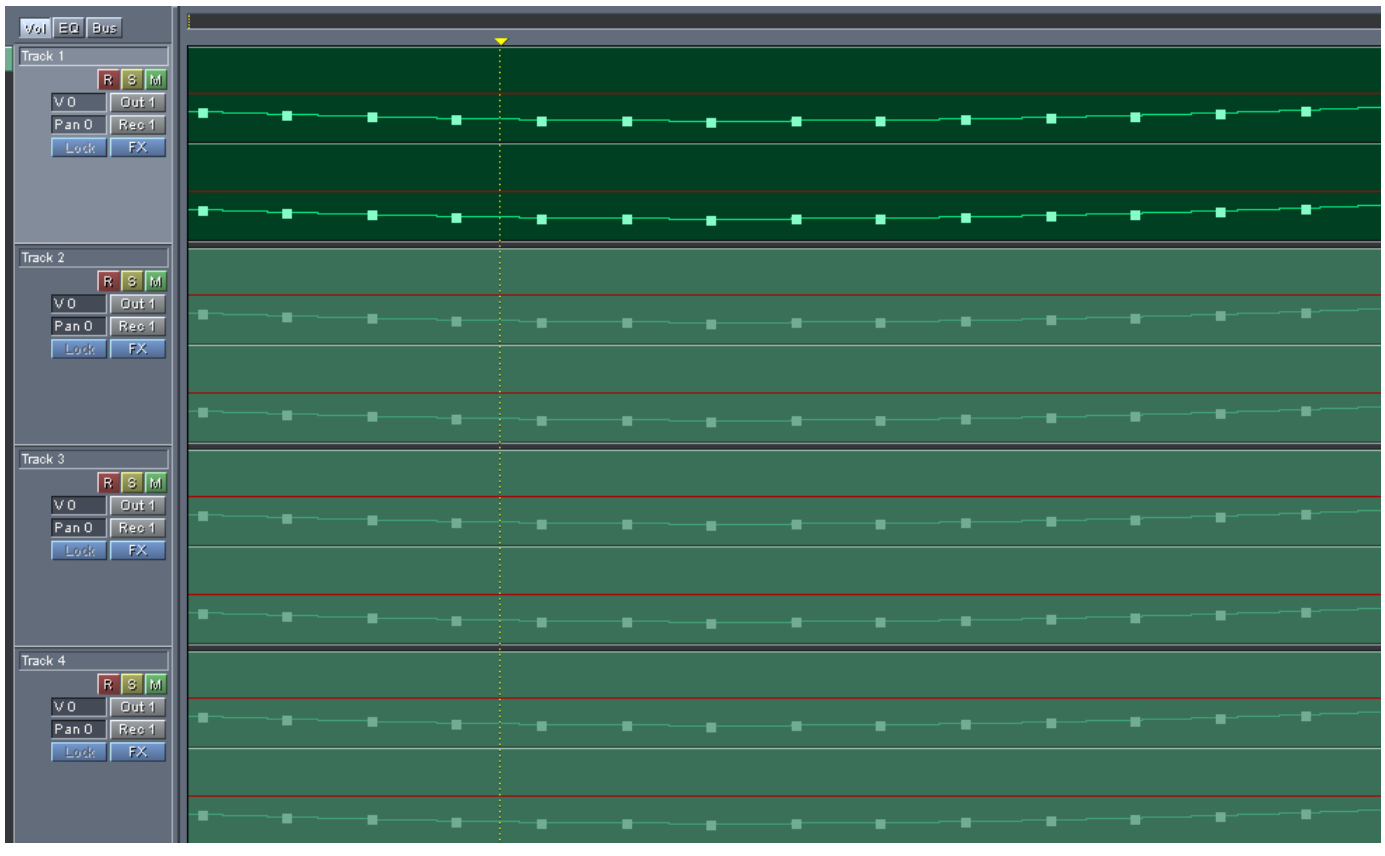


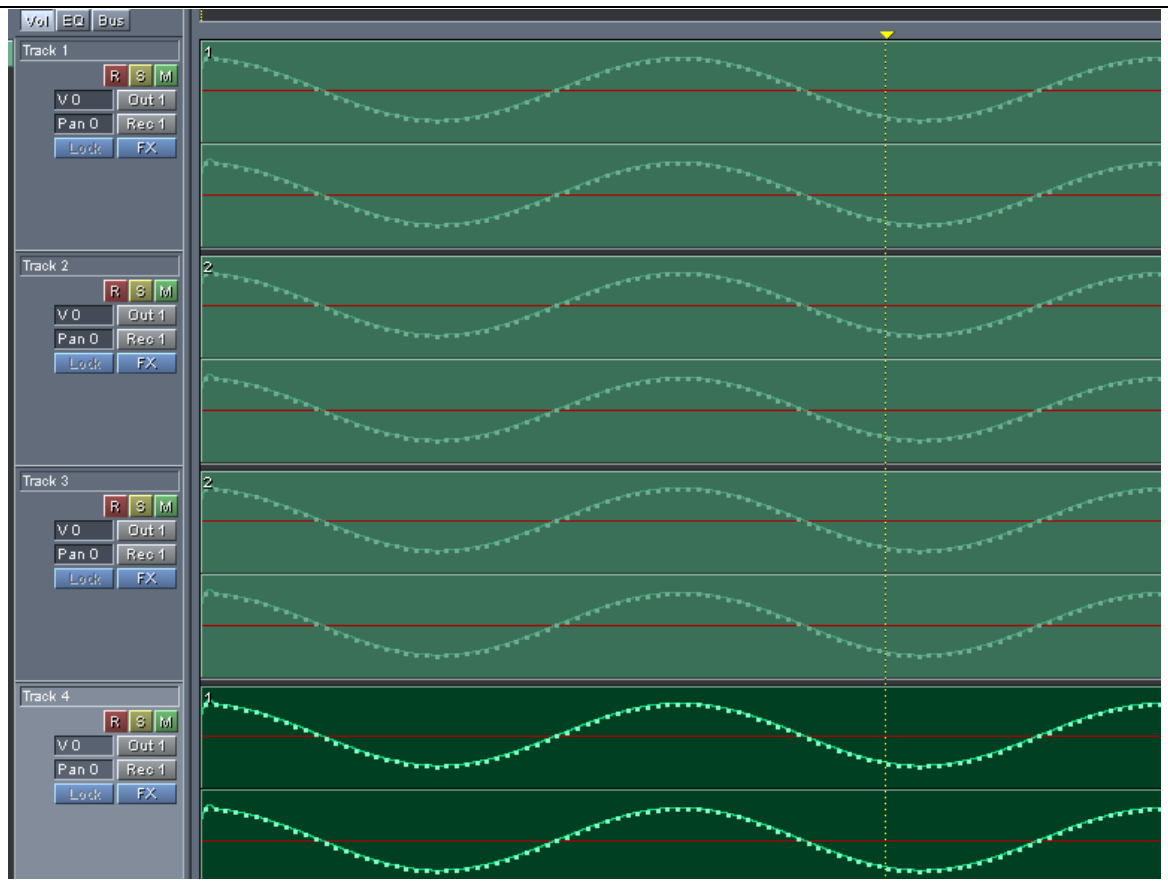
The following drawing shows the timing of TDM cascading mode.



4.8.3 Phase Difference between multiple ADCs

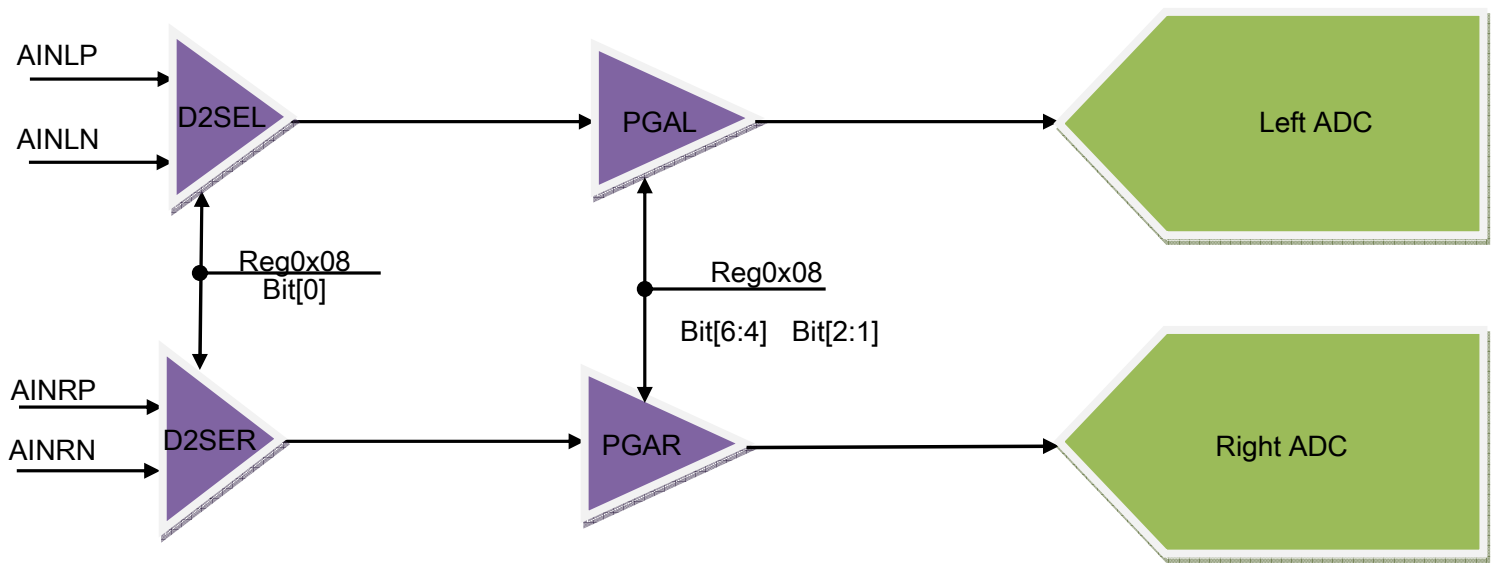
In TDM mode, there isn't phase difference existing between the data of multiple ES7243 devices. Please use audio software, for example Cooledit, to analysis the phase difference of multiple ADC data. Following picture shows the analysis result of Cooledit. It shows that no phase difference exists between 8 channels TDM cascading data.





4.9 Analog input

Below diagram shows the analog input path of ES7243.



In ES7243, there is a stereo differential analog input, AINLP-AINLN and AINRP-AINRN, followed by a stereo PGA with gain range from +1dB to +27dB. INPUT_SEL (bit0 of register 0x08) is used to enable or disable these differential inputs.

If INPUT_SEL = 1'b, the differential inputs is enabled. In register 0x08, Bit[6:4] and Bit[2:1] are used to set the PGA gain. Below table shows the definition of PGA gain.

Bit6	Bit5	Bit4	Bit2	Bit1	Gain (dB)
0	0	1	0	0	+1
0	0	1	0	1	+3.5
0	1	0	0	0	+18
0	1	0	0	1	+20.5
0	0	0	1	0	+22.5
1	0	0	0	0	+24.5
0	0	0	1	1	+25
1	0	0	0	1	+27

4.10 Power Control

In ES7243, some registers are used for power control. The following shows the power control register definition.

REGISTER 0X07 – ANALOG CONTROL REGISTER 0, DEFAULT 1000 0000

Bit Name	Bit	Description
VMIDSEL	7:6	Vmid selection: 00 – Vmid disabled 01 – 50 kΩ divide 10 – 500 kΩ divide (default) 11 – 5 kΩ divide
PDN_ADCVREFGEN	5	Power down control for ADCVREF generate module 1 – power down 0 – normal
MODTOP_RST	4	Power down control for modulator top 1 – power down 0 – normal
PDN_MODL	3	Power down control for left chanel modulator 1 – power down 0 – normal
PDN_MODR	2	Power down control for left chanel modulator 1 – power down 0 – normal
PDN_PGAL	1	Power down control for left chanel PGA 1 – power down 0 – normal
PDN_PGAR	0	Power down control for right chanel PGA 1 – power down 0 – normal

REGISTER 0X09 – ANALOG CONTROL REGISTER 2, DEFAULT 1000 0000

Bit Name	Bit	Description
ANA_PDN	7	Power down control for whole analog 1 – power down 0 – normal
VMIDLOW	6:5	Vmid voltage: 00 – vdda/2 01 – vdda/2 - 50mV 10 – vdda/2 - 100mV 11 – vdda/2 - 150mV
ADC_LP_VRP	4	Low power control for analog VRP 1 – enter low power 0 – normal
ADC_LP_VCMMOD	3	Low power control for analog VCMMOD 1 – enter low power 0 – normal
ADC_LP_PGA	2	Low power control for analog PGA 1 – enter low power 0 – normal
ADC_LP_INT1	1	Low power control for analog INT1 1 – enter low power 0 – normal
ADC_LP_FLASH	0	Low power control for analog FLASH 1 – enter low power 0 – normal

4.11 Soft Reset

In ES7243, some internal registers can be used for soft reset. If the reset bit is set to 1, the device will be in standby mode and has minimum power consumption.

The following table shows the soft reset register definition.

REGISTER 0X06 – STATE CONTROL FOR CHIP, DEFAULT 0000 0000

Bit Name	Bit	Description
SP_TRI	7	Set SDOUT pad to 'Z' state 0 – '1' or '0' state 1 – 'Z' state
MCLK_DIS	6	disable mclk from pad 0 – enable 1 – disable
SEQ_DIS	5	0 – sequence enable 1 – sequence disable
RST_DIG	4	software reset for digital logic 0 – not reset 1 – Reset all digital logic except cp logic
RST_ADCDIG	3	software reset for digital logic 0 – not reset 1 – Reset adc logic(except cp, adc clock generate logic)
FORCE_CSM	2:0	force ADC state machine 100 – force csm_chip to PowDown 101 – force csm_chip to ChipIni 110 – force csm_chip to Normal 111 – force csm_chip to PowerUp 0xx – no force

4.12 MUTE and AUTO MUTE

ES7243 has mute control which can mute ADC output. When mute control is set to 1, ADC always outputs all 0 or 1. Also, ES7243 has auto mute feature. If auto mute is enabled, ES7243 detect the input level automatically. ADC will be mute if the input level is lower than the threshold within a long duration. User can decide the threshold level and duration time.

REGISTER 0X05 – MUTE CONTROL FOR ADC, DEFAULT 0001 0011

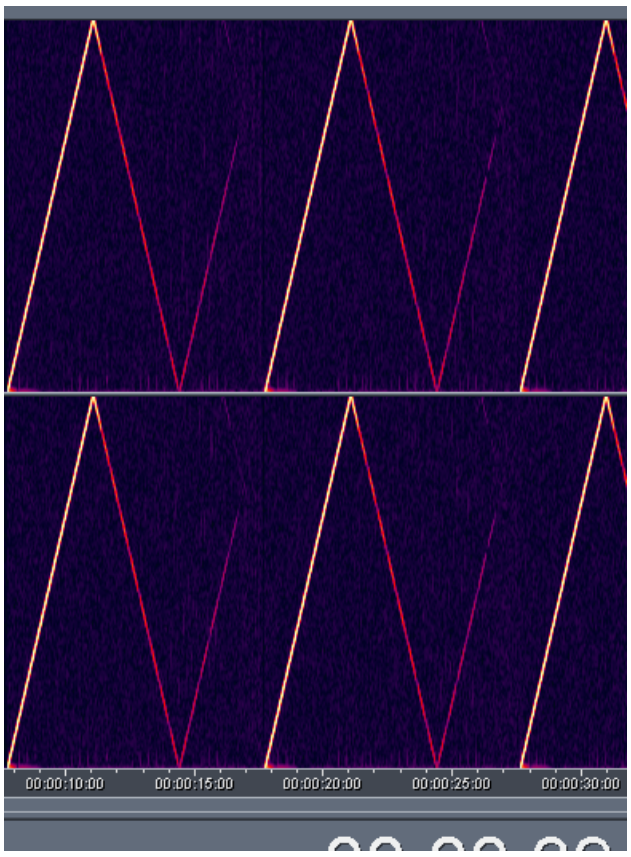
Bit Name	Bit	Description
Reserved	7:6	Reserved
AUTOMUTE_DETED	5	1 – chip is under mute state 0 – chip is under normal state
ADC_MUTE_SIZE	4	auto mute window size 0 – 4096 LRCK 1 – 8192 LRCK
ADC_SDP_MUTE	3	Software Mute Enable 0 – Disable software mute sdp output 1 – Enable software mute sdp output
ADC_NOISETHD	2:1	ADC auto mute noise gate 00 – -96dB 01 – -84dB(default) 10 – -72dB 11 – -60dB
ADC_AUTOMUTE	0	Auto-mute control 0 – Auto-mute enable 1 – Auto-mute disable

5 Effect of Anti-Aliasing Filter

Usually, the bandwidth of audio ADC is lower than FS/2, where FS is sample rate. The signal whose spectrum is higher than FS/2 is not interested by ADC. So there need a low-pass filter to restrict the bandwidth of a signal to approximately or completely satisfy the sampling theorem over the band of interest. This low-pass filter is also named by anti-aliasing filter.

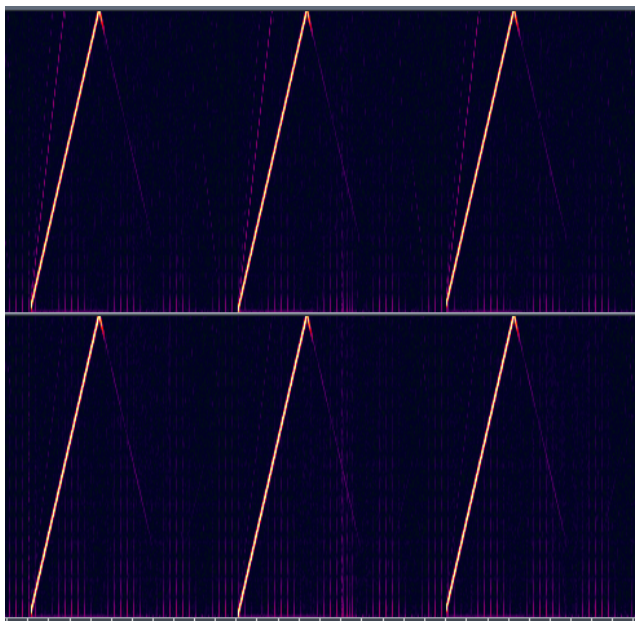
5.1 The ADC with a improper anti-aliasing filter

Some audio ADC doesn't have a proper anti-aliasing filter, so that the out band noise always exists in the output spectrum of ADC. For example, if an audio ADC is working in 16kHz sample rate, it's bandwidth is lower than 8kHz. So the voice which spectrum is higher than 8kHz is not interested by ADC. If this ADC doesn't have a proper anti-aliasing filter, this high frequency voice will have obvious influence on the output spectrum of ADC. Below picture shows the output spectrum of this type of ADC, where LRCK is 16kHz and the signal range from 20Hz to 20kHz. Such ADC can't be used in microphone array for voice recognition.



5.2 ES7243 with a proper anti-aliasing filter

Some audio ADC, such as ES7243, has a proper anti-aliasing filter, so that the signal bandwidth is restricted to completely satisfy the sampling theorem. The out band voice doesn't have influence on the output spectrum of ADC. So ES7243 is ideal for microphone array application. Below picture shows the output spectrum of ES7243, where LRCK is 16kHz and the signal range from 20Hz to 20kHz.



Please verify the effect of anti-aliasing filter before using it in microphone array.

6 Register Configuration for ES7243

The Register configuration includes ADC start up, ADC Standby and ADC Cascading mode, etc.

6.1 The Sequence for Startup – slave mode

```
WriteReg(0x00, 0x01);    //slave mode, software mode
WriteReg(0x06, 0x00);
WriteReg(0x05, 0x1B);    //Mute ADC
WriteReg(0x01, 0x0C);    //i2s -16bit
WriteReg(0x08, 0x43);    //enable AIN, PGA GAIN = 27DB
WriteReg(0x05, 0x13);    //un Mute ADC
```

6.2 The Sequence for Startup – master mode

```
WriteReg(0x00, 0x03);    //master mode, software mode, single speed mode, mclk div = 1
WriteReg(0x05, 0x1B);    //Mute ADC
WriteReg(0x06 0x10);    //RESET ADC
WriteReg(0x01, 0x0C);    //i2s -16bit
WriteReg(0x02, 0x10);    //MCLK / LRCK = 256
WriteReg(0x03, 0x04);    //MCLK / BCLK = 4
WriteReg(0x04, 0x02);    //CLK_ADC_DIV=2
WriteReg(0x0D, 0Xa0);    //CSM in normal mode, OSR = 32
WriteReg(0x08, 0x43);    //enable AIN, PGA GAIN = 27DB
WriteReg(0x06 0x00);    //UN RESET ADC
WriteReg(0x05, 0x13);    //un Mute ADC
```

6.3 The sequence for Cascading mode (slave mode)

```
WriteReg(0x00, 0x01);    //slave mode, software mode
WriteReg(0x06, 0x00);
WriteReg(0x05, 0x1B);    //Mute ADC
WriteReg(0x01, 0x8F);    //DSP-A, TDM ENABLE
WriteReg(0x08, 0x43);    //enable AIN, PGA GAIN = 27DB
WriteReg(0x05, 0x13);    //un Mute ADC
```

6.4 The sequence for Standby mode

```
WriteReg(0x06, 0x05);
WriteReg(0x05, 0x1B);
WriteReg(0x06, 0x5C);
WriteReg(0x07, 0x3F);
WriteReg(0x08 0x4B);
WriteReg(0x09 0x9F);
```