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### Development of Direct and Inverse Coupled Inductors for a Four-Phase Interleaved Boost Converter for Fuel Cell Vehicle Applications

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By

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**Bucharest, September 2025.**

**Quodus Ayinde Aromose.**

**Signature:** \_\_\_\_\_

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# Abstract

This master's thesis addresses critical challenges in fuel cell electric vehicle (FCEV) powertrains by developing advanced magnetic coupling solutions for high-efficiency DC-DC power converter. The contribution of the transport sector to greenhouse gas emissions necessitates the adoption of clean energy technologies, with FCEVs representing a promising solution that requires optimized power electronic interfaces to achieve commercial viability.

The primary objective is to design, model, implement and experimentally validate direct- and inverse-coupled inductors for a four-phase interleaved boost converter (4PIBC) for fuel cell vehicle applications. The work encompasses comprehensive electrical and magnetic modeling, simulation-based validation, detailed design of magnetic components, and experimental testing using real-time control strategies.

This research employs a systematic approach that combines analytical modeling, numerical simulation using MATLAB/Simulink and PLECS software, finite element analysis (FEMM) and experimental validation. The methodology includes small-signal linearization for control design, comprehensive loss modeling for switching devices and magnetic components, thermal analysis, and practical prototype construction using commercially available EE-type ferrite cores with custom Litz wire windings.

The investigation demonstrates that inverse coupled inductors in a cascade-cyclic 4PIBC topology achieve a remarkable input current ripple reduction from 21.4% (uncoupled configuration) to 1.6%, representing a 92.5% improvement. The developed sliding mode control (SMC) strategy significantly outperforms conventional PI control, reducing voltage overshoot from 13% to 0.8% and settling time from 2ms to 0.8ms, while maintaining 97% system efficiency. The magnetic design optimization enables a 52% reduction in total core volume when transitioning from two-phase to four-phase configurations, substantially improving power density.

A comprehensive design methodology is established for EE-type ferrite cores (3C92 material) with optimized air-gap placement achieving a coupling coefficient of  $k \approx -1/3$ . This work demonstrates successful integration of Silicon Carbide (SiC) MOSFET and Schottky diode technology, with detailed thermal analysis confirming safe operation with junction temperatures well below device limits (91°C for MOSFET, 70°C for diode vs. 175°C maximum).

Physical prototypes were constructed using E56/24/19 cores for 2PIBC and E42/21/15 cores for 4PIBC configurations, with custom twisted Litz wire assemblies (20 strands of 0.5mm diameter) to minimize high-frequency losses. Despite hardware limitations with the dSPACE 1104 platform, experimental validation using a buck converter test bench confirmed the magnetic design accuracy, with measured inductance values closely matching theoretical predictions. The design methodology and validated models facilitate technology transfer to industrial applications, supporting the broader adoption of hydrogen-based transportation solutions and accelerating the transition to sustainable mobility.

In conclusion, this thesis successfully demonstrates that properly designed inverse coupled inductors in multiphase interleaved boost converters can significantly enhance the performance of fuel cell vehicle powertrains. The combination of advanced magnetic design, wide-bandgap semiconductor technology, and robust control strategies achieves the efficiency, compactness, and reliability required for commercial FCEV applications, while providing a scalable foundation for future high-power automotive and stationary fuel cell systems.

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# List of Acronyms

**2PIBC** two-phase interleaved boost converter.

**2PIBC-CI** two-phase interleaved boost converter with coupled inductor.

**2PIBC-ICI** two-phase interleaved boost converter with inversely coupled inductor.

**4PIBC** four-phase interleaved boost converter.

**4PIBC-ICI** four-phase interleaved boost converter with inversely coupled inductor.

**ADC** Analog-to-Digital Converter.

**AFC** Alkaline Fuel Cell.

**APU** Auxiliary Power Unit.

**CCM** Continuous Conduction Mode.

**CCP** Combined Cycle Power.

**CHP** Combined Heat and Power.

**DAC** Digital-to-Analog Converter.

**DC** Direct Current.

**DC-DC** Direct-Current-to-Direct-Current.

**DMFC** Direct Methanol Fuel Cell.

**EMI** Electromagnetic Interference.

**EU** European Union.

**EV** Electric Vehicle.

**FC** Fuel Cell.

**FCEV** Fuel Cell Electric Vehicle.

**FEMM** Finite-Element Method Magnetics.

**IBC** Interleaved Boost Converter.

**ICE** Internal Combustion Engine.

**MCFC** Molten Carbonate Fuel Cell.

**MMF** Magneto-Motive Force.

**PAFC** Phosphoric Acid Fuel Cell.

**PEMFC** Polymer Electrolyte Membrane Fuel Cell.

**PI** Proportional–Integral controller.

**PLECS** Piecewise-Linear Electrical Circuit Simulation (software).

**PWM** Pulse-Width Modulation.

**SBO** Slave Bit Output.

**SMC** Sliding Mode Control.

**SMPS** Switched-Mode Power Supply.

**SOFC** Solid Oxide Fuel Cell.

# Chapter 1

## Introduction

### 1.1 Background of the Study

The transport sector plays an essential role in the economy and daily life; however, it is also a major contributor to environmental challenges [5]. In particular, it accounts for nearly a quarter of the European Union (EU) total greenhouse gas emissions. Unlike other major economic sectors, transport emissions have continued to increase since 1990, making it the only sector with a persistent upward trend [5] [6]. This ongoing increase in emissions poses a significant threat to both environmental sustainability and human health.

One of the main methods proposed to reduce greenhouse gas emissions in the transport sector is the use of Electric Vehicles (EVs), which uses low carbon-based electricity generation [7]. Among these is Fuel Cell Electric Vehicle (FCEV), which is based on Fuel Cell (FC) technology as its backbone. FCEVs, unlike conventional Internal Combustion Engine (ICE) cars, use hydrogen fuel cells to produce electricity with water as the only by-product that significantly reduces environmental impacts compared to ICE vehicles [8] [9].

FCEVs possess several important advantages, including reduced refueling time, longer driving range, and rapid refueling capability, which collectively mitigate some limitations of battery EVs [10][11]. FCEVs can also easily embrace renewable energy systems through the use of surplus renewable electricity to produce hydrogen through water electrolysis, enhancing grid flexibility and enabling sustainable energy use [8]. Recent market projections indicate high growth potential, with the worldwide FCEV market estimated to reach around 582,400 vehicles by 2030 [12].

However, despite all these advantages, the mass introduction of FCEVs faces several technical and economic challenges. Among them is the challenge of achieving efficient, compact and reliable Direct-

Current-to-Direct-Current (DC-DC) converters, particularly Interleaved Boost Converters (IBCs) for interfacing FCs with automotive powertrains [13]. IBCs play a crucial role in increasing the voltage produced by FCs to high levels of necessary Direct Current (DC) bus voltages with low current ripple and improved efficiency. It is highly needed to ensure the reliability and performance of the converters in various operating conditions and potential fault modes for the successful commercialization of FCEVs [4] [14].

In order to fulfill these demands, this thesis aims at optimizing the design of inductors (directly coupled and inversely coupled) in a four-phase interleaved boost converter (4PIBC) topology for FCEV applications. The use of coupled inductors provides numerous advantages, such as increased power density, smaller magnetic component sizes, higher efficiency, and improved fault tolerance facilitated by robust control strategies.

This project is part of a larger project that is dedicated to creating an experimental test bench for the purpose of testing fault detection and management algorithms, including open-circuit and short-circuit fault conditions, in multiphase DC-DC converters. The test bench that is to be developed shall include cyclic-cascade topologies of directly coupled and inversely coupled inductors, thereby facilitating in-depth experimental testing and performance evaluation under real operating conditions.

## 1.2 Problem Statement

Despite the growing prospects of FCEVs, issues related to the power-electronic interface remain significant challenges. Existing boost converters have significant drawbacks, such as bulky size, limited efficiency, high ripple current, and low fault tolerance. Hence, it is necessary to create advanced magnetic coupling solutions, i.e., direct and inverse coupled inductors for multiphase IBCs, to address these limitations. Furthermore, careful modeling, simulation, and experimental validation of such inductors are required to guarantee reliability, fault tolerance, and optimal performance under real operating conditions.

## 1.3 Objectives of the Thesis

The primary goal of this thesis is to design, model, implement, and experimentally validate direct and inverse coupled inductors for use in 4PIBC specifically tailored to FC vehicle applications. To achieve this, the specific missions of this thesis are as follows.

- Model direct and inverse coupled inductors from both electrical and magnetic perspectives.
- Validate developed models using numerical simulations (Matlab/PLECS software).
- Model magnetic and electrical losses accurately and validate the corresponding thermal models.
- Perform detailed design and realization of coupled inductors considering commercially available components.
- Experimentally test prototypes of direct and inverse coupled inductors using a two-phase interleaved boost converter (2PIBC) test bench integrated with closed-loop control implemented via dSPACE 1104 controller board.

## 1.4 Methodology

This research employs an extensive methodology that involves the following:

- **Analytical Modeling:** Develop comprehensive mathematical models describing electrical and magnetic behaviors of direct and inverse coupled inductors.
- **Simulation-Based Validation:** Employ numerical simulations in MATLAB and PLECS to refine theoretical models and predict system performance in various operational scenarios.
- **Loss and Thermal Analysis:** Analyze magnetic and electrical losses within inductors and validate thermal behaviors to ensure operational reliability.
- **Hardware Implementation:** Design and manufacture physical prototypes of coupled inductors, carefully selecting materials and components based on availability and practical applicability.
- **Experimental Validation:** Conduct rigorous testing of inductors developed at the laboratory level IBC system, employing real-time control strategies on a dSPACE 1104 platform.

## 1.5 Significance of the Study

This research has an essential impact on the development of FCEV technology by advancing the reliability, efficiency, and fault tolerance of the electronic building blocks of the main power. The

new design of direct and inverse coupled inductors addresses current industry issues and provides fundamental understanding of converter optimization, fault detection, and management, thus paving the way for a more extensive application of hydrogen-based transport solutions and accelerating the transition to sustainable mobility.

## 1.6 Thesis Structure

The remaining sections of this thesis are structured as outlined below.

- **Chapter 2 - Theoretical framework:** This chapter outlines fundamental principles and necessary explanations relevant to FC systems, IBCs, and coupled inductors. Describes key topics and foundational principles in order to better prepare for the following modeling and design tasks.
- **Chapter 3 - Modeling and Simulation of Coupled Inductors:** This chapter provides detailed modeling of direct and inverse coupled inductors from both electrical and magnetic perspectives, Modeling of magnetic and electrical losses and, It provides simulation results and analysis performed using MATLAB and PLECS to verify theoretical models.
- **Chapter 4 - Design and Implementation:** The practical design considerations are discussed here, including selection criteria for magnetic cores, winding configurations, wire sizing, and available market components. The chapter also offers a detailed discussion of the development and prototype fabrication of direct and inverse coupled inductors.
- **Chapter 5 - Experimental Validation:** This chapter outlines the experimental setup, procedure, and results related to a test bench of a IBC using closed-loop control through dSPACE 1104 controller board. The performance, efficiency, thermal characteristics, and operational reliability of the system are evaluated.
- **Chapter 6 - Conclusions and recommendations:** Summarizes the main findings of the thesis, identifies any limitations encountered, and suggests potential improvements or areas for future research.

# Chapter 2

## Theoretical Framework

This chapter presents an in-depth study of the basic principles and key concepts relevant to the understanding of fuel cell systems, IBCs, and coupled inductors. The explanations given aim to create a strong platform required for the modeling, design, and experimental verification of coupled inductors to be used in FCEVs.

### 2.1 Fuel Cell Systems

Fuel cells are electrochemical devices that convert chemical energy directly into electrical energy via redox reactions (oxidation-reduction reaction) that typically use hydrogen as fuel. Unlike ICE processes, fuel cells operate at high efficiency and produce only water and heat as by-products, making them environmentally friendly [15][16][1].

In automotive applications, most of the FCs operate at low ranges of voltages (from 0.6 to 1.2 volts per cell), thus necessitating high-power condition systems for fulfilling the high-voltage needs of EVs' traction systems [17].

The main characteristics of FCs are stable current output which depends on the level of voltages based on load characteristics, making them highly adaptable for connection to boost converters, which are effective in meeting voltage increase needs [18].

Different FC systems are utilized on the basis of particular uses. The classification is essentially determined by the nature of the electrolyte, which in turn determines the operating temperature, efficiency, fuel flexibility, and the corresponding areas of application [19]. The primary FC categories include the following.

**Polymer Electrolyte Membrane Fuel Cells (PEMFCs):** Also called proton exchange membrane

fuel cells (PEMFCs) operate in a temperature range of 60–100°C, these systems have a solid polymer membrane as their electrolyte [1][19]. They have a high power density, rapid start-up, and are well suited for transportation and portable applications. However, they require high-purity hydrogen and platinum-based catalysts [1][19][20].

**Alkaline Fuel Cells (AFCs):** Use an alkaline electrolyte, usually potassium hydroxide, that allows high efficiency and rapid start-up [1]. Conventionally used in space applications, AFCs show a sensitivity to carbon dioxide contamination ( $CO_2$ ), thus limiting their useful applications [1][20].

**Phosphoric Acid Fuel Cells (PAFCs):** Use liquid phosphoric acid as an electrolyte while operating at moderate temperatures of 150–200°C [1]. These systems are long-lasting, have tolerance to fuel impurities, and are used mainly for stationary power generation [1][20][21].

**Molten Carbonate Fuel Cells (MCFCs):** Use molten carbonate salts as an electrolyte and function at high temperatures between 600–700°C [19]. MCFCs can use a variety of fuel sources and are particularly applicable to large stationary power uses [19][20].

**Solid Oxide Fuel Cells (SOFCs):** Uses a solid ceramic electrolyte and operates at very high temperatures 500–1000°C [19]. SOFCs offer high efficiency and fuel flexibility, making them attractive for stationary and auxiliary power applications [19][20].

**Direct Methanol Fuel Cells (DMFCs):** Similar to PEMFCs, but using methanol directly as fuel [19]. They are mainly used in portable and small-scale applications due to their ease of fuel handling [19][20].

Table 2.1: Comparison of major fuel cell types, their electrolytes, operating temperatures, efficiency ranges, and primary applications

Type	Electrolyte	Temperature (°C)	Efficiency (%)	Applications
PEMFC	Solid Polymer Membrane	60–100	Up to 60	Transportation, backup/portable power
AFC	Alkaline (e.g., KOH)	23–70	60–70	Space, Military, submarines
PAFC	Phosphoric acid	150–200	40–50	Stationary CHP (200-400 kW), distributed generation
MCFC	Molten carbonate	600–700	45–55	Large stationary CHP/CCP (MW scale), industrial power
SOFC	Solid oxide (ceramic)	500–1000	45–60	Stationary CHP/CCP (kW-MW), APUs, large-scale power
DMFC	Polymer electrolyte membrane	50–120	30–40	Portable electronics, consumer devices

PEMFCs are the dominant technology used in FCEVs and are the main focus of research and

application in the automotive industry [1][22]. Their high power density, low operating temperature, fast start-up time, and versatility make them extremely suitable for transportation applications where considerations such as quick responsiveness, compactness, and efficiency are of major significance. Therefore, understanding the working principles of PEMFCs is critical in the successful modeling, design, and optimization of power electronics and energy management systems in FCEVs [23].

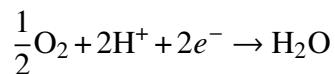
### 2.1.1 Working Principle of PEMFCs

A PEMFC generates electricity from the electrochemical reaction between hydrogen and oxygen to form water and release heat as by-products [1]. The process involves:

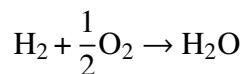
- **reaction at Anode:**



- **reaction at Cathode :**



- **Overall reaction:**



The hydrogen supplied to the anode is dissociated into electrons and protons by a platinum catalyst. Protons move towards the cathode via the polymer membrane, while electrons move via an external circuit, thus creating electric current. In the cathode, protons, electrons and oxygen react to form water [1][20].

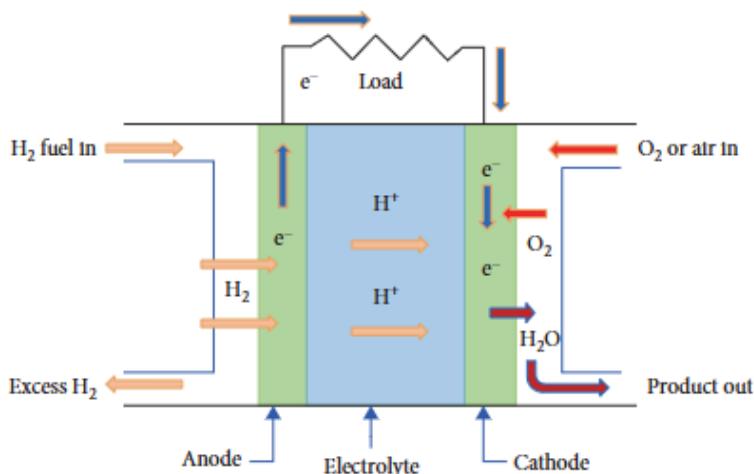


Figure 2.1: Schematic of a PEMFC illustrating the flow of reactants, products, and the generation of electricity [1].

## 2.2 DC-DC Boost Converter Fundamentals

### 2.2.1 Basic Boost Converter Operation

A boost or step-up converter is a DC-DC converter that increases the output voltage and decreases the output current from the input side to the output side [2]. This simple power electronics circuit is the foundation for the application of a step-up in voltage and is the parent for more complex interleaved topologies. The boost converter is included in the Switched-Mode Power Supply (SMPS) family that contains at least two semiconducting devices (transistor and diode) and at least an energy-storing component (capacitor, inductor, or inductor and capacitor in series or inductively coupled together) [2]

One fundamental operation for the boost converter is the requirement for an inductor to oppose changes in the current by increasing or decreasing the energy within the inductor magnetic field [2]. In terms of comparison with buck converters, the boost converter functions with a continuous input current, which is easy to filter and reduces the requirements of Electromagnetic Interference (EMI) [24].

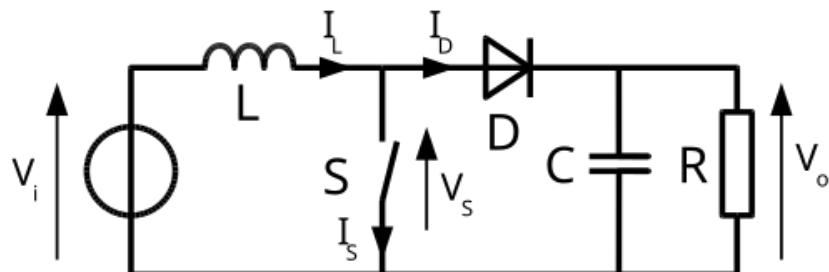


Figure 2.2: circuit diagram of a boost converter [2].

Another characteristic of the boost topology is the location of the inductor at the input side with the guarantee for constant input current flow in comparison with the discontinuous input current mode for the buck and the buck-boost topologies.

### 2.2.2 Modes of Operation

There are two switching states for the boost converter for every switching time interval [25]:

**Switch-ON State (Charging Phase):** The switch is closed in this state; the input voltage  $V_i$  appears across the inductor, causing the current through the inductor to increase linearly. The diode becomes reverse biased, preventing current flow to the output. The inductor current increase is

governed by:

$$\Delta I_L = \frac{V_i}{L} \cdot t_{on} \quad (2.1)$$

**Switch-OFF State (Discharging Phase):** This state is when the switch opens; the inductor's stored magnetic energy forces current to flow through the forward-biased diode toward the output capacitor and load. The collapsing magnetic field induces a voltage across the inductor with polarity opposite to the applied voltage, following Lenz's law. The inductor current decrease follows:

$$\Delta I_L = \frac{V_o - V_i}{L} \cdot t_{off} \quad (2.2)$$

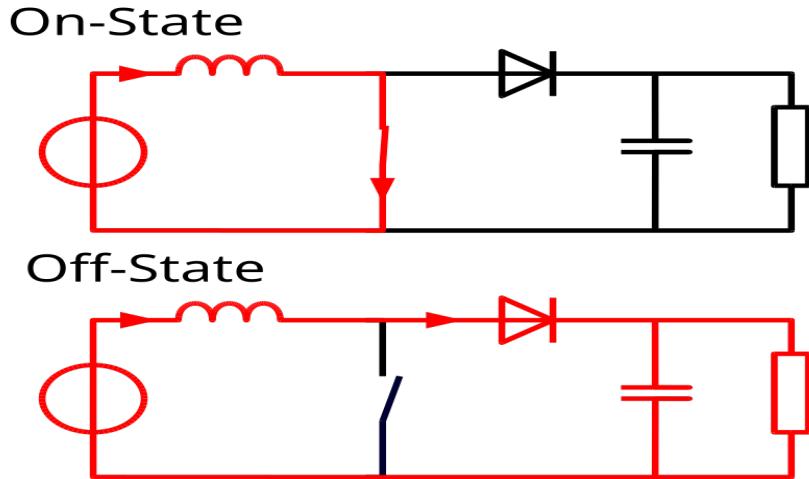


Figure 2.3: Current paths schematics of a boost converter, depending on the state of the switch S [2].

In steady-state operation, the net volt-seconds applied to the inductor over a complete switching cycle must be equal to zero [26].

During the ON period (DT):

$$v_L = V_i$$

During the OFF period ((1-D)T):

$$v_L = V_i - V_o$$

Applying volt-second balance:

$$D V_i T + (1 - D) (V_i - V_o) T = 0 \quad (2.3)$$

Simplifying and solving for the output voltage:

$$V_o = \frac{V_i}{1 - D} \quad (2.4)$$

where  $D$  represents the **duty cycle** (ratio of switch-ON time to total switching period). This fundamental relationship demonstrates that the output voltage is always greater than the input voltage for duty cycles between 0 and 1, with the voltage gain approaching infinity as  $D$  approaches unity.

## 2.3 Interleaved Boost Converters (IBCs)

Conventional boost converters, for example, single-phase boost converters, are very simple and reliable but suffer from some critical drawbacks in high-power applications due to increased current stress and larger component sizes, which compromise efficiency and system reliability [27]. To solve these challenges, an interleaving topology has emerged as a solution among which are multiphase topologies in general, and particularly the 4PIBC [4]

### 2.3.1 Fundamental Operation

IBCs have been widely applied in fuel cell systems due to their ability to increase the voltage output resulting from the low voltage DC provided in fuel cells at high voltage levels required in electric vehicle traction systems [18].

IBCs consist of  $n$  numbers of parallel boost converter modules, where each phase operates with a  $360^\circ/n$  phase shift. This kind of topology shares the input current among several phases, thus reducing the current stress of individual components and increasing the overall efficiency of the system [28].

An  $n$ -phase IBC has a time phase difference between phases ( $\Delta T$ ) given by:

$$\Delta T = \frac{T_s}{N} \quad (2.5)$$

where  $T_s$  is the switching period. This phase-shifted operation reduces input and output ripple currents. The ripple reduction factor ( $R_f$ ) for the  $N$  phases is approximately:

$$R_f = \frac{1}{N} \quad (2.6)$$

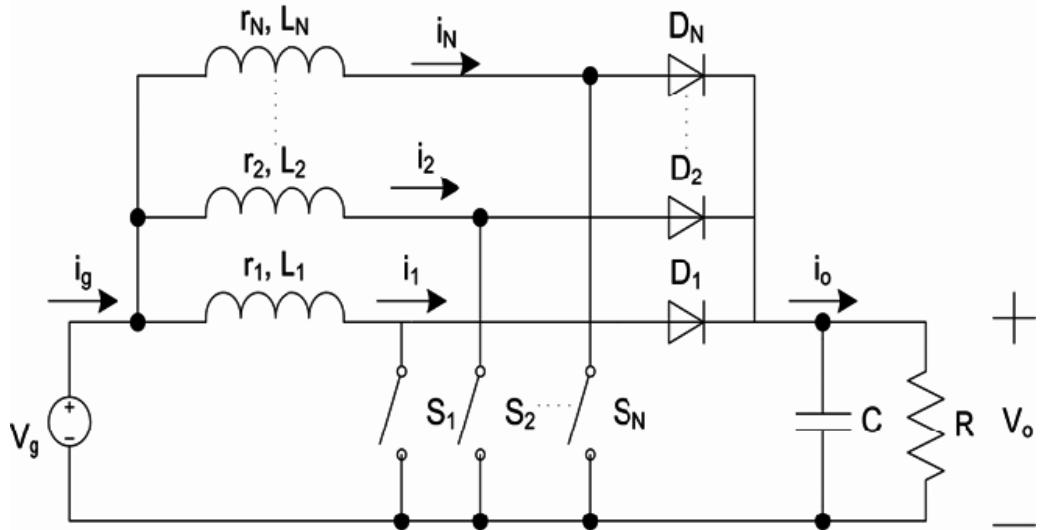


Figure 2.4:  $n$ -phase interleaved boost converter [3]

### 2.3.2 Four-Phase Interleaved Boost Converter (4PIBC)

The 4PIBC employs four identical boost stages, each shifted by  $90^\circ$  in their switching cycles. This configuration significantly reduces the ripple current through mutual cancelation, improving the converter's power quality, improving thermal management, and increasing the longevity of components [29].

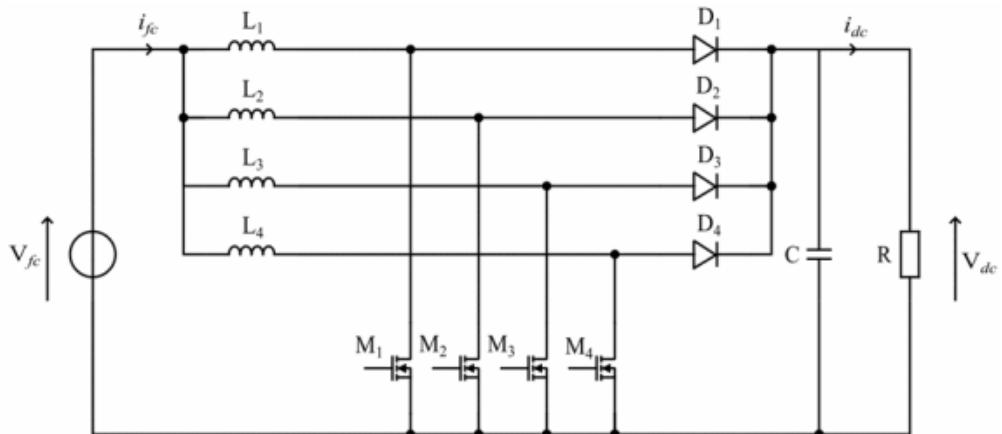


Figure 2.5: 4-phase interleaved boost converter [4]

The mathematical analysis of the 4PIBC system reveals that the input current ripple is significantly reduced compared to conventional single-phase designs. The ripple current in each phase is given by:

$$\Delta i_{fc} = \begin{cases} \frac{v_{dc}}{L f_s} \alpha (1 - 4\alpha), & 0 < \alpha \leq \frac{1}{4}, \\ \frac{v_{dc}}{L f_s} (2 - 4\alpha) \left( \alpha - \frac{1}{4} \right), & \frac{1}{4} < \alpha \leq \frac{1}{2}, \\ \frac{v_{dc}}{L f_s} (3 - 4\alpha) \left( \alpha - \frac{1}{2} \right), & \frac{1}{2} < \alpha \leq \frac{3}{4}, \\ \frac{v_{dc}}{L f_s} (4 - 4\alpha) \left( \alpha - \frac{3}{4} \right), & \frac{3}{4} < \alpha \leq 1. \end{cases} [30] \quad (2.7)$$

Here, the input voltage be represented by  $V_{dc}$ , the duty cycle by  $\alpha$ , switching frequency by  $f_s$ , and inductance by  $L$ . Due to operation in interleaved mode, the resulting input current ripple is highly reduced compared to the combined effects of each phase ripple, thanks to the phase cancellation phenomenon [4].

The power distribution across four phases enables the use of smaller magnetic components while maintaining overall system performance. Each phase processes approximately 25% of the total power, reducing the thermal stress on individual components and improving system reliability [31].

## 2.4 Coupled Inductors

### 2.4.1 Fundamental Principles

Coupled inductors represent a major breakthrough in the development of magnetic components designed for high-performance power conversion applications. These components consist of two or more inductors that share a common magnetic core, which enables higher energy efficiency, reduces physical size, and significantly enhances performance in the area of ripple current [32]. The operating principle of mutual inductance is ensured by the fact that current variations in one inductor create a voltage in adjacent inductors through the common magnetic flux [33].

The magnetic coupling between inductors is characterized by the mutual inductance  $M$ , which relates the flux linkage between windings. For two coupled inductors, the voltage equations are:

$$v_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}, \quad (2.8)$$

$$v_2 = L_2 \frac{di_2}{dt} + M \frac{di_1}{dt}, \quad (2.9)$$

where  $L_1$  and  $L_2$  are the self-inductances, and  $M$  is the mutual inductance. The coupling coefficient  $k$  quantifies the degree of magnetic coupling between inductors and is defined as [33]:

$$k = \frac{M}{\sqrt{L_1 L_2}}. \quad (2.10)$$

## 2.4.2 Coupling Methods and Configurations

Within the scope of power electronic applications two primary coupling methods are employed namely:

### Directly Coupled Inductors (Magnetic Fields Enhance)

When two windings of inductors carry currents in a parallel circuit around a common core, the resulting magnetic fields reinforce each other, and we conclude that the inductors are in direct coupling. In this case, the mutual inductance is taken as positive, and we often write:

$$M = +|M|.$$

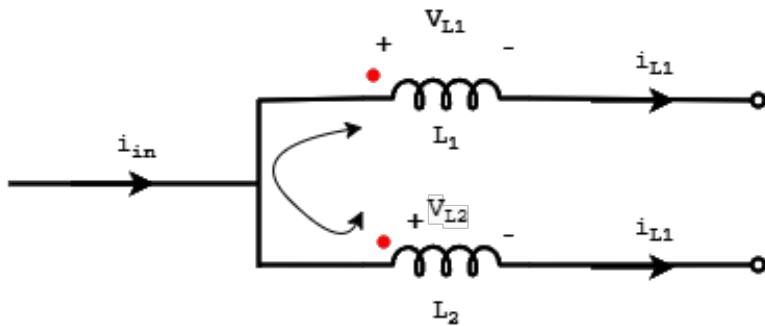


Figure 2.6: Directly coupled inductors.

If the currents are in opposite directions, the fields would oppose, giving a negative sign for  $M$ . This inductors are inversely coupled in this case. This configuration is particularly beneficial for applications requiring high energy density and compact form factors.

## Inversely Coupled Inductors (Magnetic Fields Oppose)

When two inductor currents flow in such a way that the currents oppose each other in a shared core, this configuration of inductors is called *inversely* (or *opposing*) coupled inductors. In such cases,

$$M = -|M|,$$

This means that the mutual flux subtracts from the self-flux. The inverse coupling configuration is especially advantageous in interleaved converter applications where ripple current minimization is paramount.

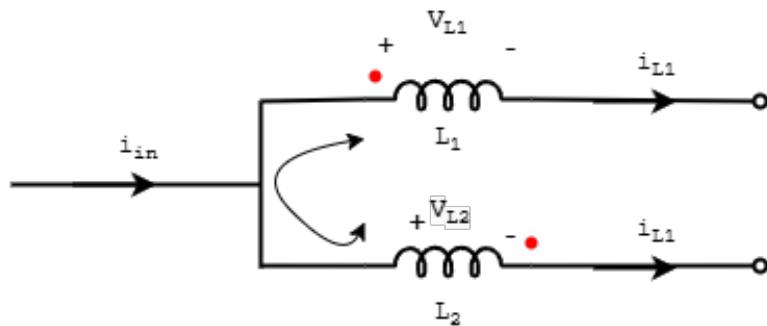


Figure 2.7: Inversely coupled inductors.

# Chapter 3

## Modeling and Simulation of Coupled Inductors

### 3.1 Electrical View of directly Coupled Inductors

From circuit theory, we have that the voltage across an inductor is given by:

$$V_L = L \frac{di_L}{dt} \quad (3.1)$$

According to equation 3.1, the voltage equations of two directly coupled inductors in Fig. 2.6 can be written as:

$$\begin{aligned} V_{L1} &= L_1 \frac{di_{L1}}{dt} + M_{21} \frac{di_{L2}}{dt}, \\ V_{L2} &= L_2 \frac{di_{L2}}{dt} + M_{12} \frac{di_{L1}}{dt}. \end{aligned} \quad (3.2)$$

Assuming that both windings are symmetrical,

$$L_1 = L_2 = L$$

$$M_{12} = M_{21} = M$$

Then,

$$\begin{aligned} V_{L1} &= L \frac{di_{L1}}{dt} + M \frac{di_{L2}}{dt}, \\ V_{L2} &= L \frac{di_{L2}}{dt} + M \frac{di_{L1}}{dt}. \end{aligned} \quad (3.3)$$

where,  $L$  is the self-inductance of the winding and  $M$  is the mutual inductance

## 3.2 Magnetic View of directly Coupled Inductors

The linkage of fluxes in a magnetic circuit can be described as:

$$\lambda = N\Phi \quad (3.4)$$

where  $N$  is the number of turns of the winding and  $\Phi$  is the flux.

The total flux linkages in each winding is the sum of self-flux and mutual-flux in the winding

$$\begin{aligned}\lambda_1 &= N_1(\Phi_1 + \Phi_{21}) \\ \lambda_2 &= N_2(\Phi_2 + \Phi_{12})\end{aligned} \quad (3.5)$$

where  $\Phi_1$  is the flux produced by winding 1,  $\Phi_2$  is the flux produced by winding 2 and  $\Phi_{xy}$  is the mutual flux. For *direct coupling*, both fluxes add in each winding (assuming currents flow so that fields reinforce).

The Magneto-Motive Force (MMF) is given by:

$$\text{MMF} = Ni, \quad (3.6)$$

and the flux in a simple reluctance model is

$$\Phi = \frac{\text{MMF}}{\mathcal{R}} = \frac{Ni}{\mathcal{R}}. \quad (3.7)$$

Hence, for each winding,

$$\Phi_1 = \frac{N_1 i_1}{\mathcal{R}}, \quad \Phi_2 = \frac{N_2 i_2}{\mathcal{R}}. \quad (3.8)$$

## 3.3 Electrical View of inversely Coupled Inductors

Again, the voltage equations remain the same as in equation 3.3. However,  $M$  takes a negative value because both of their fields oppose each other Fig.2.7.

so;

$$\begin{aligned} V_{L1} &= L_1 \frac{di_{L1}}{dt} - M_{21} \frac{di_{L2}}{dt}, \\ V_{L2} &= L_2 \frac{di_{L2}}{dt} - M_{12} \frac{di_{L1}}{dt}. \end{aligned} \quad (3.9)$$

Assuming that both windings are symmetric  $L_1 = L_2 = L$  and  $M_{12} = M_{21} = M$ , then

$$\begin{aligned} V_{L1} &= L \frac{di_{L1}}{dt} - M \frac{di_{L2}}{dt}, \\ V_{L2} &= L \frac{di_{L2}}{dt} - M \frac{di_{L1}}{dt}. \end{aligned} \quad (3.10)$$

### 3.4 Magnetic View of inversely Coupled Inductors

The flux linkages in opposing-coupling scenarios is:

$$\begin{aligned} \lambda_1 &= N_1(\Phi_1 - \Phi_{21}) \\ \lambda_2 &= N_2(\Phi_2 - \Phi_{12}) \end{aligned} \quad (3.11)$$

The net flux linkage in each winding may decrease if the fields oppose strongly.

### 3.5 Coupling Factor

A common way to express  $M$  is via the coupling factor  $k$ :

$$M = k \sqrt{L_1 L_2}, \quad 0 \leq k \leq 1. \quad (3.12)$$

Here,  $k = 1$  indicates the coupling *perfect* (no leakage flux), while  $k = 0$  means that the windings are completely uncoupled.

$$L_1 = L_2 = L$$

$$M = kL,$$

$k$  is always positive for the direct coupling and  $k$  is always negative for the inverse coupling.

### 3.6 Validation of Electrical Model of 2PIBC-ICI on PLECS

When designing and simulating a cascade-cyclic form coupled inductors for 4PIBC, it is important to follow a step-by-step validation procedure. The procedure involves the initial development and

testing of a relatively simpler 2PIBC with coupled inductors in Fig. 3.1 as a starting point to deal with complexity related to the four-phase architecture later. Such a step-by-step procedure is vital to tackle several technical considerations related to control design, magnetic coupling behavior, and global system stability.

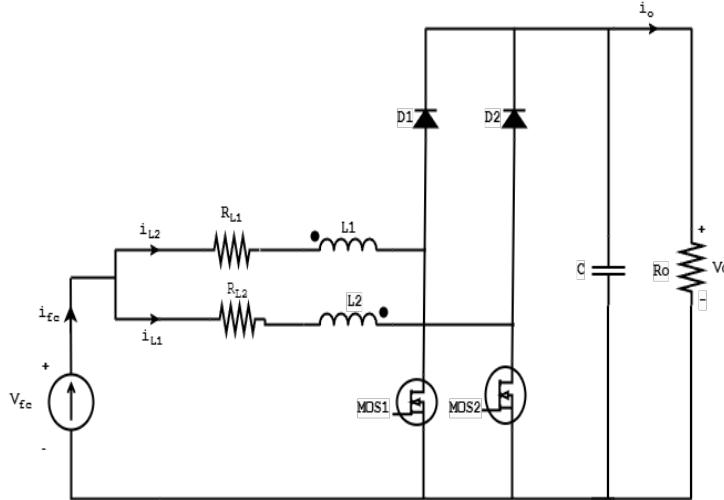


Figure 3.1: 2IBC-ICI Electrical Circuit.

The use of coupled inductors provides complex dynamical coupling between the phases that is important to reduce current ripple in the converter while affecting their electromagnetic behavior and their transient response. The study of a two-phase configuration provides ample scope to study coupling effects in detail and thus permit a detailed understanding of application of coupling factor and testing of magnetic behavior over different load and duty cycle conditions. This provides a good basis to move to a four-phase configuration with more sophisticated inter-phase interactions.

The analysis of an interleaved four-phase boost converter using cyclic-cascade coupled inductors is achieved by going through eight different modes per cycle due to a phase shift of  $T_s/4$  per switch among four switches. In contrast to this, a two-phase interleaved converter uses two switches with each undergoing a phase shift of  $T_s/2$ . This setup reduces the number of distinct conduction intervals within each switching period to four modes, down from eight:

1. **n°1 Mode:** Switch  $S_1$  ON,  $S_2$  OFF
2. **n°2 Mode:** Both  $S_1$  and  $S_2$  ON (overlap depends on  $d$ )
3. **n°3 Mode:** Switch  $S_1$  OFF,  $S_2$  ON
4. **n°4 Mode:** Both  $S_1$  and  $S_2$  OFF (again, depends on  $d$ )

Therefore, every stage operates with a phase shift of  $360^\circ/n$ , where  $n$  is the total number of phases.

The actual configuration and relationship between these modes depend on the duty cycle  $\alpha$ . For example, if  $\alpha < 0.5$ , both switches will be in the OFF state at some very small time period. In case  $\alpha > 0.5$ , both switches will be in the ON state in a very short time period.

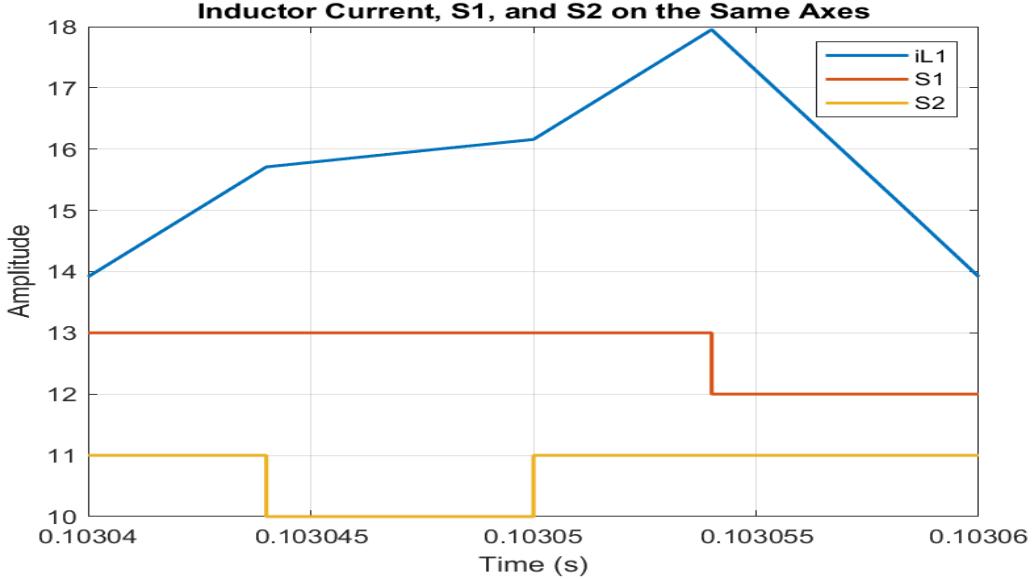


Figure 3.2: Waveform of  $i_{L1}$  and switch signal.

The waveform in Fig. 3.2 illustrates the behavior of the current through the inductor  $i_{L1}$  and the switching signals of switches  $S_1$  and  $S_2$  in the simulation of 2PIBC that uses coupled inductors, simulation clearly shows system behavior over a range of duty cycles  $\alpha$ . In our Simulation duty cycle  $\alpha > 0.5$  and that has a significant effect on the sequence and overlap of conduction modes.

We can observe from the waveform that switch  $S_1$  is ON for a longer time, while  $S_2$  turns ON for a portion of the active period of  $S_1$ . This observation confirms the existence of **n°2 Mode**, where both  $S_1$  and  $S_2$  are simultaneously turned ON because of the high duty cycle.

The rising slope of  $i_{L1}$  marks the active period of  $S_1$ , where energy is accumulated. The current peaks when both switches are turned ON, thus maximizing the magnetizing current via the coupling effect. After  $S_1$  is turned OFF while  $S_2$  is still conducting, the converter enters **n°3 Mode**, resulting in the decrease of inductor current while energy is being transferred to the load and the output capacitor. The following drop in  $i_{L1}$  marks the transition to **n°4 Mode**, which is where both switches are non-conducting or the end of the  $S_2$ 's conduction cycle.

### 3.6.1 Open Loop Simulation of 2PIBC-CI

The design of small-scale fuel cell converters with an output voltage of 48V and a power limitation of 500W effectively balances safety, efficiency, and usability requirements. The 48V voltage level

selection complies with low voltage safety standards to minimize the risk of electrical shock and is compatible with common industrial and residential backup systems. The chosen voltage level also enables conduction loss minimization and thermal stress reduction by reducing current flow compared to lower-voltage systems to allow economical and low-cost availability of power electronic components. The 500W power rating is suitable for small-scale applications such as micro-CHP, portable backup systems, and DC microgrids to allow compactness and cost-effectiveness. The 48V configuration is also consistent with the typical output range of stacks of PEMFC and supports seamless integration with standard 48V battery storage systems to provide stable DC bus operation and efficient integration of hybrid renewable energy systems.

Table 3.1: Conveter Specifications

Parameters	Value	Unit
Output Voltage ( $V_o$ )	48	V
Input Voltage ( $V_{fc}$ )	14.4	V
Output Power ( $P_{o,max}$ )	500	W
Switching Frequency $f_s$	50	kHz
Desired Efficiency ( $\eta$ )	97%	–
Tolerated Voltage Ripple ( $\Delta V_o$ )	$\leq 1\%$	–
Tolerated Current Ripple ( $\Delta I_{fc}$ )	$\leq 10\%$	–

To increase the input voltage of the fuel cell to the desired output voltage level, the specifications are presented in Table 3.1. The interleaved structure improves current ripple reduction and enhances system efficiency, making it well-suited for fuel cell applications. Given the two-phase configuration, the switches are operated with a phase shift  $180^\circ$ , ensuring that each phase conducts alternately, thus reducing the ripple of the input current and evenly distributing the thermal stress between the components. The converter model is developed and simulated in the Piecewise-Linear Electrical Circuit Simulation (software) (PLECS), with the simulation running up to  $t = 0.5$  s to observe the steady state behavior and dynamic performance of the system under the defined operating conditions.

The current of a coupled inductor in 2PIBC with a coupled inductor is shown in Fig. 3.3 while the simulation output voltage is shown in 3.4.

It is interesting to compare the input current ripple of the inductor in directly coupled, inversely coupled, and uncoupled inductors within a 2PIBC as each configuration highlights the impact of magnetic coupling on current ripple reduction and overall converter performance.

Based on the input current waveforms, the measured current ripple in the directly coupled inductor configuration is approximately 12% shown in Fig. 3.5, while the inversely coupled and uncoupled

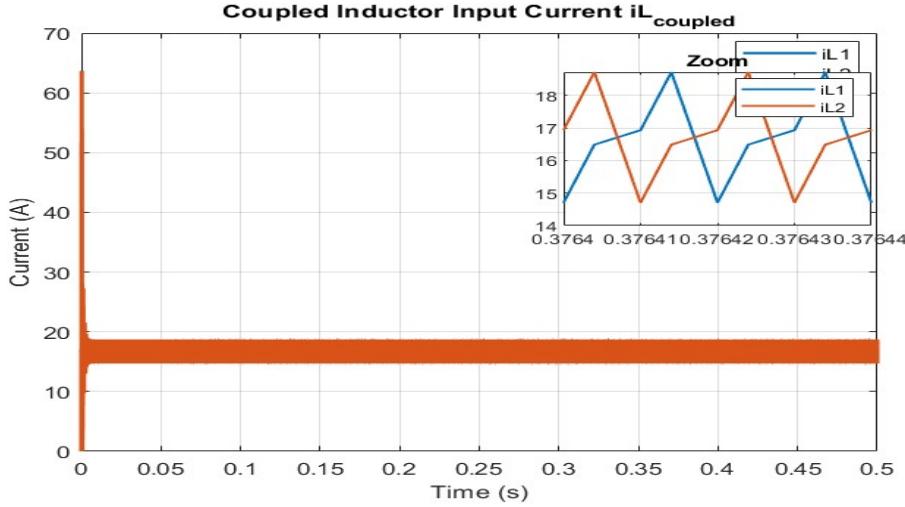


Figure 3.3: coupled inductor current in 2PIBC.

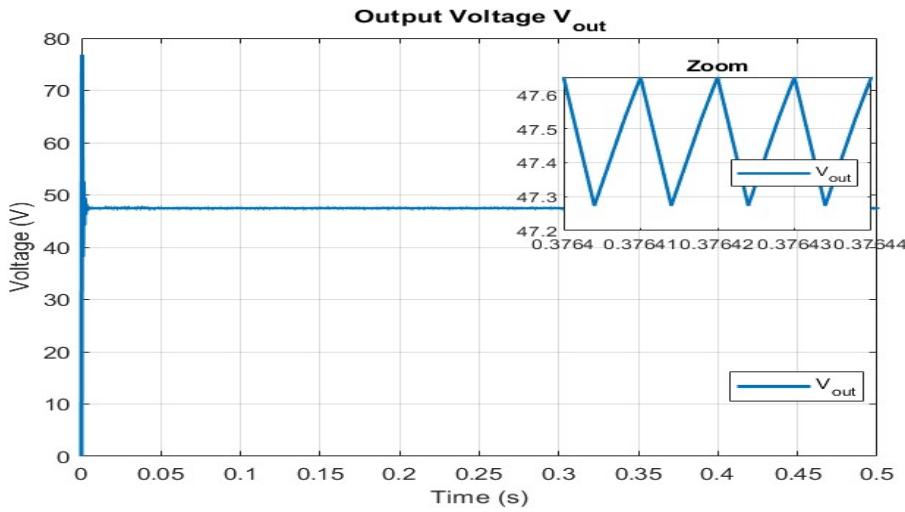


Figure 3.4: 2PIBC output voltage.

inductors configurations are 10.7% ripple illustrated in Fig. 3.6 and Fig. 3.7. However, because uncoupled inductors operate independently, the total ripple across two phases effectively adds up to around 21.4%, demonstrating their limitation in ripple cancelation.

Direct coupling allows very little ripple cancellation between phases through magnetic coupling, which in turn reduces input ripple stress and eases the loads on capacitors and other components, leading to an overall improvement in efficiency. However, this configuration does increase the vulnerability to core saturation from cumulative magnetic flux under high-load conditions, requiring careful core sizing and material selection. Though core losses can see a small increase due to increased flux density, direct coupling offers good load sharing and a more uniform transient response, making it beneficial in applications involving multi-phase scaling where ripple management is effectively important.

Consequently, the inversely coupled topologies achieve a minimum per-phase ripple of 10.7%

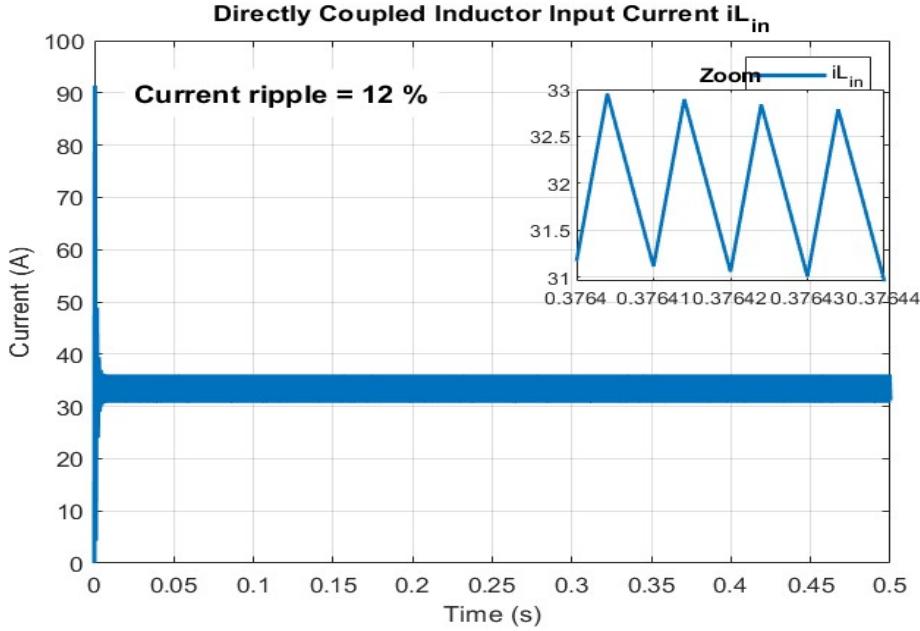


Figure 3.5: inductor input current in 2PIBC-Directly Coupled Inductor.

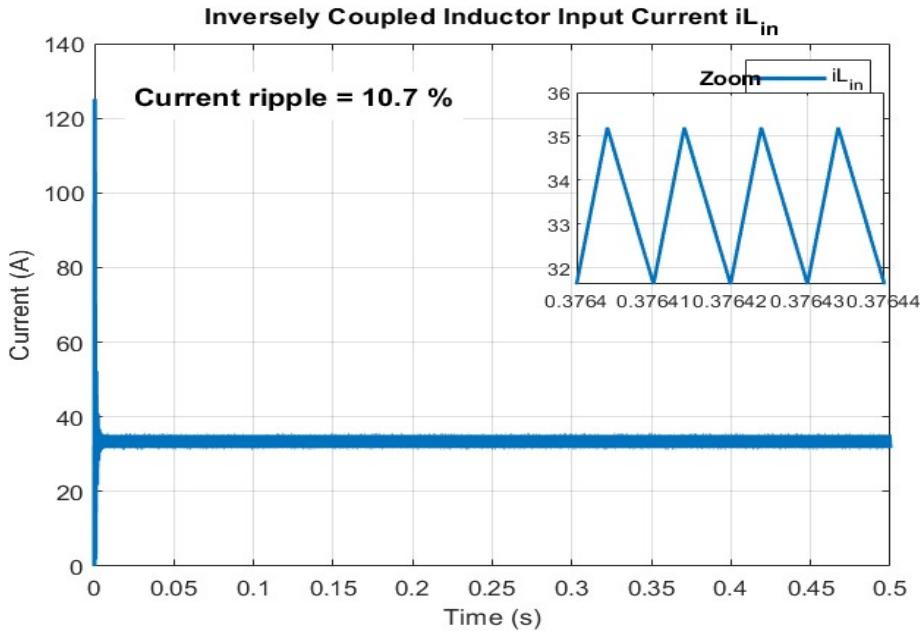


Figure 3.6: inductor input current in 2PIBC-Inversely Coupled Inductor.

due to destructive magnetic coupling that also enhances ripple effect cancelation. The opposing magnetic forces reduce the overall core flux, hence reducing saturation occurrence and allowing smaller magnetic parts with low core loss and improved thermal capability. In addition, this topological design ensures balanced load distribution and fast transient response, which make it particularly well suited to high-power multiphase applications that demand good ripple suppression.

Meanwhile, the uncoupled configuration lacks magnetic interaction, forcing each inductor to handle the phase current independently. Consequently, the ripple adds up to 21.4%, much higher than coupled designs. Although it avoids saturation risk and simplifies the design, it demands

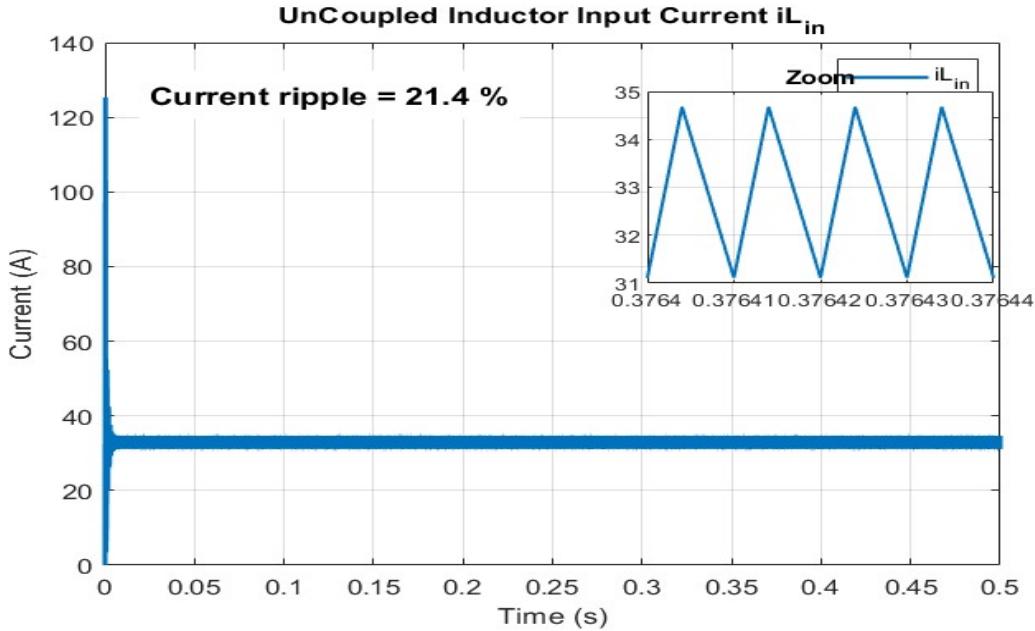


Figure 3.7: inductor input current in 2PIBC-Uncoupled Inductor.

larger inductors, increasing the size and weight of the system. Furthermore, poor load sharing and slower transient response limit its suitability for multiphase applications where ripple and dynamic performance are critical.

The table below gives the comparison of uncoupled, directly coupled, and inversely coupled inductors in 2PIBC

Table 3.2: Comparison of Coupling Types in 2PIBC

Parameter	Uncoupled	Directly Coupled	Inversely Coupled
Input Current Ripple	High (21.4%)	Moderate (12%)	Low (10.7%)
Core Saturation Risk	Low	High	Low
Core Losses	High	Moderate	Low
Load Sharing	Poor	Moderate	Excellent
Size	Large	Moderate	Small
Transient Response	Fast but noisy	Fast	Fast & stable
Best for Multi-Phase?	No	No	Yes

## 3.7 Two-Phase Coupled-Inductor Converter Controller

To maintain a stable, regulated output in varying loads, a robust digital controller is required for two-phase interleaved boost converter with coupled inductor (2PIBC-CI). The coupled-inductor structure introduces complex dynamics due to magnetic coupling, so the controller must handle non-linearities and provide good transient response.

The design uses a conventional feedback architecture (Fig. 3.8). The measured output voltage,

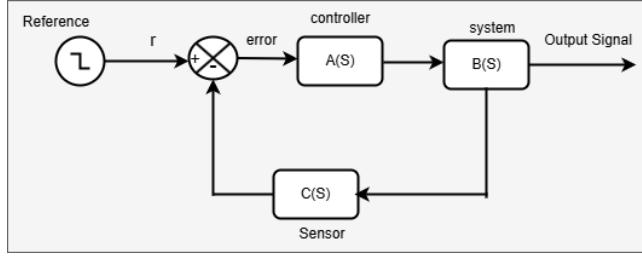


Figure 3.8: Close-Loop Control block diagram.

obtained via the transfer function  $B(s)$ , is compared to the reference  $r$ ; the resulting error is regulated by  $A(s)$ , typically a Proportional–Integral controller (PI), to ensure zero steady state error and improved stability.

The controller adjusts the duty cycle of the converter to minimize error and regulate the output voltage. The sensor block  $C(s)$  continuously measures the output and feeds the comparator, so the closed loop reacts to changes in load and input while maintaining the target voltage.

The design accounts for coupled-inductor dynamics, enabling optimal two-phase operation with balanced current sharing and reduced ripple. The proposed controller stabilizes the output and maximizes performance through fast transients and minimized EMI, which is crucial for reliable operation.

From the block diagram Fig. 3.8, the closed-loop gain is as follows.

$$G(s) = \frac{A(s)B(s)}{1 + A(s)B(s)C(s)}. \quad (3.13)$$

The reference must include the sensor gain  $C(s)$ . Design specifications typically require unity steady-state gain,

$$G(s) = 1, \quad (3.14)$$

so with  $B(s)$  and  $C(s)$  fixed,  $A(s)$  is chosen to satisfy (3.14).

Given the interleaved structure, dual-loop PI control is selected to ensure balanced current sharing while improving dynamics and stability.

The controller uses a cascaded outer-voltage/inner-current scheme. The measured output is compared with a reference; the outer loop generates the inductor current reference. This is compared to the average inductor current, and the inner current controller sets the duty cycle to drive the switches. This structure improves current regulation, reduces ripple, and ensures accurate voltage control (Fig. 3.9).

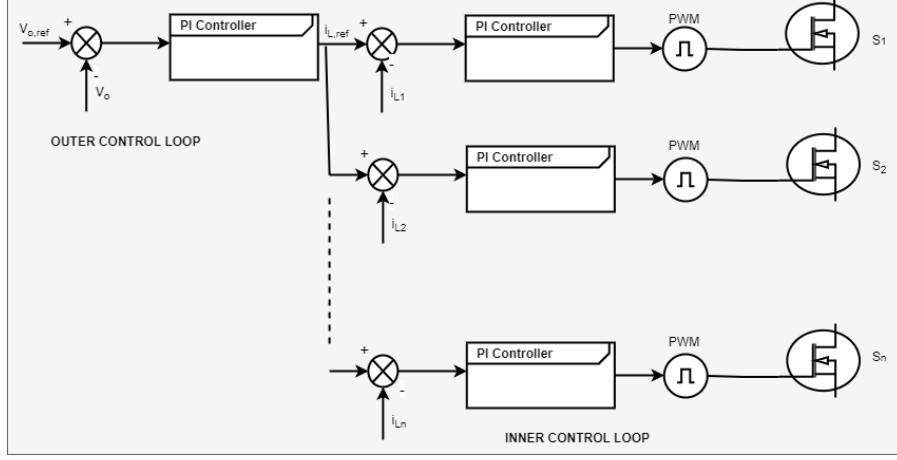


Figure 3.9: Dual-loop PI control.

### 3.7.1 Small Signal Modelling of 2PIBC

The small-signal modeling follows Barry et al. [34], who analyzed coupled-inductor boost converters in CCM and DCM.

Designing a PI controller for a IBC requires a clear understanding of the dynamic behavior of the system, which is highly nonlinear due to switching actions and coupled inductor effects. To simplify this complexity, a small signal model is essential as it linearizes the converter around its steady-state operating point, allowing the derivation of a transfer function that accurately represents the dynamics of the system.

We analyze the equivalent circuit of the 2PIBC-CI (Fig. 3.1) under:

$$\begin{aligned} i_{L1} &= i_{L2}, & L_{k1} &= L_{k2} = L_k, \\ \alpha_{c1} &= \alpha_{c2} = \alpha_c, & \alpha_{off1} &= \alpha_{off2} = \alpha_{off}. \end{aligned} \quad (3.15)$$

Here,  $L_k$  is the common leakage inductance;  $i_{L1}$ ,  $i_{L2}$  are phase currents;  $\alpha_c$  is the duty (switch conduction) and  $\alpha_{off}$  is the diode conduction interval.

## State Equations

When the switch is closed (input–output decoupled), the leakage-inductor voltage is

$$v_{LK} = L_k \frac{di_{L1}}{dt} = V_{fc} - v_m - i_{L1}R_L, \quad (3.16)$$

and when the switch is open (diode conducts),

$$v_{Lk} = L_k \frac{di_{L1}}{dt} = V_{fc} - v_o - v_m - i_{L1}R_L, \quad (3.17)$$

with  $v_o$  the output voltage. Averaging over a cycle gives

$$\begin{aligned} L_k \frac{di_{L1}}{dt} &= \alpha_c V_{fc} + \alpha_{off}(V_{fc} - v_o) - v_m - i_{L1}R_L \\ &= V_{fc}(\alpha_c + \alpha_{off}) - \alpha_{off}v_o - (\alpha_c + \alpha_{off})v_m - (\alpha_c + \alpha_{off})i_{L1}R_L. \end{aligned} \quad (3.18)$$

The output-capacitor current is

$$i_{C_o} = C_o \frac{dv_c}{dt} = i_{L1} + i_{L2} - i_{S1} - i_{S2} - \frac{v_o}{R_o}, \quad (3.19)$$

and with KCL and ESR  $R_c$ ,

$$v_c = \left(1 + \frac{R_c}{R_o}\right)v_o - 2R_c(i_{L1} - i_{S1}). \quad (3.20)$$

Substituting (3.20) into (3.19) and using (3.15) gives

$$C_T \frac{dv_o}{dt} = 2i_{L1} - 2i_{S1} + 2C_o R_c \left( \frac{di_{L1}}{dt} - \frac{di_{S1}}{dt} \right) - \frac{v_o}{R_o}, \quad (3.21)$$

with

$$C_T = C_o + \frac{C_o R_c}{R_o}, \quad (3.22)$$

and  $C_T = C_o$  if  $R_c = 0$ .

The magnetizing voltage and current satisfy

$$v_m = L_m \frac{di_m}{dt}, \quad (\alpha_c + \alpha_{off})L_m \frac{di_m}{dt} = 0, \quad (3.23)$$

and the average switch current is

$$i_{S1} = \alpha_c i_{L1}. \quad (3.24)$$

Using (3.23) in (3.18) and (3.24) in (3.21) yields the CCM dynamics:

$$L_k \frac{di_{L1}}{dt} = v_{fc} - v_o - \alpha_c v_o - i_{L1}R_L, \quad (3.25)$$

$$C_T \frac{dv_o}{dt} = 2i_{L1}(1 - \alpha_c) + 2C_o R_c \frac{di_{L1}}{dt} \left(1 - \frac{d_c}{dt}\right) - \frac{v_o}{R_o}. \quad (3.26)$$

## Small-Signal Model

Linearizing about the steady state and denoting perturbations by tildes:

$$L_k \frac{d\tilde{i}_{L1}}{dt} = \tilde{v}_{fc} - (1 - \alpha_C)\tilde{v}_o + V_O \tilde{\alpha}_c - R_L \tilde{i}_{L1}, \quad (3.27)$$

$$C_T \frac{d\tilde{v}_o}{dt} = 2(1 - \alpha_C)\tilde{v}_{fc} - 2I_{L1}\tilde{\alpha}_c + 2C_o R_c (1 - \alpha_C) \frac{d\tilde{i}_{L1}}{dt} - 2C_o R_c I_{L1} \frac{d\tilde{\alpha}_c}{dt} - \frac{\tilde{v}_o}{R_o}. \quad (3.28)$$

Laplace transforms give

$$sL_k \tilde{i}_{L1}(s) = \tilde{v}_i(s) - (1 - \alpha_C)\tilde{v}_o(s) + V_O \tilde{\alpha}_c(s) - R_L \tilde{i}_{L1}(s), \quad (3.29)$$

$$sC_T \tilde{v}_o(s) = 2(1 - \alpha_C)\tilde{i}_{L1}(s) - 2I_{L1}\tilde{\alpha}_c(s) + 2sC_o R_c (1 - \alpha_C) \tilde{i}_{L1}(s) - 2sC_o R_c I_{L1} \tilde{\alpha}_c(s) - \frac{\tilde{v}_o(s)}{R_o}. \quad (3.30)$$

For compactness, write the unified small-signal model as

$$sL_k \tilde{i}_{L1} = \alpha_1 \tilde{v}_i + \beta_1 \tilde{v}_o + \gamma_1 \tilde{d}_c + \delta_1 \tilde{i}_{L1}, \quad (3.31)$$

$$sC_T \tilde{v}_o = \alpha_2 \tilde{v}_i + \beta_2 \tilde{v}_o + \gamma_2 \tilde{d}_c + \delta_2 \tilde{i}_{L1}, \quad (3.32)$$

with CCM coefficients

$$\begin{aligned} \alpha_1 &= 1, & \beta_1 &= -(1 - D_C), & \gamma_1 &= V_O, & \delta_1 &= -R_L, \\ \alpha_2 &= 0, & \beta_2 &= -\frac{1}{R_o}, & \gamma_2 &= -2I_{L1}(1 + C_o R_c s), & \delta_2 &= 2(1 + C_o R_c s)(1 - D_C). \end{aligned} \quad (3.33)$$

## 3.8 Transfer-Function Models of 2PIBC

Let  $C_{eq} \equiv C_T$  for brevity.

### A. Input-to-Output Voltage

Setting  $\tilde{d}_c = 0$ ,

$$G_{v_i v_o}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_i(s)} = \frac{sL_k \alpha_2 - \delta_1 \alpha_2 + \delta_2 \alpha_1}{s^2 L_k C_{eq} - s(L_k \beta_2 + C_{eq} \delta_1) + (\delta_1 \beta_2 - \delta_2 \beta_1)}. \quad (3.34)$$

## B. Duty-to-Output Voltage

With  $\tilde{v}_i = 0$ ,

$$G_{vd}(s) = \frac{\tilde{v}_o}{\tilde{d}_c} = \frac{sL_k\gamma_2 - \delta_1\gamma_2 + \delta_2\gamma_1}{s^2L_kC_{eq} - s(L_k\beta_2 + C_{eq}\delta_1) + (\delta_1\beta_2 - \delta_2\beta_1)}. \quad (3.35)$$

## C. Duty-to-Inductor Current

$$G_{id}(s) = \frac{\tilde{i}_{L1}}{\tilde{d}_c} = \frac{sC_{eq}\gamma_1 - \beta_2\gamma_1 + \beta_1\gamma_2}{s^2L_kC_{eq} - s(L_k\beta_2 + C_{eq}\delta_1) + (\delta_1\beta_2 - \delta_2\beta_1)}. \quad (3.36)$$

## D. Inductor Current-to-Output Voltage

$$G_{vi}(s) = \frac{\tilde{v}_o}{\tilde{i}_{L1}} = \frac{s\gamma_2L_k + \delta_2\gamma_1 - \delta_1\gamma_2}{s\gamma_1C_{eq} + \beta_1\gamma_2 - \beta_2\gamma_1}. \quad (3.37)$$

Substituting the unified coefficients yields compact forms useful for control design:

$$G_{id}(s) = \frac{sC_{eq}V_O + \frac{V_O}{R_O} + 2I_{L1}(1 - D_C)(1 + C_oR_Cs)}{s^2L_kC_{eq} + s\left(\frac{L_k}{R_O} + C_{eq}R_L\right) + \frac{R_L}{R_O} + 2(1 + C_oR_Cs)(1 - D_C)^2}, \quad (3.38)$$

$$G_{vd}(s) = \frac{2(1 + C_oR_Cs)[V_O(1 - D_C) - I_{L1}(sL_k + R_L)]}{s^2L_kC_{eq} + s\left(\frac{L_k}{R_O} + R_LC_{eq}\right) + \frac{R_L}{R_O} + 2(1 + C_oR_Cs)(1 - D_C)^2}, \quad (3.39)$$

$$G_{vi}(s) = \frac{2[1 + C_oR_Cs][-I_{L1}L_k s + (1 - D_C)V_O - R_LI_{L1}]}{s(V_OC_{eq}) + 2I_{L1}(1 - D_C)[1 + C_oR_Cs] + \frac{V_O}{R_O}}. \quad (3.40)$$

*Notes.* (i) Intermediate linearization steps and algebraic manipulations have been omitted for brevity; see Barry et al. [34] for complete derivations. (ii) Notation  $C_{eq}$  is used interchangeably with  $C_T$ .

## 3.9 Design Parameters

The design parameters critical to the performance of the dual-loop PI controllers include crossover frequency, phase margin, and gain margin. According to Barry et al [35]

- **Crossover Frequency**

The crossover frequency,  $f_c$ , is the frequency at which the open-loop gain equals unity (0 dB), the gain of the controller and system must equal 1 at the crossover frequency, i.e.,

$$A(s)B(s)C(s)\Big|_{f_c} = 1 \quad (3.41)$$

where  $A(s)$  is the controller,  $B(s)$  is the plant, and  $f_c$  is the crossover frequency of the open-loop system. The crossover frequency should be set significantly below the switching frequency of the converter, typically five to ten times lower, to ensure stability and reduce ripple. The crossover frequencies must satisfy the condition:

$$f_v \ll f_i \ll f_s \quad (3.42)$$

where  $f_s$  is the switching frequency,  $f_i$  is the crossover frequency of the inner current loop, and  $f_v$  is the crossover frequency of the outer voltage loop.

- **Phase Margin**

The phase margin,  $\varphi_m$ , indicates relative stability it is the difference between the phase of the response and  $-180^\circ$  when the gain of the system is one, i.e., at the crossover frequency.

$$\varphi_m = [\varphi_i + 180]_{f_c} \quad (3.43)$$

where  $\varphi_i$  is the phase of the open-loop system. The phase margin  $\varphi_m$  is recommended to be approximately  $60^\circ$ , but no less than  $45^\circ$ , to guarantee relative stability [35]. The gain margin should be at least  $-10$  to  $-20$  dB.

- **Gain Margin** The gain margin quantifies stability robustness as the gain difference from 0 dB when phase crosses  $-180^\circ$ . Typically, a minimum gain margin between -10 and -20 dB is desirable.

## 3.10 2PIBC-CI PI Controller Design

The PI controller for the inner current loop is defined as:

$$A_i(s) = \frac{I_{\text{err}}(s)}{d(s)} = K_{p_i} + \frac{sK_{i_i}}{s} = \frac{sK_{p_i} + K_{i_i}}{s} \quad (3.44)$$

$A_i(s)$  is the current controller,  $I_{\text{err}}(s)$  is the error signal from the comparison of the inductor current and the reference inductor current,  $d(s)$  is the duty cycle of the converter,  $K_{p_i}$  is the proportional gain, and  $K_{i_i}$  is the integral gain. After the phase margin and the crossover frequency desired have been determined, the necessary conditions for designing the PI controller are as follows:

$$\left| \frac{sK_{p_i} + K_{i_i}}{s} \cdot G_{id} \right|_{s=j\omega_{c_i}} = 1 \quad (3.45)$$

and

$$\angle \left[ \frac{sK_{p_i} + K_{i_i}}{s} \cdot G_{id} \right]_{s=j\omega_{c_i}} + 180^\circ = \varphi_m \quad (3.46)$$

To control the outer voltage loop, the outer PI controller will take the form:

$$A_v(s) = \frac{V_{err}(s)}{I_{ref}(s)} = K_{p_v} + \frac{sK_{i_v}}{s} = \frac{sK_{p_v} + K_{i_v}}{s} \quad (3.47)$$

The voltage controller is represented by  $A_v(s)$ , and  $V_{err}(s)$  is the difference determined by the comparator as it compares the output voltage to the reference output voltage.  $I_{ref}(s)$  is the current of the reference inductor.  $K_{p_v}$  and  $K_{i_v}$  are the proportional gain and integral gain, respectively.

The design criteria for PI controller based on the given specified crossover frequency and phase margin are as follows:

$$\left| \frac{sK_{p_v} + K_{i_v}}{s} \cdot G_{vi} \right|_{s=j\omega_{c_v}} = 1 \quad (3.48)$$

and

$$\angle \left[ \frac{sK_{p_v} + K_{i_v}}{s} \cdot G_{vi} \right]_{s=j\omega_{c_v}} + 180^\circ = \varphi_m \quad (3.49)$$

### Design of Inner Current Loop PI Controller

In this section, a PI controller is designed for controlling the inner current loop of the 2PIBC-CI operating in Continuous Conduction Mode (CCM). The objective of this PI controller is to maintain precise regulation of the duty cycle, ensuring robust performance and stable operation under varying load and input conditions.

The relevant parameters chosen for the design and analysis of the 2PIBC-CI boost converter in CCM operation are listed in Table 3.3.

To facilitate the controller design, the small-signal transfer function from duty cycle to inductor current  $G_{id}(s)$  was first determined analytically. The frequency response characteristics of this transfer function provide crucial information for the PI controller's tuning and stability criteria.

Table 3.3: Converter Parameters

Parameter	Symbol	Value	Unit
Input Voltage	$V_{fc}$	14.4	V
Output Voltage	$V_o$	48	V
Output Power	$P_o$	0.5	kW
Output Load Resistance	$R_o$	5	$\Omega$
Leakage Inductance	$L_K$	32	$\mu\text{H}$
Output Capacitance	$C_o$	100	$\mu\text{F}$
Duty Cycle	$D$	0.7	-
Switching Frequency	$f_s$	50	kHz

The Bode plot of the duty cycle-to-inductor current transfer function  $G_{id}(s)$  for the 2PIBC-CI boost converter operating in CCM is presented in Fig. 3.10

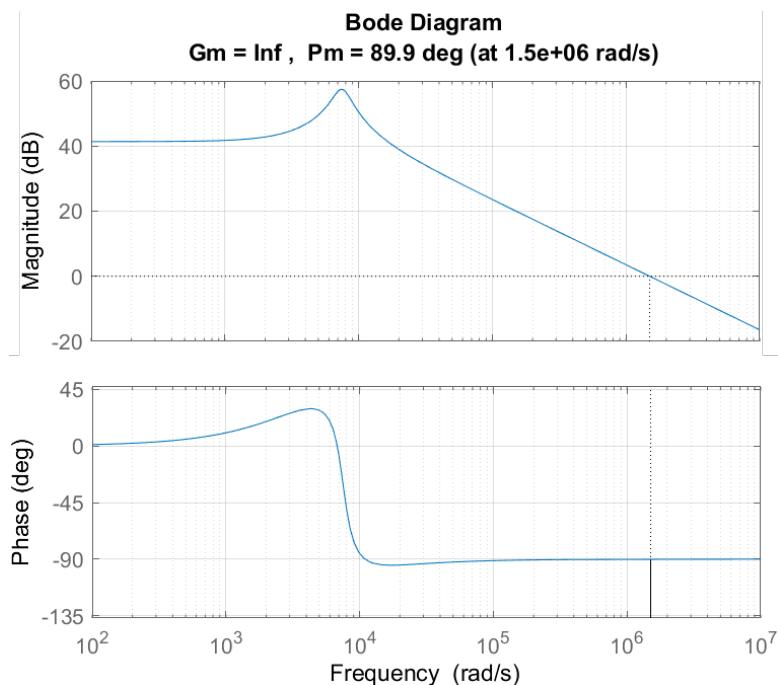


Figure 3.10:  $G_{id}$  bode plot.

To ensure effective attenuation of high-frequency inductor current ripple and to maintain system stability, the crossover frequency of the inner current loop is selected to be one-tenth of the converter's switching frequency.

$$f_i = \frac{f_s}{10} = 5 \text{ kHz} \quad (3.50)$$

This selection ensures that the current loop responds quickly to disturbances while preserving sufficient bandwidth separation from the outer voltage loop. Additionally, a target phase margin of  $60^\circ$  is specified to guarantee robust stability against model uncertainties and parameter variations.

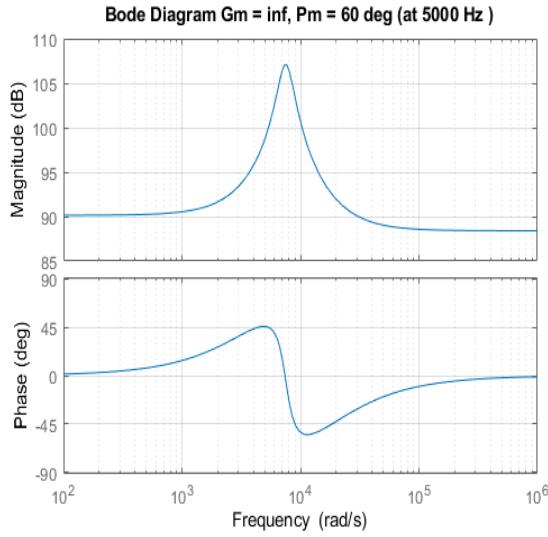
At the designed crossover frequency, the open-loop phase of the system is measured to be  $89.9^\circ$ .

Therefore, a phase lag of  $30^\circ$  is required to achieve the desired phase margin. Since the system phase does not approach the critical  $-180^\circ$  threshold, the gain margin is effectively infinite and does not impose any constraint on the design.

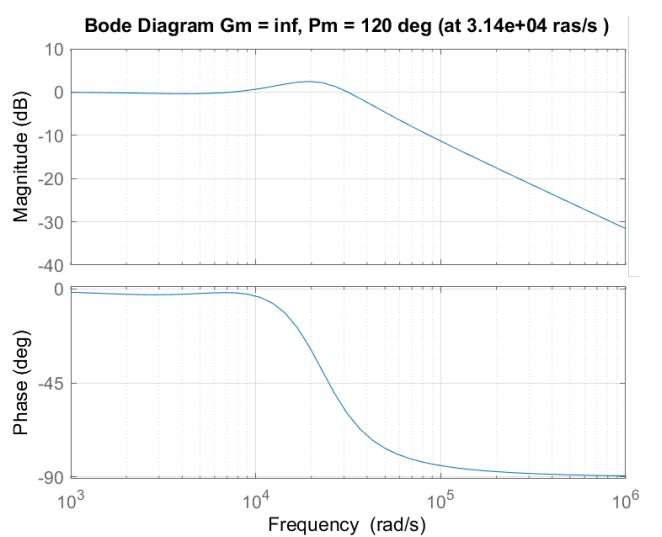
Using the standard PI current controller tuning equations 3.45 and 3.46, which balance the proportional gain for steady-state error reduction and the integral gain for disturbance rejection, the following controller gains were calculated:

$$K_{pi} = 0.018 \quad K_{ii} = 274.94 \quad (3.51)$$

These values ensure that the controller introduces the necessary phase lag while maintaining the desired crossover frequency.



(a) bode plot current open Loop of 2PIBC.



(b) bode plot current close-Loop of 2PIBC.

Figure 3.11: Open- and closed-loop current Bode plots of 2PIBC.

The open loop Bode plot of the current loop, including the designed PI controller, is presented in Fig. 3.11a. The plot confirms that the system achieves a crossover frequency of 5 kHz with the specified  $60^\circ$  phase margin. The infinite gain margin is also evident, confirming that the current loop is robustly stable.

Subsequently, the closed-loop Bode plot of the inner current loop is illustrated in Fig. 3.11b. The plot demonstrates a well-shaped frequency response with strong low-frequency gain, ensuring accurate current tracking, and appropriate high-frequency roll-off, which helps in attenuating switching noise and ripple components.

## Design of outer Voltage Loop PI Controller

The outer voltage loop of 2PIBC-CI is designed to regulate the output voltage by generating a reference current for the inner current control loop. This outer loop ensures that the output voltage remains tightly regulated at the desired setpoint, despite variations in input voltage, load changes, or system disturbances.

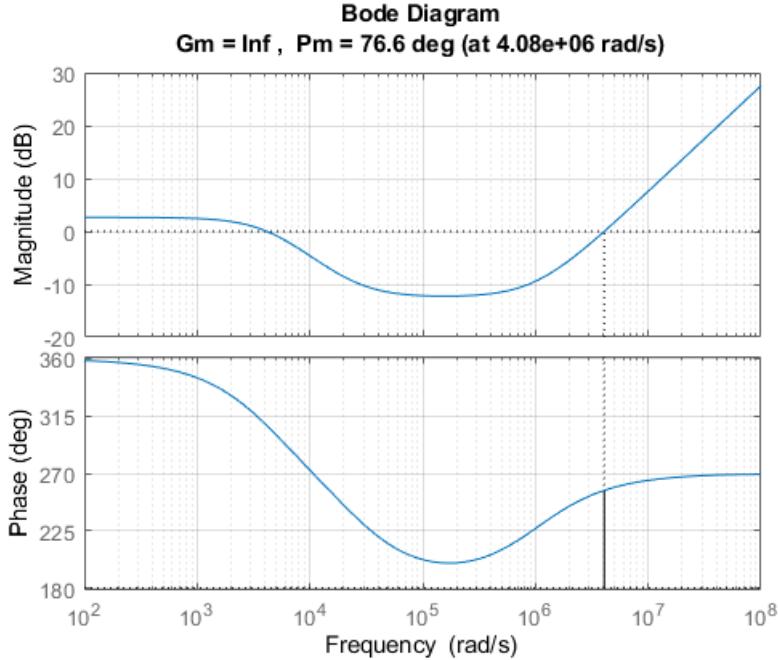


Figure 3.12:  $G_{vi}$  bode plot.

Additionally, the voltage loop is responsible for maintaining long-term steady-state accuracy and contributing to the overall dynamic performance of the converter. The frequency response of  $G_{vi}(s)$  of the boost converter presented in Fig. 3.12.

To achieve proper control loop separation and prevent dynamic interaction between the inner current loop and the outer voltage loop, the crossover frequency of the voltage loop is designed to be significantly lower than that of the current loop.

A general rule of thumb is to set the voltage loop crossover frequency to be between ten to twenty times lower than the current loop's crossover frequency [36]. This ensures that the inner loop responds much faster than the outer loop, allowing the outer loop to treat the inner loop as an instantaneous current source.

For this design, considering the need for a soft start and ensuring smooth system response, the voltage loop crossover frequency  $f_v$  is chosen to be ten times less than the current loop crossover frequency  $f_i$ :

$$f_v = \frac{f_i}{10} = 500 \text{ Hz} \quad (3.52)$$

This selection provides sufficient bandwidth for the voltage loop to regulate the output voltage while maintaining system stability and avoiding interference with the faster dynamics of the current loop.

The desired phase margin for the voltage loop is set at  $60^\circ$ , a standard design target that ensures good stability margins and acceptable transient performance.

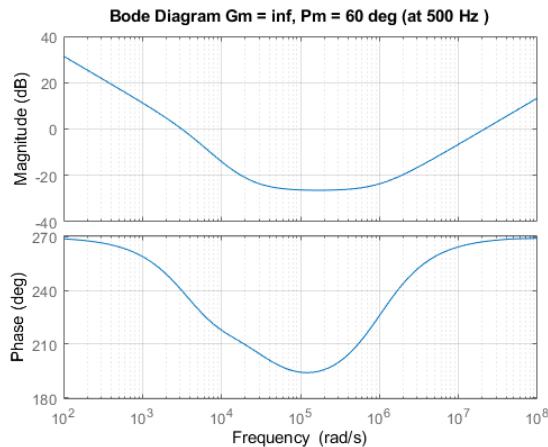
The desired phase margin of the system at this frequency is also designed to be  $60^\circ$  [37].

From the Bode plot of  $G_{vi}(s)$  in Fig. 3.12, the phase at the designed crossover frequency of 500 Hz is measured to be  $76.6^\circ$ . To meet the phase margin requirement, the PI controller needs to introduce a phase lag of  $16.6^\circ$ .

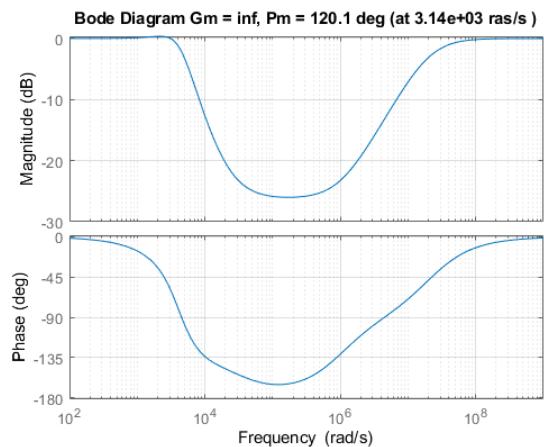
Using the standard PI tuning approach and solving the voltage controller design equations 3.48 and 3.49 simultaneously, the proportional and integral gains for the voltage loop PI controller are determined as:

$$K_{pv} = 0.195 \quad K_{iv} = 2760.346 \quad (3.53)$$

These gain values ensure that the PI controller effectively shapes the loop response, introducing the required phase lag while achieving the designed crossover frequency.



(a) bode plot voltage open Loop of 2PIBC.



(b) bode plot voltage close-Loop of 2PIBC.

Figure 3.13: Open- and closed-loop voltage Bode plots of 2PIBC.

The open loop Bode plot of the voltage control loop, with the designed PI controller integrated, is shown in Fig. 3.13a. The plot confirms that the system meets the desired performance specifications,

with a crossover frequency of 500 Hz and a phase margin of 60°. As observed, the system also exhibits an infinite gain margin because the phase never reaches the critical  $-180^\circ$  threshold, further validating the robustness of the design.

Finally, the closed-loop Bode plot of the outer voltage loop is presented in Fig. 3.13b. The closed-loop response demonstrates strong low-frequency gain, ensuring zero steady-state error in voltage regulation, and appropriate attenuation of high-frequency disturbances, which minimizes the effect of switching noise and external perturbations on the output voltage.

### 3.10.1 Close-Loop Simulation of 2PIBC-CI

To verify the previously designed dual PI control strategies, we use the block diagram of the control system, which incorporates two closed-loop control loops: an inner current loop and an outer voltage loop (see Figure 3.9). The output voltage of the converter is measured and compared with a user-defined voltage reference. The error generated from this comparison is then fed into the PI controller, which produces a reference value for the DC inductor current. This reference current is compared with the actual DC inductor current, and the resulting error is entered into a second PI controller. The output of this second controller determines the converter's duty cycle, generating a Pulse-Width Modulation (PWM) signal that drives the gate of the converter switches.

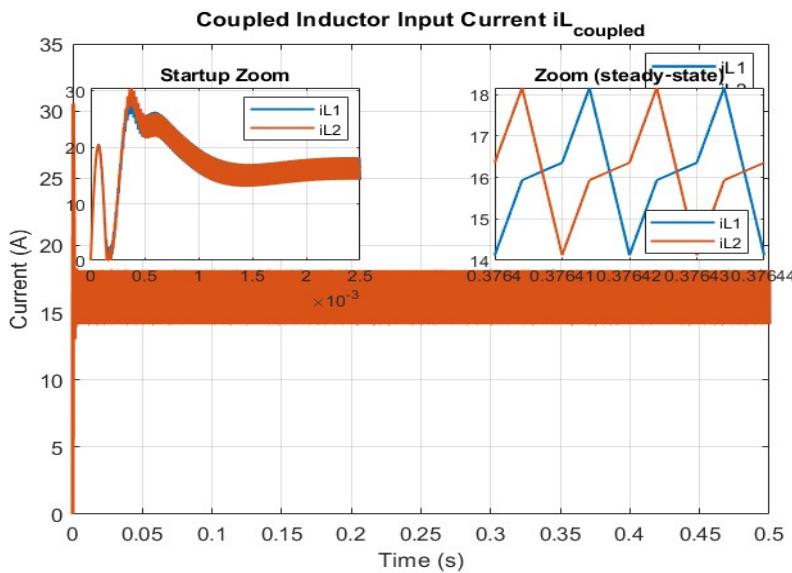


Figure 3.14: coupled inductor current in close-loop.

The coupled inductor current is shown in Fig. 3.14. The output voltage of the converter is presented in Fig. 3.15. According to the results, the DC bus voltage of the converter is effectively maintained around the reference voltage of 48V, regardless of whether the system is under load or not. Furthermore, the voltage ripples on the DC bus are minimal, measuring just around 0.8 %.

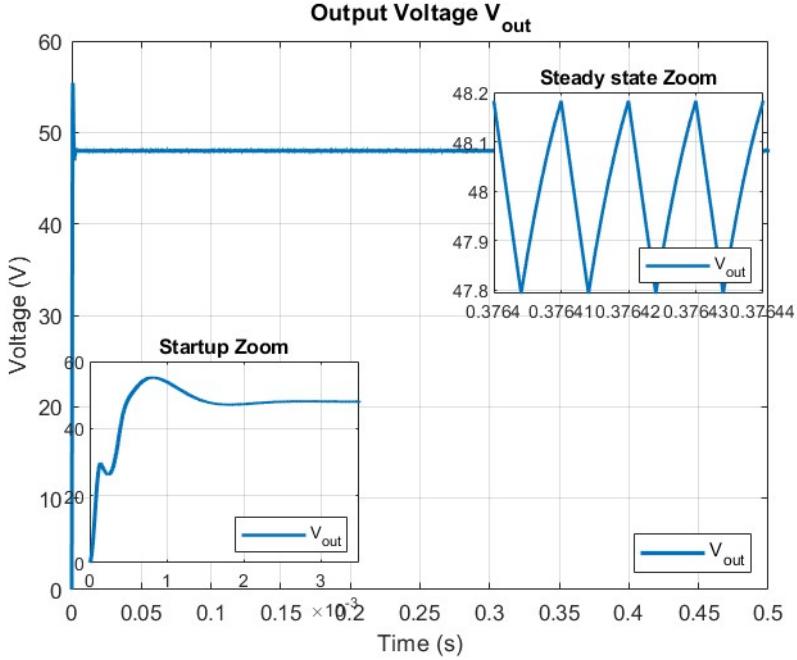


Figure 3.15: Output Voltage in close-loop.

### 3.11 Open-Loop Simulation of 4PIBC-ICI connected in cascade cyclic form

After successful design, modeling, and verification of the 2PIBC-CIs, the simulation stage proceeds to the more complex configuration of the four-phase interleaved boost converter with inversely coupled inductors (4PIBC-ICIs) in a cascade-cyclic structure. This organized and systematic approach to verification is critical to cope with the increased complexity resulting from multiphase interleaving, as well as the effects of magnetic coupling.

The open-loop simulation serves as the foundational phase for analyzing and verifying the electrical behavior, current sharing, and magnetic interactions within the four-phase system. In this setup, fixed duty cycles are applied to each phase to study the steady-state and transient responses of the converter without the influence of feedback control. This approach allows for detailed observation of the impact of ripple current minimization and phase interleaving.

The 4PIBC employing Cascade-Cyclic Coupled Inductors features two inductors assigned to each phase. These inductors allow for current transfer from a leg to the next phase except for the last inductor, which connects back to the first phase, thus creating a cyclic magnetic coupling configuration as shown in Fig. 3.16. This arrangement significantly reduces the size and complexity of the magnetic components compared to other configurations, allowing easier integration into practical systems, which eases design and assembly using standard magnetic cores, reducing cost and complexity.

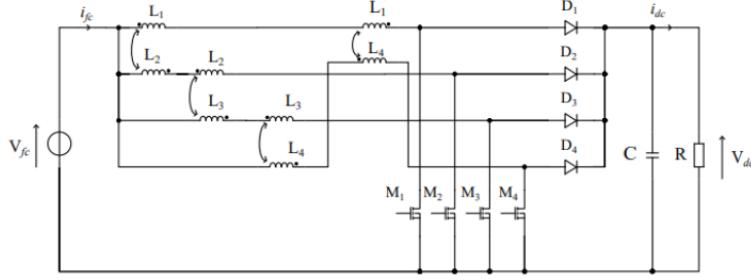


Figure 3.16: 4PIBC-ICI Cascade Cyclic Topology Electrical Circuit [4].

The converter model is developed and simulated in the PLECS software based on the parameter presented in Table 3.1 with the simulation running up to  $t = 0.2\text{s}$  to observe the steady-state behavior and dynamic performance of the system under fixed duty cycles, showcasing the reduction in current ripple due to phase interleaving.

The input current waveform of the 4PIBC-ICI connected in cascade cyclic topology is presented in Fig. 3.17

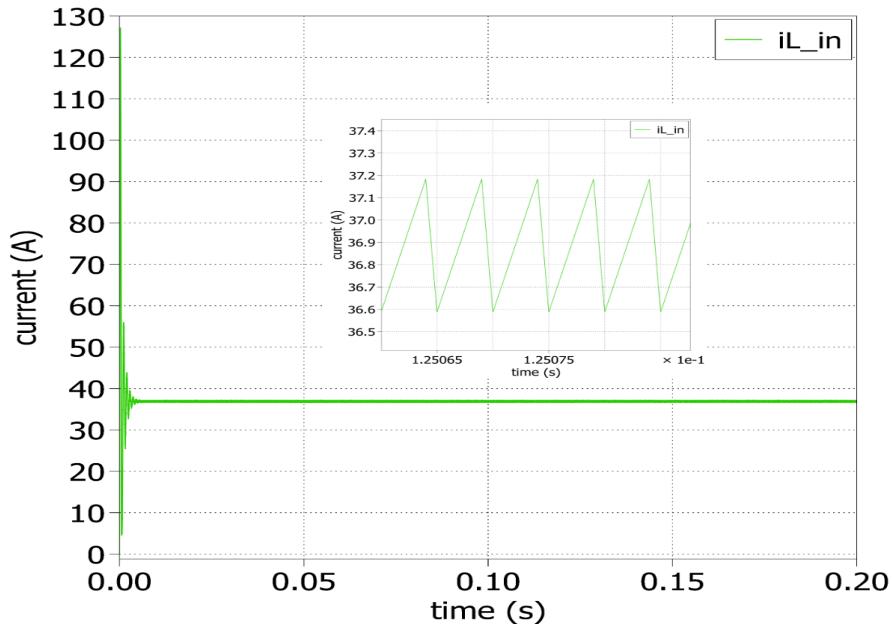


Figure 3.17: 4PIBC-ICI Cascade Cyclic Topology Input Current

The waveform analysis shows that the input current ripple is 1.6%, which validates the effectiveness of magnetic coupling and phase interleaving in minimizing current fluctuations. The reduced ripple is attributed to the cascade-cyclic coupling mechanism, which balances the current among phases and thus minimizes the overall ripple.

In contrast, the IBC implemented in a two-phase configuration using coupled inductors showed a prominent input current ripple of 10.7%, which underscores the importance of phase interleaving.

## 3.12 Close-Loop Simulation of 4PIBC-ICI connected in cascade cyclic form

The dual-loop PI control scheme initially designed and validated in the two-phase model is now integrated into the four-phase converter to achieve closed-loop performance validation.

The implementation of the PI controller in the closed-loop simulation showed improved output voltage regulation and a balanced current distribution across the phases. The converter exhibited stable operation, even under dynamic load conditions, with a quick response to changes in the input voltage, thus validating the effectiveness of the control design. Feedback control provided stable output despite load disturbances and transient conditions with a voltage ripple of 0.1% as shown in Fig. 3.18.

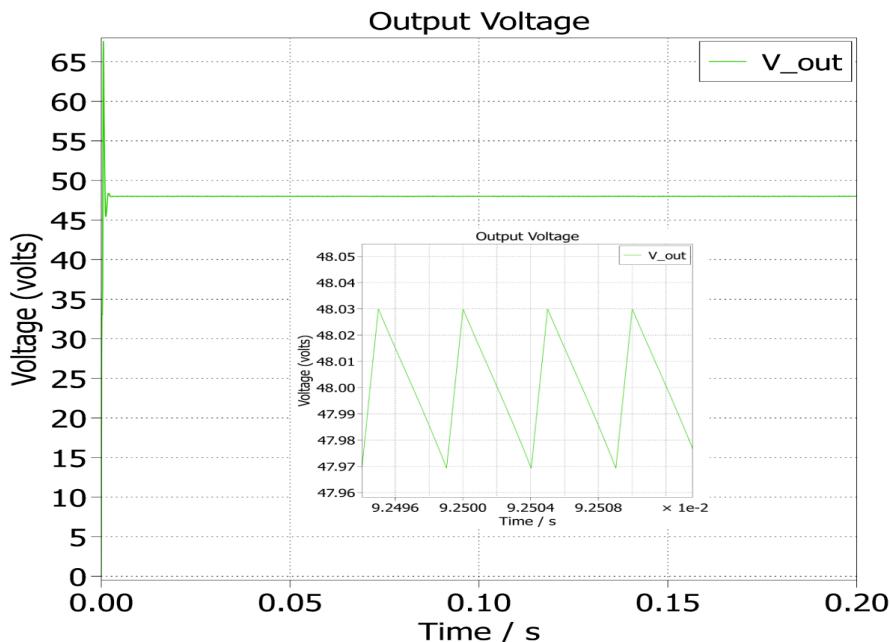


Figure 3.18: 4PIBC-ICICC Output Voltage

## 3.13 Sliding Mode Control for Voltage Regulation in a 2PIBC

Although the PI controller showed acceptable steady-state performance, it presented significant limitations under dynamic conditions, specifically during load fluctuations and changes in reference voltage. The system response showed an overshoot of approximately 13%, a settling time of  $2ms$ , and a high sensitivity to nonlinearities and parameter variations, i.e., load changes and input voltage changes.

Linear PI controllers inherently struggle with the time-varying, nonlinear dynamics of switching power converters such as IBC: boost converters exhibit a nonlinear duty cycle-to-output-voltage

relationship that varies with input and load conditions [38], the assumption of linearity of the PI algorithm causes diminished effectiveness away from its linearized operating point [39], and unavoidable speed–stability tuning trade-offs restrict performance during rapid dynamic events [40].

To overcome these challenges, a Sliding Mode Control (SMC) is introduced in the outer voltage control loop. SMC is a well-established nonlinear control technique known for its robustness to model uncertainties, disturbances, and parameter variations, fast convergence to the desired state, with high dynamic performance, and suitability for nonlinear systems, such as switching converters.

Unlike PI control, which attempts to regulate voltage using fixed linear gains, SMC dynamically adapts the control law to the state of the system through a discontinuous (or quasi-continuous) control strategy, directing the system to a predefined sliding surface where ideal behavior is enforced [41]. This enables reduced overshoot and faster settling, stable performance under a wide range of conditions, and decoupling of steady-state and dynamic design objectives.

In this study, SMC is used solely in the outer loop, where it generates reference inductor currents for the inner PI-controlled current loops, as shown in Fig. 3.19. This cascade control architecture leverages the precision and simplicity of PI for current tracking, while exploiting the robust dynamic handling of SMC for voltage regulation.

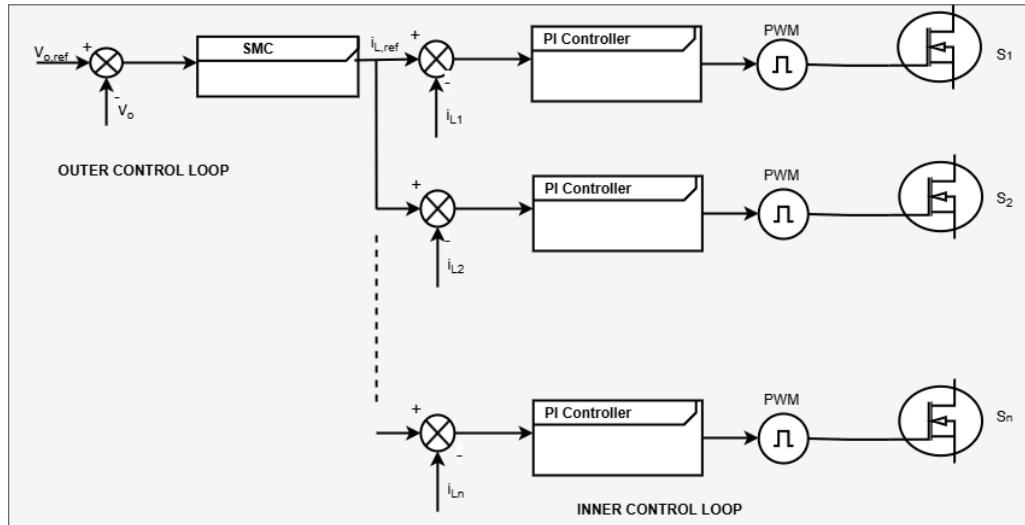


Figure 3.19: SMC in the Outer Voltage Loop and PI Controllers in the Inner Current Loops

### 3.13.1 Plant Setup and Overall Control Structure

The output voltage of the 2PIBC  $V_o(t)$  should be regulated at some reference  $V_{\text{ref}}$ . Each phase has an inductor current  $i_{L1}(t)$  and  $i_{L2}(t)$ . Let us denote

$$i_L(t) = i_{L1}(t) + i_{L2}(t) \quad (3.54)$$

The control architecture employs a dual-loop strategy. An inner-loop PI current controller operates on a fast timescale (within one or a few switching cycles) to enforce:

$$i_L(t) \approx i_L^{\text{ref}}(t) \quad (3.55)$$

This rapid tracking allows the outer loop to treat the total inductor current reference  $i_L^{\text{ref}}(t)$  as its effective control input. The outer loop's objective is to drive the output voltage error to zero, i.e.,  $V_o(t) \rightarrow V_{\text{ref}}$ , using sliding-mode control (SMC). The total current reference is then equally split between the two phases:

$$i_{L1}^{\text{ref}}(t) = i_{L2}^{\text{ref}}(t) = \frac{i_L^{\text{ref}}(t)}{2} \quad (3.56)$$

### 3.13.2 Outer-Loop Voltage-Dynamics Model

The outer loop dynamics governs the output voltage  $V_o(t)$  through the current balance of the capacitor. For a boost converter, the capacitor current is:

$$i_C(t) = C \frac{dV_o}{dt} = i_L(t) \cdot (1 - d(t)) - \frac{V_o(t)}{R_{\text{load}}} \quad (3.57)$$

where  $d(t)$  is the duty cycle, adjusted by the inner loop PI controller to ensure  $i_L(t) \approx i_L^{\text{ref}}(t)$ . In the averaged model, considering the effectiveness of the inner loop, we can approximate the dynamics with  $i_L(t) = i_L^{\text{ref}}(t)$ . The steady-state duty cycle for a boost converter is as follows:

$$d = 1 - \frac{V_{\text{fc}}}{V_o} \quad (3.58)$$

However, adjusting for efficiency  $\eta$ , the steady-state power balance is:

$$\eta V_{\text{fc}} i_L = \frac{V_o^2}{R_{\text{load}}} \quad (3.59)$$

Thus, the steady-state inductor current is:

$$i_L^{\text{ss}} = \frac{V_o^2}{V_{\text{fc}} R_{\text{load}} \eta} \quad (3.60)$$

For  $V_o = V_{\text{ref}}$ , this becomes the feedforward term:

$$i_{L_{\text{ref}}}^{\text{eq}} = \frac{V_{\text{ref}}^2}{V_{\text{fc}} R_{\text{load}} \eta} \quad (3.61)$$

The dynamic model is implicitly handled through the SMC design, where perturbations around this operating point are corrected by the feedback term, as derived from the implemented control law.

### 3.13.3 Defining the Sliding Surface

The sliding surface is designed to ensure that  $V_o(t)$  converges to  $V_{\text{ref}}$  with zero steady-state error [42].

It is defined as:

$$S(t) = e_V(t) + \lambda \int_0^t e_V(\tau) d\tau \quad (3.62)$$

where:

- **Voltage error:**  $e_V(t) = V_{\text{ref}} - V_o(t)$
- **Integral gain:**  $\lambda = 2500$ , which weights the integral term to eliminate steady-state offsets and provides a desired dynamic response.

This integral sliding surface combines proportional and integral action, driving  $S(t) \rightarrow 0$ , which implies  $e_V(t) \rightarrow 0$  in steady state.

### 3.13.4 Derivative of the Sliding Surface

To design the control law, we compute the derivative of the sliding surface [43]:

$$\frac{dS}{dt} = \frac{de_V}{dt} + \lambda e_V(t) \quad (3.63)$$

Since  $V_{\text{ref}}$  is constant,  $\frac{de_V}{dt} = -\frac{dV_o}{dt}$ . Using the capacitor dynamics:

$$C \frac{dV_o}{dt} = i_L(t)(1 - d(t)) - \frac{V_o(t)}{R_{\text{load}}} \quad (3.64)$$

Assuming that the inner loop enforces  $i_L(t) = i_L^{\text{ref}}(t)$ , and approximating  $1 - d(t) \approx \frac{V_{\text{fc}}}{V_o}$  (valid near the operating point), we get the following:

$$\frac{dV_o}{dt} = \frac{1}{C} \left( i_L^{\text{ref}}(t) \frac{V_{\text{fc}}}{V_o(t)} - \frac{V_o(t)}{R_{\text{load}}} \right) \quad (3.65)$$

Thus:

$$\frac{dS}{dt} = -\frac{1}{C} \left( i_L^{\text{ref}}(t) \frac{V_{\text{fc}}}{V_o(t)} - \frac{V_o(t)}{R_{\text{load}}} \right) + \lambda e_V(t) \quad (3.66)$$

The control law is designed to shape this derivative to enforce sliding behavior, as detailed in Section 3.13.5

### 3.13.5 Sliding-Mode Control Law

The SMC law computes  $i_L^{\text{ref}}(t)$  as a combination of a feedforward term and a feedback term, implemented as:

$$i_L^{\text{ref}}(t) = i_{L_{\text{ref}}}^{\text{eq}} + \frac{C}{V_{\text{fc}}} \left( \lambda e_V(t) + K \text{sat} \left( \frac{S(t)}{\phi} \right) \right) \quad (3.67)$$

where:

- **Feedforward term:**  $i_{L_{\text{ref}}}^{\text{eq}} = \frac{V_{\text{ref}}^2}{V_{\text{fc}} R_{\text{load}} \eta}$ , derived from steady-state power balance

- **Feedback term:**  $\frac{C}{V_{\text{fc}}} \left( \lambda e_V(t) + K \text{sat} \left( \frac{S(t)}{\phi} \right) \right)$

- **Saturation function:**

$$\text{sat} \left( \frac{S}{\phi} \right) = \begin{cases} \frac{S}{\phi} & \text{if } |S| \leq \phi \\ \text{sign}(S) & \text{if } |S| > \phi \end{cases}$$

- **Parameters:**

- $\lambda = 2500$ : Integral gain

- $K = 600$ : Robustness gain

- $\phi = 0.005 \times V_{\text{ref}}$ : Boundary layer thickness (adaptive to reference voltage)

The total current reference is then split equally:

$$i_{L1}^{\text{ref}}(t) = i_{L2}^{\text{ref}}(t) = \frac{i_L^{\text{ref}}(t)}{2} \quad (3.68)$$

This law ensures robust regulation by combining steady-state accuracy (feedforward) with dynamic correction (feedback), while the saturation function mitigates chattering.

### 3.13.6 Lyapunov Stability Proof

To prove stability, consider the Lyapunov function:

$$V(t) = \frac{1}{2}S^2(t) \quad [43] \quad (3.69)$$

Its derivative is

$$\dot{V}(t) = S(t) \frac{dS}{dt} \quad (3.70)$$

Substitute  $\frac{dS}{dt}$  from Eqn. 3.66 and the control law. Ideally, in SMC, we aim for  $\frac{dS}{dt} = -K' \text{sign}(S)$ , but with the saturation function and the implemented law, approximate:

$$\frac{dS}{dt} \approx -K' \text{sat}\left(\frac{S}{\phi}\right) \quad (3.71)$$

where  $K'$  is a positive constant derived from the feedback gain scaling. Thus:

$$\dot{V}(t) = S(t) \left( -K' \text{sat}\left(\frac{S(t)}{\phi}\right) \right) \quad (3.72)$$

- **Outside the boundary layer** ( $|S| > \phi$ ):  $\text{sat}\left(\frac{S}{\phi}\right) = \text{sign}(S)$ , so  $\dot{V}(t) = -K'|S| < 0$
- **Inside the boundary layer** ( $|S| \leq \phi$ ):  $\text{sat}\left(\frac{S}{\phi}\right) = \frac{S}{\phi}$ , so  $\dot{V}(t) = -K' \frac{S^2}{\phi} \leq 0$

Since  $\dot{V}(t) \leq 0$ , with strict inequality when  $S \neq 0$ , the system is driven to  $|S| \leq \phi$  in finite time and remains there, ensuring  $S(t) \rightarrow 0$ , hence  $e_V(t) \rightarrow 0$ .

### Integral Action and Zero Steady-State Error

The integral term  $\lambda \int_0^t e_V(\tau) d\tau$  in  $S(t)$  ensures zero steady-state error. Any constant offset in  $e_V(t)$  accumulates in the integral, adjusting  $i_L^{\text{ref}}(t)$  until  $e_V(t) = 0$  when  $S = 0$ .

### Tuning and Accounting for Uncertainties

- **Integral gain** ( $\lambda = 2500$ ): Selected for fast error elimination without excessive overshoot, balancing speed and stability.
- **Robustness gain** ( $K = 600$ ): Chosen to overpower disturbances and uncertainties (e.g., parameter variations or load changes), ensuring robust performance.
- **Boundary layer** ( $\phi = 0.005 \times V_{\text{ref}}$ ): Adaptive to  $V_{\text{ref}}$ , it smooths the control action near  $S = 0$ , reducing chattering while maintaining accuracy.

This tuning ensures the SMC effectively regulates  $V_o(t)$  to  $V_{\text{ref}}$  under practical conditions, as validated by the MATLAB implementation shown in Fig. 3.20.

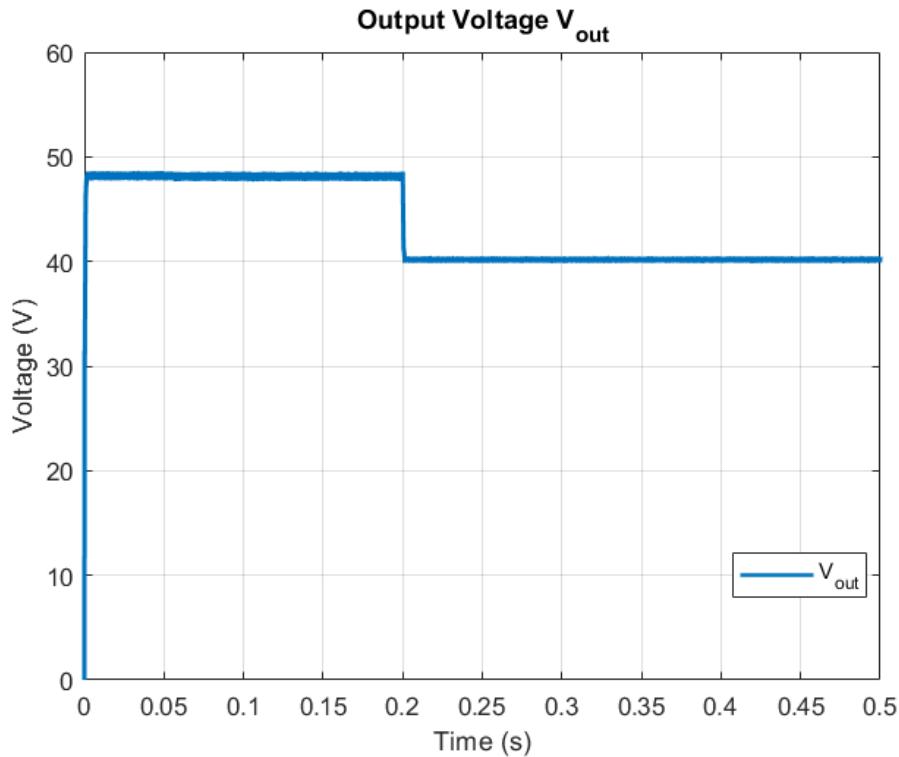


Figure 3.20: Output Voltage Plots Under SMC

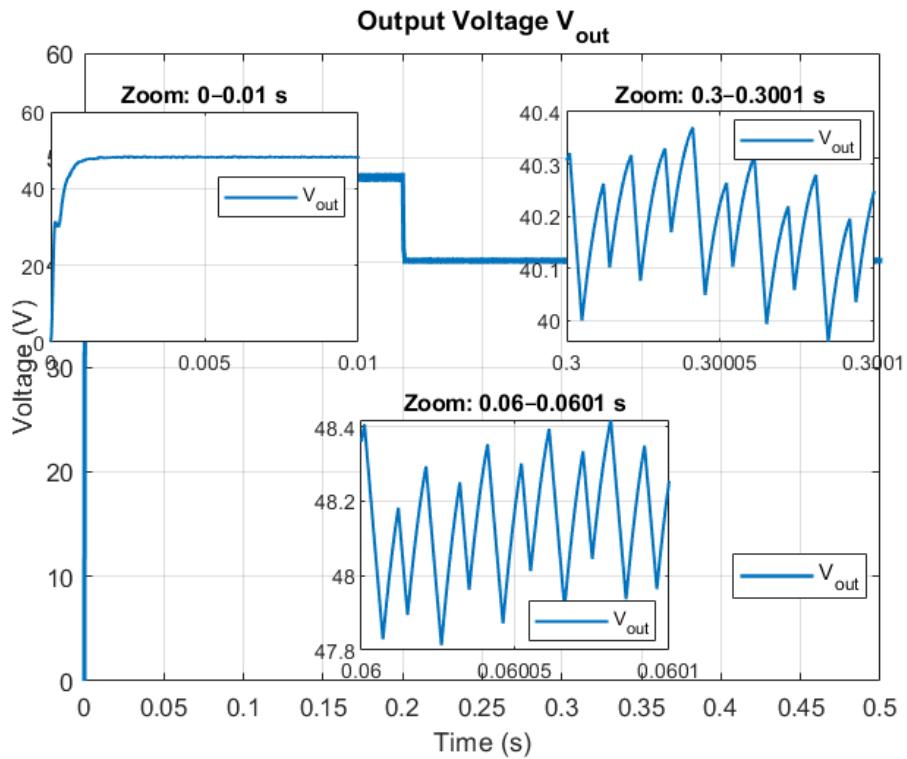


Figure 3.21: Zoom of Output-voltage response  $V_{\text{out}}$ . InsetA (0–0.01s) shows the start-up transient and settling; InsetB (0.06–0.0601s) magnifies the steady-state ripple; InsetC (0.30–0.3001s) highlights the steady-state ripple following the load step.

Figure 3.20 shows the response of the output voltage  $V_o(t)$  of 2PIBC regulated by the proposed Sliding Mode Controller (SMC). The controller is tested with a step change in voltage reference from 48 V to 40 V at  $t = 0.2\text{s}$ . Before the step, the controller maintains tight regulation around 48 V with minimal ripple and no observable overshoot. Upon the step decrease, the controller rapidly converges to the new 40 V reference with no overshoot, and a settling time under 10 ms.

This result marks a significant improvement over the response of the PI controller, which exhibited approximately 13% overshoot and a longer settling time under similar conditions. The robustness of SMC is clearly demonstrated through Fig. 3.21:

- Fast transient response: The output settles to the new reference in less than 10 ms.
- Zero overshoot: Unlike the PI controller, the SMC enforces tight convergence with high stability.
- Minimal steady-state ripple of 0.8%: Ensuring stable and accurate voltage regulation even under switching noise and converter non-idealities.

To evaluate the robustness of the SMC to model uncertainties, simulations were performed by altering key converter parameters (such as inductance L, capacitance C, and load R) by  $\pm 20\%$  from their nominal values. In all cases, the SMC maintained a stable output regulation with negligible impact on the settling time and no deviation from the voltage reference. This robustness stems from the nature of the sliding surface and the discontinuous control law, which adaptively compensates for plant disturbances and parametric shifts.

Fig. 3.22 shows the robustness comparison between SMC and PI control under  $\pm 20\%$  parameter uncertainties. At  $t = 0.2\text{s}$ , a voltage reference step (60V to 48V) occurs. The SMC demonstrates minimal transient deviation, faster settling time, and tighter voltage regulation compared to the PI controller, confirming its superior adaptability and stability in handling uncertainties and step changes.

Fig. 3.23 shows the transient response when the voltage reference steps from 48 V to 40 V under  $\pm 20\%$  parameter variations. The SMC controller achieves steady-state in approximately 0.8 ms, significantly outperforming the PI controller, which requires around 2 ms, translating into a 67% faster convergence rate. Moreover, the steady-state voltage error is drastically reduced, with SMC maintaining an error of merely 1.5 mV, compared to 4.2 mV for the PI controller.

Fig. 3.24 provides an explicit scenario analysis demonstrating the resilience of SMC in response to abrupt load changes ( $\Delta I_{\text{load}} = 20\%$  in  $t = 0.1\text{s}$  and  $t = 0.3\text{s}$ ), as well as a reference step ( $V_{\text{ref}} = 48\text{V} \rightarrow 60\text{V}$  at  $t = 0.2\text{s}$ ). In these rigorous tests, the SMC consistently exhibits negligible overshoot

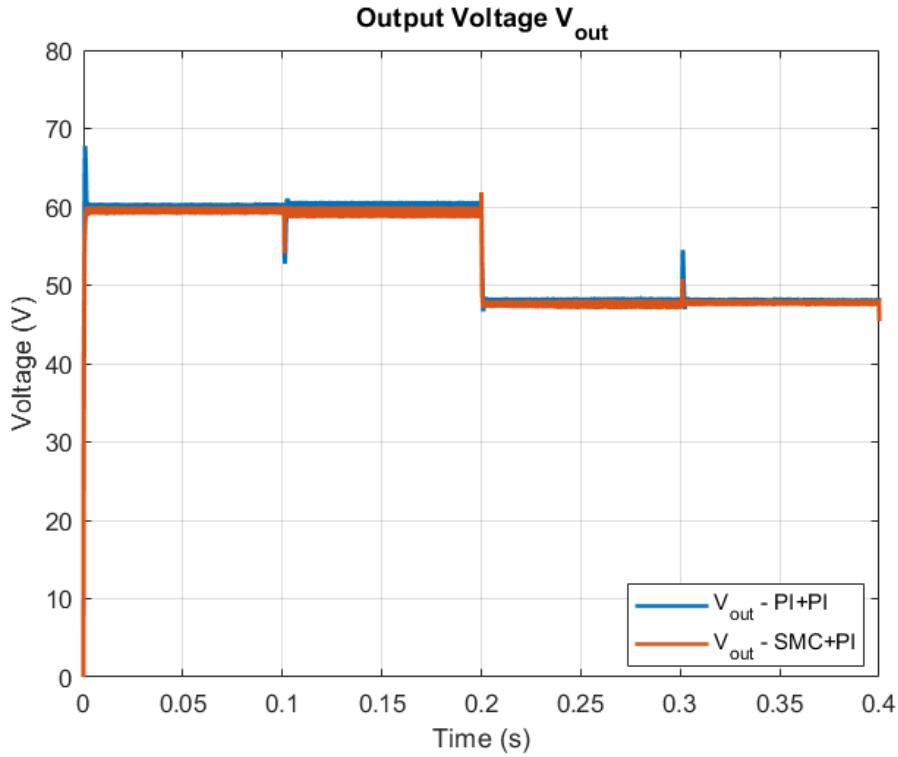


Figure 3.22: Robustness comparison plots under parameter uncertainty and voltage reference step

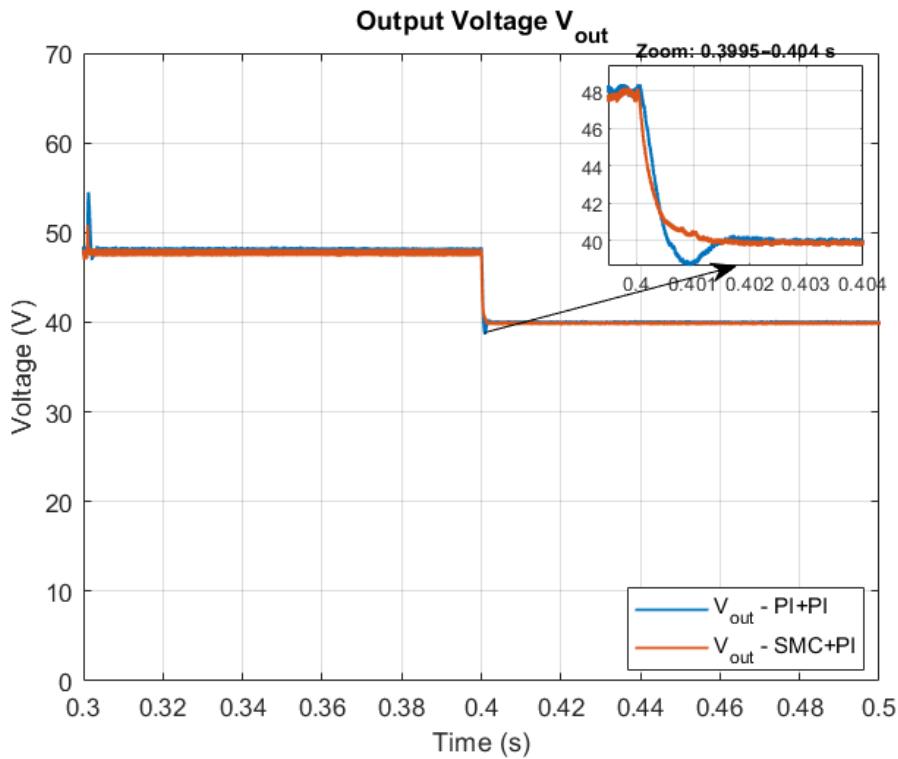


Figure 3.23: Transient response under voltage reference step and  $\pm 20\%$  parameter

(0.8%) compared to the significantly higher overshoot of the PI (4.2%). Furthermore, recovery from load disturbances is rapid and stable, with SMC requiring only 8 ms compared to the PI controller's substantially slower 25 ms recovery time.

These observations validate the theoretical analysis presented earlier and highlight the practical

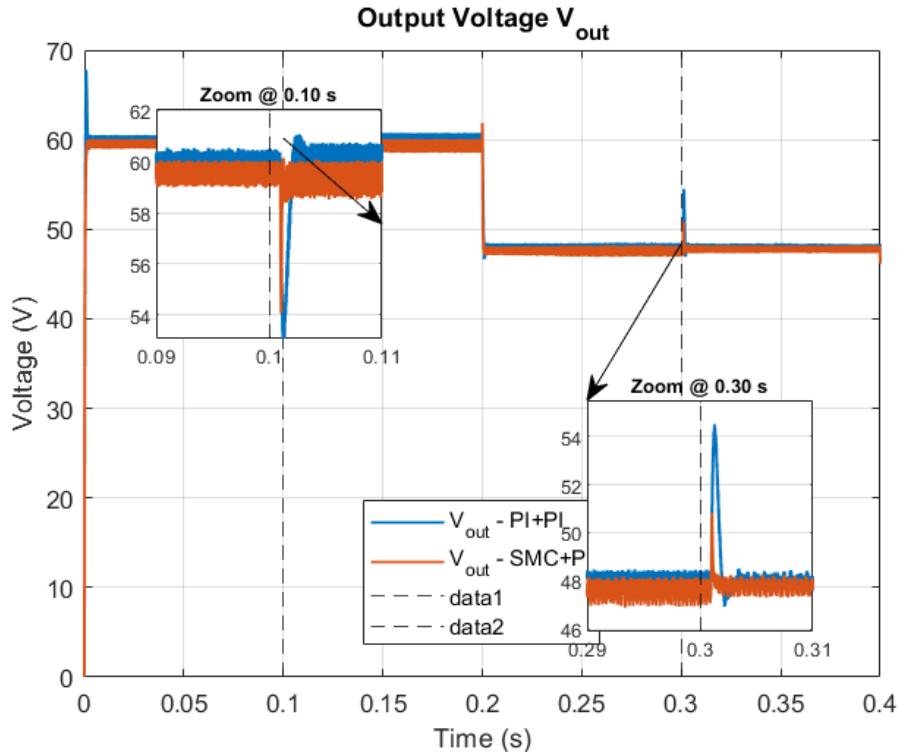


Figure 3.24: Dynamic response to load steps ( $\pm 20\%$ ) and voltage reference step

Table 3.4: Performance Comparison Between PI and SMC Controllers

Metric	PI+PI	SMC+PI
Load Change Overshoot (%)	4.2%	0.8%
Load Recovery Time (ms)	25 ms	8 ms
Settling Time (ms)	2 ms	0.8 ms
Steady-State Voltage Error (mV)	4.2 mV	1.5 mV

viability of SMC for voltage regulation in IBCs operating under real-world uncertainties and load dynamics.

## 3.14 Power Loss Modeling of Switching Devices

For high performance IBCs, accurate estimation of power losses related to switching devices is important for thermal design, optimization of control strategies, and overall efficiency evaluations.

### 3.14.1 Power Losses in MOSFET

#### MOSFET Conduction Losses

With the MOSFET ON, channel resistance  $R_{ds,ON}(T_j)$  causes loss [44]:

$$P_{cond,M} = R_{ds,ON}(T_j) I_{M,rms}^2 \quad (3.73)$$

In a boost converter (CCM, triangular ripple) the MOSFET current equals the inductor current during the ON interval, giving

$$I_{M,\text{rms}}^2 = D \left( I_{L,\text{rms}}^2 + \frac{1}{12} \Delta i_L^2 \right). \quad (3.74)$$

Temperature dependence [44]:

$$R_{\text{ds,}on}(T_j) = R_{\text{ds,}on,25^\circ C} [1 + \alpha (T_j - 25)]. \quad (3.75)$$

## Switching Losses in MOSFETs

Switching loss arises from voltage–current overlap [44]:

$$P_{\text{sw,M}} = f_s (E_{\text{on}} + E_{\text{off}}). \quad (3.76)$$

Using datasheet energies at test conditions, a practical scaling is

$$P_{\text{on/off,M}} = f_s E_{\text{test,}on/\text{off}} \left( \frac{V_{\text{sw}}}{V_{\text{test,}on/\text{off}}} \right) \left( \frac{I_{\text{sw}}}{I_{\text{test,}on/\text{off}}} \right). \quad (3.77)$$

## Gate Driver Losses

Gate-drive power (charging/discharging input charge) [45, 46]:

$$P_{\text{gate}} = f_s Q_g V_{gs}. \quad (3.78)$$

### 3.14.2 Diode Conduction Losses

During conduction, a diode exhibits a forward drop  $V_f$  and series resistance  $R_{d,\text{on}}$ . The averaged loss is

$$P_{\text{cond,D}} = V_f I_{D,\text{avg}} + R_{d,\text{on}} I_{D,\text{rms}}^2. \quad (3.79)$$

In boost CCM (diode conducts during MOSFET OFF-time),

$$I_{D,\text{avg}} = (1 - D) I_{L,\text{avg}}, \quad (3.80)$$

$$I_{D,\text{rms}}^2 = (1 - D) \left( I_{L,\text{rms}}^2 + \frac{1}{12} \Delta i_L^2 \right). \quad (3.81)$$

### 3.14.3 Diode Reverse Recovery Losses

Reverse recovery dissipates approximately

$$P_{\text{rr,D}} = f_s E_{\text{rr}}, \quad E_{\text{rr}} \approx \frac{1}{2} V_{\text{rr}} Q_{\text{rr}}. \quad (3.82)$$

For SiC Schottky diodes,  $Q_{\text{rr}} \approx 0$  so  $P_{\text{rr,D}} \approx 0$ , favoring high-frequency, high-efficiency designs.

### 3.14.4 Inductor Power Losses

In IBCs, inductors are key energy-storage elements and a major loss source. Inductor losses comprise (i) **copper losses** from winding resistance and (ii) **core losses** from hysteresis and eddy currents [47].

#### Copper Losses

Copper losses include a DC term (uniform current) and an AC term from skin/proximity effects at high frequency:

$$P_{\text{copper}} = I_{L,\text{dc}}^2 R_{L,\text{dc}} + \Delta i_{L,\text{rms}}^2 R_{L,\text{ac}} \quad (3.83)$$

with  $I_{L,\text{dc}} = I_{\text{in}}/N_{\text{phase}}$ ,  $\Delta i_{L,\text{rms}}$  the ripple RMS, and  $R_{L,\text{dc}}$ ,  $R_{L,\text{ac}}$  the DC/AC winding resistances.

#### Core Losses

Core losses depend on material, flux swing, and switching frequency. For ferrites (Ferroxcube, 3C92), manufacturer data are used via fitted models. The nonlinear B–H relation is

$$\mathcal{B}(\mathcal{H}) = \left( \frac{a_1 + b_1 \mathcal{H} + c_1 \mathcal{H}^2}{1 + d_1 \mathcal{H} + e_1 \mathcal{H}^2} \right)^{x_1} \quad (3.84)$$

where  $a_1, b_1, c_1, d_1, e_1, x_1$  are material parameters. The (Improved) Steinmetz-type core-loss density is

$$P_{\text{core,density}} = a \mathcal{B}_{\text{pk}}^b f_s^c \quad (3.85)$$

with peak flux density

$$\mathcal{B}_{\text{pk}} = \frac{\Delta \mathcal{B}}{2} = \frac{1}{2} (\mathcal{B}_{\text{ac,max}} - \mathcal{B}_{\text{ac,min}}). \quad (3.86)$$

In CCM, the inductor current has a DC component with a superimposed ripple; applying Ampère's law gives the ripple extrema of field strength as

$$\mathcal{H}_{\max/\min} = \frac{N_t}{\ell_e} \left( I_{L,\text{dc}} \pm \frac{\Delta I}{2} \right),$$

so  $\mathcal{B}_{\text{ac,max/min}} = \mathcal{B}(\mathcal{H}_{\max/\min})$ . Total core loss is

$$P_{\text{core}} = P_{\text{core,density}} V_{\text{core}},$$

with  $V_{\text{core}}$  the core volume.

### 3.14.5 Total Power Loss Model and Device Technology Selection

Aggregating MOSFET conduction/switching, diode conduction/reverse-recovery, and inductor copper/core losses, the  $N$ -phase IBC total loss is

$$P_{\text{loss,total}} = N(P_{\text{MOSFET}} + P_{\text{diode}} + P_{\text{inductor}}), \quad (3.87)$$

where

$$P_{\text{MOSFET}} = P_{\text{cond,M}} + P_{\text{on,M}} + P_{\text{off,M}} + P_{\text{gate}}, \quad (3.88)$$

$$P_{\text{diode}} = P_{\text{cond,D}} + P_{\text{rr,D}}, \quad (3.89)$$

$$P_{\text{inductor}} = P_{\text{copper}} + P_{\text{core}}. \quad (3.90)$$

This unified model supports fair efficiency and thermal comparisons across operating points and design choices.

# Chapter 4

## Design and Implementation

Practical design considerations are discussed in this chapter, which include selection criteria for magnetic cores, winding configurations, wire sizing, and available market components. The chapter also offers a detailed discussion of the development and prototype fabrication of direct and inverse coupled inductors.

### 4.1 Selection of Magnetic Cores for coupled Inductor Sizing

The choice of the core is made according to the algorithm in Fig. 4.1:

#### 4.1.1 Design and Sizing of the Magnetic Cores

The sizing of the magnetic core for 4PIBC-ICI is based on the analysis of two-phase interleaved boost converter with inversely coupled inductor (2PIBC-ICI) as first proposed by Benzine [30]. This simplification is justified, as the magnetic structure of the 4IBC-ICI is effectively constructed from multiple pairs of coupled inductors, and the magnetic behavior of each pair mirrors that of the 2IBC-ICI configuration.

For this study, an EE-type magnetic core is selected due to its widespread industrial use, ease of winding, and compatibility with coupled inductor structures [30]. The inclusion of air gaps in the core is essential to increase the saturation current capability and to fine-tune the magnetic coupling between the phases. The coupling factor is mainly determined by the size and placement of the air gaps: larger air gaps in the central branch combined with smaller air gaps in the side branches result in stronger coupling and vice versa [48].

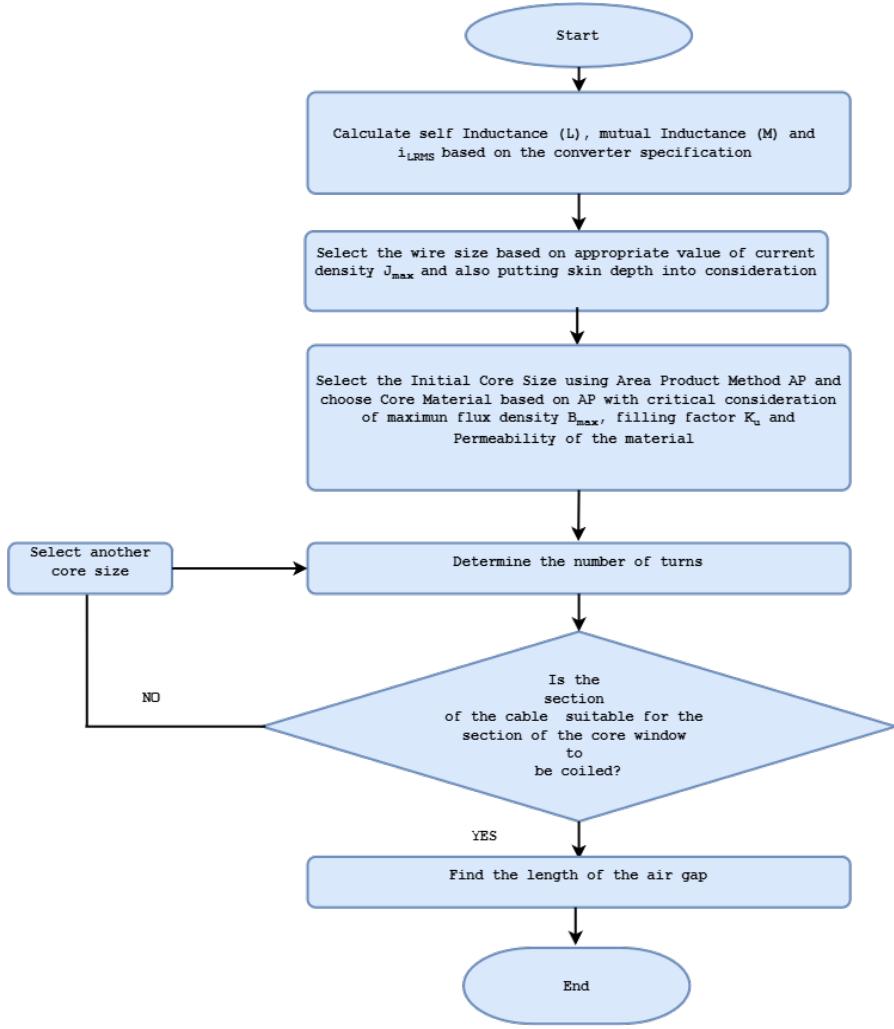


Figure 4.1: Flowchart of coupled inductor design.

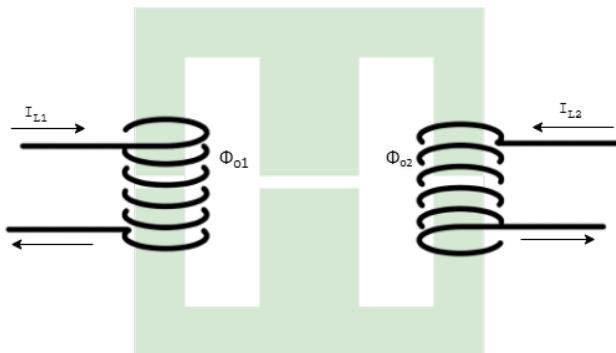
The nature of the coupling (direct or inverse) is dictated by the sign of the coupling coefficient  $k$ . A positive  $k$  denotes direct coupling, while a negative  $k$  indicates inverse coupling. In this analysis, inverse coupling is considered with a typical coupling coefficient of approximately  $k = -\frac{1}{3}$  [48], consistent with standard EE core geometries.

Figures 4.2a and 4.2b illustrate the magnetic equivalent diagram and its reluctance model, respectively. The windings are placed symmetrically on the outer legs of the core, with magnetic fluxes from each winding opposing one another. This configuration facilitates flux cancelation within the core, enabling a reduction in the overall core size and material volume.

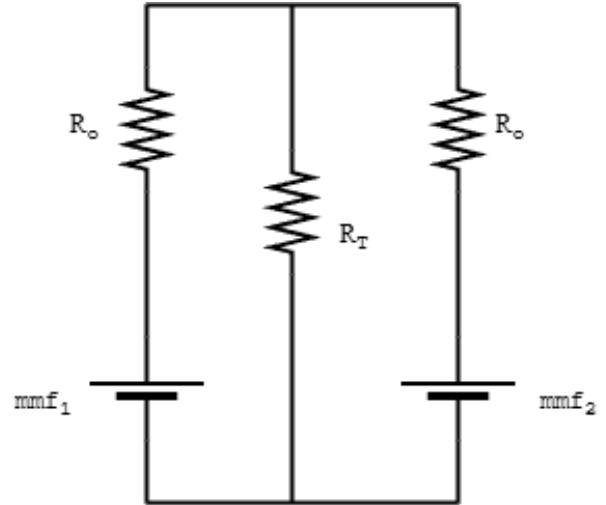
where  $\mathcal{R}_o$  is reluctance of the outer branches and the reluctance of the central branch is  $\mathcal{R}_T$ .

Applying Ampère's law and Hopkinson's analogy yields the magnetic circuit equations governing the system.

$$\begin{cases} mmf_1 = N_1 i_{L1} = \Phi_{o1} \mathcal{R}_o + (\Phi_{o1} + \Phi_{o2}) \mathcal{R}_T \\ mmf_2 = N_2 i_{L2} = \Phi_{o2} \mathcal{R}_o + (\Phi_{o1} + \Phi_{o2}) \mathcal{R}_T \end{cases} \quad (4.1)$$



(a) Equivalent diagram of the magnetic core with inversely coupled inductances.



(b) magnetic circuit based on the reluctances.

Figure 4.2: Equivalent diagram and magnetic circuit.

$\Phi_{o1}$  and  $\Phi_{o2}$  are the fluxes generated by the outside / side branches as shown in Fig. 4.2a.  $N_1$  and  $N_2$  are the number of turns of the side windings.

To have an equal distribution of the current, the number of turns of the two windings is assumed to be equal:  $N_1 = N_2 = N$ , which allows us to consider that the inductances are equal in each phase.

From the MMF equation 4.1

$$\begin{bmatrix} Ni_{L_1} \\ Ni_{L_2} \end{bmatrix} = \begin{bmatrix} \mathcal{R}_o + \mathcal{R}_T & \mathcal{R}_T \\ \mathcal{R}_T & \mathcal{R}_o + \mathcal{R}_T \end{bmatrix} \begin{bmatrix} \phi_{o1} \\ \phi_{o2} \end{bmatrix}. \quad (4.2)$$

$$\begin{bmatrix} \phi_{o1} \\ \phi_{o2} \end{bmatrix} = \mathcal{R}^{-1} \begin{bmatrix} Ni_{L_1} \\ Ni_{L_2} \end{bmatrix}. \quad (4.3)$$

$$\mathcal{R} = \begin{bmatrix} \mathcal{R}_o + \mathcal{R}_T & \mathcal{R}_T \\ \mathcal{R}_T & \mathcal{R}_o + \mathcal{R}_T \end{bmatrix}. \quad (4.4)$$

$$\mathcal{R}^{-1} = \frac{1}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} \begin{bmatrix} \mathcal{R}_o + \mathcal{R}_T & -\mathcal{R}_T \\ -\mathcal{R}_T & \mathcal{R}_o + \mathcal{R}_T \end{bmatrix}. \quad (4.5)$$

From equation 4.1, the fluxes can be expressed as:

$$\begin{bmatrix} \Phi_{o1} \\ \Phi_{o2} \end{bmatrix} = \begin{pmatrix} \frac{N(\mathcal{R}_o + \mathcal{R}_T)}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} & -\frac{N\mathcal{R}_T}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} \\ -\frac{N\mathcal{R}_T}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} & \frac{N(\mathcal{R}_o + \mathcal{R}_T)}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} \end{pmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \end{bmatrix} \quad (4.6)$$

According to Faraday's law and neglecting the internal resistances of the windings, the voltages

across the inductances are given by:

$$v_{L_1} = N \frac{d\Phi_{o1}}{dt}, \quad v_{L_2} = N \frac{d\Phi_{o2}}{dt} \quad (4.7)$$

Thus,

$$\begin{pmatrix} v_{L_1} \\ v_{L_2} \end{pmatrix} = N \frac{d}{dt} \begin{pmatrix} \frac{N(\mathcal{R}_o + \mathcal{R}_T)}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} & -\frac{N\mathcal{R}_T}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} \\ -\frac{N\mathcal{R}_T}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} & \frac{N(\mathcal{R}_o + \mathcal{R}_T)}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} \end{pmatrix} \begin{pmatrix} i_{L_1} \\ i_{L_2} \end{pmatrix} \quad (4.8)$$

$$\begin{pmatrix} v_{L_1} \\ v_{L_2} \end{pmatrix} = \begin{pmatrix} \frac{N^2(\mathcal{R}_o + \mathcal{R}_T)}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} & -\frac{N^2\mathcal{R}_T}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} \\ -\frac{N^2\mathcal{R}_T}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} & \frac{N^2(\mathcal{R}_o + \mathcal{R}_T)}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} \end{pmatrix} \begin{pmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_2}}{dt} \end{pmatrix} \quad (4.9)$$

Or,

$$\begin{cases} v_{L_1} = L_1 \frac{di_{L_1}}{dt} - M \frac{di_{L_2}}{dt} \\ v_{L_2} = L_2 \frac{di_{L_2}}{dt} - M \frac{di_{L_1}}{dt} \end{cases} \quad (4.10)$$

Neglecting magnetic leakage, the coupling coefficient is defined as:  $k = \frac{M}{\sqrt{L_1 L_2}}$  where  $L_1$  and  $L_2$  are the self-inductances, and  $M$  is the mutual inductance. Assuming the inductances are equal, then  $L_1 = L_2 = L$  and  $k = M/L$ . Due to the inverse coupling of the inductances, the coupling coefficient  $k$  is conventionally indicated with a negative sign.

By drawing an analogy between Equation 4.9 and Equation 4.10, the expressions for the self-inductance and mutual inductance in terms of the number of turns and the reluctances of the core can be derived according to [48]:

$$L = \frac{N^2(\mathcal{R}_o + \mathcal{R}_T)}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)}, \quad M = \frac{N^2\mathcal{R}_T}{\mathcal{R}_o(\mathcal{R}_o + 2\mathcal{R}_T)} \quad (4.11)$$

The coupling coefficient is defined by the relation:

$$k = \frac{M}{L} = \frac{\mathcal{R}_T}{\mathcal{R}_o + \mathcal{R}_T} \quad (4.12)$$

where,

$$\mathcal{R}_o = \frac{\delta}{\mu_0 A_o}, \quad \mathcal{R}_T = \frac{\delta}{\mu_0 A_T} \quad (4.13)$$

Here,  $A_o$  and  $A_T$  are the cross-sectional areas of the outer and central branches, respectively. The

core thickness,  $\delta$ , is assumed to be the same for all branches.

In standard EE-type cores,  $A_T \approx 2A_o$ , and thus  $\mathcal{R}_o \approx 2\mathcal{R}_T$ . Consequently,  $k = 1/3$  and  $L \approx 3M$ .

The current ripple of a boost converter with two uncoupled parallel phases (2IBC-UCI) is given by:

$$\Delta i_{fc} = \Delta i_{fc_{uncoupled}} \begin{cases} \frac{V_{fc}(1-2\alpha)}{L f_s(1-\alpha)}, & 0 < \alpha < 0.5 \\ \frac{V_{fc}(2\alpha-1)}{L f_s \alpha}, & 0.5 < \alpha < 1 \end{cases} \quad (4.14)$$

To safeguard the power converter from long-term degradation, the inductor ripple current in the power stage should not exceed 10 % of the nominal current [49].

The ratio of the ripple current in the coupled architecture to that in the uncoupled architecture is defined as follows:

$$\frac{\Delta i_{fc_{coupled}}}{\Delta i_{fc_{uncoupled}}} = \frac{1}{1-k} = \frac{L}{L-M} \quad (4.15)$$

Consequently, the coupled inductor ripple current is given by:

$$\Delta i_{fc_{coupled}} = \begin{cases} \frac{V_{fc}(1-2\alpha)}{f_s(1-\alpha)(L-M)}, & 0 < \alpha < 0.5 \\ \frac{V_{fc}(2\alpha-1)}{f_s \alpha (L-M)}, & 0.5 < \alpha < 1 \end{cases} \quad (4.16)$$

From Equation 4.16 and a standard EE core, the expression for self-inductance can be written as:

$$L = \begin{cases} \frac{3V_{fc}(1-2\alpha)}{2\Delta i_{fc}(1-\alpha)f_s}, & 0 < \alpha < 0.5 \\ \frac{3V_{fc}(2\alpha-1)}{2\Delta i_{fc}f_s}, & 0.5 < \alpha < 1 \end{cases} \quad (4.17)$$

The mutual inductance  $M$  can be found using the relation  $M = kL$ .

According to Yang et al. [50], the equivalent inductance can be expressed as:

$$L_{eq} = \begin{cases} \frac{1-k^2}{1-k\alpha} L, & 0 < \alpha < 0.5 \\ \frac{1-k^2}{1-k(1-\alpha)} L, & 0.5 < \alpha < 1 \end{cases} \quad (4.18)$$

Substituting Eq. 4.15 into Eq. 4.18  $L_{eq}$  becomes:

$$L_{eq} = \begin{cases} \frac{(L-M)(L+M)}{(L-M)(\frac{\alpha_{max}}{1-\alpha_{max}})}, & 0 < \alpha < 0.5 \\ \frac{(L-M)(L+M)}{(L-M)(\frac{1-\alpha_{max}}{\alpha_{max}})}, & 0.5 < \alpha < 1 \end{cases} \quad (4.19)$$

The worst-case effective inductor current is given by:

$$I_{L_{rms}} = \sqrt{I_{L_{max}}^2 + \frac{\Delta i_L^2}{12}} \quad (4.20)$$

where,

$$\Delta i_L = \frac{V_{fc}\alpha_{max}}{L_{eq}f_s} \quad (4.21)$$

and the average current  $I_{L_{max}}$  is:

$$I_{L_{max}} = \frac{P_{o,max}}{2\eta V_o(1-\alpha_{max})} \quad (4.22)$$

where  $\eta$  is the converter efficiency,  $P_{o,max}$  is the maximum output power,  $\alpha_{max}$  is the maximum duty cycle, and  $f_s$  is the switching frequency.

Hence, the worst-case effective inductor current is calculated as:

$$I_{L_{rms}} = \sqrt{\left(\frac{P_{o,max}}{2\eta V_o(1-\alpha_{max})}\right)^2 + \frac{1}{12} \left(\frac{V_{fc}\alpha_{max}}{L_{eq}f_s}\right)^2} \quad (4.23)$$

To prevent saturation of the core, it is essential to consider the maximum flux density under the worst-case scenario. For the coupled inductor structures illustrated in Figure 4.2a, the maximum flux density occurs in the outer leg of the core and can be expressed as:

$$B_{max} = \frac{\phi_o + \Delta\phi_o}{2A_o}, \quad (4.24)$$

where  $A_o$  is the cross-sectional area of the outer leg, and  $\phi_o$  is the DC flux of the outer leg under the worst case, which can be obtained from the magnetic circuits shown in Fig. 4.2b as:

$$\phi_o = \left(1 - \frac{\mathcal{R}_T}{\mathcal{R}_o + \mathcal{R}_T}\right) \frac{NI_{L_{dc,max}}}{\mathcal{R}_o + \mathcal{R}_o \parallel \mathcal{R}_T}, \quad (4.25)$$

where  $N$  is the actual number of turns of one phase,  $\mathcal{R}_o$  is the reluctance of the outer leg, and  $\mathcal{R}_T$  is the reluctance of the centre leg

$\Delta\phi_o$  is the peak to peak flux of the outer leg under the worst case, which can be derived from Faraday's law as:

$$\Delta\phi_o = \frac{V_{fc}\alpha_{max}}{N \cdot f_s} \quad (4.26)$$

Using the above equation 4.26, the maximum flux density under the worst case can be rewritten as:

$$B_{max} = \frac{1}{NA_o} \left[ \left( 1 - \frac{\mathcal{R}_T}{\mathcal{R}_o + \mathcal{R}_T} \right) \frac{N^2 \cdot I_{L_{dc,max}}}{\mathcal{R}_o + \mathcal{R}_o \parallel \mathcal{R}_T} + \frac{V_{fc}\alpha_{max}}{2f_s} \right] \quad (4.27)$$

Substituting equation 4.11 into equation 4.27 gives:

$$B_{max} = \frac{1}{NA_o} \left[ (L - M) I_{L_{dc,max}} + \frac{V_{fc}\alpha_{max}}{2f_s} \right] \quad (4.28)$$

From equation 4.28, The number of turns N can be calculated as:

$$N = \frac{\left[ (L - M) I_{L_{dc,max}} + \frac{V_{fc}\alpha_{max}}{2f_s} \right]}{B_{max} A_o} \quad (4.29)$$

In order to choose the Area of the wire to be used for winding, the condition below must be fulfilled.

$$A_{cu} \geq \frac{I_{L_{rms}}}{J_{max}} \quad (4.30)$$

For one core window area, the ampere-turns of one phase are equal to the current density times the conductor area of one phase, which in the worst case can be expressed as:

$$NI_{L_{rms}} = J_{max} W_a K_u \quad (4.31)$$

where  $J_{max}$  is the maximum current density,  $W_a$  is the windable surface area of one core window, and  $K_u$  filling factor or utilization factor

It is essential to verify that the windable section in the core window accommodates the wire's cross-section; therefore, this condition must be checked.

$$NA_{cu} \leq k_u W_a \quad (4.32)$$

substituting eq. 4.29 into eq. 4.31, we have

$$\frac{\left[ (L - M) I_{L_{\max}} + \frac{V_{fc} \alpha_{\max}}{2f_s} \right]}{B_{\max} A_o} I_{L_{\text{rms}}} = J_{\max} W_a K_u \quad (4.33)$$

Because  $A_T \approx 2A_o$ , Eq. 4.33 can be written as:

$$\frac{2I_{L_{\text{rms}}} \left[ (L - M) I_{L_{\max}} + \frac{V_{fc} \alpha_{\max}}{2f_s} \right]}{B_{\max} A_T} \approx J_{\max} W_a K_u \quad (4.34)$$

The Area Product AP is the Product of the windable surface area of one core window and effective cross-sectional areas of the core.

Hence,

$$AP = W_a A_T$$

$$AP = \frac{2 \times 10^4 I_{L_{\text{rms}}} \left[ (L - M) I_{L_{\max}} + \frac{V_{fc} \alpha_{\max}}{2f_s} \right]}{B_{\max} J_{\max} K_u} cm^4 \quad (4.35)$$

From equation 4.13 and assuming  $A_T \approx 2A_o$ , the air gap length  $\delta$  is

$$\delta = \frac{3N^2 \mu_o A_o}{4L} \quad (4.36)$$

where  $\mu_o$  is the permeability of vacuum

The series resistance of the inductor can be calculated from:

$$R_L = \rho_{cu} \frac{l_{cu}}{A_{cu}} \quad (4.37)$$

where  $\rho_{cu}$  is the conductivity of copper  $l_{cu}$  is the total length of the wire

At very high frequencies, the current tends to concentrate near the surface of the conductor, reducing the effective cross-sectional area which limits current penetration into the conductor. This phenomenon is known as the **skin effect**, and it increases the resistance. The skin depth  $\delta$  (in meters) is given by:

$$\delta = \sqrt{\frac{\rho_{cu}}{\pi \mu_0 f_s}} \quad (4.38)$$

Where  $\rho_{cu}$  is the resistivity of copper,  $\mu_0$  is the permeability of free space, and  $f_s$  is the switching frequency. Assuming round wire of diameter  $D_{\text{outer}}$ , the cross-sectional areas for DC and AC current flow are:

$$A_{\text{cu}} = \frac{\pi}{4} D_{\text{outer}}^2 \quad (4.39)$$

$$A_{\text{dc}} = \frac{\pi}{4} D_{\text{inner}}^2 = \frac{\pi}{4} (D_{\text{outer}} - 2\delta)^2 \quad (4.40)$$

$$A_{\text{ac}} = A_{\text{wire}} - A_{\text{dc}} \quad (4.41)$$

Hence, the resistances are given by:

$$R_{L,\text{dc}} = \rho_{\text{cu}} \cdot \frac{l}{A_{\text{dc}}}, \quad R_{L,\text{ac}} = \rho_{\text{cu}} \cdot \frac{l}{A_{\text{ac}}} \quad (4.42)$$

where  $l$  is the total winding length.

substituting  $\rho_{\text{cu}} = 1.7 \times 10^{-8} \Omega \cdot m$ ,  $\mu_0 = 4\pi \times 10^{-7} H/m$  and  $f_s = 50 \text{ kHz}$  into eq. 4.38

The skin depth  $\delta = 0.3 \text{ mm}$

The type of wire selected is **Litz wire** because in high-frequency applications, eddy current losses occur due to high frequencies. Eddy current losses increase with the frequency of the current. The root of these losses is the skin effect and proximity effect, which can be reduced by using high-frequency litz wire. In addition, the Litz wire is easier to bend in comparison to a large solid conductor. For carrying a large amount of current, several Litz wires are used.

The skin effect, which causes the current to be concentrated on a conductor's surface, requires the stranded wire dimensions to be specified on the basis of the skin depth to maximize the area of conduction. The diameter of the stranded wire,  $d_{\text{strand}}$ , is therefore set twice the depth of the skin  $\delta$ .

$$d_{\text{strand}} \leq 2\delta$$

$$d_{\text{strand}} \leq 0.6 \text{ mm}$$

From the technical table of Elektrisola Litz wire by dimensions, the chosen Litz wire has the following specifications:

The diameter  $d_{\text{strand}}$  of Litz wire chosen is 0.5mm.

The number of strands chosen is 20

The cross section of the wire to be  $3.93 \text{ mm}^2 > 2.98 \text{ mm}^2$  as calculated from Eq.4.30. Thus, the wire satisfies both current density and skin depth requirements.

### 4.1.2 Design Parameters of Coupled Inductors for 2PIBC

After completing all the necessary analytical calculations in Section 4.1.1, Table 4.1 summarizes the key design parameters of the coupled inductors used in 2PIBC. The parameters were carefully chosen to ensure maximum performance, considering factors such as magnetic characteristics, core material, winding characteristics, and other relevant factors that influence the operational behavior of the converter.

Table 4.1: 2PIBC Core Parameters from Datasheet and Calculated Values

Parameter	Calculated Value	Chosen Value (from datasheet)	Unit
Core Ref.	–	E56/24/19	–
Effective Core Area ( $A_e$ )	–	337	$\text{mm}^2$
Effective Core Length ( $l_e$ )	–	107	mm
Core Weight	–	90 x 4	g
Effective Core Volume ( $V_e$ )	–	36000 x 4	$\text{mm}^3$
Winding Area ( $W_a$ )	–	222	$\text{mm}^2$
Average Winding Length	–	112	mm
Area Product ( $A_e \times W_a$ )	–	74800	$\text{mm}^4$
Material Type	–	3C92	–
Material Permeability ( $\mu_e$ )	–	1320	–
Max. Saturation Flux Density ( $B_{max}$ )	–	0.3	T
Number of Turns (N)	14	14	–
Air Gap ( $\delta$ )	0.65	$\approx 0$	mm
Cable Cross Section ( $A_{cu}$ )	2.98	3.31	$\text{mm}^2$
Total Cable Length (l)	1.57	1.57	m
Max. Current Density ( $J_{max}$ )	–	6	$\text{A/mm}^2$
Filling Factor ( $K_u$ )	–	0.3	–
Copper Resistivity ( $\rho_{cu}$ )	–	$1.7 \times 10^{-8}$	$\Omega \cdot \text{m}$
Inductance Series Resistance (rL)	8.05	10	$\text{m}\Omega$
Self-Inductance (L)	48	47	$\mu\text{H}$
Coupling Coefficient (k)	–	-1/3	–
Capacitance (C)	–	100	$\mu\text{F}$

### 4.1.3 Core Selection for 4PIBC-ICI connected in cascaded cyclic architecture

The design of the cascaded cyclic 4PIBC-ICI topology was carried out following the same algorithm as shown in Figure 4.1. This structured process ensures consistency in the design process while supporting the unique requirements characteristic of the four-phase structure. However, because of the increased number of phases and improved current distribution, the current through each inductor is significantly reduced. This reduction in inductor current allows for the minimization of core size and volume.

For the four-phase topology, the maximum rms current  $I_{LRMS}$  is 10.2 A. Based on this current

rating, the core size was re-evaluated. As a result, the new core reference chosen and adapted for the cascaded cyclic 4PIBC-ICI topology is E42/21/15. This core provides the necessary magnetic characteristics and physical size suitable for reducing current stress while at the same time enabling efficient operation, proper thermal management, and reduced magnetic losses.

In addition, the optimization process led to a 52% reduction in the total volume of the four magnetic cores compared to the initial two-phase converter setup. This significant reduction enables better overall power density and reduces the compactness of the converter. The detailed sizing of the optimized magnetic cores utilized by the four-phase converter are shown in Table 4.2

Table 4.2: 4PIBC Core Parameters from Datasheet and Calculated Values

Parameter	Calculated Value	Chosen Value (from datasheet)	Unit
Core Ref.	–	E42/21/15	–
Effective Core Area ( $A_e$ )	–	178	$\text{mm}^2$
Effective Core Length ( $l_e$ )	–	97	mm
Core Weight	–	44 x 4	g
Effective Core Volume ( $V_e$ )	–	17300 x 4	$\text{mm}^3$
Winding Area ( $W_a$ )	–	178	$\text{mm}^2$
Average Winding Length	–	93	mm
Area Product ( $A_e \times W_a$ )	–	31700	$\text{mm}^4$
Material Type	–	3C92	–
Material Permeability ( $\mu_e$ )	–	1350	–
Max. Saturation Flux Density ( $B_{max}$ )	–	0.3	T
Number of Turns (N)	16	16	–
Air Gap ( $\delta$ )	0.45	$\approx 0$	mm
Cable Cross Section ( $A_{cu}$ )	1.7	2.08	$\text{mm}^2$
Total Cable Length (l)	1.5	1.5	m
Max. Current Density ( $J_{max}$ )	–	6	$\text{A/mm}^2$
Filling Factor (K <sub>u</sub> )	–	0.3	–
Copper Resistivity ( $\rho_{cu}$ )	–	$1.7 \times 10^{-8}$	$\Omega \cdot \text{m}$
Inductance Series Resistance (rL)	12.3	15	$\text{m}\Omega$
Self-Inductance (L)	48	47	$\mu\text{H}$
Coupling Coefficient (k)	–	-1/3	–
Capacitance (C)	–	100	$\mu\text{F}$

## 4.2 Validation of Magnetic Model of 2PIBC-CI on PLECS

The PLECS software includes a complete set of components intended for magnetic environment modeling. This feature allows for accurate simulation of magnetic components such as saturable magnetic cores through the description of their non-linear magnetic characteristics. In the simulation environment, users are provided with the ability to input core parameters e.g. B-H curve, core material characteristics, geometric setup, and air gaps, thus ensuring an accurate representation of the core behavior in the real world under different operating conditions.

In this study, the magnetic core of the coupled inductor is modeled using the Magnetic Circuit feature in the PLECS software, shown in Fig. 4.3. The core configuration consists of two EE-type cores, which align according to the physical arrangement shown in Figure 4.2a. This is a model of the traditional structure of inversely coupled inductors used in multiphase IBCs.

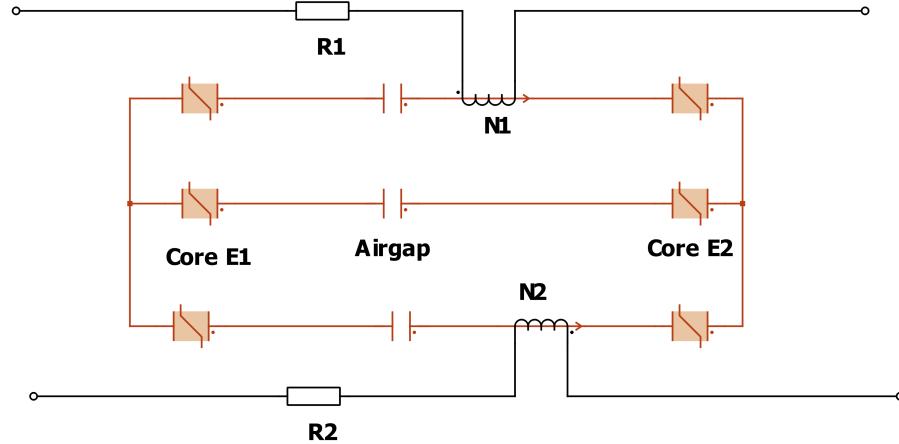


Figure 4.3: Modeling of the core with two coupled inductances on PLECS software

#### 4.2.1 Simulation results and design validation of Magnetic Models on PLECS

To validate the design, the coupled inductance was simulated on PLECS software for  $t=0.2s$ . The simulation aimed to assess the magnetic behavior, particularly the flux density distribution in the core legs, and ensure that the design operates within the defined magnetic limits.

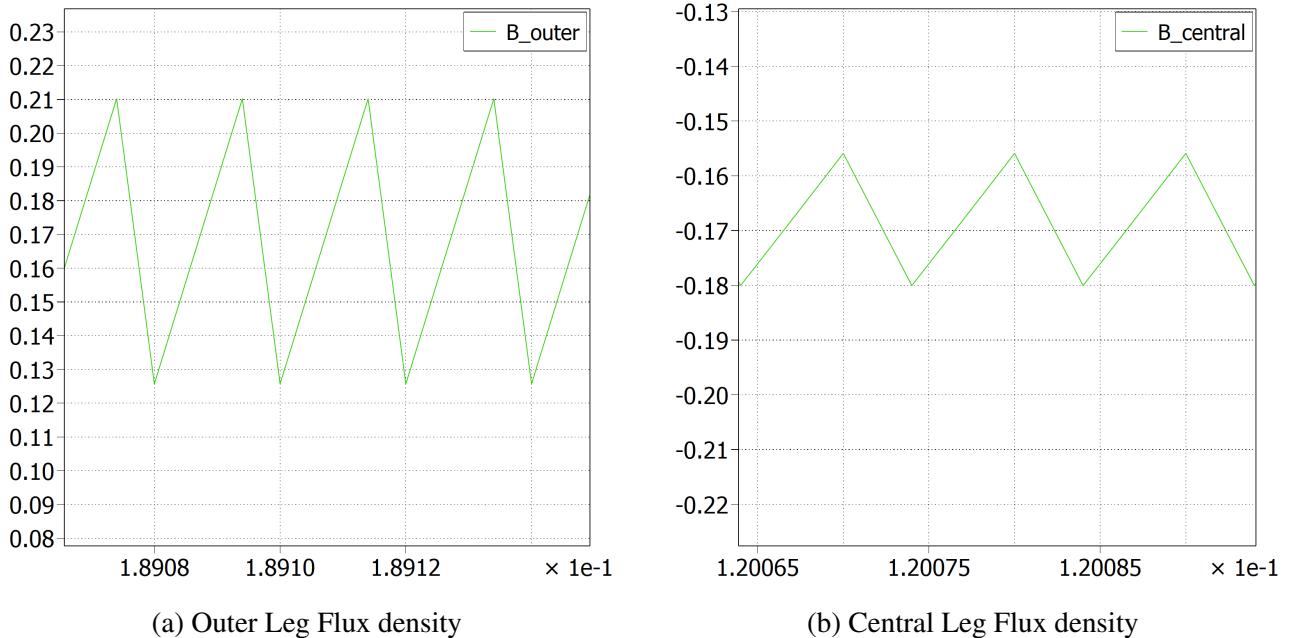


Figure 4.4: Flux densities in the outer and central legs

The result in outer legs of the EE core Fig. 4.4a shows that flux density ranges from  $0.13T$  (min) to  $0.21T$  (max)

with a mean value of  $0.17T$ . Also, the flux densities in the right outer leg is identical to the left outer leg

The result in the central leg of the core in Fig. 4.4b shows that the flux density ranges from  $-0.18T(\min)$  to  $-0.16T(\max)$  with a mean value of  $-0.17T$ , confirming the expected inverse magnetic behavior.

The results validate the inverse coupling properties of the core, where the central leg carries flux in the opposite direction to the outer legs. Importantly, the mean flux density ( $0.17T$ ) in the outer legs of the design is below the target  $B_{max} = 0.3T$ , it is well below the core saturation flux density,  $B_{sat} = 0.52T$ . This confirms that the core operates safely in the linear region without the risk of magnetic saturation.

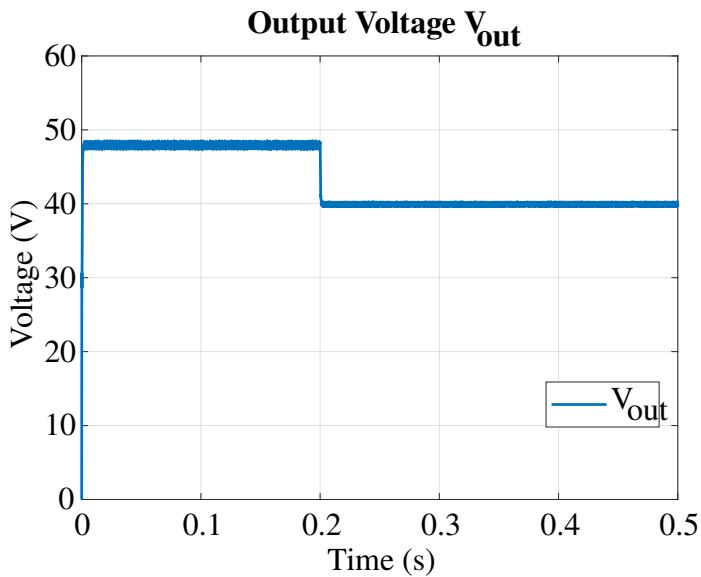


Figure 4.5: Output Voltage Plots of Magnetic Model

Additionally, the simulation verifies that the output voltage and coupled inductor voltage waveforms in Fig.4.5 closely match the expected results from the electrical model in Fig.3.20, demonstrating the accuracy of both magnetic and electrical modeling in PLECS.

#### 4.2.2 FEMM Finite Element Validation

The use of Finite-Element Method Magnetics (FEMM) allows us to extensively assess the electromagnetic fields, which are a great addition to PLECS circuit simulations. This method is particularly beneficial for studying the magnetic flux densities' distribution in the cores of the coupled inductor [51].

A 2-D magnetostatic model of the same EE core was solved in FEMM to independently verify

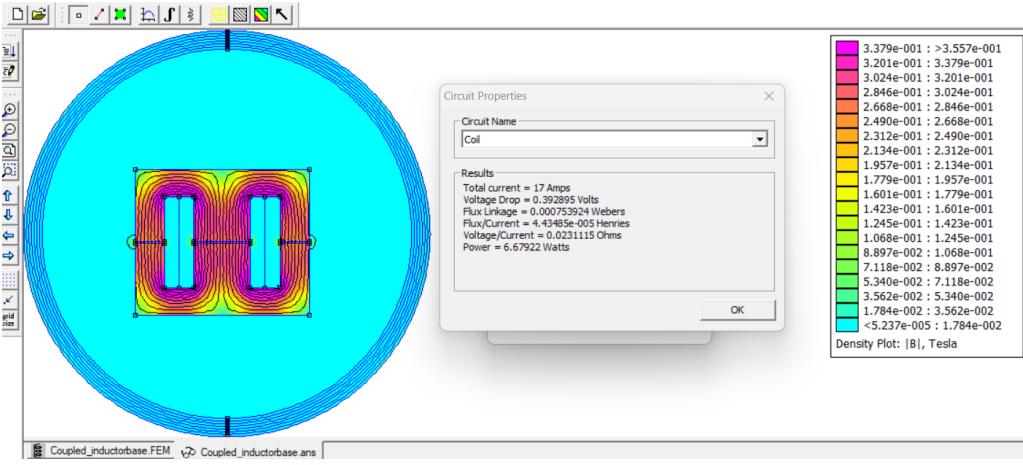


Figure 4.6: Finite Element Method Magnetics (FEMM) of coupled inductor

the analytical and PLECS results. The coil was excited with the rated current, and the post-processor returned a flux linkage of  $7.539 \times 10^{-4}$  Wb for a total current of 17 A. Using

$$L = \frac{\Psi}{I}, \quad (4.43)$$

the inductance is  $L_{\text{FEMM}} = 44.3 \mu\text{H}$ . This agrees closely with the analytical prediction  $L_{\text{analytical}} = 48 \mu\text{H}$ , giving a deviation of

$$\frac{|48 - 44.3|}{48} \times 100\% \approx 7.7\%.$$

Such an error margin is acceptable considering the 2-D approximation, discretisation errors, and neglected leakage/fringing paths in the analytical model.

The FEMM density plot (Fig. 4.6) shows that the outer legs operate between roughly 0.17 T and 0.30 T, which is consistent with the PLECS time-domain results (0.13–0.21 T averaged at 0.17 T). Minor hotspots near sharp corners and air interfaces reveal a small fringing effect: the flux lines slightly bulge out of the core window and around the air gaps. This raises the local flux density, but remains below the saturation threshold. The fringing also increases the effective cross-sectional area seen by the gap, explaining part of the small discrepancy between analytical and FEMM inductance values.

Table 4.3: Comparison of key results across methods

Parameter	Analytical	FEMM	PLECS
Inductance $L$ [ $\mu\text{H}$ ]	48	44.3	—
Outer leg $B$ range [T]	—	0.17–0.30	0.13–0.21
Mean $B$ outer leg [T]	—	$\approx 0.20$	0.17
Central leg $B$ sign	Opposite	Opposite	Opposite

## 4.3 Practical Prototype Construction of the Coupled Inductor

This section gives a step-by-step detail process for preparing the windings, assembling the EE cores, and implementing protective measures to achieve a reliable and functional coupled inductor.

### 4.3.1 Wire Preparation

Due to the unavailability of a single wire with the required cross-sectional area in the market, a custom wire was fabricated by twisting 20 strands of 0.5mm enameled copper wire into a single conductor. This process was performed manually in the laboratory to achieve the necessary current-carrying capacity and minimize skin-effect loss at high frequencies, which are critical for 2PIBC performance. The strands were carefully aligned and twisted uniformly to ensure consistent electrical properties along the length of the wire. The resulting twisted wire was then wound around the EE core, as specified in the design calculations in the table. 4.1. Figure 4.7 illustrates the twisted wire bundle prepared for the inductor wires.



Figure 4.7: Twisted bundle of 20 strands of 0.5mm enameled copper wire prepared in the laboratory.

### 4.3.2 EE Core Assembly with Air Gaps

The magnetic core chosen for the coupled inductor was the E56/24/19 EE core made of 3C92 ferrite material, as selected in Table 4.1. The EE core was assembled with air gaps with a coupling coefficient of  $k = -\frac{1}{3}$ , as discussed in Section 4.1.1 to control inductance and prevent core saturation, a critical

requirement for high-current operation in the 2PIBC topology. To maintain the air-gap spacing during operation, a small amount of industrial-grade glue was applied between the core halves and the spacers. This ensured mechanical stability without affecting the magnetic properties of the core.

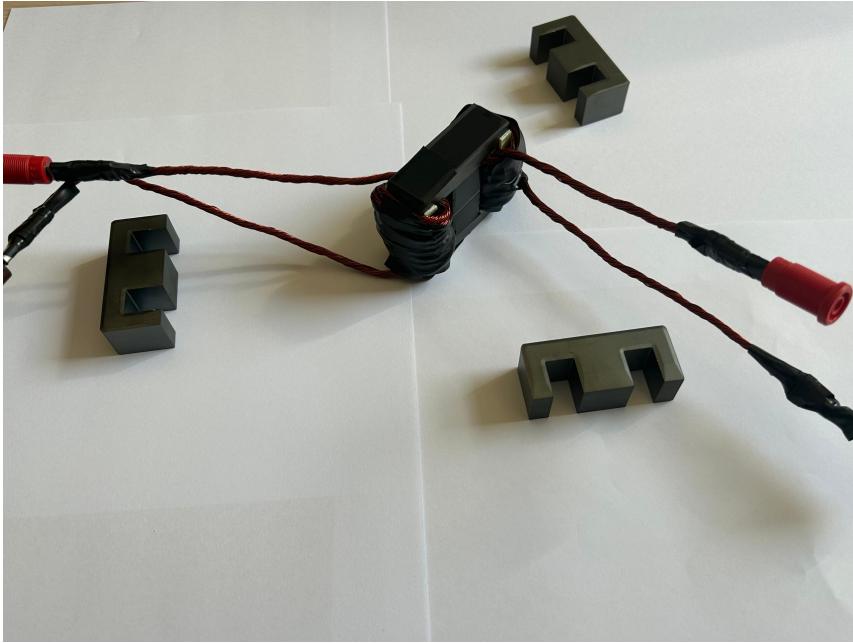


Figure 4.8: Assembled coupled inductor with EE cores, air gaps, protective PCB strips, and insulating tape securing the assembly.

To prevent twisted wire from scratching the EE core surface, which could damage the wire insulation and lead to short circuits, residual printed circuit board material (PCB) was utilized. The PCB was cut into thin strips using a precision tool and placed between the wire and the core at points of contact. This protective layer protected the integrity of the wire and maintained the structural reliability of the windings during assembly and operation.

Finally, to hold the EE core halves firmly together, insulating tape was wrapped around the core assembly. Multiple layers of tape were applied to ensure mechanical stability, preventing movement of the core halves under operational stresses such as vibration or thermal expansion. This simple yet effective method secured the air gaps and windings in place, ensuring the inductor performance during testing and integration into the 2PIBC prototype. Figure 4.8 shows the coupled inductor assembled with the EE cores, air gaps, protective PCB strips, and insulating tape.

## 4.4 Justification for SiC Device Selection

In this study, Silicon Carbide (SiC) MOSFETs and Schottky diodes are selected for all switching and rectifying functions in the IBC topology. This decision is based on the detailed analysis and

recommendations in the doctoral work of Wang [45], which highlight the thermal and efficiency advantages of wide-bandgap (WBG) devices over conventional silicon components, especially in high-power, high-frequency applications.

In order to maintain high efficiency and compact design, the **C3M0015065D** discrete SiC power MOSFET, manufactured by **CREE® (Wolfspeed)**, has been selected. This device offers several advantages in high-frequency DC-DC converter applications, including reduced switching losses and improved thermal performance. The key electrical characteristics are summarized in **Table 4.4**. Specifically, the **maximum drain-source voltage** is **650 V**, which comfortably exceeds the maximum output voltage of the converter  $V_{out_{max}}$  of 48 V. Furthermore, the **continuous drain current** capability at a case temperature of 100 °C is **96 A**, well above the worst-case  $I_{L_{max}}$  of 17.9 A, ensuring safe operation under all expected conditions.

Similarly, the **C6D20065D** SiC Schottky diode from **CREE® (Wolfspeed)** has been chosen. Its essential parameters are listed in **Table 4.5**. The diode offers a **repetitive peak reverse voltage** ( $V_{RRM}$ ) of **650 V**, satisfying the requirement set by  $V_{out_{max}}$ . Under the worst-case thermal condition ( $T_c = 155$  °C), the device supports a continuous forward current ( $I_F$ ) of **20 A**, and up to **40 A** when the case temperature is limited to 125 °C. Given that the expected ambient operating temperature of the converter is approximately **25 °C**, the actual junction temperature will remain well below critical limits during operation. Therefore, the selected SiC Schottky diode provides a reliable and thermally safe solution for the intended application.

Both the SiC MOSFET and Schottky diode meet and exceed the electrical and thermal requirements of the converter, supporting efficient and reliable operation while contributing to a compact and lightweight system design.

Table 4.4: The parameters of SiC MOSFET (C3M0015065D) used in the converter

Symbol	Parameter	Value	Unit	Test Conditions
$V_{DSS}$	Drain-Source Voltage	650	V	$V_{GS} = 0$ V, $I_D = 100$ µA
$I_D$	Continuous Drain Current	120 96	A	1) $T_C = 25$ °C 2) $T_C = 100$ °C
$T_J, T_{stg}$	Junction and Storage Temp.	-40 to +175	°C	-
$R_{DS(on)}$	On-State Resistance	15 20	mΩ	1) $T_J = 25$ °C 2) $T_J = 175$ °C
$E_{ON}$	Turn-On Energy	1.5	mJ	$V_{DS} = 400$ V, $I_D = 55.8$ A, $T_J = 175$ °C
$E_{OFF}$	Turn-Off Energy	0.7	mJ	Same as above
$R_{\theta JC}$	Thermal Resistance (J-C)	0.35	°C/W	-

Table 4.5: The parameters of SiC Schottky diode (C6D20065D) used in the converter

Symbol	Parameter	Value	Unit	Test Conditions
$V_{RRM}$	Repetitive Peak Reverse Voltage	650	V	-
$I_F$	Continuous Forward Current (leg/device)	38/76	A	1) $T_C = 25^\circ\text{C}$
		20/40		2) $T_C = 125^\circ\text{C}$
		10/20		3) $T_C = 155^\circ\text{C}$
$T_J$	Junction Temperature Range	-55 to +175	°C	-
$T_{stg}$	Storage Temperature	-55 to +175	°C	-
$V_F$	Forward Voltage	1.5	V	$I_F = 10 \text{ A}, T_J = 25^\circ\text{C}$
$I_R$	Reverse Leakage Current	50 $\mu\text{A}$		$V_R = 650 \text{ V}, T_J = 25^\circ\text{C}$
$Q_C$	Total Capacitive Charge	35	nC	$V_R = 400 \text{ V}, T_J = 25^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance (J-C)	0.64(min) 1.3(max)	°C/W	per device

#### 4.4.1 Power Loss Analysis and Efficiency Comparison

The total power losses and efficiency of the converters are shown in Table 4.6. Since the parameter values of SiC MOSFETs and SiC Schottky diodes vary significantly with the semiconductor junction temperature, it is important to evaluate the maximum power losses of each component under the worst-case thermal conditions. we will consider a junction temperature of  $T_j = 125^\circ\text{C}$  as the worst case for both devices, according to the manufacturers' datasheets.

The analytical calculations gives the following component losses: 7.9 W for the SiC MOSFET, 5.5 W for the SiC Schottky diode, and 4.2 W for the inductor. This results in a total loss of 17.6 W at a nominal output power of 500 W, leading to an estimated efficiency of approximately 97%.

However, simulation results from PLECS showed 5.76 W for the MOSFET, 3.7 W for the diode, and 4.2 W for the inductor. The total simulated losses were 13.84 W at a measured output power of 477 W, which also yields an efficiency of 97%.

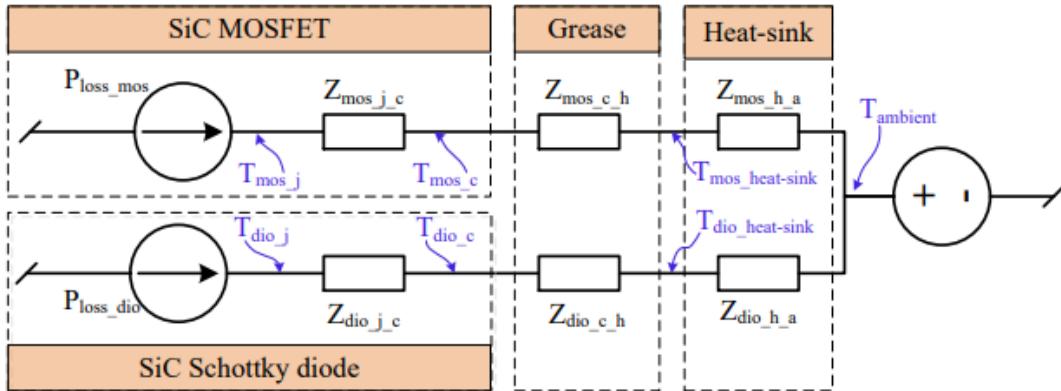
Table 4.6: Comparison of Analytical and Simulated Power Losses and Efficiency

Component / Metric	Analytical Results	Simulation Results
SiC MOSFET Loss	7.9 W	5.76 W
SiC Diode Loss	5.5 W	3.7 W
Inductor Loss	4.2 W	4.2 W
<b>Total Power Loss</b>	<b>17.6 W</b>	<b>13.66 W</b>
Output Power	500 W (nominal)	477 W (simulated)
<b>Efficiency</b>	<b>97%</b>	<b>97%</b>

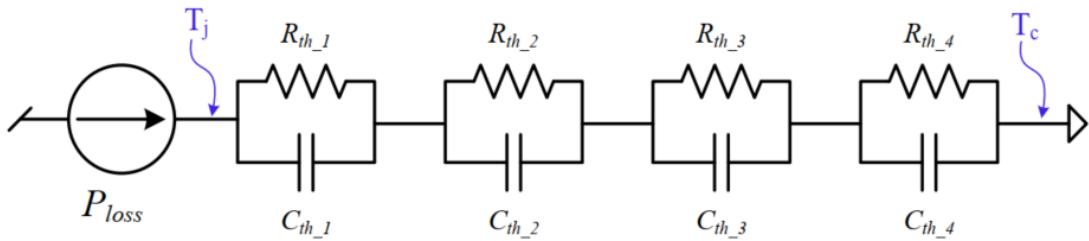
The discrepancies between analytical and simulation results arise because analytical models use fixed worst-case values leading to overestimated losses, while simulations account for realistic temperature changes, duty cycles, and switching overlaps, resulting in lower average losses.

#### 4.4.2 Thermal Analysis

The thermal performance of semiconductor devices greatly impacts converter reliability, efficiency, and compactness. Given the high power density and switching frequency of the selected SiC MOSFET and Schottky diode, careful thermal analysis is critical. The thermal equivalent circuits used for both the SiC MOSFET and the diode are presented in Fig. 4.9.



(a) Single SiC MOSFET and SiC Schottky diode thermal model from junction to ambient. [45].



(b) Junction-to-case Foster RC thermal network for the switching device. [45].

Figure 4.9: The thermal model of the SiC MOSFET and SiC Schottky diode from junction to ambient

The thermal model includes three main parts: the device junction-to-case resistance ( $R_{\theta JC}$ ), thermal grease resistance ( $R_{\theta CS}$ ), and the heat sink resistance ( $R_{\theta SA}$ ). The total thermal impedance from the device junction to ambient ( $R_{\theta JA}$ ) is the sum of these components as:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (4.44)$$

To ensure safe thermal operation, the junction temperature  $T_j$  must remain below the maximum allowable temperature provided by the manufacturer's datasheet (typically 175,°C for SiC devices). The design equation used to determine the required heat-sink resistance is given by:

$$R_{\theta SA} = \frac{T_j - T_a}{P_{loss}} - (R_{\theta JC} + R_{\theta CS}) \quad (4.45)$$

where:  $T_j$ : Maximum junction temperature (selected as 125°C)

$T_a$ : Ambient temperature (assumed 25°C)

$P_{loss}$ : Device power loss obtained from analytical calculations and simulation

$R_{\theta JC}$ : Junction-to-case thermal resistance (from the datasheet)

$R_{\theta CS}$ : Thermal grease resistance (assumed 0.1°C/W as per standard practice)

Simulated power losses are used to select practical heat sinks based on available datasheet parameters, including a safety margin of 20 to 30%.

#### 4.4.3 SiC MOSFET Thermal Analysis

For the selected SiC MOSFET (C3M0015065D), the simulation results from PLECS indicated power losses of approximately 5.94,W under steady-state operation. The MOSFET junction-to-case thermal resistance provided by the datasheet is  $R_{\theta JC} = 0.35^\circ\text{C}/\text{W}$ .

Using the selected values:

$T_j = 125^\circ\text{C}$ ,  $T_a = 25^\circ\text{C}$ ,  $P_{loss} = 5.94\text{ W}$  We obtain the thermal impedance required as follows:

$$R_{\theta SA, \text{MOSFET}} = \frac{125 - 25}{5.94} - (0.35 + 0.1) \approx 17^\circ\text{C}/\text{W}$$

However, this heatsink-ambient thermal impedance operation will be very close to the target junction temperature ( $125^\circ\text{C}$ ), which may affect long-term reliability. Based on the provided heatsink datasheet Fig. 4.11, a more robust thermal management strategy is recommended. Selecting a heat sink with significantly lower thermal impedance (approximately  $11^\circ\text{C}/\text{W}$  or lower) ensures a lower junction temperature and improved reliability. The following updated calculation is considered to ensure a safer operating margin.

$$P_{loss,mos} @ 5.76\text{W} \approx 49^\circ\text{C}$$

Under ideal conditions, the temperature of the environment remains constant.

$$R_{\theta SA, \text{mos}} = \frac{49^\circ\text{C}}{5.76} = 8.5^\circ\text{C}/\text{W}$$

Applying a 30% safety factor to account for uncertainties and practical limitations:

$$R_{\theta SA, \text{MOSFET (safe)}} = 8.5 \times 1.3 \approx 11^\circ\text{C}/\text{W}$$

To verify the suitability of the selected heat sink ( $11^\circ\text{C}/\text{W}$ ), analytical calculations were performed to estimate the junction temperature ( $T_j$ ) of the MOSFET shown in Fig.4.10, which is then compared with the simulation results obtained from PLECS.

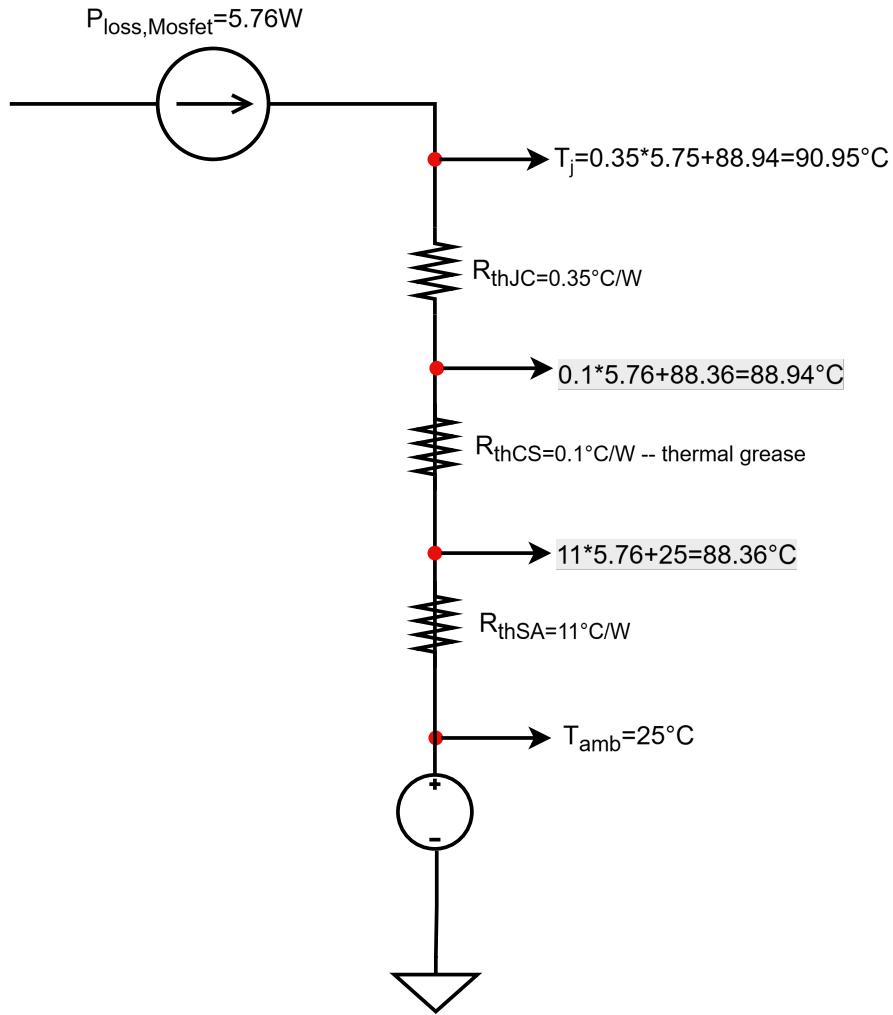


Figure 4.10: Analytical Estimation of MOSFET Junction Temperature  $T_j$

#### 4.4.4 SiC Schottky Diode Thermal Analysis

For the selected SiC Schottky diode (C6D20065D), the simulation results of PLECS showed power losses of approximately 3.7,W. The thermal impedance from the diode junction to the case in the datasheet is  $R_{\theta JC} = 1.3^{\circ}\text{C}/\text{W}$ .

Using the selected values:

$T_j = 125^{\circ}\text{C}$ ,  $T_a = 25^{\circ}\text{C}$ ,  $P_{loss} = 3.7 \text{ W}$  We obtain the required thermal impedance as follows:

$$R_{\theta SA, \text{Diode}} = \frac{125 - 25}{3.7} - (1.3 + 0.1) \approx 26^{\circ}\text{C}/\text{W}$$

Again, this thermal impedance will make the junction temperature approach the safe limit. A significantly lower heat-sink impedance is preferable, a more conservative selection is recommended, and can be calculated based on the provided datasheet in Fig.4.11.

$$P_{loss,dio} @ 3.7 \text{ W} \approx 32^{\circ}\text{C}$$

Under ideal conditions, the temperature of the environment remains constant.

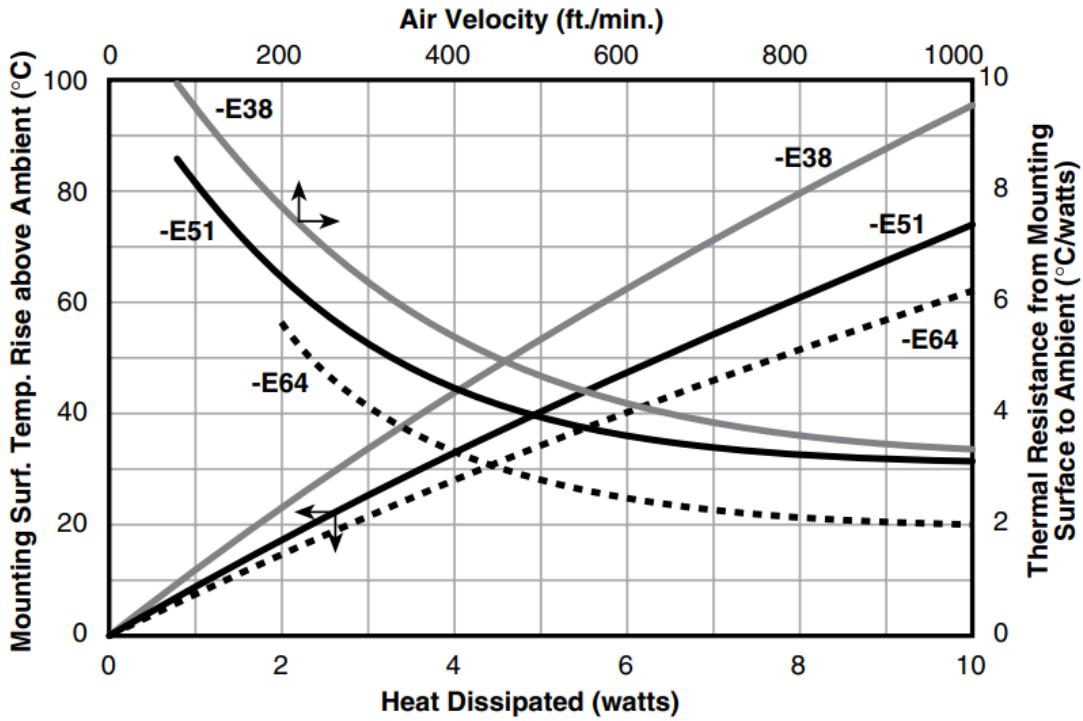


Figure 4.11: E-Series HeatSinks Datasheet

$$R_{\theta SA,mos} = \frac{32^\circ C}{3.7} = 8.6^\circ C/W$$

Applying a 30% safety factor to account for uncertainties and practical limitations:

$$R_{\theta SA,MOSFET \text{ (safe)}} = 8.6 \times 1.3 \approx 11^\circ C/W$$

Thus, to improve reliability and long-term performance, a heat sink with a thermal impedance of  $11^\circ C/W$  or lower is recommended for both the MOSFET and the diode.

Furthermore, to verify the suitability of the selected heat sink ( $11^\circ C/W$ ), analytical calculations were performed to estimate the junction temperatures ( $T_j$ ) of the diode shown in Fig.4.12, which is then compared with the simulation results obtained from PLECS.

#### 4.4.5 Thermal Simulation Results

The results of the PLECS simulation further validate the selected heatsink and provide steady-state and transient temperature profiles for both devices, shown in Fig.4.13 and Fig.4.14. The MOSFET and diode junction temperatures reach steady-state values significantly below the maximum allowable limit ( $125^\circ C$ ), confirming the suitability of the selected thermal management solution.

The analytical values in Fig.4.10 and Fig.4.12 closely match the junction temperature obtained in the PLECS thermal simulations, which indicated a steady-state junction temperature around  $91^\circ C$  for MOSFET in Fig.4.13. The analytical calculation of the diode is again closely aligned with the PLECS

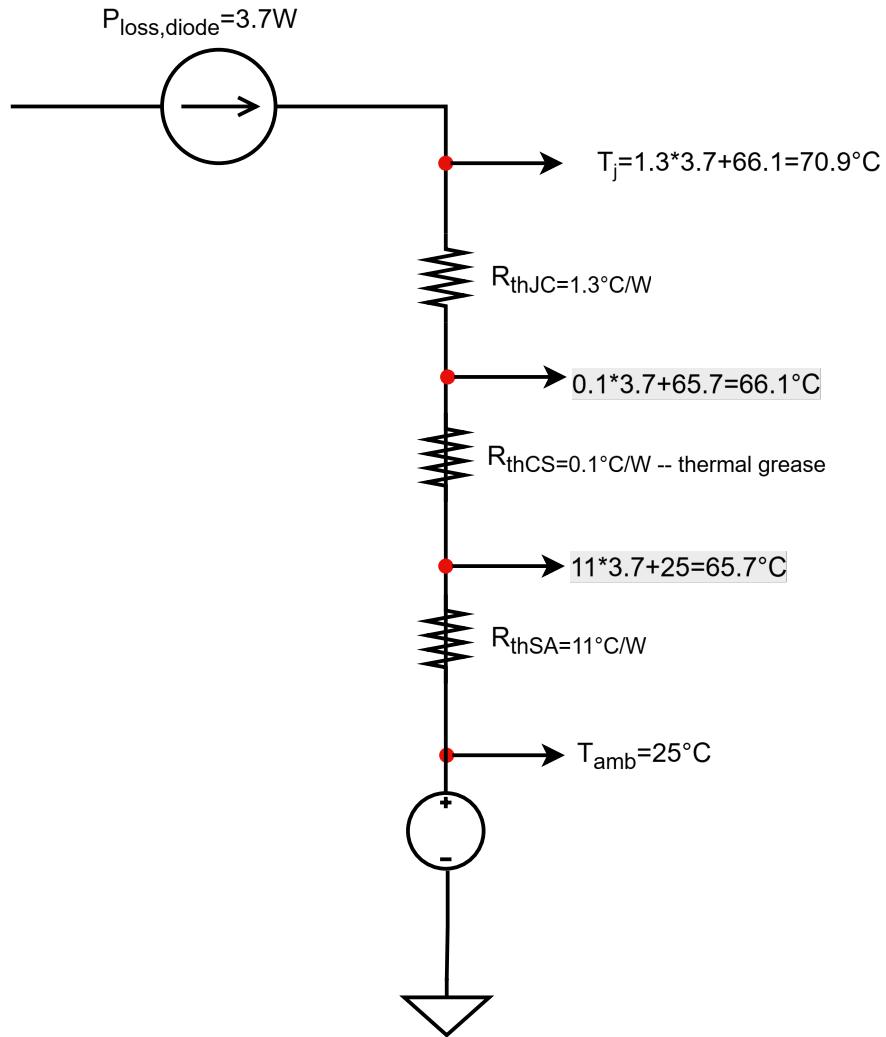


Figure 4.12: Analytical Estimation of Diode Junction Temperature  $T_j$

simulation results in Fig.4.14, which indicated a junction temperature around  $70^\circ\text{C}$ . This confirms the accuracy of the analytical approach and the appropriateness of the heat sink chosen.

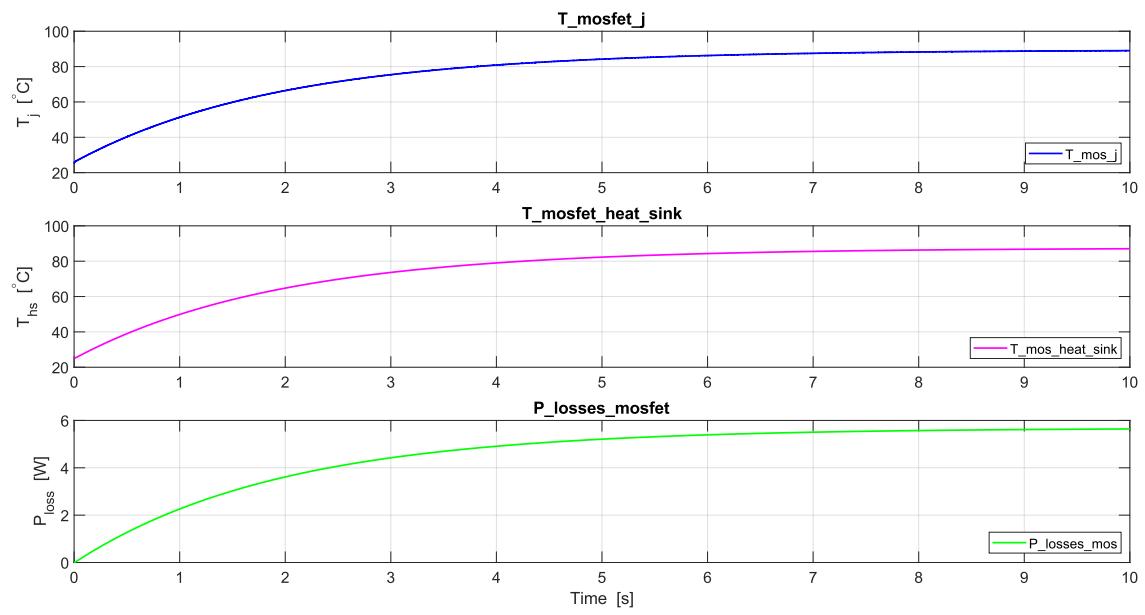


Figure 4.13: MOSFET thermal simulation: Junction temperature, heat-sink temperature, and power loss evolution

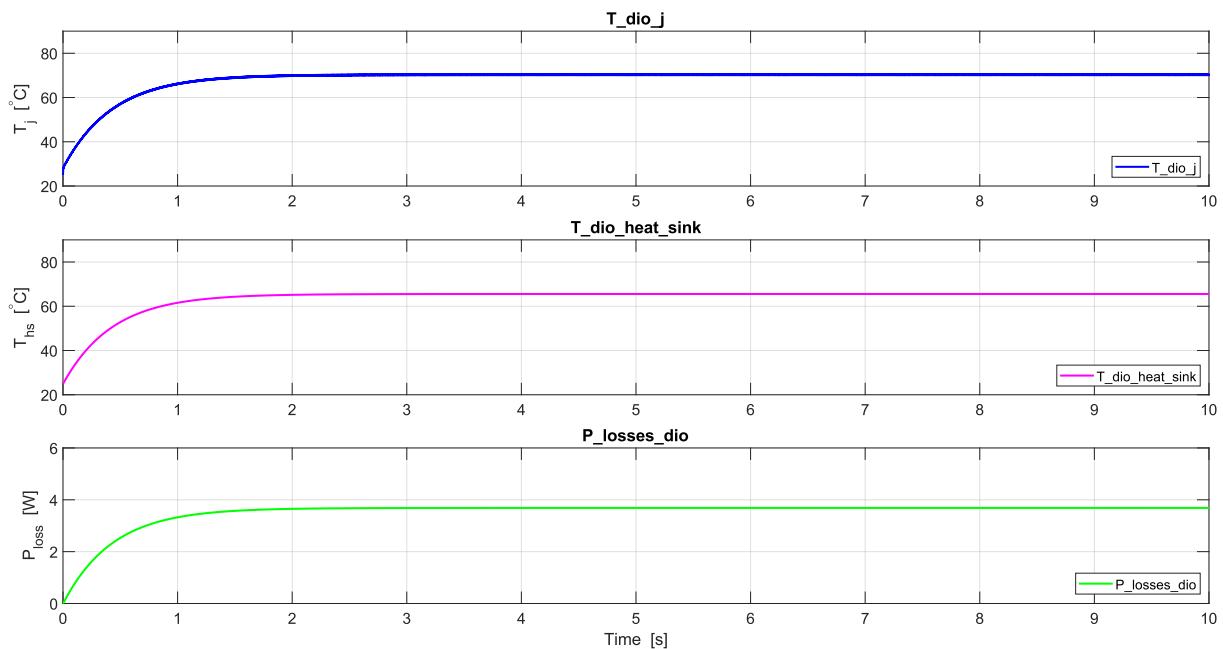


Figure 4.14: Diode thermal simulation: Junction temperature, heat-sink temperature, and power loss evolution.

# Chapter 5

## Experimental Validation

The experimental validation of the two-phase interleaved boost converter (2PIBC) with coupled inductors was performed using the dSPACE 1104 real-time control platform. The objective was to implement and test the control strategy developed for 2PIBC, focusing on generating PWM signals with a 180-degree phase shift to drive the MOSFET gates and to measure critical output signals such as the coupled inductor current and voltage. The main laboratory hardware setup shown in Fig. 5.1. This section details the experimental setup, the challenges encountered during PWM signal generation, and the implications for the converter's performance.

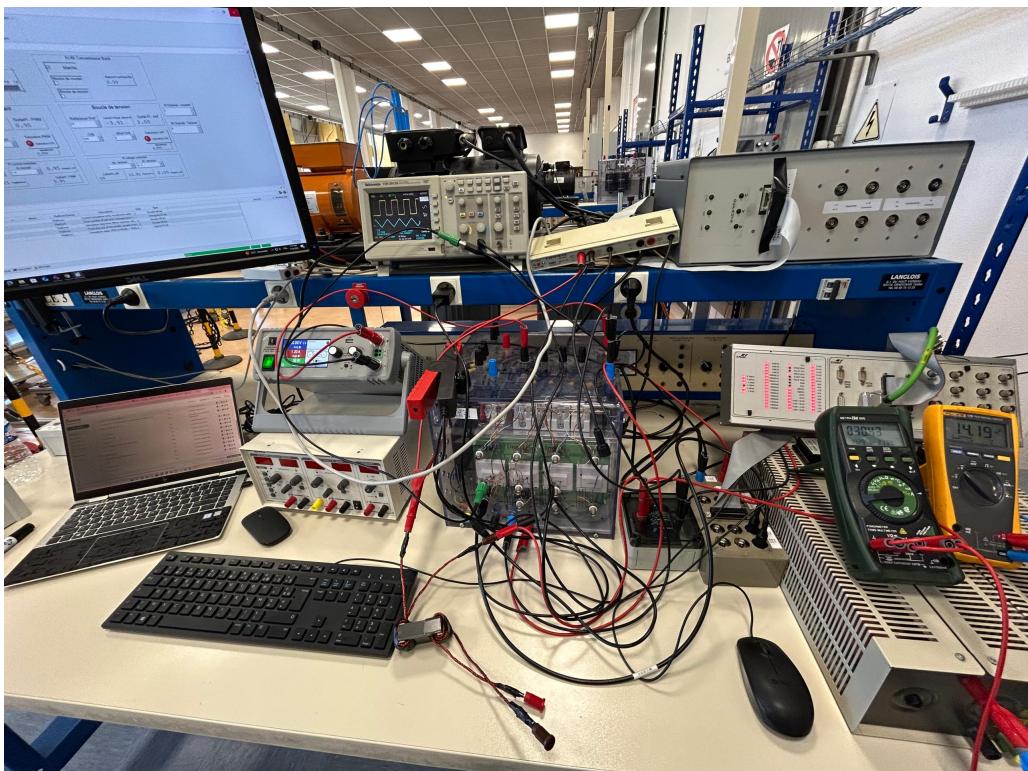


Figure 5.1: Test-bench Experimental Set Up.

## 5.1 Experimental Setup and Procedure

The experimental setup was configured according to the schematics provided in Fig. 5.2. The slave bit output of the dSPACE 1104 was used to generate PWM signals based on the control algorithm, which were then transmitted via the slave bit input to drive the gates of the MOSFETs in the 2PIBC. A Digital-to-Analog Converter (DAC) was employed to measure output signals, including the coupled inductor current and voltage, while an Analog-to-Digital Converter (ADC) sent the measured voltage back to the control system for comparison with the reference voltage, enabling closed-loop control. The PWM signals were monitored and adjusted in real-time using the CONTROL DESK software interface.

The 2PIBC requires PWM signals with a 180-degree phase shift between its two phases to ensure proper interleaving, which reduces input current ripple and enhances efficiency. The target operating frequency of the converter was 50 kHz, critical for achieving the desired performance in fuel cell vehicle applications. Oscilloscope captures were recorded to analyze the PWM signals and verify their characteristics, including phase shift, duty cycle accuracy, and frequency.

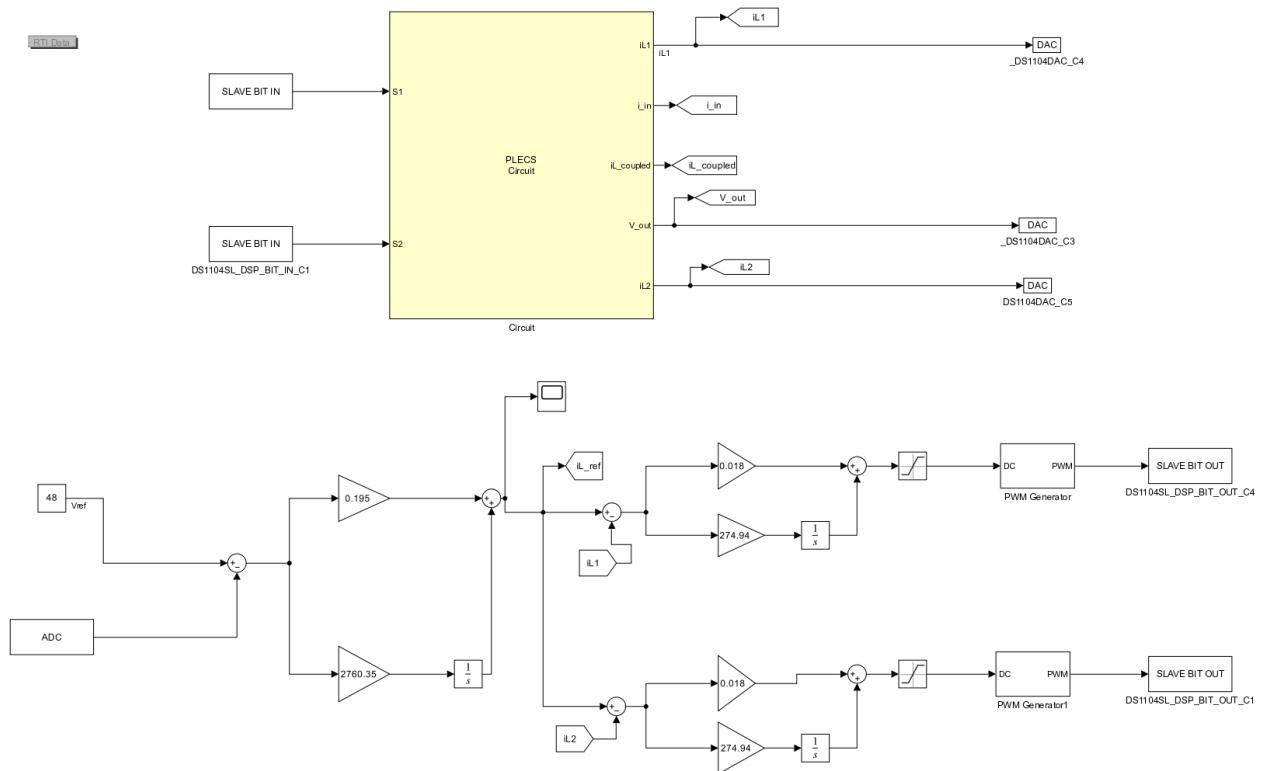


Figure 5.2: Test-bench schematic of the 2PIBC driven by DS1104 slave *bit-out* blocks.

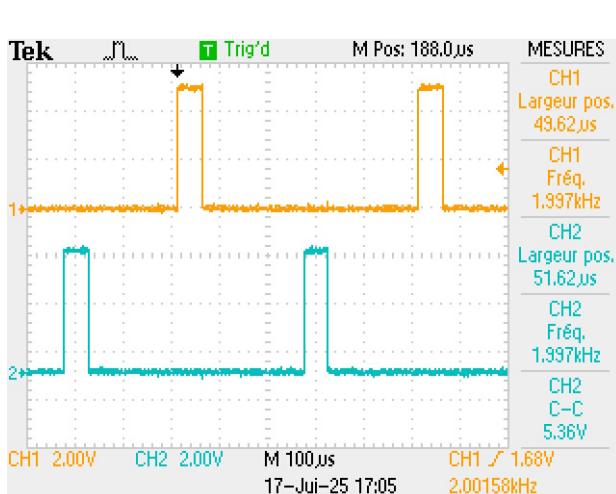
### 5.1.1 Observation and Limitations of the DS1104

Upon sweeping the duty ratio in CONTROL DESK from 0.10 to 0.11, the oscilloscope traces indicated virtually no change in the pulse width. The calculated duty cycle,

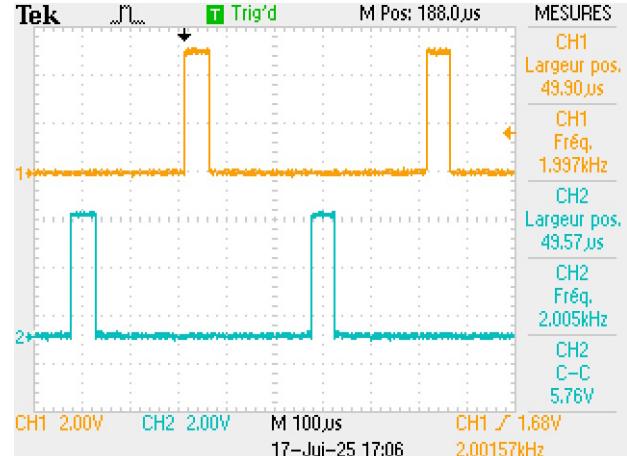
$$D = \frac{t_{ON(max)}}{T_{PWM}},$$

was identical for both set points, revealing insufficient resolution in the slave *bit-out* path.

At low duty cycles (specifically 0.1 and 0.11) as shown in Fig. 5.3, oscilloscope captures demonstrated no measurable difference in PWM signals, indicating that the Slave Bit Output (SBO) resolution was insufficient to capture small incremental duty cycle changes. This lack of resolution directly impacts the 2PIBC control system, as precise duty cycle modulation is critical for achieving accurate voltage regulation and maintaining stable interleaving operations. Consequently, small control adjustments intended to fine-tune voltage and current ripples cannot be realized effectively, reducing converter efficiency and dynamic performance.



(a) Slave *bit-out* PWM at  $D_{set} = 0.10$ .



(b) Slave *bit-out* PWM at  $D_{set} = 0.11$ : no discernible change.

Figure 5.3: Slave *bit-out* PWM at 0.1 & 0.11 duty-cycle set-points.

Increasing the command further to 0.12 resulted in an abrupt jump to  $D \approx 0.20$ , as shown in the scope captures in Fig. 5.4.

When the duty cycle settings on the CONTROL DESK were increased further to 0.13, 0.14, and 0.15, the corresponding oscilloscope captures in Fig. 5.5a, Fig 5.5b. and Fig 5.5c. respectively revealed minimal to negligible changes in the PWM signals, confirming the lack of sufficient resolution at these intermediate duty cycles.

These unpredictable duty cycle variations undermine precise control of the converter's output

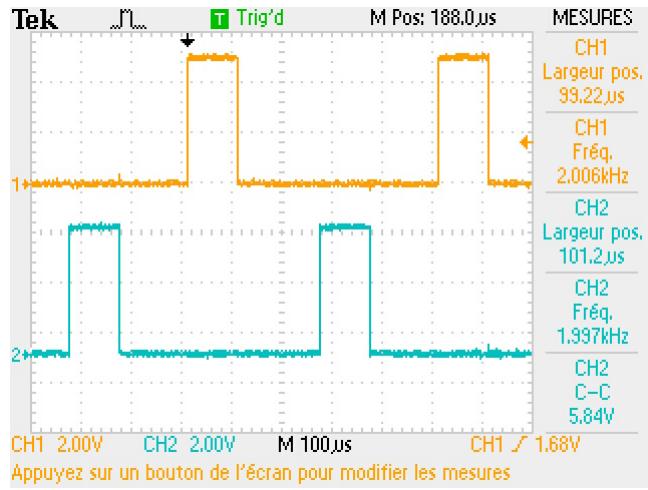
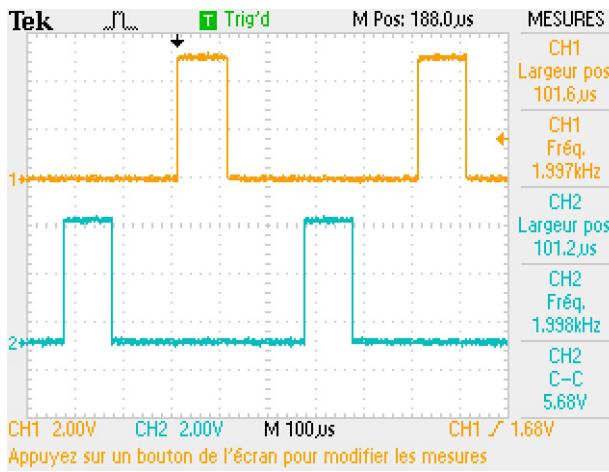
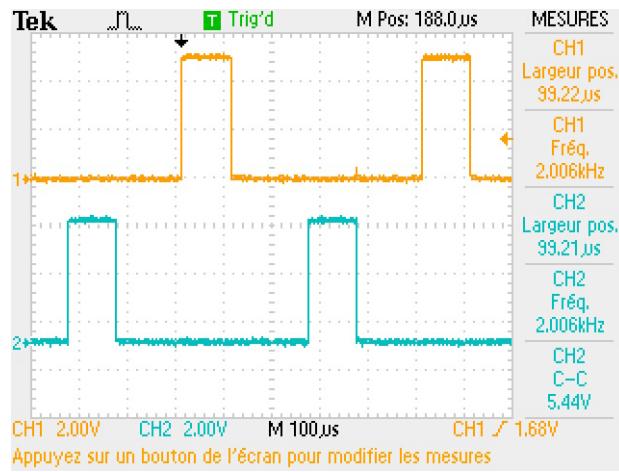


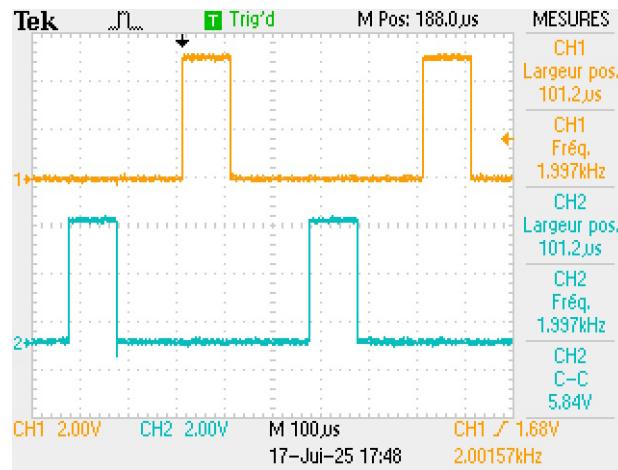
Figure 5.4: Slave bit-out PWM at  $D_{\text{set}} = 0.12$ .



(a) Slave bit-out PWM at  $D_{\text{set}} = 0.13$ .



(b) Slave bit-out PWM at  $D_{\text{set}} = 0.14$ .



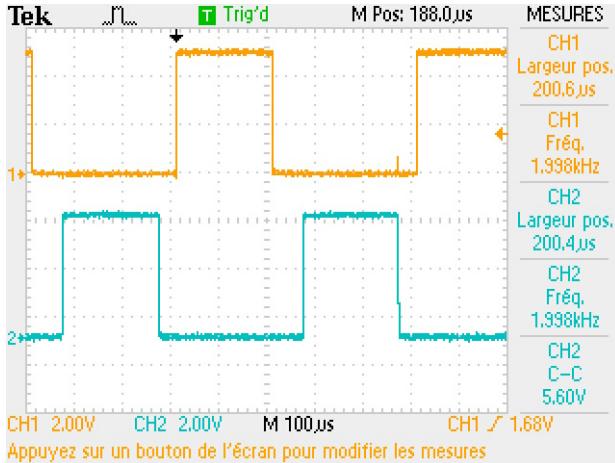
(c) Slave bit-out PWM at  $D_{\text{set}} = 0.15$ .

Figure 5.5: Slave bit-out PWM at  $D_{\text{set}} = 0.13, 0.14, 0.15$ .

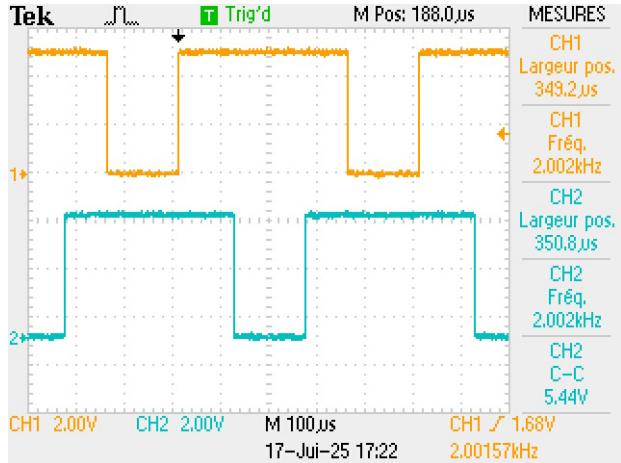
voltage, lead to unintended transient responses, increased ripple currents, and ultimately compromise the reliability of the control strategy.

At relatively higher duty cycles (0.4 and 0.7, as shown in captures Fig. 5.6a and Fig. 5.6b, PWM signals appeared better defined, but the primary frequency limitation persisted, significantly below

the desired converter operating frequency.



(a) Slave *bit-out* PWM at  $D_{\text{set}} = 0.4$ .



(b) Slave *bit-out* PWM at  $D_{\text{set}} = 0.7$ .

Figure 5.6: Slave *bit-out* PWM at 0.4 & 0.7 duty-cycle set-points.

The SBO was practically limited to frequencies around 7.5 kHz, with optimal PWM performance observed near 2 kHz, far below the designed switching frequency of 50 kHz for the 2PIBC. While alternative options such as the dSPACE PWM Channel Block offer slightly higher frequencies (up to around 15 kHz), they lack essential phase-shifting capabilities necessary for interleaved configurations, further restricting their suitability.

### 5.1.2 Alternative Approach with PWM Channels Block

To address the limitations of the SBO, an alternative approach was explored using the PWM Channels block from the dSPACE 1104 library as shown in Fig. 5.7. This block is designed specifically for PWM signal generation and was expected to offer improved resolution for duty cycle adjustments.

The PWM Channel Block supports frequencies up to approximately 15 kHz, as confirmed in all oscilloscope captures, offering better support for high-speed switching. This is an improvement over the practical frequency of the SBO ( $\approx 7.5 \text{ kHz}$ ).

Unlike SBO, PWM signals generated by the PWM Block show a clear incremental variation with changes in duty cycle.

Low 0.1 and 0.11 duty cycles shown in Fig. 5.8 show distinguishable narrow pulse widths. In addition, the duty cycles of 0.5 and 0.55 show smooth and predictable increases in pulse width, as shown in Fig. 5.9.

The oscilloscope captures confirm that the PWM duty width aligns more closely with the commanded values, providing more reliable switching behavior. This increased accuracy enhances the

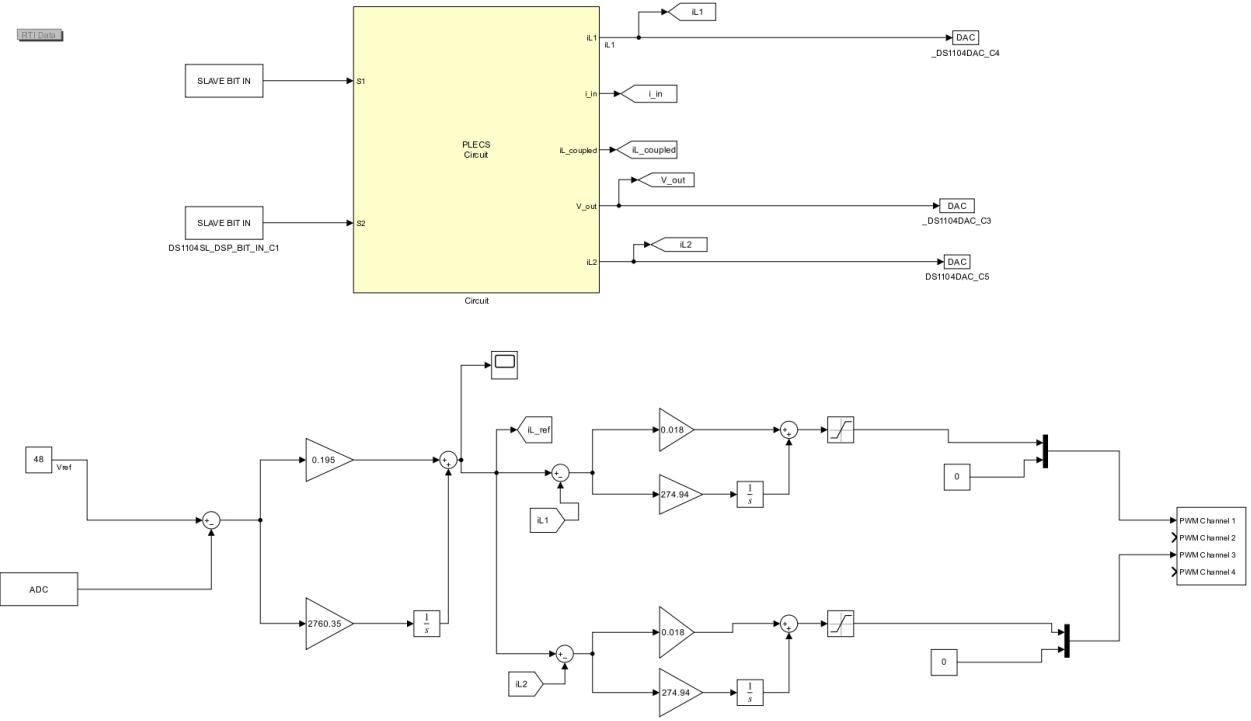
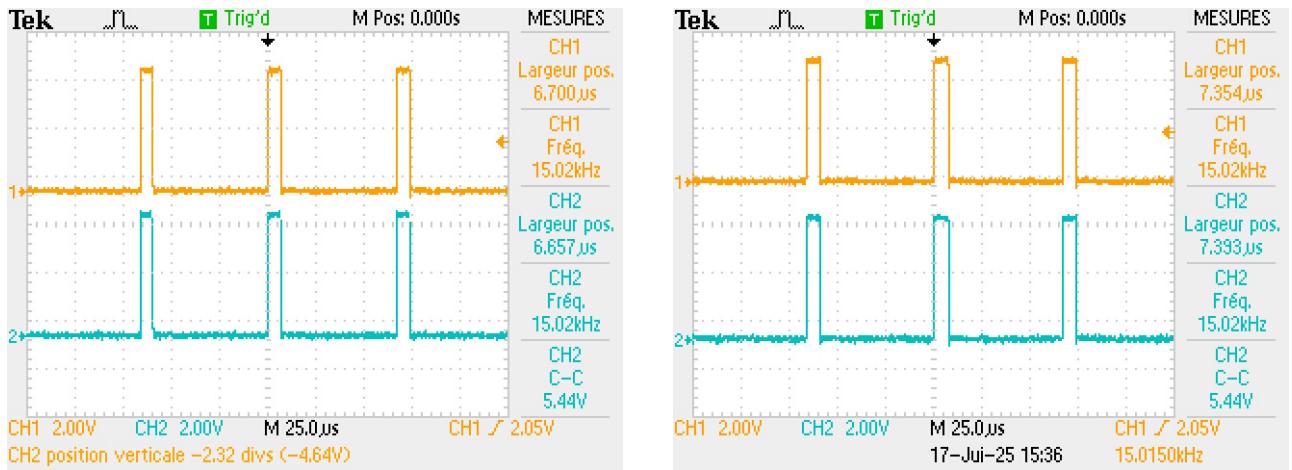


Figure 5.7: Test-bench schematic of the 2PIBC driven by DS1104 *PWM-Channels* blocks.



(a) *PWM-Channels* block PWM at  $D_{set} = 0.10$ .

(b) *PWM-Channels* block PWM at  $D_{set} = 0.11$

Figure 5.8: *PWM-Channels* block's PWM at 0.1 & 0.11 duty-cycle set-points.

control fidelity of the converter, reducing voltage deviations and enabling smoother inductor current transitions.

However, the PWM Channel Block also presents limitations. Most notably, it lacks the ability to implement the required 180 degree phase shift between the two interleaved PWM signals. This absence

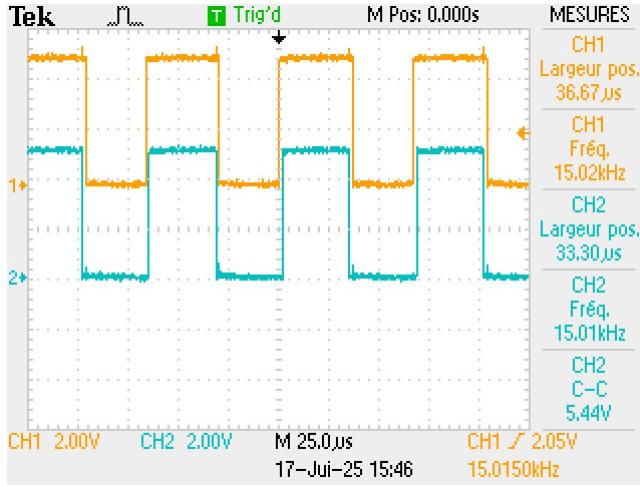


Figure 5.9: *PWM-Channels* block's PWM at 0.5 & 0.55 duty-cycle set-points.

of phase interleaving support undermines the fundamental operational strategy of the converter, leading to increased input current ripple and diminished power density benefits. Furthermore, while 15 kHz is a substantial improvement over the 7.5 kHz of the SBO, it still falls short of the optimal 50 kHz switching frequency needed to fully exploit the advantages of the 2PIBC. This frequency limitation affects the ability of the system to minimize ripple, shrink passive component sizes, and respond effectively to fast load transients.

## 5.2 Modified Experimental Validation Strategy

The experimental validation of the coupled inductor designed for the 2PIBC was initially planned to be carried out using the dSPACE DS1104 R&D Controller Board. However, this platform presented hardware limitations that hindered full implementation of the 2PIBC topology. The DS1104 has a restricted number of real-time PWM outputs and lacks the flexibility required to precisely synchronize the control of multi-phase interleaved converters, especially in four-phase or cascade-coupled topologies.

### 5.2.1 Alternative Setup Using Buck Converter Test Bench

To overcome these limitations, an alternative test strategy was adopted. The coupled inductor was tested on a laboratory single phase buck converter test bench already integrated with a closed-loop control system developed at the FEMTO-ST Institute's Hydrogen Energy Platform. This platform, using the ControlDesk interface with DS1104, allowed real-time control of current and voltage and observation of switching behavior.

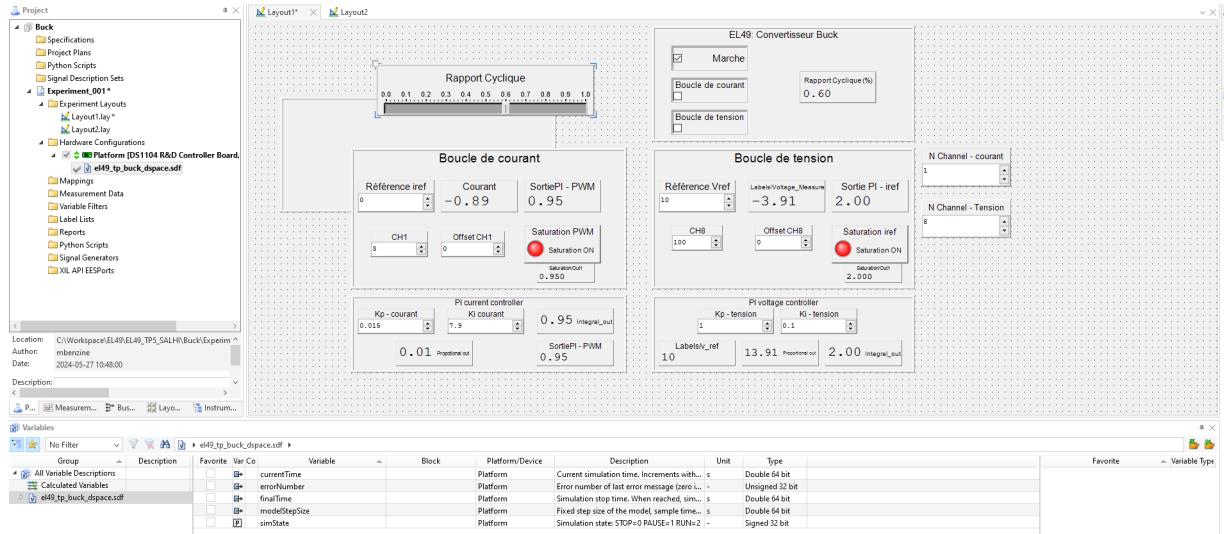


Figure 5.10: ControlDesk interface of the Buck converter test bench used for coupled inductor validation.

Despite the difference in topology, the buck converter provided a controlled switching environment with appropriate voltage and current levels to characterize the magnetic performance of the fabricated inductor. This approach enabled validation of the inductor's fundamental electromagnetic properties while maintaining measurement accuracy and safety protocols.

## 5.2.2 Theoretical Inductor Sizing for Buck Converter Operation

For the experimental validation, theoretical calculations were performed to determine the expected inductance value when the coupled inductor operates in buck converter mode. The inductance requirement for a buck converter is given by:

$$L = \frac{(V_{in} - V_{out}) \cdot D}{\Delta I_L \cdot f_s} \quad (5.1)$$

where  $V_{in}$  is the input voltage,  $V_{out}$  is the output voltage,  $D$  is the duty cycle,  $\Delta I_L$  is the peak-to-peak ripple current, and  $f_s$  is the switching frequency.

Using the experimental operating conditions in Table 5.1, the theoretical inductance for buck operation was calculated to be  $71.4\mu H$ . Additionally, considering the coupling factor  $k = -\frac{1}{3}$  established in the design phase, the mutual inductance was determined as  $M = \pm 23.8\mu H$ .

## 5.2.3 Experimental Inductance Measurement

The experimental inductance was determined through oscilloscope analysis of the inductor voltage and current waveforms during both ON and OFF switching states shown in Fig. 5.11. The inductance

Table 5.1: Buck Converter Test Conditions

Parameter	Value
Switching frequency $f_s$	15.03 kHz
Input voltage $V_{in}$	19 V
Output voltage $V_{out}$	10 V
Current ripple $\Delta I_L$	3.84 A
Duty ratio $D$	0.52
CH1	Inductor voltage
CH2	Inductor current

was calculated using Faraday's law applied to the measured voltage and current slopes:

**For the ON-state:**

$$L_{on} = \frac{(V_{in} - V_{out}) \cdot t_{on}}{\Delta I_L} \quad (5.2)$$

**For the OFF-state:**

$$L_{off} = \frac{V_{out} \cdot t_{off}}{\Delta I_L} \quad (5.3)$$

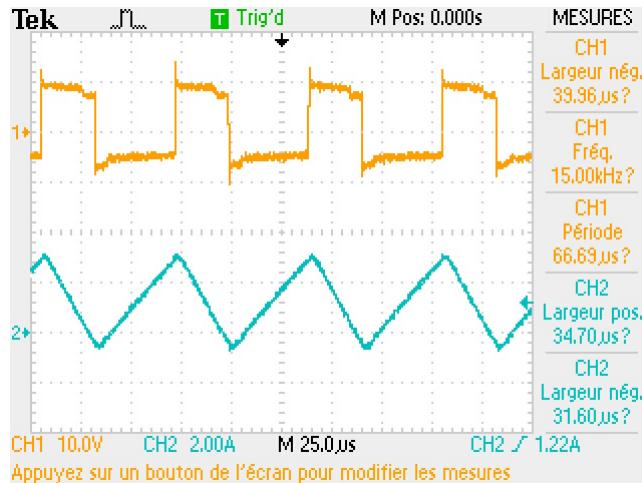


Figure 5.11: Inductor voltage (CH1) and inductor current (CH2) waveforms of the Buck converter operating at 15 kHz switching frequency.

The final experimental inductance was calculated as the average of both states:

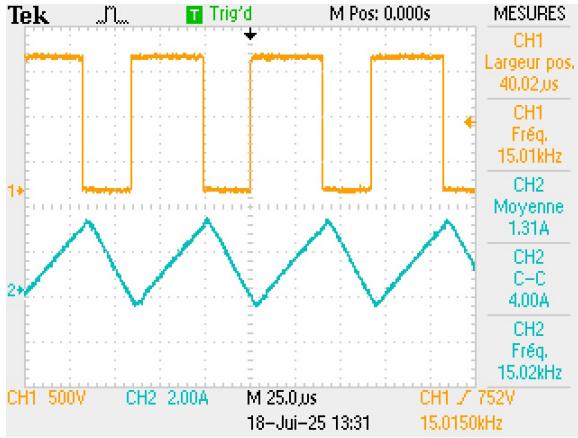
$$L_{exp} = \frac{L_{on} + L_{off}}{2} \quad (5.4)$$

From the oscilloscope measurements in Fig. 5.12, the following values were obtained:  $L_{on} = 81.3\mu H$ ,  $L_{off} = 82.3\mu H$  and  $L_{exp} = 81.8\mu H$

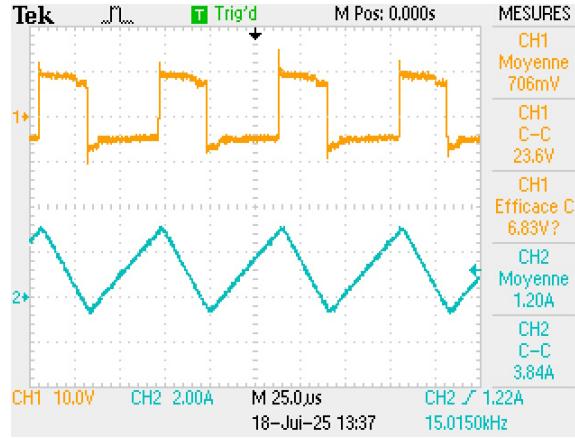
Table 5.2: Comparison of Theoretical and Experimental Results

Parameter	Theoretical Value	Experimental Value	Deviation
Buck Design Inductance	71.4 $\mu H$	81.8 $\mu H$	+14.6%
Boost Design Inductance	48 $\mu H$	81.8 $\mu H$	+70.4%

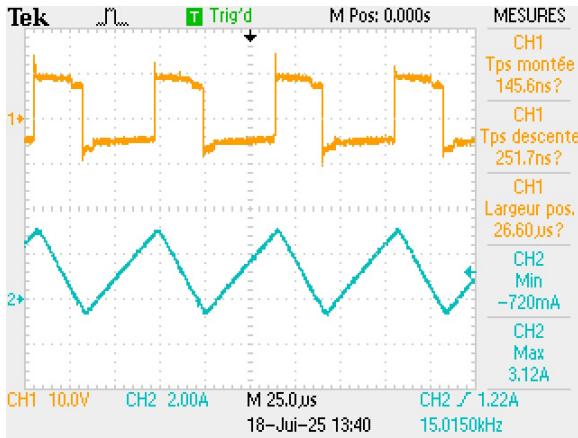
The experimental inductance of  $81.8\mu H$  was 14.6% higher than the theoretical buck converter



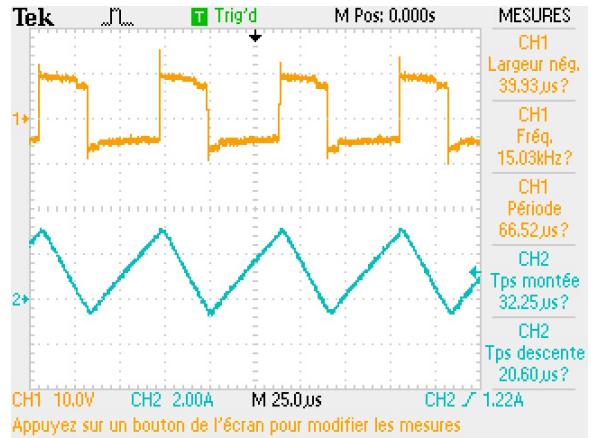
(a) Switching waveform (CH1) and inductor triangular current waveform (CH2).



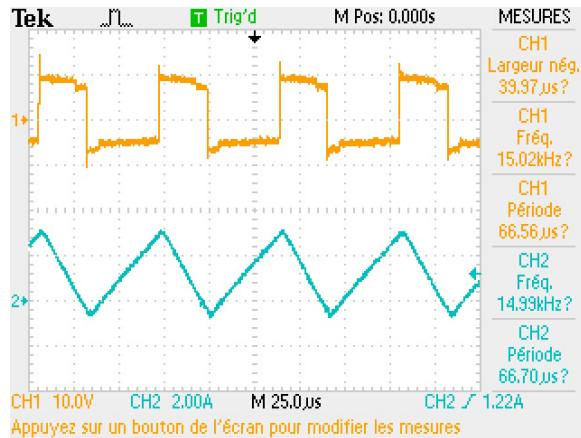
(b) Inductor current (CH2), confirming current ripple



(c) Min/Max inductor current (CH2): Ripple span and slope validation.



(d) Duty cycle and pulse width for inductance calculation.



(e) Repeated duty cycle capture for ON/OFF time verification.

Figure 5.12: Inductor behavior captures confirm reliable real-world performance under buck-mode validation.

value of  $71.4\mu H$ , probably due to measurement uncertainties from probe calibration, sampling rate limitations, and noise, as well as differences between actual and assumed operating conditions caused by the circuit parasitic element.

The large difference between the boost-designed inductance ( $48 \mu\text{H}$ ) and the experimentally measured value in buck mode ( $81.8 \mu\text{H}$ ) is primarily due to fundamental differences in converter topologies and their respective inductance requirements: in a boost converter, the inductor is sized using

$$L_{\text{boost}} = \frac{V_{\text{in}} \cdot D}{f_s \cdot \Delta I_L} \quad (5.5)$$

which is designed to limit input current ripple and benefits from inverse coupling which allows for smaller inductance; in contrast, a buck converter typically requires a higher inductance, calculated by

$$L_{\text{buck}} = \frac{(V_{\text{in}} - V_{\text{out}}) \cdot D}{f_s \cdot \Delta I_L} \quad (5.6)$$

to ensure proper output filtering and energy storage. In this mode, the coupled inductor reveals its full self-inductance without any ripple-canceling effects, resulting in the higher measured value.

The coupled inductor design introduces additional complexity through magnetic coupling between phases. In boost operation, the inverse coupling ( $k = -\frac{1}{3}$ ) provides ripple cancellation benefits, allowing smaller individual inductance values. However, when operated in buck mode, the same physical inductor exhibits full self-inductance without interleaving benefits, resulting in higher measured values.

#### 5.2.4 Validation of Coupling Behavior

The experimental results confirm the presence of inverse coupling in the fabricated inductor. The measured inductance of  $81.8 \mu\text{H}$  closely matches the theoretical equivalent inductance for inverse coupling in the operating duty cycle, validating the design methodology. This shows that despite the topology mismatch, the fundamental magnetic properties of the coupled inductor are confirmed as designed, verifying its suitability for the intended 2PIBC application.

# Chapter 6

## Conclusions and Future Work

This master thesis addresses the main challenge of enhancing efficiency, compactness, and reliability in DC-DC power conversion for FCEV applications through the comprehensive development, modeling, and experimental validation of direct and inverse coupled inductors in a 4PIBC topology. By focusing on the design and integration of these advanced magnetic components (direct and inverse coupled inductors), this work directly confronts industry limitations such as excessive current ripple, bulky magnetic components, and limited fault tolerance in state-of-the-art powertrains for FCEV.

The main contributions of this Master thesis are summarized as follows.

- The thesis provides in-depth electrical and magnetic models for both direct- and inverse-coupled inductors, including small-signal linearization and transfer function derivation required for advanced controller design.
- Detailed simulation studies using PLECS, FEMM, and MATLAB/Simulink validate the analytical models, demonstrating accuracy across both magnetic and electrical models.
- A step-by-step methodology is presented for optimal sizing of industrial EE-type ferrite cores with air-gap tuning to set the inverse coupling around  $k \approx \frac{-1}{3}$ , custom Litz wire windings, and a practical route to implementation, including the effects of air gap placement, winding techniques, and mitigation of skin and proximity effects..
- Experimental and simulation results confirm that the integration of inverse coupled inductors in a 4PIBC topology achieves outstanding input current ripple reduction (down to 1.6% in simulation), better load balancing between converter phases, reduced core saturation risk, and allows downsizing of magnetic elements - the main factors behind increased power density and

improved system robustness.

- The work implements dual-loop PI control (inner current and outer voltage loops) and introduces sliding mode control for the outer loop, achieving excellent closed-loop voltage regulation, swift transient recovery, minimal steady-state error, and superior disturbance rejection compared to classical PI approaches.
- Detailed analytical and simulation-based loss breakdowns are provided for switching devices (SiC MOSFETs and Schottky diodes) and inductors, including conduction, switching, core, and copper losses. This research demonstrates that with proper magnetic and thermal design, junction temperatures remain well below device maximums, confirming safe system operation under worst-case scenarios.
- Despite hardware limitations on available digital control platforms, the research succeeds in validating the fabricated coupled inductors using a single-phase buck converter test bench, with measured inductance and performance closely matching theoretical and simulation predictions. Laboratory measurements confirm robust closed-loop operation and validate the feasibility of the proposed magnetic designs for next-generation FCEV powertrains.

The achievements of this thesis lay a strong foundation for further exploration, and several directions for future research are outlined to broaden its scope and impact.

1. The limitations of the dSPACE 1104 platform, particularly in resolution and multiphase synchronization, suggest the need for more advanced control hardware. Future investigations could adopt FPGA-based systems or upgraded real-time controllers to achieve precise PWM signal generation and improved phase coordination, enabling more accurate validation of multiphase interleaved converters.
2. The current design was tailored to a specific power level for FCEV applications. Extending the coupled inductor approach to higher power ratings or alternative converter topologies, such as multi-level or resonant converters, could broaden its applicability to larger vehicles or stationary fuel cell systems, enhancing its versatility.
3. Further optimization of the coupling coefficient and exploration of advanced magnetic materials (e.g., amorphous or nanocrystalline cores) could reduce core losses and improve thermal

performance. Parametric studies on winding arrangements and core geometries may also yield designs with even greater efficiency and compactness.

4. Integrating the 4PIBC with an actual fuel cell stack would provide critical insight into its performance under realistic conditions. This step would validate the converter response to dynamic fuel cell behavior, such as voltage sags or load transients, and ensure compatibility with automotive standards.
5. The thesis noted the potential of sliding mode control for dynamic performance. Future work could implement adaptive, predictive, or AI-based controllers that further enhance efficiency and stability under varied and complex FCEV drive cycles.
6. Many FCEVs employ hybrid architectures that combine fuel cells with batteries or supercapacitors. Investigating the integration of 4PIBC into such systems, including the development of coordinated control algorithms, could optimize power distribution and improve overall vehicle efficiency.

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