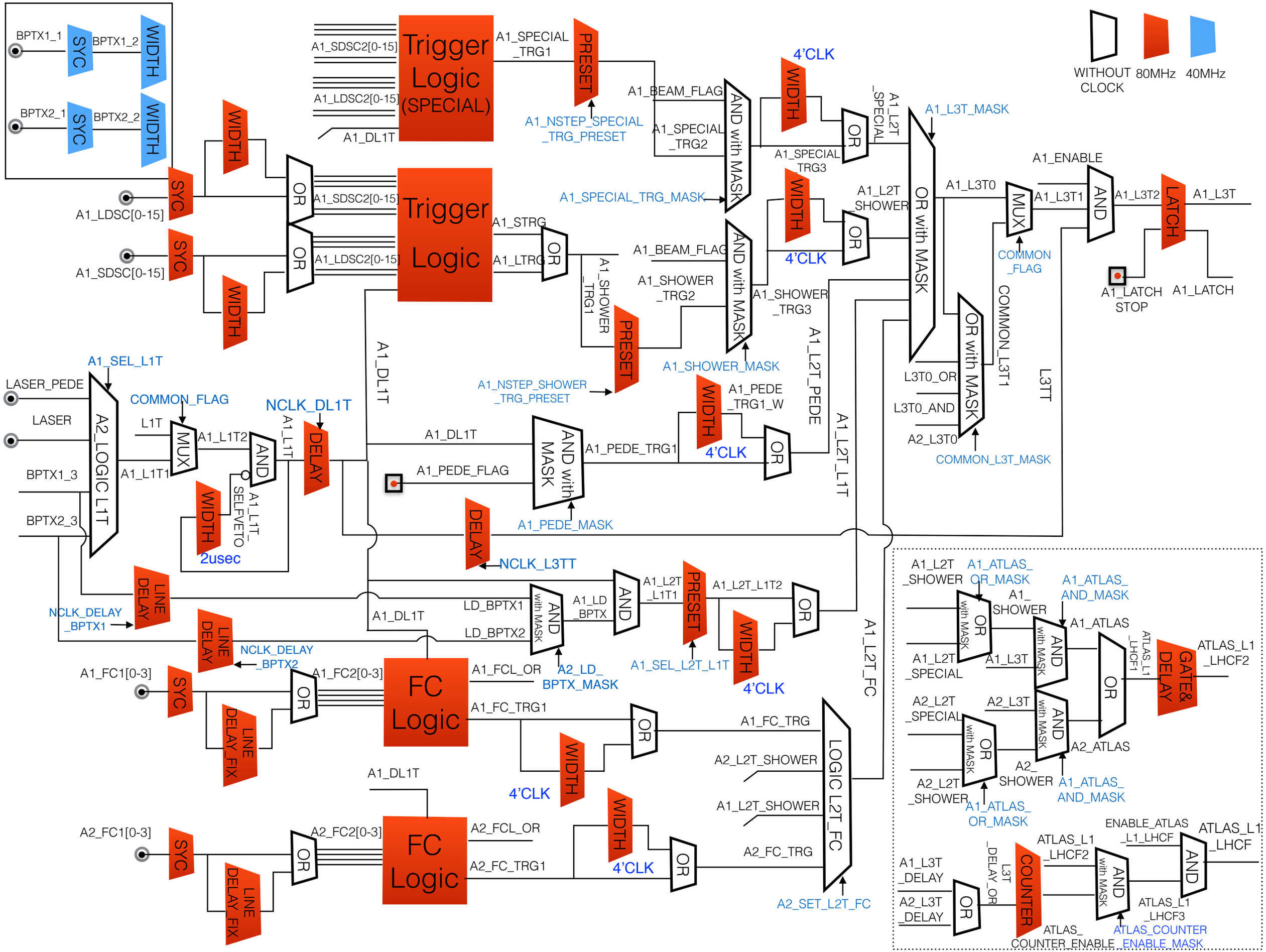
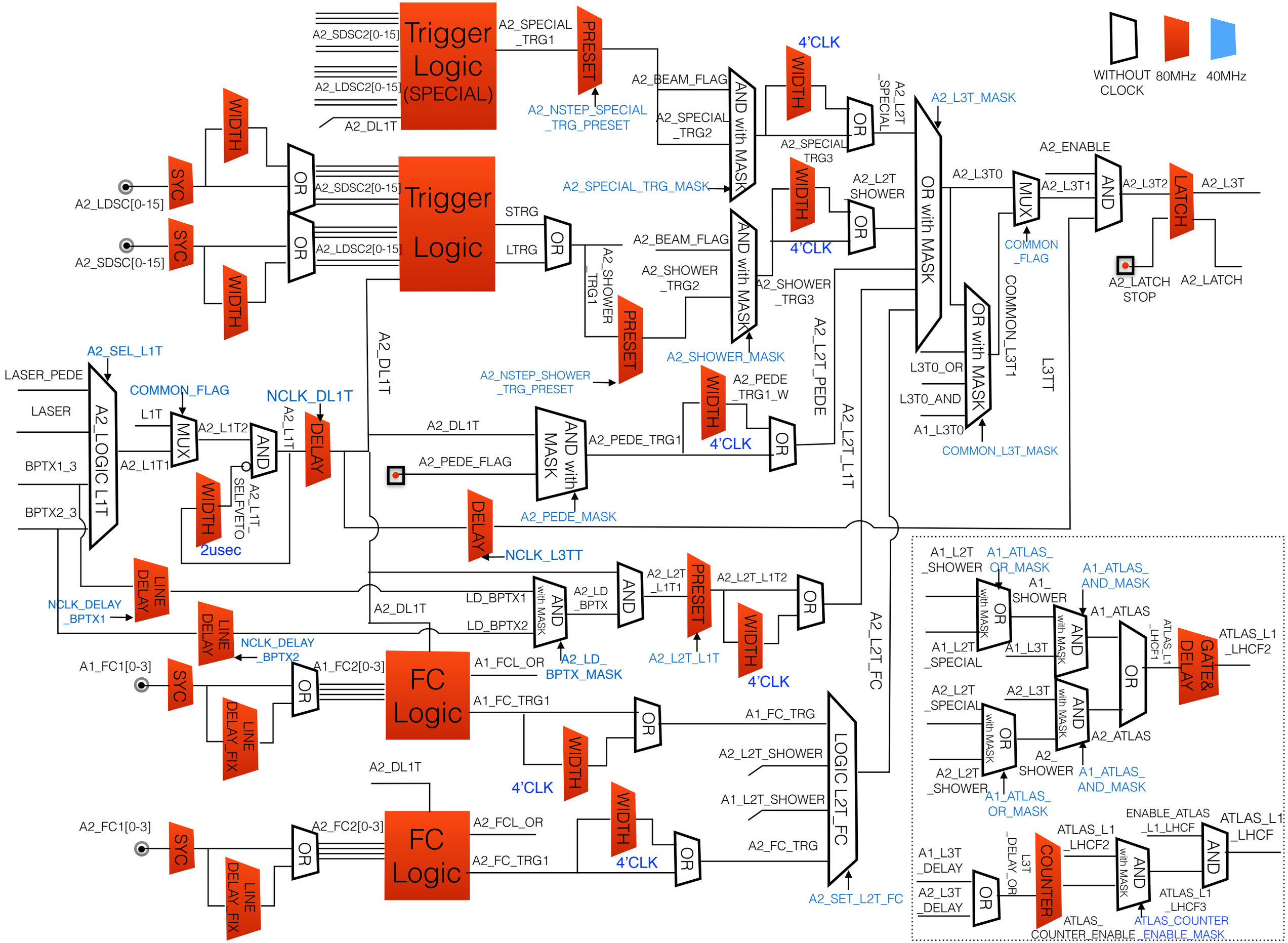
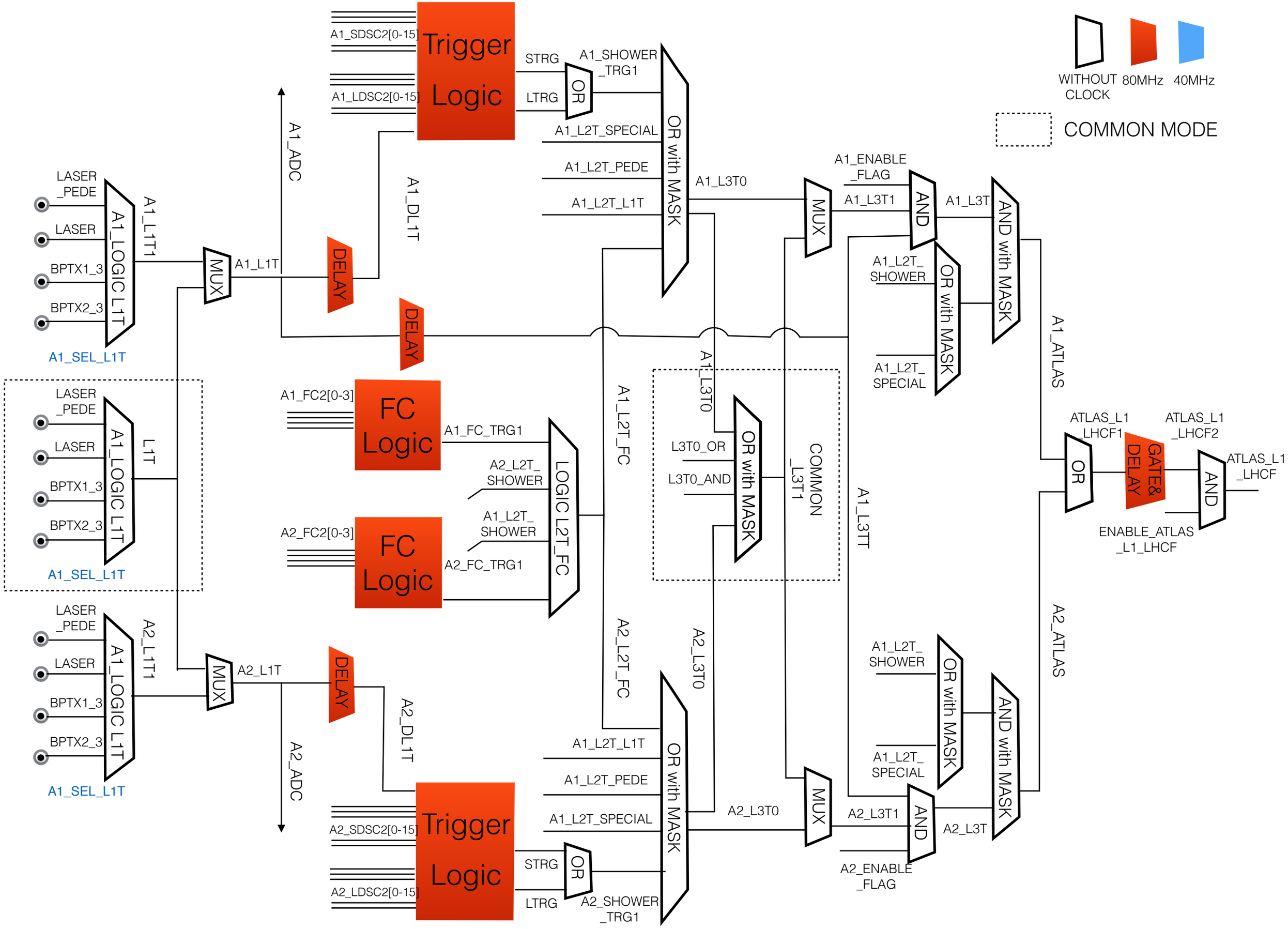
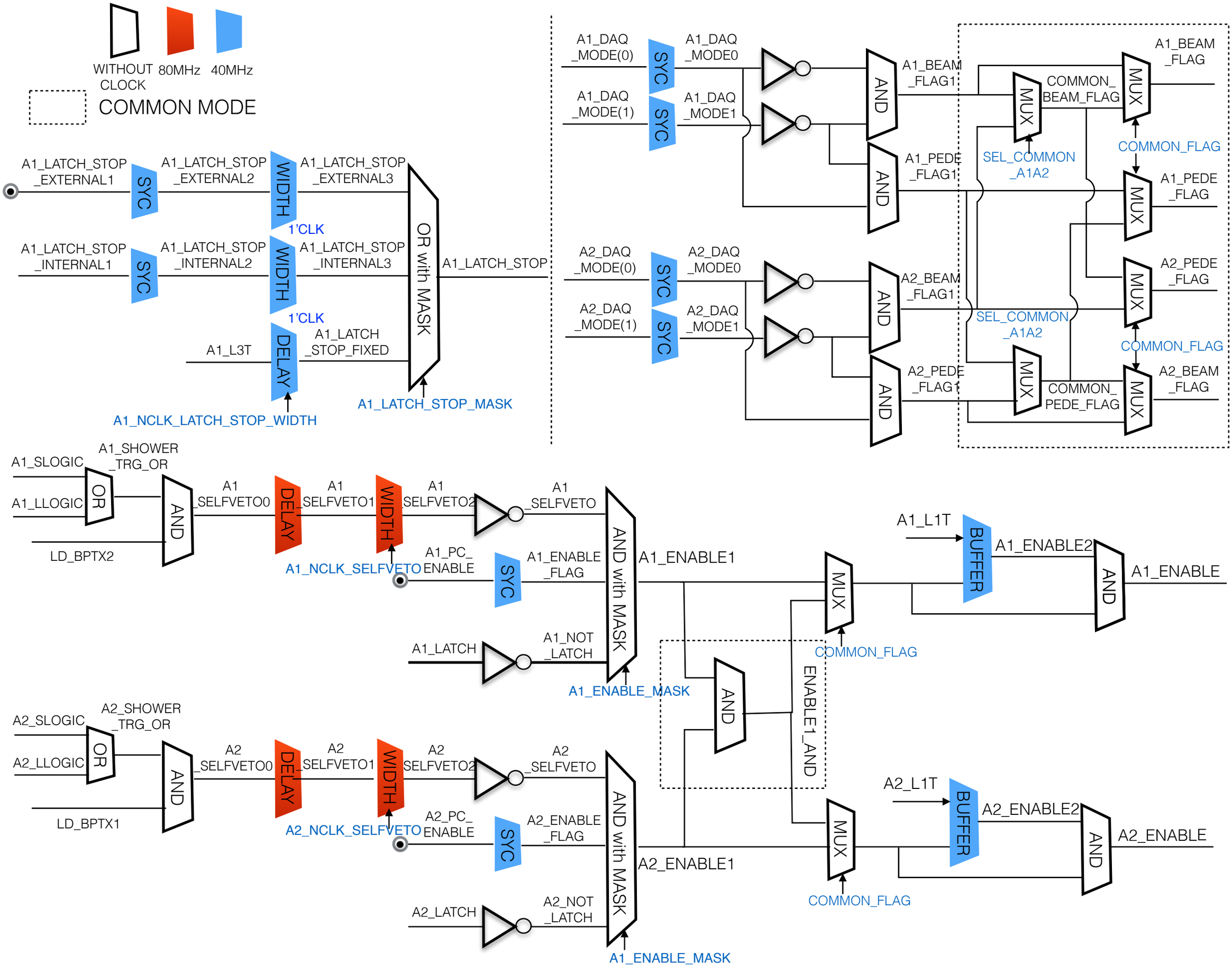

WITHOUT CLOCK
80MHz
40MHz
BPTX1_1
BPTX1_2
BPTX2_1
BPTX2_2
SYC
WIDTH
A1_LDSC[0-15]
A1_SDSC[0-15]
OR
A1_SDSC2[0-15]
A1_LDSC2[0-15]
A1_DL1T
Trigger Logic (SPECIAL)
Trigger Logic
A1_SPECIAL_TRG1
PRESET
A1_NSTEP_SPECIAL_TRG_PRESET
A1_BEAM_FLAG
A1_SPECIAL_TRG2
AND with MASK
A1_SPECIAL_TRG_MASK
4'CLK
A1_SPECIAL_TRG3
A1_L2T_SPECIAL
A1_L2T_SHOWER
A1_L3T_MASK
OR with MASK
A1_L3T0
A1_ENABLE
MUX
A1_L3T1
AND
A1_L3T2
LATCH
A1_L3T
COMMON_FLAG
A1_LATCH STOP
A1_LATCH
A1_STRG
A1_LTRG
A1_SHOWER_TRG1
A1_SHOWER_TRG2
A1_SHOWER_TRG3
A1_SHOWER_MASK
A1_NSTEP_SHOWER_TRG_PRESET
A1_L2T_PEDE
A1_L2T_L1T
COMMON_L3T1
L3TT
L3T0_OR
L3T0_AND
A2_L3T0
COMMON_L3T_MASK
A1_SEL_L1T
LASER_PEDE
LASER
BPTX1_3
BPTX2_3
A2_LOGIC L1T
COMMON_FLAG
L1T
A1_L1T2
A1_L1T1
NCLK_DL1T
DELAY
A1_L1T_SELFVETO
2usec
A1_PEDE_TRG1_W
A1_PEDE_TRG1
A1_PEDE_FLAG
A1_PEDE_MASK
NCLK_L3TT
LINE DELAY
NCLK_DELAY_BPTX1
NCLK_DELAY_BPTX2
LD_BPTX1
LD_BPTX2
A1_LD_BPTX
A2_LD_BPTX_MASK
A1_L2T_L1T1
A1_L2T_L1T2
A1_SEL_L2T_L1T
A1_FC1[0-3]
A1_FC2[0-3]
FC Logic
A1_FCL_OR
A1_FC_TRG1
A1_FC_TRG
A2_L2T_SHOWER
A1_L2T_SHOWER
LOGIC L2T_FC
A1_L2T_FC
A2_SET_L2T_FC
LINE DELAY_FIX
A2_FC1[0-3]
A2_FC2[0-3]
A2_FCL_OR
A2_FC_TRG1
A2_FC_TRG
A1_L2T_SHOWER
A1_ATLAS_OR_MASK
A1_ATLAS_AND_MASK
A1_SHOWER
A1_L2T_SPECIAL
A1_L3T
A1_ATLAS
ATLAS_L1_LHCF1
ATLAS_L1_LHCF2
GATE& DELAY
A2_L2T_SPECIAL
A2_L3T
A2_ATLAS
A2_SHOWER
A1_L3T_DELAY
A2_L3T_DELAY
L3T_DELAY_OR
COUNTER
ATLAS_COUNTER_ENABLE
ENABLE_ATLAS_L1_LHCF
ATLAS_L1_LHCF3
ATLAS_COUNTER ENABLE_MASK


WITHOUT CLOCK
80MHz
40MHz
Trigger Logic (SPECIAL)
A2_SDSC2[0-15]
A2_LDSC2[0-15]
A2_DL1T
A2_SPECIAL _TRG1
PRESET
A2_NSTEP_SPECIAL _TRG_PRESET
A2_BEAM_FLAG
A2_SPECIAL _TRG2
AND with MASK
A2_SPECIAL_TRG_MASK
4'CLK
WIDTH
OR
A2_L2T _SPECIAL
A2_SPECIAL TRG3
A2_L3T_MASK
A2_L2T SHOWER
OR with MASK
A2_L3T0
A2_ENABLE
MUX
A2_L3T1
AND
A2_L3T2
LATCH
A2_L3T
COMMON _FLAG
A2_LATCH STOP
A2_LATCH
A2_LDSC[0-15]
A2_SDSC[0-15]
SYC
Trigger Logic
STRG
LTRG
A2_SHOWER _TRG1
A2_SHOWER _TRG2
A2_SHOWER _TRG3
A2_SHOWER_MASK
A2_NSTEP_SHOWER _TRG_PRESET
A2_L2T_PEDE
A2_PEDE _TRG1_W
A2_PEDE_TRG1
A2_PEDE_FLAG
A2_PEDE_MASK
A2_L2T_L1T
COMMON_L3T1
L3TT
L3T0_OR
L3T0_AND
A1_L3T0
COMMON_L3T_MASK
A2_SEL_L1T
LASER_PEDE
LASER
BPTX1_3
BPTX2_3
A2_LOGIC L1T
COMMON_FLAG
L1T
A2_L1T2
A2_L1T1
NCLK_DL1T
A2_L1T
A2_L1T_ SELFVETO
2usec
NCLK_L3TT
LINE DELAY
NCLK_DELAY _BPTX1
NCLK_DELAY _BPTX2
LD_BPTX1
LD_BPTX2
A2_LD _BPTX
A2_LD_ BPTX_MASK
A2_L2T _L1T1
A2_L2T_L1T2
A2_L2T_L1T
A2_L2T_FC
A1_FC1[0-3]
A1_FC2[0-3]
A1_FCL_OR
A1_FC_TRG1
FC Logic
LINE DELAY_FIX
A1_FC_TRG
A2_L2T_SHOWER
A1_L2T_SHOWER
LOGIC L2T_FC
A2_SET_L2T_FC
A2_FC1[0-3]
A2_FC2[0-3]
A2_FCL_OR
A2_FC_TRG1
A2_FC_TRG
A1_L2T _SHOWER
A1_ATLAS_ OR_MASK
A1_ATLAS_ AND_MASK
A1_ SHOWER
A1_ATLAS
A1_L2T _SPECIAL
A1_L3T
ATLAS_L1 _LHCF1
GATE& DELAY
ATLAS_L1 _LHCF2
A2_L2T _SPECIAL
A2_L3T
A2_ATLAS
A2_ SHOWER
A2_L2T _SHOWER
A1_L3T _DELAY
A2_L3T _DELAY
L3T _DELAY_OR
COUNTER
ATLAS_L1 _LHCF2
ENABLE_ATLAS _L1_LHCF
ATLAS_L1 _LHCF
ATLAS_L1 _LHCF3
ATLAS_ COUNTER_ENABLE
ATLAS_COUNTER _ENABLE_MASK


WITHOUT CLOCK
80MHz
40MHz
COMMON MODE
Trigger Logic
A1_SDSC2[0-15]
A1_LDSC2[0-15]
STRG
LTRG
OR
A1_SHOWER_TRG1
A1_L2T_SPECIAL
A1_L2T_PEDE
A1_L2T_L1T
OR with MASK
A1_L3T0
A1_ADC
A1_DL1T
DELAY
LASER_PEDE
LASER
BPTX1_3
BPTX2_3
A1_LOGIC L1T
A1_L1T1
A1_SEL_L1T
MUX
A1_L1T
A1_ENABLE_FLAG
A1_L3T1
AND
A1_L3T
AND with MASK
A1_L2T_SHOWER
A1_L2T_SPECIAL
A1_ATLAS
A1_FC2[0-3]
FC Logic
A1_FC_TRG1
A2_L2T_SHOWER
A1_L2T_SHOWER
A2_FC2[0-3]
A2_FC_TRG1
LOGIC L2T_FC
A1_L2T_FC
L1T
A1_L3T0
L3T0_OR
L3T0_AND
COMMON_L3T1
A1_L3TT
ATLAS_L1_LHCF1
ATLAS_L1_LHCF2
GATE&DELAY
ATLAS_L1_LHCF
ENABLE_ATLAS_L1_LHCF
A2_L1T1
A2_L1T
A2_ADC
A2_DL1T
A2_L2T_FC
A2_L3T0
A2_ATLAS
A2_SDSC2[0-15]
A2_LDSC2[0-15]
A2_L3T1
A2_L3T
A2_ENABLE_FLAG
A2_SHOWER_TRG1


WITHOUT CLOCK
80MHz
40MHz
COMMON MODE
A1_LATCH_STOP_EXTERNAL1
SYC
A1_LATCH_STOP_EXTERNAL2
WIDTH
1'CLK
A1_LATCH_STOP_EXTERNAL3
A1_LATCH_STOP_INTERNAL1
A1_LATCH_STOP_INTERNAL2
A1_LATCH_STOP_INTERNAL3
A1_L3T
DELAY
A1_LATCH_STOP_FIXED
OR with MASK
A1_LATCH_STOP
A1_LATCH_STOP_MASK
A1_NCLK_LATCH_STOP_WIDTH
A1_DAQ_MODE(0)
A1_DAQ_MODE0
A1_DAQ_MODE(1)
A1_DAQ_MODE1
AND
A1_BEAM_FLAG1
A1_PEDE_FLAG1
MUX
COMMON_BEAM_FLAG
SEL_COMMON_A1A2
A1_BEAM_FLAG
COMMON_FLAG
A1_PEDE_FLAG
A2_DAQ_MODE(0)
A2_DAQ_MODE0
A2_DAQ_MODE(1)
A2_DAQ_MODE1
A2_BEAM_FLAG1
A2_PEDE_FLAG1
COMMON_PEDE_FLAG
A2_PEDE_FLAG
A2_BEAM_FLAG
A1_SHOWER_TRG_OR
A1_SLOGIC
A1_LLOGIC
OR
LD_BPTX2
A1_SELFVETO0
A1_SELFVETO1
A1_SELFVETO2
A1_NCLK_SELFVETO
A1_PC_ENABLE
A1_SELFVETO
A1_ENABLE_FLAG
AND with MASK
A1_ENABLE1
A1_LATCH
A1_NOT_LATCH
A1_ENABLE_MASK
A1_L1T
BUFFER
A1_ENABLE2
A1_ENABLE
ENABLE1_AND
A2_SHOWER_TRG_OR
A2_SLOGIC
A2_LLOGIC
LD_BPTX1
A2_SELFVETO0
A2_SELFVETO1
A2_SELFVETO2
A2_NCLK_SELFVETO
A2_PC_ENABLE
A2_SELFVETO
A2_ENABLE_FLAG
A2_ENABLE1
A2_LATCH
A2_NOT_LATCH
A2_L1T
A2_ENABLE2
A2_ENABLE