

ECE253 Midterm Cheatsheet

Boolean Algebra

De Morgan's Theorem tells us

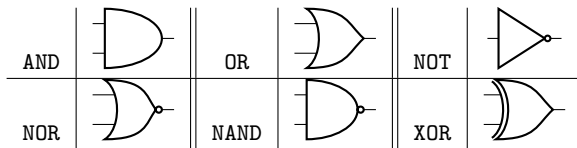
$$\overline{xy} = \overline{x} + \overline{y}, \quad \overline{x + y} = \overline{x} \overline{y} \quad (1)$$

Inverting the inputs to an **or** gate is the same as inverting the outputs to an **and** gate, and the other way around.

We also have:

- $(x + y)(y + z)(\overline{x} + z) = (x + y)(\overline{x} + z)$
- $x + yz = (x + y)(x + z)$
- $x + xy = x$
- $xy + x\overline{y} = x$
- $(x + y)(x + \overline{y}) = x$
- $x + \overline{x}y = x + y$
- $x(\overline{x} + y) = xy$
- $xy + yz + \overline{x}z = xy + \overline{x}z$

Gates



SOPs and POSs

We can create boolean algebra expressions for truth tables.

Minterm: Corresponds to each row of truth table, i.e. $m_3 = \overline{x}_2 x_1 x_0$ such that when $3 = 0b011$ is substituted in, $m_3 = 1$ and $m_3 = 0$ otherwise.

Maxterm: They give $M_i = 0$ if and only if the input is i . For example, $M_3 = x_2 + \overline{x}_1 + \overline{x}_0$.

SOP and POS: Truth tables can be represented as a sum of minterms, or product of maxterms.

Cost

The cost of a logic circuit is given by

$$\text{cost} = \text{gates} + \text{inputs} \quad (2)$$

If an inversion (**NOT**) is performed on the primary inputs, then it is not included. If it is needed inside the circuit, then the **NOT** gate is included in the cost.

Karnaugh Map

Method of finding a minimum cost expression: We can map out truth table on a grid for easier pattern recognition. Example of a four variable map is shown below:

		$x_2 x_1$			
		00	01	11	10
$x_4 x_3$	00	1	1	1	0
	01	1	1	1	0
	11	0	0	1	1
	10	0	0	1	1

and the representation is $\overline{x}_2 \cdot \overline{x}_4 + x_2 \cdot x_1 + \overline{x}_4 \cdot x_2$. Some rules:

- Side lengths should be powers of 2 and be as large as possible.
- Use **graycoding**: adjacent rows/columns should share one bit.

Some definitions:

- **Literal:** variables in a product term: $x_1 \overline{x}_2 x_3$ has three literals.
- **Implicant:** a product term that indicates the input valuation(s) for which a given function is equal to 1.
- **Prime Implicant:** an implicant that cannot be combined into another implicant with fewer literals. *They are as big as possible.*
- **Cover:** A collection of implicants that account for all valuations for which function equals 1.
- **Essential Prime Implicant:** A prime implicant that includes a minterm not included in any other prime implicant. *They contain at least one minterm not covered by another prime implicant.*

In the above example, $\overline{x}_2 \cdot \overline{x}_4 + x_2 x_1 + \overline{x}_4 x_2$ are prime implicants.

Minimization Procedure

1. Generate all prime implicants for given function f
2. Find the set of essential prime implicants
3. If the set of essential prime implicants cover all valuations for which $f = 1$, then this set is the desired cover. Otherwise, determine the nonessential prime implicants that should be added.

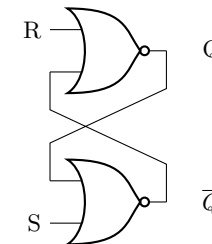
Common Logic Gates

To save space, boolean expressions will be written instead of drawing diagrams. You should be familiar with how to construct diagrams from expressions.

- **Mux 2→1:** $\text{mux2to1}(s, x_0, x_1) = \overline{s}x_0 + sx_1$
- **Mux 4→1:** $\text{mux4to1}(s, x) = \text{mux2to1}(s_1, \text{mux2to1}(s_0, x_0, x_1), \text{mux2to1}(s_0, x_2, x_3))$
- **TO BE ADDED**

RS Latch

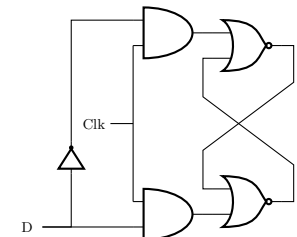
Sequential circuits depend on sequence of inputs. A **SR Latch** are cross-coupled **NOR** gates.



S	R	Q	\overline{Q}
0	0	0/1	1/0
0	1	0	1
1	0	1	0
1	1	0	0

When $S = R = 0$, it stores the last Q value. In practice, we should not have $S = R = 1$.

Gated D Latch and Clock Signal



Clk	S	R	$Q(t+1)$
0	x	x	$Q(t)$
1	0	0	$Q(t)$
1	0	1	0
1	1	0	1
1	1	1	1

Where the Clk = 1 cases refer to **retain**, **reset**, **set**, and last one is not used.

TBA

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