Q0.1.1 Consider the unsigned binary integer $(11110100001)_2$
What would be its equivalent representation in the octal number system?
(a) $(7502)_8$
(b) $(1641)_8$
(c) $(3502)_8$
(d) $\mathbf{(3641)_8}$

Q0.1.2 Consider the unsigned binary integer $(11011011001101)_2$ What would be its equivalent representation in the hexadecimal number system?
(a) $(6D99)_{16}$
(b) $(6D9A)_{16}$
(c) $(DB34)_{16}$
(d) $\mathbf{(36CD)_{16}}$

Q0.2.1 On a hypothetical computer, real numbers are stored in a two's complement fixed-point binary format:
● The first five bits represent the integer part of the number.
● The last four bits represent the fractional part of the number.
Compute the binary representation of the answer to the arithmetic equation
$(11101.1101)_2 - (00110.0111)_2$
(a) 110111011
(b) 110100010
(c) 001000100
(d) 101110110

Q0.2.2 On a hypothetical computer, real numbers are stored in a two's complement fixed-point binary format:
● The first five bits represent the integer part of the number.
● The last four bits represent the fractional part of the number.
Compute the binary representation of the answer to the arithmetic equation
$(00111.0111)_2 - (10101.1101)_2$
(a) 110001101
(b) 100011010
(c) 101101010
(d) 111010100

Q0.3.1 In Java, what is the result of the following: -7.5/0?
(a) +0
(b) -infinity
(c) +infinity
(d) NaN
(e) -0

Q0.3.2 In Java, what is the result of the following: Math.sqrt(-1)?
(a) +infinity
(b) -infinity
(c) +0
(d) -0
(e) NaN

Q0.4.1 Consider the octal number $(76417)_8$
What would be its equivalent representation in the hexadecimal number system?
(a) 7D0F
(b) 7D1E
(c) FA0F
(d) FA1E

Q0.4.2 Consider the hexadecimal number $(4A8C)_{16}$
What would be its equivalent representation in the octal number system?
(a) 19084
(b) 45214
(c) 11243
(d) 22506

Q0.5.1 Most computer architectures have a set of registers. What are the advantages of instructions using registers compared to fetching operands and storing the result in memory?
(a) Registers can represent 2's complement values more efficiently.
(b) Registers are cheaper than main memory.
(c) The number of registers can be changed dynamically, as the program requires.
(d) The number of bits required to specify a register is fewer than to reference a main memory address. Therefore the instructions can be smaller (in size) and faster to load.
(e) Access to registers is faster than access to main memory.

Q0.5.2 Most computer architectures have a set of registers. What are the disadvantages when instructions need to access main memory compared to accessing registers?
(a) The number of bits required to reference a memory address is higher than to specify a register.
Therefore the instructions will be longer (in size) and slower to load.
(b) Access to main memory is slower than access to registers.
(c) Main memory is more expensive than registers.
(d) Main memory is volatile whereas registers are persistent.
(e) Main memory cannot represent 2's complement values

Q0.6.1 A hypothetical computer stores real numbers in floating point format in 8-bit words:
● The first bit is used for the sign of the number (1 is negative).
● The second bit used for the sign of the exponent (1 is negative).
● The next two bits are used for the magnitude of the exponent. (We do not use an offset to the exponent).
● The final four bits are used for the magnitude of the mantissa.
Convert the value $(11111011)_2$ in this representation into its decimal equivalent.
(a) -1.2109375
(b) -0.0390625
(c) -1.0390625
(d) -0.2109375

Q0.6.2 A hypothetical computer stores real numbers in floating point format in 8-bit words:
● The first bit is used for the sign of the number (1 is negative).
● The second bit used for the sign of the exponent (1 is negative).
● The next two bits are used for the magnitude of the exponent. We do not add an offset to the exponent.
● The final four bits are used for the magnitude of the mantissa.
Convert the value $(11101001)_2$ in this representation into its decimal equivalent.
(a) -0.109375
(b) -1.109375
(c) -0.390625
(d) -1.390625

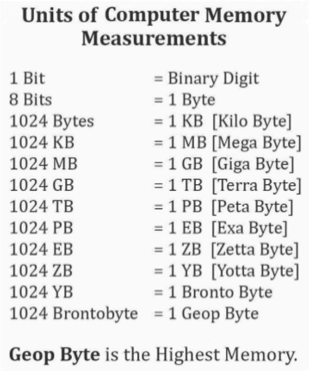
Q0.7.1 The range of integers that can be stored in a 10-bit register is ___________________?
(a) -512 to +511
(b) -511 to +512
(c) -254 to +255
(d) 0 to 1023
(e) 0 to 1024
(f) -255 to +254

Q0.7.2 The range of integers that can be stored in a 12-bit register is ________________?
(a) -2048 to +2047
(b) -2047 to +2048
(c) -1024 to +1023
(d) -1023 to +1024
(e) 0 to 4095
(f) 0 to 4096

Q0.8.1 The data-type Float (32-bit total = 23-bit mantissa, 8-bit exponent) gives us about 7-8 significant decimal digits.
The data-type Double (64-bit total = 52-bit mantissa, 11-bit exponent) gives us about 15-16 significant decimal digits.
Let's create a new data-type called Triple, which has 96-bits total; a 78-bit mantissa and a 17-bit exponent.
Roughly how many significant decimal digits will this type give us?
(a) 21-22 significant decimal digits
(b) 23-24 significant decimal digits
(c) 25-26 significant decimal digits
(d) 27-28 significant decimal digits

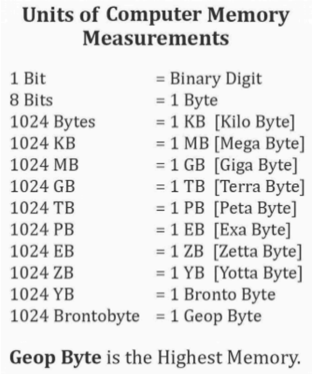
Q0.8.2 The data-type Float (32-bit total = 23-bit mantissa, 8-bit exponent) gives us about 7-8 significant decimal digits.
The data-type Double (64-bit total = 52-bit mantissa, 11-bit exponent) gives us about 15-16 significant decimal digits.
Let's create a new data-type called Triple, which has 96-bits total; a 84-bit mantissa and an 11-bit exponent.
Roughly how many significant decimal digits will this type give us?
(a) 21-22 significant decimal digits
(b) 23-24 significant decimal digits
(c) 25-26 significant decimal digits
(d) 27-28 significant decimal digits

Q0.9.1 Consider that you are designing a world-wide database for keeping the passport records of every human being alive on earth. Let's assume that the current human population is approx. 9 billion people. For each person, you will be keeping the following information in your database:

Database Field	Space Required	Memory Units (for reference)
Passport Type	2 bytes	 Units of Computer Memory Measurements 1 Bit = Binary Digit 8 Bits = 1 Byte 1024 Bytes = 1 KB [Kilo Byte] 1024 KB = 1 MB [Mega Byte] 1024 MB = 1 GB [Giga Byte] 1024 GB = 1 TB [Terra Byte] 1024 TB = 1 PB [Peta Byte] 1024 PB = 1 EB [Exa Byte] 1024 EB = 1 ZB [Zetta Byte] 1024 ZB = 1 YB [Yotta Byte] 1024 YB = 1 Bronto Byte 1024 Brontobyte = 1 Geop Byte **Geop Byte** is the Highest Memory.
Passport Number	14 bytes	
First Name	48 bytes	
Last Name	48 bytes	
Nationality	36 bytes	
Date of Birth	8 bytes	
Expiry Date	8 bytes	

Estimate the total amount of space that you will need to store the above information for all the people alive on earth today?
(a) 1.16 TB
(b) 1.34 TB
(c) 1.48 TB
(d) 11.6 TB
(e) 13.4 TB

Q0.9.2 Consider that you are designing a world-wide database for keeping the passport records of every human being alive on earth. Let's assume that the current human population is approx. 8 billion people. For each person, you will be keeping the following information in your database:

Database Field	Space Required	Memory Units (for reference)
Passport Type	4 bytes	 **Units of Computer Memory Measurements** 1 Bit = Binary Digit 8 Bits = 1 Byte 1024 Bytes = 1 KB [Kilo Byte] 1024 KB = 1 MB [Mega Byte] 1024 MB = 1 GB [Giga Byte] 1024 GB = 1 TB [Terra Byte] 1024 TB = 1 PB [Peta Byte] 1024 PB = 1 EB [Exa Byte] 1024 EB = 1 ZB [Zetta Byte] 1024 ZB = 1 YB [Yotta Byte] 1024 YB = 1 Bronto Byte 1024 Brontobyte = 1 Geop Byte **Geop Byte** is the Highest Memory.
Passport Number	16 bytes	
First Name	40 bytes	
Last Name	56 bytes	
Nationality	24 bytes	
Date of Birth	10 bytes	
Expiry Date	10 bytes	

Estimate the total amount of space that you will need to store the above information for all the people alive on earth today?
(a) 1.16 TB
(b) 1.28 TB
(c) 1.34 TB
(d) 11.6 TB
(e) 13.4 TB

Q0.10.1 A 32-bit computer system has 4 GB of memory installed in it; these represent addresses $(00000000)_{16}$ - $(FFFFFFFF)_{16}$. However, the system programmer is told that she can only use memory from $(B1002000)_{16}$ to $(EA001FFF)_{16}$. The memory below the address $(B1002000)_{16}$ is unavailable and the memory above $(EA001FFF)_{16}$ is also unavailable.
How much memory is available to the system programmer?
(a) 956301.31 KB
(b) 933888 KB
(c) 37.19 MB
(d) 39 MB
(e) 912 MB
(f) 956.30 MB

Q0.10.2 A 32-bit computer system has 4 GB of memory installed in it; these represent addresses $(00000000)_{16}$ - $(FFFFFFFF)_{16}$. However, the system programmer is told that she can only use memory from $(CA009000)_{16}$ to $(FF008FFF)_{16}$. The memory below the address $(CA009000)_{16}$ is unavailable and the memory above $(FF008FFF)_{16}$ is also unavailable.
How much memory is available to the system programmer?
(a) 868352 KB
(b) 889192.45 KB
(c) 33.38 MB
(d) 35 MB
(e) 848 MB
(f) 889.19 MB

Q1.1.1 Represent the decimal number -19.75 in binary using the sign-and-magnitude binary representation (negative = 1).
(a) 111111.001
(b) 111100.100
(c) 110011.110

(d) 101100.010

Q1.1.2 Represent the decimal number -28.50 in binary using the sign-and-magnitude binary representation (negative = 1).
(a) 111111.001
(b) 111100.100
(c) 110011.110
(d) 100011.100

Q1.1.3 Represent the decimal number -31.125 in binary using the sign-and-magnitude binary representation (negative = 1).
(a) 111111.001
(b) 111100.100
(c) 110011.110
(d) 100000.111

Q1.2.1 Consider the unsigned binary integer $(1100101111)_2$
What would be its equivalent representation in the octal number system?
(a) $(6274)_8$
(b) $(3260)_8$
(c) $(1457)_8$
(d) $(0815)_8$

Q1.2.2 Consider the unsigned binary integer $(1011001010011)_2$
What would be its equivalent representation in the hexadecimal number system?
(a) $(5715)_{16}$
(b) $(1653)_{16}$
(c) $(45720)_1$
(d) $(B298)_{16}$

Q1.2.3 Consider the unsigned binary integer $(1000110010110)_2$
What would be its equivalent representation in the hexadecimal number system?
(a) $(4502)_{16}$
(b) $(8CB0)_{16}$
(c) $(36016)_{16}$
(d) $(1196)_{16}$

Q1.3.1 Which of these statements are true?
(a) Registers can be accessed more quickly than main memory.
(b) Registers can be addressed with fewer address bits than a main memory address.
(c) Every instruction has an equal likelihood of being executed.
(d) Accessing data from cache is faster than accessing main memory.
(e) Using cache changes the result that a program will produce

Q1.3.2 Which of these statements are false?
(a) Caching is effective because the likelihood of an address being accessed is greater if it has been accessed recently.
(b) In a von Neumann machine there are separate memory pathways to data and instructions.
(c) Accessing data from main memory is faster than accessing instructions.
(d) Main memory is larger than cache memory.
(e) Programs will run faster if the instructions are smaller.

Q1.3.3 Which of these statements are true?
(a) We need 32 bits to address either a register or main memory location.
(b) The purpose of a cache is to reduce the number of bits needed to address main memory.
(c) The goal of using a cache is to reduce the time taken to access data and instructions.
(d) Main memory can be accessed faster than registers
(e) An advantage of the Harvard architecture is that instruction and data memories can be accessed in parallel

Q1.4.1 On a hypothetical computer, real numbers are stored in a two's complement fixed-point binary format:

- The first five bits represent the integer part of the number.
- The last three bits represent the fractional part of the number.

Compute the binary representation of the answer to the arithmetic equation
(01010.101) - (11100.100)
(a) 10111001
(b) 01111101
(c) 01110001
(d) 00111001

Q1.4.2 On a hypothetical computer, real numbers are stored in a two's complement fixed-point binary format:

- The first five bits represent the integer part of the number.
- The last three bits represent the fractional part of the number.

Compute the binary representation of the answer to the arithmetic equation
(00010.111) - (10011.010)
(a) 10110001
(b) 01111101
(c) 00110001
(d) 01111011

Q1.4.3 On a hypothetical computer, real numbers are stored in a two's complement fixed-point binary format:

- The first five bits represent the integer part of the number.
- The last three bits represent the fractional part of the number.

Compute the binary representation of the answer to the arithmetic equation
(01110.100) - (11111.001)
(a) 11101101
(b) 01111011
(c) 01110001
(d) 01101101

Q1.5.1 Consider the binary integer $(10011010)_2$
If it is an unsigned integer, the decimal equivalent is _________.
If it is a 2's complement integer, the decimal equivalent is _________.
(a) -154
(b) -102
(c) -100
(d) 100
(f) 102
(e) 154

Q1.5.2 Consider the binary integer $(10101101)_2$
If it is an unsigned integer, the decimal equivalent is _________.
If it is a 2's complement integer, the decimal equivalent is _________.
(a) -173
(b) -83
(c) -81
(d) 81
(e) 83
(f) 173

Q1.5.3 Consider the binary integer $(11010010)_2$
If it is an unsigned integer, the decimal equivalent is _________.
If it is a 2’s complement integer, the decimal equivalent is _________.
(a) -210
(b) -46
(c) -44
(d) 44
(e) 46
(f) 210

Q1.6.1 Which of these statements are true?
(a) A pipeline allows successive instructions to be at different stages of the execution cycle.
(b) Using a pipeline will increase the throughput of the processor.
(c) Instructions which transfer control (e.g. jump instructions) will reduce the effectiveness of the pipeline.
(d) A 5 stage pipeline will mean that one instruction is completed on every clock tick.
(e) If the processor clock speed is doubled then programs will run at twice the speed.

Q1.6.2 Which of these statements are true?
(a) The Data Fetch stage of instruction execution loads the next instruction into the instruction register.
(b) Data is transferred between processor and memory using the control bus.
(c) Doubling the length of a pipeline will double the throughput of the processor.
(d) Conditional jump instructions will affect the benefit gained from pipelining.
(e) The use of cache is transparent to the programmer

Q1.6.3 Which of the following are true?
(a) The number of instructions executed per second is equal to the clock speed.
(b) An instruction set architecture specifies the instruction set precisely.
(c) The throughput of a pipeline is affected by the number of ‘jump’ instructions.
(d) An instruction normally specifies each of a) the operation to be performed b) the two operands c) the location to store the result d) the address of the next instruction.
(e) The value of an ‘immediate’ operand is stored in a register.

Q1.7.1 A hypothetical computer stores real numbers in floating point format in 7-bit words:
● The first bit is used for the sign of the number (1 is negative).
● The second bit used for the sign of the exponent (1 is negative).
● The next two bits are used for the magnitude of the exponent. (We do not add an offset to the exponent).
● The final three bits are used for the magnitude of the mantissa.
Convert the value (1011101)2 in this representation into its decimal equivalent.
(a) -13
(b) -5
(c) -0.203125
(d) -0.078125

Q1.7.2 A hypothetical computer stores real numbers in floating point format in 7-bit words:
● The first bit is used for the sign of the number (1 is negative).
● The second bit used for the sign of the exponent (1 is negative).
● The next two bits are used for the magnitude of the exponent. (We do not add an offset to the exponent).
● The final three bits are used for the magnitude of the mantissa.
Convert the value $(1010110)_2$ in this representation into its decimal equivalent.
(a) -7
(b) -3
(c) -0.4375
(d) -0.1875

Q1.7.3 A hypothetical computer stores real numbers in floating point format in 7-bit words:

- The first bit is used for the sign of the number (1 is negative).
- The second bit used for the sign of the exponent (1 is negative).
- The next two bits are used for the magnitude of the exponent. (We do not add an offset to the exponent).
- The final three bits are used for the magnitude of the mantissa.

Convert the value $(1001100)_2$ in this representation into its decimal equivalent.
(a) -3
(b) -1
(c) -0.75
(d) -0.25

Q1.8.1 Which of the following decimal integers can be stored in a 7-bit register?
(a) -128
(b) -64
(c) 63
(d) 64
(e) 128
(f) 255

Q1.8.2 Which of the following decimal integers can be stored in a 9-bit register?
(a) -512
(b) -256
(c) 255
(d) 256
(e) 512
(f) 1023

Q1.8.3 Which of the following decimal integers can be stored in a 11-bit register?
(a) -2048
(b) -1024
(c) 1023
(d) 1024
(e) 2048
(f) 4095

Q1.9.1 Which of these statements are true?
(a) An interpreter is a software implementation of an existing Instruction Set Architecture.
(b) A just in time compiler generates executable code at runtime.
(c) A compiler must generate binary machine code that can be loaded and run directly.
(d) A program compiled using a compiler will generate the same result as one executed through an interpreter.
(e) The JVM is only capable of executing programs written in Java.

Q1.9.2 Which of these statements are true?
(a) Code optimisation typically transforms the code into an equivalent program that will run faster.
(b) A compiler must generate binary code for the machine on which it is running.
(c) An assembler just maps instruction mnemonics written in assembler code into the corresponding bit pattern.
(d) Interpreters are well suited to a development environment whilst compilers are more suited to production environments.
(e) A compiler must check the syntactic correctness of a program.

Q1.9.3 Which of these statements are true?
(a) An interpreter written in a high level language will be portable across different computer architectures.
(b) Cross compilation means that we generate code for a different machine to that on which we compile it.
(c) Interpreters have to generate machine code at execution time.
(d) Pure interpreters provide a software implementation of a machine.
(e) In general, an interpreted program will execute faster than a compiled one.

Q1.10.1 Consider the following RPN expression: 7 3 5 4 * 9 - * +
Evaluate this expression using a stack and select the correct answer from the given choices.
(a) -44
(b) -21
(c) 7
(d) 35
(e) 40
(f) 44

Q1.10.2 Consider the following RPN expression: 7 3 * 5 4 9 + * -
Evaluate this expression using a stack and select the correct answer from the given choices.
(a) -44
(b) -21
(c) 7
(d) 35
(e) 40
(f) 44

Q1.10.3 Consider the following RPN expression: 7 3 5 + 4 9 * - +
Evaluate this expression using a stack and select the correct answer from the given choices.
(a) 40
(b) -44
(c) -21
(d) 7
(e) 44
(f) 35

Q2.1.1 Which of the following statements about system calls are true?
(a) Most system calls are accessed via an Application Programming Interface (API).
(b) All system calls are written in assembly language, as they need to communicate with the hardware.
(c) A system call is an interface to request services from the Operating System kernel.
(d) System calls can only be used through a command line interface.
(e) Most modern smartphone Operating Systems (e.g. iOS, Android) do not provide system calls because they are simplified for handheld devices.

Q2.1.2 Which of the following statements about system calls are true?
(a) Modern smartphone Operating Systems (e.g. iOS, Android) do not provide system calls because they are simplified for handheld devices.
(b) System calls are typically written in a high-level programming language (e.g. C, C++)
(c) System calls can be invoked through a GUI or a command line interface.
(d) System calls are only used for handling file I/O.
(e) System calls can only be used in compiled programs.

Q2.1.3 Which of the following statements about system calls are true?
(a) System calls are all written in assembly language, as they need to communicate with the hardware.
(b) System calls provide an interface to request services from the Operating System kernel.
(c) System calls can only be used through a command line interface.
(d) Modern smartphone Operating Systems (e.g. iOS, Android) provide system calls to mobile applications.
(e) System calls are only used for handling file I/O.

Q2.2.1 Which of the following statements about interrupts are true?
(a) The hardware triggers interrupts by sending a signal to the CPU
(b) Hardware can trigger an interrupt at any time
(c) Interrupts cannot be triggered by software
(d) Interrupts can be triggered by both hardware and software
(e) Hardware can only trigger interrupts at specific times

Q2.2.2 Which of the following statements about interrupts are true?
(a) Interrupts cannot be triggered by hardware
(b) Software interrupts are invoked through the hardware
(c) Interrupts can be triggered by both hardware and software
(d) Software triggers interrupts by executing a special operation
(e) System calls are invoked using a software interrupt

Q2.2.3 Which of the following statements about interrupts are true?
(a) When an interrupt occurs, the CPU waits until the current process is completed before transferring control to the interrupt service routine
(b) Hardware can only trigger interrupts at specific times
(c) Software interrupts are invoked through the hardware
(d) When an interrupt occurs, the CPU immediately stops what it is doing and transfers control to the interrupt service routine
(e) Hardware devices can trigger an interrupt at any time

Q2.3.1 What is the time complexity of this algorithm?

```
sum=0
product=1
for i=1 .. 7*n
  for j=1 .. n
    sum = sum+i*j
for j=20 .. 100*n
  product = product*j
```

(a) O(n)
(b) O(7n)
(c) O(7n+n)
(d) O(n^2)
(e) O(7n^2)

Q2.3.2 What is the time complexity of the following algorithm?

```
sum=0
product=1
for i=1 .. 10*n
  sum = sum+10*i
for i=1 .. 10*n
  for j=1 .. 10*n
    product = product+i*j
```

(a) O(10n)
(b) O(10n + 10n)
(c) O(20n)

(d) O(n^2)
(e) O(10n + 100n^2)

Q2.3.3 What is the time complexity of the following algorithm?

```
sum=0
product=1
for i=20 ... 100*n
  for j=20 .. 100*n
    sum=sum+a[i,j]
for i=1..100*n
  for j=1 .. 100*n
    product=product*a[i,j]
```

(a) O(n^2)
(b) O(2n^2)
(c) O(10000n^2)
(d) O(6400n^2 + 10000n^2)
(e) O(16400n^2)

Q2.4.1 Select all the following statements that are true:
(a) A CPU (short term) scheduler should execute considerably faster than a Job scheduler.
(b) A Job (long term) scheduler is invoked infrequently compared to a CPU scheduler.
(c) A Job (long term) scheduler selects a process from the processes that are in the ready queue.
(d) A CPU (short term) scheduler controls the degree of multiprogramming in a system, particularly when a multi-core CPU is used.
(e) A Job (long term) scheduler determines which programs are admitted to the system for processing.

Q2.4.2 Select all the following statements that are true:
(a) I/O-bound processes perform a lot of I/O operations, that is why they usually occupy the CPU for a long period.
(b) I/O-bound processes perform a lot of I/O operations, but they also do computations.
(c) I/O-bound processes generally have shorter CPU bursts than CPU-bound processes.
(d) I/O-bound processes usually take longer to execute than CPU-bound processes, as they spend most of the time waiting for data to be read or written.
(e) CPU-bound processes focus on doing computations, therefore, they do not spend any time doing I/O.

Q2.4.3 Select all the following situations that are considered voluntary process terminations:
(a) The operating system terminates an idle process to free up memory space.
(b) A process terminates with an error code.
(c) The user closes a process by clicking the close button of an application.
(d) A process completes its execution and exits.
(e) A process is terminated when it tries to access the (n+1)th element of an array which has n elements.

Q2.5.1 Which of the following statements are true about OS memory management and multitasking?
(a) Virtual memory abstracts main memory, separating logical and physical memory.
(b) Data that has been used recently is likely to be stored in a fast memory (cache), which lies between RAM and the CPU.
(c) CPU scheduling is the process of deciding which job in the ready queue is to be executed next
(d) CPU scheduling is the process of deciding which process in the blocked queue should be executed next.
(e) Virtual memory increases the size of the physical memory in the system

Q2.5.2 Which of the following statements are true about OS memory management and multitasking?
(a) CPU scheduling is the process of deciding which job in the ready queue is to be executed next

(b) The CPU performs multitasking by executing multiple jobs and switching frequently between them
(c) CPU scheduling is the process of deciding which process in the blocked queue should be executed next.
(d) Virtual memory allows the execution of a process that it is not completely in memory
(e) Data that has been used recently is stored in cache memory, which is managed by software.

Q2.5.3 Which of the following statements are true about OS memory management and multitasking?
(a) The CPU performs multitasking by executing multiple jobs and switching frequently between them.
(b) A process is allocated a maximum time quantum after which it is interrupted. This has the effect of multiple processes appearing to execute concurrently.
(c) Virtual memory increases the size of the physical memory in the system.
(d) Virtual memory maps logical addresses to physical memory addresses, which includes the secondary storage (swap area) as well.
(e) Data that has been used recently is likely to be stored in a fast memory (cache), which lies between RAM and the CPU.

Q2.6.1 Consider the following Java function:

```
public static void compute(long a){
  double b = 3.141;
  float c = 94.93;
  short d = 42;
  <some more code here>
}
```

Choose option(s) indicating the correct slots allocation for this function in the Java bytecode.
(a) this = slot 0; a = slot 1; b = slot 2; c = slots 3,4; d = slots 5,6
(b) this = slot 0; a = slots 1,2; b = slots 3,4; c = slot 5; d = slot 6
(c) a = slots 0,1; b = slots 2,3; c = slot 4; d = slot 5
(d) a = slot 0; b = slot 1; c = slots 2,3; d = slots 4,5

Q2.6.2 Consider the following Java function:

```
public static void compute(long a){
  float b = 94.93;
  short c = 42;
  double d = 3.141;
  <some more code here>
}
```

Choose option(s) indicating the correct slots allocation for this function in the Java bytecode.
(a) this = slot 0; a = slot 1; b = slots 2,3; c = slots 4,5; d = slot 6
(b) this = slot 0; a = slots 1,2; b = slot 3; c = slot 4; d = slots 5,6
(c) a = slots 0,1; b = slot 2; c = slot 3; d = slots 4,5
(d) a = slot 0; b = slots 1,2; c = slots 3,4; d = slot

Q2.6.3 Consider the following Java function:

```
public void compute(long a){
  float b = 94.93;
  double c = 3.141;
  short d = 42;
  <some more code here>
}
```

Choose option(s) indicating the correct slots allocation for this function in the Java bytecode.
(a) this = slot 0; a = slot 1; b = slots 2,3; c = slot 4; d = slots 5,6
(b) this = slot 0; a = slots 1,2; b = slot 3; c = slots 4,5; d = slot 6
(c) a = slots 0,1; b = slot 2; c = slots 3,4; d = slot 5
(d) a = slot 0; b = slots 1,2; c = slot 3; d = slots 4,5

Q2.7.1 Consider the following program:

```
int main(){
  printf("A");
  fork();
  printf("B");
  fork();
  fork();
  printf("C");
  fork();
  return 0;
}
```

How many times will the letters “A”, “B” and “C” be printed?
(a) A: 1 time, B: 2 times, C: 4 times
(b) A: 1 time, B: 2 times, C: 8 times
(c) A: 1 time, B: 4 times, C: 4 times
(d) A: 1 time, B: 4 times, C: 8 times

Q2.7.2 Consider the following program:

```
int main(){
  fork();
  printf("A");
  fork();
  printf("B");
  fork();
  printf("C");
  fork();
  return 0;
}
```

How many times will the letters “A”, “B” and “C” be printed?
(a) A: 1 time, B: 2 times, C: 8 times
(b) A: 1 time, B: 2 times, C: 4 times
(c) A: 2 time, B: 2 times, C: 8 times
(d) A: 2 time, B: 4 times, C: 8 times

Q2.7.3 Consider the following program:

```
int main(){
  printf("A");
  fork();
  fork();
  printf("B");
  fork();
  printf("C");
  fork();
  return 0;
}
```

How many times will the letters “A”, “B” and “C” be printed?
(a) A: 1 time, B: 4 times, C: 8 times
(b) A: 2 time, B: 4 times, C: 8 times

(c) A: 1 time, B: 8 times, C: 16 times
(d) A: 2 time, B: 8 times, C: 16 times

Q2.8.1 Which of the following statements about the JVM stack are true?
(a) The slots in the calling method's stack frame are accessible to the callee method.
(b) Slot 0 always contains a reference to 'this'.
(c) Local variables (of the method) are stored in the stack frame.
(d) The value of each parameter in a method call is stored in the stack frame.
(e) A local variable or parameter can use two slots in the stack frame.

Q2.8.2 Which of the following statements about the JVM stack are true?
(a) The JVM stack can be infinitely large.
(b) A value of type 'double' uses two slots in the stack frame.
(c) When a method returns, the values in its stack frame are accessible to the calling method.
(d) Slot 0 always contains a reference to 'this'.
(e) When a method is called a new stack frame is created.

Q2.8.3 Which of the following statements about the JVM stack are true?
(a) A called method can access the slots in the calling method's stack frame.
(b) The values in a method's stack frame are accessible to the recursive calls of the same method.
(c) A new stack frame is created for every method call.
(d) For 'static' methods the slot 0 contains a reference to 'this'.
(e) Values of type 'long' occupy two slots in the stack frame.

Q2.9.1 Consider the following set of processes:

Processes	Arrival Time	Burst Time
P1	0 ms	8 ms
P2	3 ms	4 ms
P3	5 ms	6 ms
P4	7 ms	2 ms

What is the Average Waiting Time using SRTF CPU scheduling policy?
(a) 3.75 ms
(b) 5.75 ms
(c) 6.00 ms
(d) 6.25 ms

Q2.9.2 Consider the following set of processes:

Processes	Arrival Time	Burst Time	Priority
P1	0 ms	8 ms	3
P2	3 ms	4 ms	2
P3	5 ms	6 ms	1
P4	7 ms	2 ms	2

What is the Average Waiting Time using Preemptive Priority CPU scheduling policy?
A lower priority number indicates higher priority. Ties are broken using FCFS order.
(a) 3.75 ms
(b) 5.75 ms
(c) 6.00 ms
(d) 6.25 ms

Q2.9.3 Consider the following set of processes:

Processes	Arrival Time	Burst Time
P1	0 ms	8 ms
P2	3 ms	4 ms
P3	5 ms	6 ms
P4	7 ms	2 ms

What is the Average Waiting Time using Round Robin CPU scheduling policy?
(a) 3.75 ms
(b) 5.75 ms
(c) 6.00 ms
(d) 6.25 ms

Q2.10.1 Consider the following set of processes:

Processes	Arrival Time	Burst Time
P1	0 ms	8 ms
P2	3 ms	4 ms
P3	5 ms	6 ms
P4	7 ms	2 ms

What is the Average Turnaround Time using SRTF CPU scheduling policy?
(a) 8.50 ms
(b) 10.75 ms
(c) 11.00 ms
(d) 11.25 ms

Q2.10.2 Consider the following set of processes:

Processes	Arrival Time	Burst Time	Priority
P1	0 ms	8 ms	3
P2	3 ms	4 ms	2
P3	5 ms	6 ms	1
P4	7 ms	2 ms	2

What is the Average Turnaround Time using Preemptive Priority CPU scheduling policy?
A lower priority number indicates higher priority. Ties are broken using FCFS order.
(a) 8.50 ms
(b) 10.75 ms
(c) 11.00 ms
(d) 11.25 ms

Q2.10.3 Consider the following set of processes:

Processes	Arrival Time	Burst Time
P1	0 ms	8 ms
P2	3 ms	4 ms
P3	5 ms	6 ms
P4	7 ms	2 ms

What is the <u>Average Turnaround Time</u> using <u>Round Robin</u> CPU scheduling policy?
(a) 8.50 ms
(b) 10.75 ms
(c) 11.00 ms
(d) 11.25 ms

Q3.1.1 Which of the following statement(s) is/are true?
(a) The behaviour of a multi-threaded process is always deterministic.
(b) One disadvantage of multithreading is that it always leads to memory consistency errors.
(c) Threads within a process share the same data section.
(d) Race conditions can occur between threads within a process.
(e) Every thread within a process must be mapped to a separate kernel thread.

Q3.1.2 Which of the following statement(s) is/are true?
(a) The behaviour of a multi-threaded process can be non-deterministic.
(b) Threads within a process can be mapped to the same kernel thread.
(c) Each thread within a process maintains its own copy of shared data.
(d) A process can have 0 threads.
(e) Threads within a process are guaranteed not to interfere with each other.

Q3.1.3 Which of the following statement(s) is/are true?
(a) Threads within a process can interact with each other through shared data.
(b) Memory consistency errors occur when multiple threads “race” to modify the same shared data item.
(c) Race condition occurs when multiple processes compete to finish their tasks in the shortest amount of time.
(d) Preventing all but one thread from writing to the same shared data item concurrently is adequate to avoid memory consistency errors.
(e) All threads are managed directly by the operating system.

Q3.2.1 Which of the following protocols are used in the Application Layer?
(a) HTTP
(b) TCP
(c) SMTP
(d) IP
(e) UDP

Q3.2.2 Which of the following protocols are used in the Transport Layer?
(a) HTTP
(b) TCP
(c) SMTP
(d) IP
(e) UDP

Q3.2.3 Which of the following protocols are used in the Network Layer?
(a) HTTP
(b) TCP

(c) SMTP
(d) IP
(e) UDP

Q3.3.1 The term ‘Latency’ refers to ...
(a) Rate at which something is able to move
(b) Delay that happens in data communication over a network
(c) Transmission capacity of a network
(d) Rate at which bits are transferred end-to-end between sender and receiver
(e) Strength of the connection between two hosts in the network

Q3.3.2 The term ‘Bandwidth’ refers to ...
(a) Rate at which bits are transferred end-to-end between sender and receiver
(b) Strength of the connection between two hosts in the network
(c) Transmission capacity of a network
(d) Delay that happens in data communication over a network
(e) Rate at which something is able to move

Q3.3.3 The term ‘Throughput’ refers to ...
(a) Length of time a packet needs to queue in the buffer
(b) Delay that happens in data communication over a network
(c) Transmission capacity of a network
(d) Strength of the connection between two hosts in the network
(e) Rate at which bits are transferred end-to-end between sender and receiver

Q3.4.1 Which of the following statements about ‘Hosts’ are true?
(a) Hosts can be clients on the network
(b) Hosts are the same thing as End Systems
(c) Hosts can be routers in the network core
(d) Hosts can be servers on the network
(e) Hosts must be connected to the network via a wired connection

Q3.4.2 Which of the following statements about the ‘Network Edge’ are true?
(a) Network Edge includes all clients in the network
(b) Network Edge includes all routers in the network
(c) Network Edge is where packet switching takes place
(d) Network Edge means the physical wires that send bits on the network
(e) Network Edge includes all servers in the network

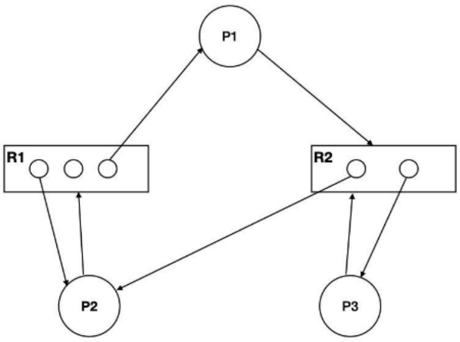
Q3.4.3 Which of the following statements about the ‘Network Core’ are true?
(a) Network Core is where packet routing takes place
(b) Network Core includes all hosts in the network
(c) Network Core is a mesh of interconnected routers
(d) Network Core means the physical wires that send bits on the network
(e) Network Core is where packet forwarding takes place

Q3.5.1 You and your friend John are working on a Parallel Programming project, which is an application that does not use IO functions. You have been told by your project manager that your software should have at-least 6 times speedup as compared to its sequential implementation. You have also been told that your application will run on a system with 16 CPUs. Estimate the minimum percentage of the code that needs to be parallelized in your application, in order to meet the above performance requirement?
(a) 86.75%
(b) 88.89%
(c) 92.90%
(d) 93.92%
(e) 98.07%

Q3.5.2 You and your friend Alice are working on a Parallel Programming project, which is an application that does not use IO functions. You have been told by your project manager that your software should have at-least 10 times speedup as compared to its sequential implementation. You have also been told that your application will run on a system with 24 CPUs. Estimate the minimum percentage of the code that needs to be parallelized in your application, in order to meet the above performance requirement?
(a) 86.75%
(b) 88.89%
(c) 92.90%
(d) 93.92%
(e) 98.07%

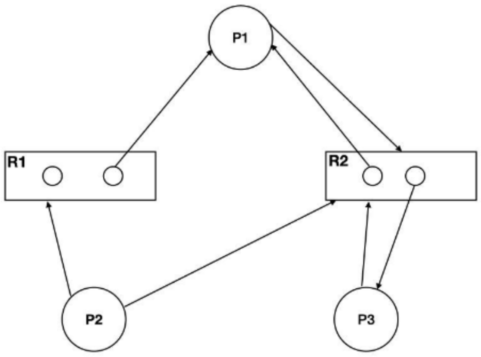
Q3.5.3 You and your friend Ahmad are working on a Parallel Programming project, which is an application that does not use IO functions. You have been told by your project manager that your software should have at-least 20 times speedup as compared to its sequential implementation. You have also been told that your application will run on a system with 32 CPUs. Estimate the minimum percentage of the code that needs to be parallelized in your application, in order to meet the above performance requirement?
(a) 86.75%
(b) 88.89%
(c) 92.90%
(d) 93.92%
(e) 98.07%

Q3.6.1 Consider the following resource allocation graph (RAG) of three processes and two types of resources:



From the following statements, select all that are valid for the above set of processes and resources.
(a) If we remove the currently available instance of R1, processes P1, P2, and P3 will be deadlocked.
(b) Only process P3 is currently blocked.
(c) If we add one more instance to R2, the deadlock will be resolved.
(d) Process P2 can complete its execution, followed by either P1 or P3.
(e) Processes P1, P2, and P3 are currently deadlocked.

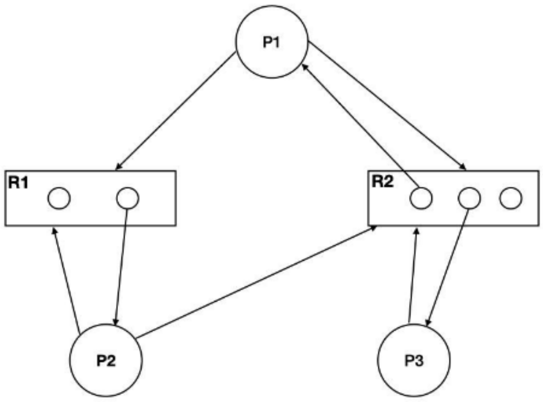
Q3.6.2 Consider the following resource allocation graph (RAG) of three processes and two types of resources:



From the following statements, select all that are valid for the above set of processes and resources.

(a) If we add one more instance to R2, the deadlock will be resolved.
(b) If we add one more instance to R1, the deadlock will be resolved.
(c) Process P2 can complete its execution, followed by either P1 or P3.
(d) Only processes P1 and P3 are currently blocked.
(e) Processes P1, P2, and P3 are currently deadlocked.

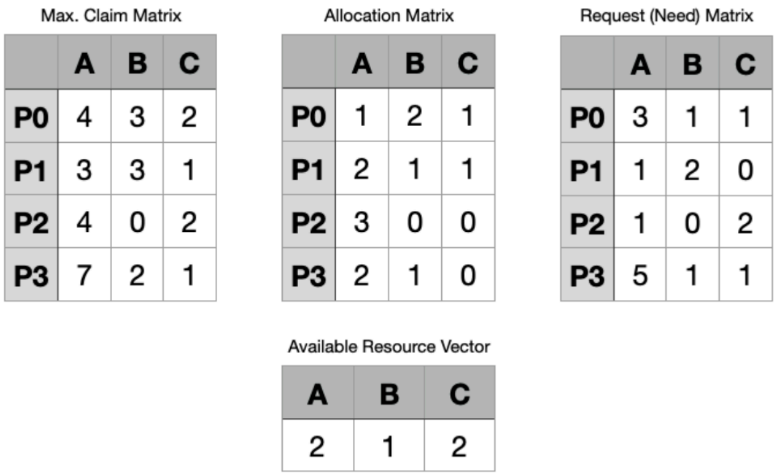
Q3.6.3 Consider the following resource allocation graph (RAG) of three processes and two types of resources:



From the following statements, select all that are valid for the above set of processes and resources.

(a) Only process P3 is currently blocked.
(b) Process P2 can complete its execution, followed by either P1 or P3.
(c) Process P1 can complete its execution, followed by either P2 or P3.
(d) Processes P1, P2, and P3 are currently deadlocked.
(e) If we add one more instance to R1, the deadlock will be resolved.

Q3.7.1 A resource allocation system that uses Banker's algorithm for 3 resource types (A, B, C) and 4 processes (P0, P1, P2, P3) is currently in the following state.



Max. Claim Matrix

	A	B	C
P0	4	3	2
P1	3	3	1
P2	4	0	2
P3	7	2	1

Allocation Matrix

	A	B	C
P0	1	2	1
P1	2	1	1
P2	3	0	0
P3	2	1	0

Request (Need) Matrix

	A	B	C
P0	3	1	1
P1	1	2	0
P2	1	0	2
P3	5	1	1

Available Resource Vector

A	B	C
2	1	2

(Max. Claim Matrix: max need of each process. Allocation Matrix: resources held by each process. Request (Need) Matrix: resources needed to complete. Available Resource Vector: free resources.)

Presuming that the system is currently in Safe State, which one(s) of the following safe sequence(s) is/are possible?

(a) P2,P0,P1,P3

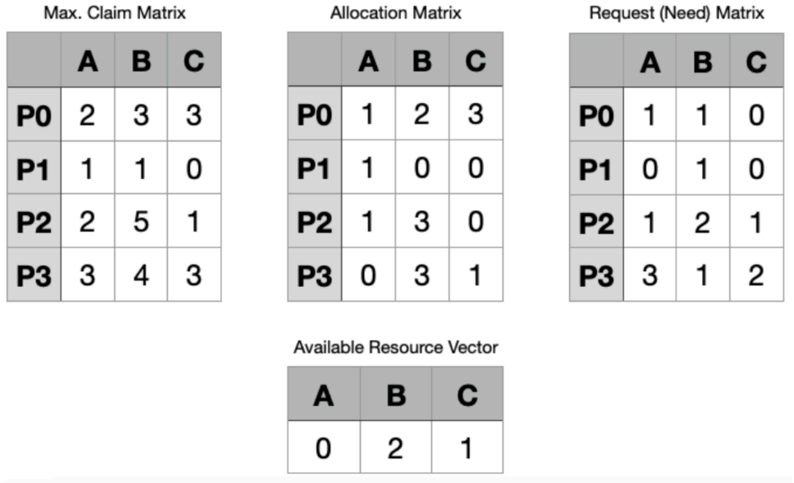
(b) P2,P0,P3,P1

(c) P2,P1,P0,P3

(d) P2,P1,P3,P0

(e) The presumption is incorrect, the system is not in a Safe State

Q3.7.2 A resource allocation system that uses Banker's algorithm for 3 resource types (A, B, C) and 4 processes (P0, P1, P2, P3) is currently in the following state.



Max. Claim Matrix

	A	B	C
P0	2	3	3
P1	1	1	0
P2	2	5	1
P3	3	4	3

Allocation Matrix

	A	B	C
P0	1	2	3
P1	1	0	0
P2	1	3	0
P3	0	3	1

Request (Need) Matrix

	A	B	C
P0	1	1	0
P1	0	1	0
P2	1	2	1
P3	3	1	2

Available Resource Vector

A	B	C
0	2	1

(Max. Claim Matrix: max need of each process. Allocation Matrix: resources held by each process. Request (Need) Matrix: resources needed to complete. Available Resource Vector: free resources.)

Presuming that the system is currently in Safe State, which one(s) of the following safe sequence(s) is/are possible?

(a) P1,P2,P0,P3

(b) P1,P2,P3,P0

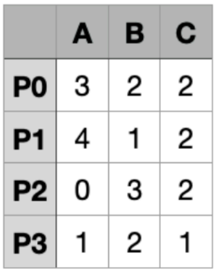
(c) P1,P3,P0,P2

(d) P1,P3,P2,P0

(e) The presumption is incorrect, the system is not in a Safe State.

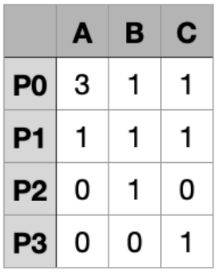
Q3.7.3 A resource allocation system that uses Banker's algorithm for 3 resource types (A, B, C) and 4 processes (P0, P1, P2, P3) is currently in the following state.

Max. Claim Matrix



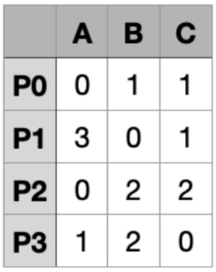
	A	B	C
P0	3	2	2
P1	4	1	2
P2	0	3	2
P3	1	2	1

Allocation Matrix



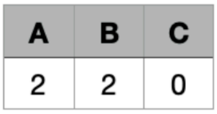
	A	B	C
P0	3	1	1
P1	1	1	1
P2	0	1	0
P3	0	0	1

Request (Need) Matrix



	A	B	C
P0	0	1	1
P1	3	0	1
P2	0	2	2
P3	1	2	0

Available Resource Vector



A	B	C
2	2	0

(Max. Claim Matrix: max need of each process. Allocation Matrix:resources held by each process. Request (Need) Matrix: resources needed to complete. Available Resource Vector: free resources.)
Presuming that the system is currently in Safe State, which one(s) of the following safe sequence(s) is/are possible?
(a) P3,P0,P1,P2
(b) P3,P0,P2,P1
(c) P3,P2,P1,P0
(d) P3,P2,P0,P1
(e) The presumption is incorrect, the system is not in a Safe State.

Q3.8.1 Let's assume we have two hosts A & B connected through 2 routers with zero propagation delay. We would like to transmit a 20 Mbit file from A to B, where the link bandwidths are given as R_1 = 10Mbps, R_2 = 4Mbps and R_3 = 5Mbps. Assume that the file is completely stored by a router before it starts sending it to the next link.
What would be the end-to-end delay between the hosts A & B?
(a) 2 seconds
(b) 5 seconds
(c) 11 seconds
(d) 13 seconds
(e) 17 seconds

Q3.8.2 Let's assume we have two hosts A & B connected through 2 routers with zero propagation delay. We would like to transmit a 24 Mbit file from A to B, where the link bandwidths are given as R_1 = 8Mbps, R_2 = 4Mbps and R_3 = 6Mbps. Assume that the file is completely stored by a router before it starts sending it to the next link.
What would be the end-to-end delay between the hosts A & B?
(a) 3 seconds
(b) 6 seconds
(c) 11 seconds
(d) 13 seconds
(e) 17 seconds

Q3.8.3 Let's assume we have two hosts A & B connected through 2 routers with zero propagation delay. We would like to transmit a 45 Mbit file from A to B, where the link bandwidths are given as R_1 = 5Mbps, R_2 = 15Mbps and R_3 = 9Mbps. Assume that the file is completely stored by a router before it starts sending it to the next link.
What would be the end-to-end delay between the hosts A & B?
(a) 3 Seconds
(b) 9 seconds
(c) 11 seconds

(d) 13 seconds
(e) 17 seconds

Q3.9.1 A packet propagates over an optical fibre link of distance 3600 km with a transmission rate of 36 Mbps. The length of the packet is 1500 bytes and the propagation speed is 2.5 x 10_8 m/s.
Select all the following statements that are true:
(a) The propagation delay d_{prop} = 14.40 ms
(b) The propagation delay d_{prop} = 14.40 sec
(c) The transmission delay d_{trans} = 41.67 µs
(d) The transmission delay d_{trans} = 333.33 µs
(e) The propagation delay depends on packet length.

Q3.9.2 A packet propagates over an optical fibre link of distance 2700 km with a transmission rate of 22 Mbps. The length of the packet is 1400 bytes and the propagation speed is 2.5 x 10_8 m/s.
Select all the following statements that are true:
(a) The propagation delay d_{prop} = 10.80 ms
(b) The propagation delay d_{prop} = 10.80 sec
(c) The transmission delay d_{trans} = 63.63 µs
(d) The transmission delay d_{trans} = 509.09 µs
(e) The propagation delay depends on the length of the link.

Q3.9.3 A packet propagates over an optical fibre link of distance 4300 km with a transmission rate of 41 Mbps. The length of the packet is 1350 bytes and the propagation speed is 2.5 x 10_8 m/s.
Select all the following statements that are true:
(a) The propagation delay d_{prop} = 17.20 ms
(b) The propagation delay d_{prop} = 17.20 sec
(c) The transmission delay d_{trans} = 32.93 µs
(d) The transmission delay d_{trans} = 263.41 µs
(e) The propagation delay depends on the packet length.

Q3.10.1 Which of the following does the TCP protocol provide?
(a) Congestion control
(b) Flow control
(c) In-order delivery
(d) Low delay
(e) Reasonable throughput

Q3.10.2 Which of the following does the UDP protocol provide?
(a) Best-effort communication
(b) Connectionless communication
(c) Delay guarantees
(d) Flow control
(e) In-order delivery

Q3.10.3 Which of the following cannot be provided by TCP?
(a) Bandwidth guarantees
(b) Congestion control guarantees
(c) Delay guarantees
(d) Ordered delivery guarantees
(e) Throughput guarantees