QIN, YUAN

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EDUCATION

ETH Zurich, Dept. of Information Technology and Electrical Engineering — Zurich, Switzerland
Master of Science, Electrical Engineering and Information Technology — 09/2023 - Present

- **Relevant coursework**: High-Level Synthesis, Graph Theory, Mathematical Optimization, Computer Architecture, Machine Learning.

Southeast University, School of Electronic Science & Engineering — Nanjing, China
Bachelor of Engineering, Electronic Science and Technology — 09/2019 - 07/2023

- **GPA: 3.96/4.00**; Ranking: Top 3%

RESEARCH EXPERIENCES

Refactoring & Extending MILP-Based Buffer Placement (Master Project) — 10/2024 - 06/2025

Supervised by Prof. Lana Josipović, DYNAMO Group, ETH Zurich

- Worked on Dynamatic (an open-source MLIR-based HLS compiler developed at EPFL and hosted on GitHub), focusing on infrastructure refactoring and algorithm integration for buffer placement optimization.
- Redesigned the buffer placement infrastructure from timing-attribute-only to explicit buffer-type classification, enabling diverse buffer implementations with area-elasticity trade-offs.
- Refactored the MILP framework into modular constraint components, enabling flexible algorithm composition and reducing code duplication across multiple buffer placement algorithms.
- Integrated the CostAwareBuffers algorithm (developed in previous work) by implementing enhanced throughput constraints to support generalized buffer behaviors and incorporating an area-cost objective with LUT-usage-based penalties to guide buffer selection.
- Identified and resolved several critical modeling issues in the buffer placement infrastructure including component redundancy, latency imbalances, and memory bottlenecks, improving circuit throughput and modeling accuracy.
- Proposed a two-stage optimization strategy using precomputed optimal throughput values to linearize quadratic constraints, achieving 100x+ speedup in MIQCP solving time on complex benchmarks while maintaining solution optimality.

Cost-Aware Buffer Placement for Dataflow Circuit (Master Project) — 02/2024 - 07/2024

Supervised by Prof. Lana Josipović, DYNAMO Group, ETH Zurich

- Proposed a mathematical formulation that introduces minimum and maximum latency bounds for modeling four distinct buffer types with different area and elasticity characteristics, enabling finer-grained buffer optimization in dataflow circuits.
- Formulated a MILP-based buffer placement model that jointly maximizes throughput and minimizes buffer area cost by selecting low-cost buffer types where appropriate.
- Implemented the optimization model in a Python framework and validated it through Vivado synthesis, achieving 4.8 to 25.5% area reduction without throughput degradation on nine PolyBench benchmarks, compared to state-of-the-art work.
- Explored a theoretical framework for handling variable latency and initiation interval units in dataflow circuits, providing a foundation for robust buffer optimization under uncertainty.

Statistical Cell Delay Modeling under Input Transition Time Variability (Bachelor Thesis) — 12/2022 - 05/2023

Supervised by Prof. Peng Cao, National ASIC System Engineering Center, Southeast University

- Quantified delay statistics of sub-threshold inverter chains under correlated threshold-voltage and input-slew

variations.
- Derived a closed-form delay expression by fitting input slews with a piecewise-log function, yielding one unified formula for all stages.
- Validated the stage-propagation model in a 28 nm PDK: HSPICE Monte-Carlo results show 2.9–3.7 × lower error than previous work.

Roadside Cone Detection and Tracking for Racing Track Calibration (Summer Project) 07/2022 - 09/2022
Supervised by Prof. Quoc-Viet Dang, Samueli School of Engineering, University of California, Irvine (remote)
- Detected roadside cones in onboard racing videos using template matching enhanced by shape and color filters.
- Predicted cone motion using vehicle dynamics and matched detections across frames based on spatial proximity, achieving reliable multi-cone tracking.
- Projected cone detections to vehicle-centric world coordinates through homography.
- Calibrated the racing track's GPS trajectory with a Gurobi-solved optimization that minimized cone-to-vehicle positional error.

Interdependent Flip-flop Timing Analysis & Optimization for Near-Threshold Voltage Design 08/2021 - 06/2022
Supervised by Prof. Peng Cao, National ASIC System Engineering Center, Southeast University
- Developed an ANN-based interdependent timing model to capture the nonlinear setup/hold time and clock-to-q delay relationships in Near-Threshold Voltage flip-flops; trained on SPICE data within a strategically defined hexagonal region to achieve <0.69% MARE while minimizing simulation overhead.
- Integrated the model into Static Timing Analysis flow and implemented a GA-based iterative optimization algorithm that balances timing slack across critical paths, reducing minimum clock period by 1.70-6.28% without hardware cost.
- Validated on ISCAS'89 benchmarks under SMIC 40nm process at 0.6V, achieving up to 6.7% performance improvement with logarithmic runtime scaling for large-scale circuits.
- Co-first authored "Timing Analysis and Optimization Method with Interdependent Flip-flop Timing Model for Near-threshold Design," *Electronics* 2022.

HONORS & AWARDS

- **National Scholarship** for academic year 2020-2021, awarded by China's Ministry of Education & Southeast University (**0.2%** nationwide).
- **Zhongnan Scholarship for Realizing Dreams** for academic year 2020-2021, awarded to 1 student in School of Electronic Science & Engineering.
- **1st Prize**, The Advanced Mathematics Competition for Undergraduates at Southeast University (**2%**, 09/2020)
- **1st Prize**, The 17th Advanced Mathematics Competition for Undergraduates in Jiangsu Province (**3.5%**, 11/2020)
- **1st Prize**, The 12th National College Mathematics Competition (**7%**, 12/2020)
- **Southeast University Single-course Scholarships** (top **5%** in seven major courses)
- **Individual Scholarship for Excellence in Social Work** for academic year 2020-2021, awarded to 1 student in School of Electronic Science & Engineering.

SKILLS & ADDITIONAL

Skills: C++, Python, Verilog, Gurobi, MLIR, MATLAB, x86 Assembly, Git, LaTeX
Standardized Tests: GRE 331 (V: 161, 87%; Q: 170, 96%; taken in 2022); TOEFL 100 (R30, L25, W25, S20; taken in 2021)