QIN, YUAN

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EDUCATION

Southeast University, School of Electronic Science & Engineering — Nanjing, China
Bachelor of Engineering, Electronic Science and Technology — 09/2019 - 07/2023

- **GPA: 3.96/4.00**; Ranking: Top 3%

PUBLICATION

Peng Cao[1], **Yuan Qin**[1], Haiyang Jiang. **Timing Analysis and Optimization Method with Interdependent Flip-flop Timing Model for Near-threshold Design.** Electronics-2022.

RESEARCH EXPERIENCES

Identification and Tracking of Roadside Cones for Racing Track Calibration 07/2022 - 09/2022

Supervised by Dr. Quoc-Viet Dang, Samueli School of Engineering, University of California, Irvine (remote)

- Used template matching and shape and color filters to recognize cones at the roadside in racing videos, which achieved 100% recall rate and precision rate in a short time period.
- Designed a function with the speed and the steering of the car as input to predict the movement of cones from in-car perspective.
- Tracked each cone by applying the Euclidean distance between real and predicted location of the cone, which successfully achieved multi-object tracking in the target area.
- Adopted Projective Mappings for Image Warping to map out cones based on the camera view.
- Constructed optimization models to calibrate GPS locations of the track according to the difference of relative positions between the cones and the car. The optimization models were solved using the Gurobi optimizer.

Timing Analysis and Optimization of Interdependent Flip-flop Timing Model for NTV Design 08/2021 - 06/2022

Supervised by Assoc. Prof. Peng Cao, National ASIC System Engineering Center, Southeast University

- Established a timing analysis and optimization framework for NTV circuit design by leveraging the interdependency between the setup/hold time and clock-to-q delay for flip-flops to improve circuit performance without any additional area and power cost.
- Predicted the interdependent clock-to-q delay of flip-flop by ANN model, whose training data was generated by SPICE simulation in a restricted hexagonal area in the two-dimensional setup-hold time space, leading to high prediction accuracy and low simulation cost.
- Proposed an iterative circuit optimization method by integrating the ANN-based interdependent timing model into STA flow to minimize the clock period without any timing violations by balancing the timing slacks among iteratively selected paths.
- Employed Genetic Algorithm to find the optimal setup time and hold time for each flip-flop in the selected paths.
- Participated as the co-first author of *Timing Analysis and Optimization Method with Interdependent Flip-flop Timing Model for Near-threshold Design, Electronics*-2022.

Fast Timing Analysis Method for Multi-corner Scenarios Based on Machine Learning 03/2021 - 07/2021

Supervised by Assoc. Prof. Peng Cao, National ASIC System Engineering Center, Southeast University

- Adopted machine learning to predict the timing path delay data of multiple PVT corners according to some typical corners selected by greedy deletion.
- Reproduced results in an article which applied Multiple Linear Regression. Compared them with the results obtained by using SVM, Feedforward Neural Network, Random Forest, etc., with no improvement in prediction performance.
- Predicted the differences between results from Multiple Linear Regression and golden timing analysis through Neural Network based on XGBoost concept to achieve smaller Mean Square Errors in the prediction of most corners.

COURSE PROJECTS

Reproduction of the Forward Process of an Artificial Neural Network by Verilog 05/2022 - 06/2022

- Reproduced the forward process of an artificial neural network, including a convolution layer, a batch normalization process, a rectified linear unit (ReLU) and a fully connected layer, with MATLAB and Verilog RTL codes respectively, in order to implement it in FPGA.
- Used numerical analysis methods to analyze and design bit widths of integer bits and decimal places of each fixed-point number in each step to maintain a high precision and save memory space. Experimental results showed no precision loss compared with the input data.
- Schedule data and reuse computing units by the finite state machine.
- Implemented Verilog RTL codes in Vivado for simulation.

Design and Simulation of Coupled Waveguide for Blackbody Emission 03/2022 - 04/2022

- Explored the relationship between power efficiency and the combination of incident angle and coupling distance in a planar dielectric waveguide model based on some theories of waveguide and coupling effects.
- Verified a linear increase followed by a linear decrease of the logarithm of power efficiency with the increase of clad width in the Otto model through experiments using COMSOL Multiphysics. The turning point showed a peak value of the power efficiency.

Game Design: Tank Battle 07/2020

- Applied C++ GUI Qt4 in the design and production of a video game, including different map modules created from Qlabel class, different tanks owning special skills created from tank and cannonball classes, hitboxes and their related response functions implemented inline in the time-event functions, computer-controlled tanks, single-player and double-player modes, game interface, etc.

HONORS & AWARDS

- **National Scholarship** for academic year 2020-2021, awarded by China's Ministry of Education & Southeast University (**0.2%** nationwide).
- **Zhongnan Scholarship for Realizing Dreams** for academic year 2020-2021, awarded to 1 student in School of Electronic Science & Engineering.
- **1st Prize**, The Advanced Mathematics Competition for Undergraduates at Southeast University (**2%**, 09/2020)
- **1st Prize**, The 17th Advanced Mathematics Competition for Undergraduates in Jiangsu Province (**3.5%**, 11/2020)
- **1st Prize**, The 12th National College Mathematics Competition (**7%**, 12/2020)
- **Southeast University Single-course Scholarships** (top **5%** in seven major courses)
- **Individual Scholarship for Excellence in Social Work** for academic year 2020-2021, awarded to 1 student in School of Electronic Science & Engineering.

SKILLS & ADDITIONAL

Skills: Python, MATLAB, C++, Verilog, Assembly language (8086 CPU), Multisim, COMSOL Multiphysics

Standardized Tests: GRE 331 (V: 161, 87%; Q: 170, 96%); TOEFL 100 (R30, L25, W25, S20)