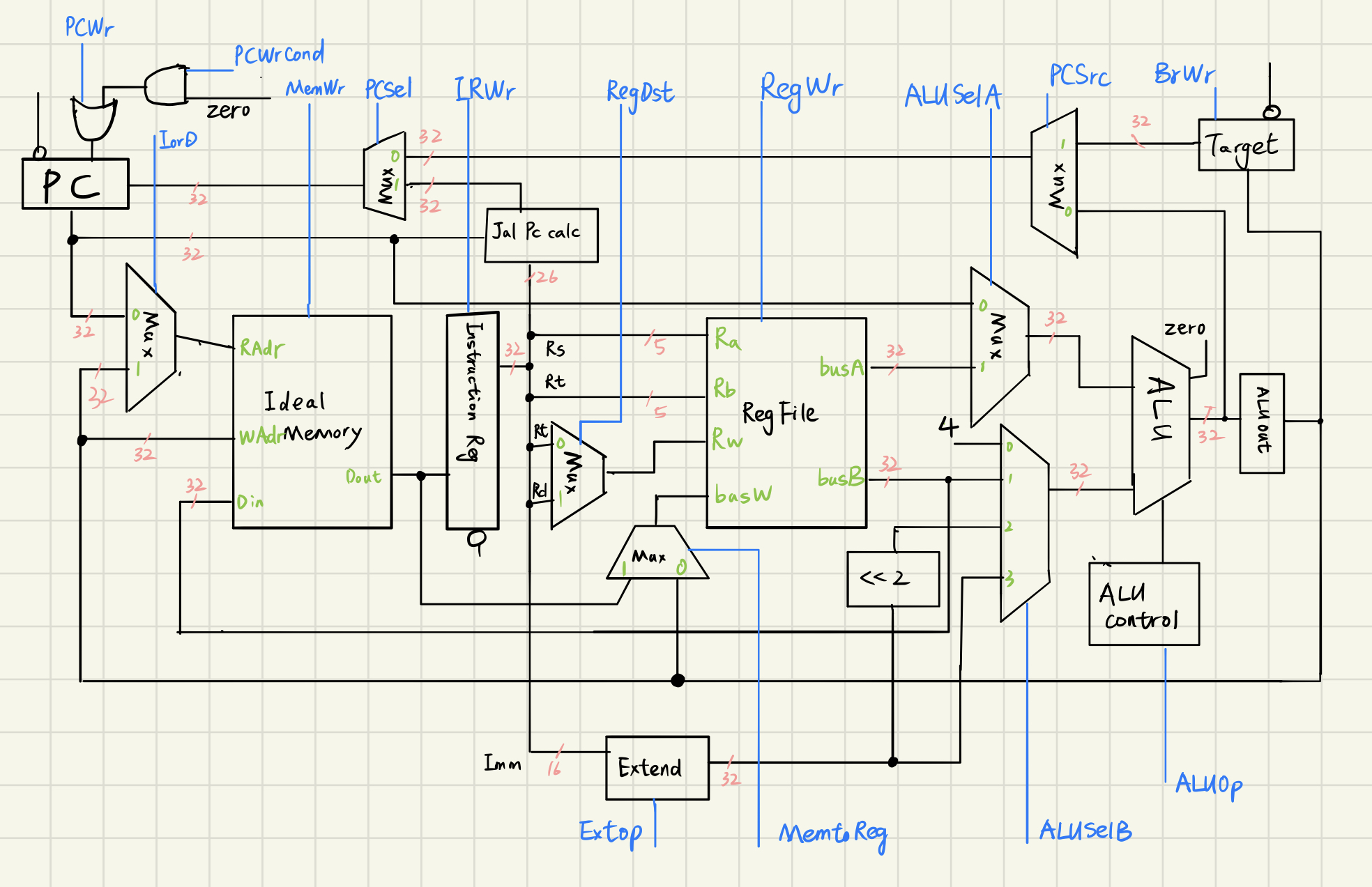
**多周期MIPS处理器设计报告**

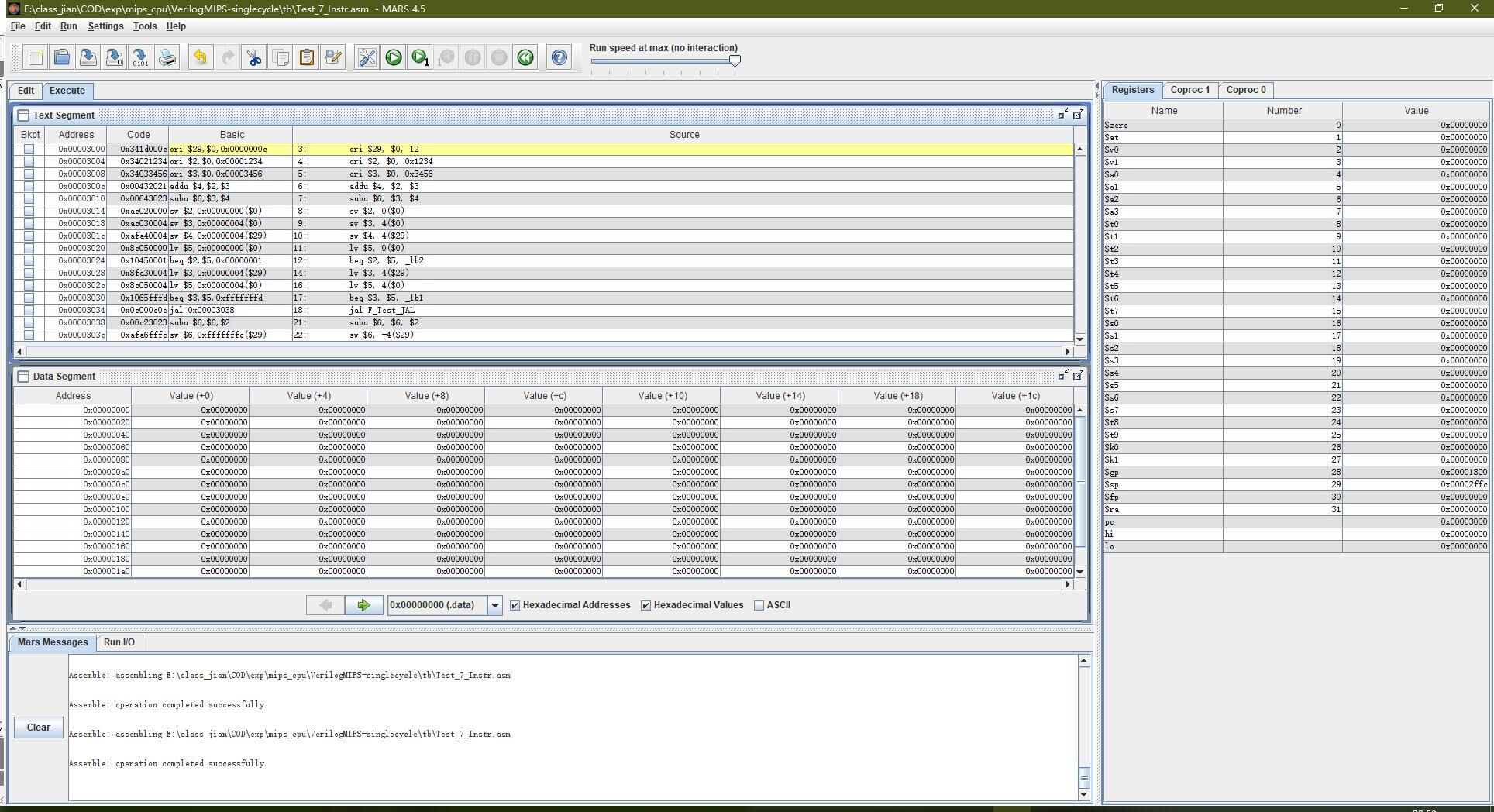
**数据通路设计**

****

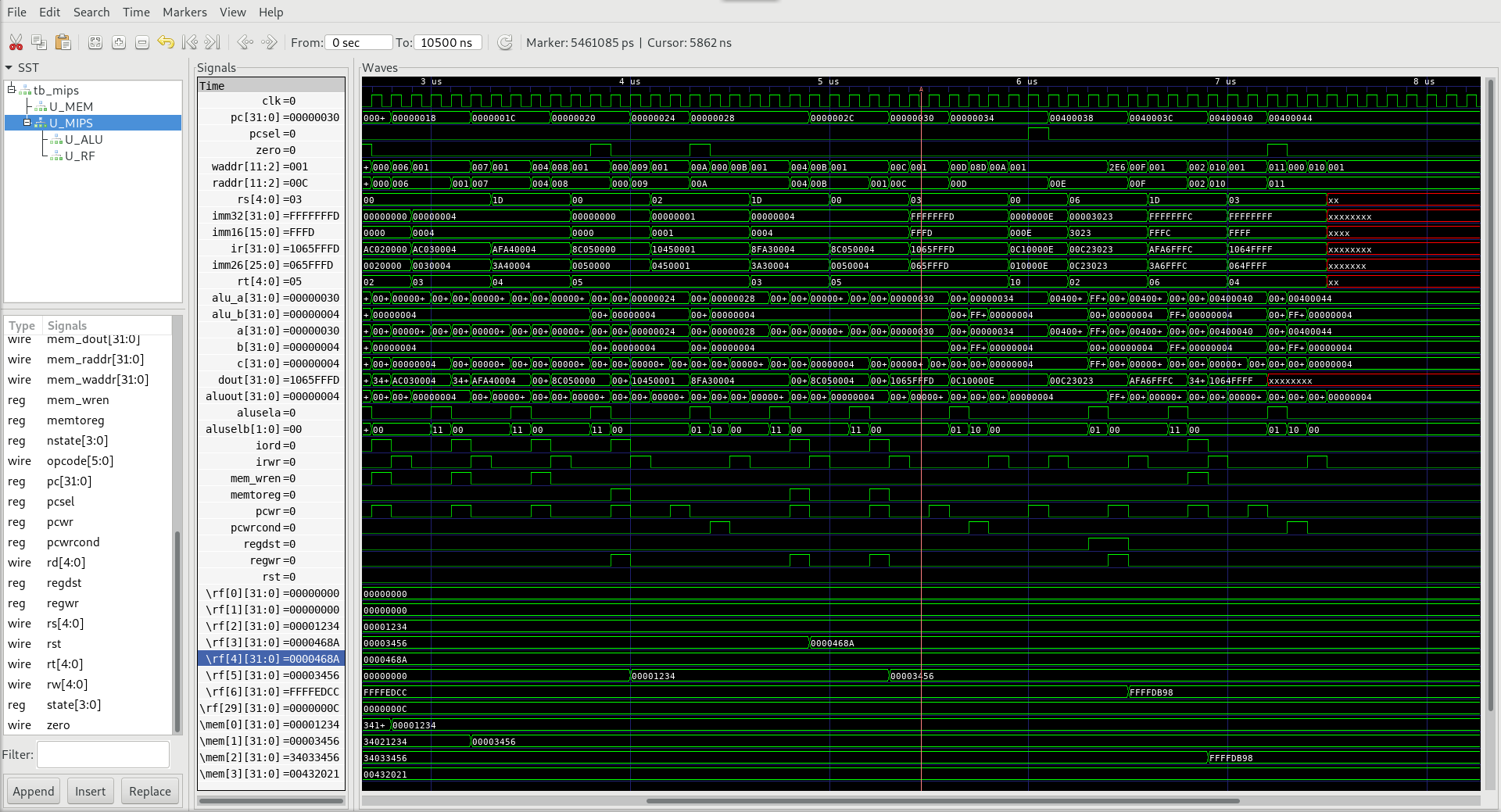
**控制通路设计**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | fetch | decode | rtype | ori | lw | sw | Beq | Beqcmp | BeqWr | J | rwrite | oriwrite | lwwrite | swwrite |
| pcwr | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| pcwrcond | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| pcsel | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| iord | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| memwr | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Regdst | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Irwr | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Regwr | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| alusela | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| aluselb | 0 | 0 | 1 | 3 | 3 | 3 | 0 | 1 | 2 | 0 | 0 | 0 | 0 | 0 |
| extop | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| memtoreg | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| aluop | 0 | 0 | ADDSUB | OR | ADD | ADD | ADD | SUB | ADD | 0 | ADD | ADD | ADD | ADD |

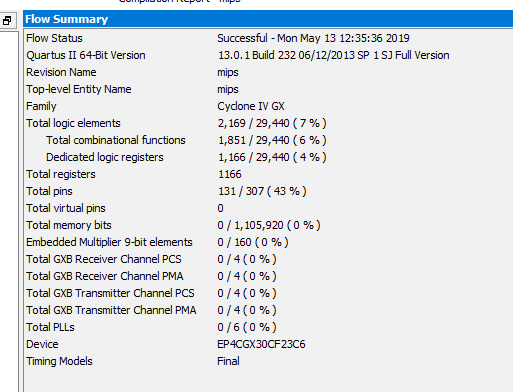
**仿真结果**

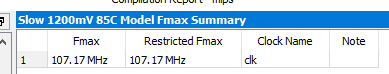


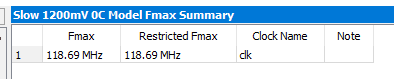
**仿真波形**

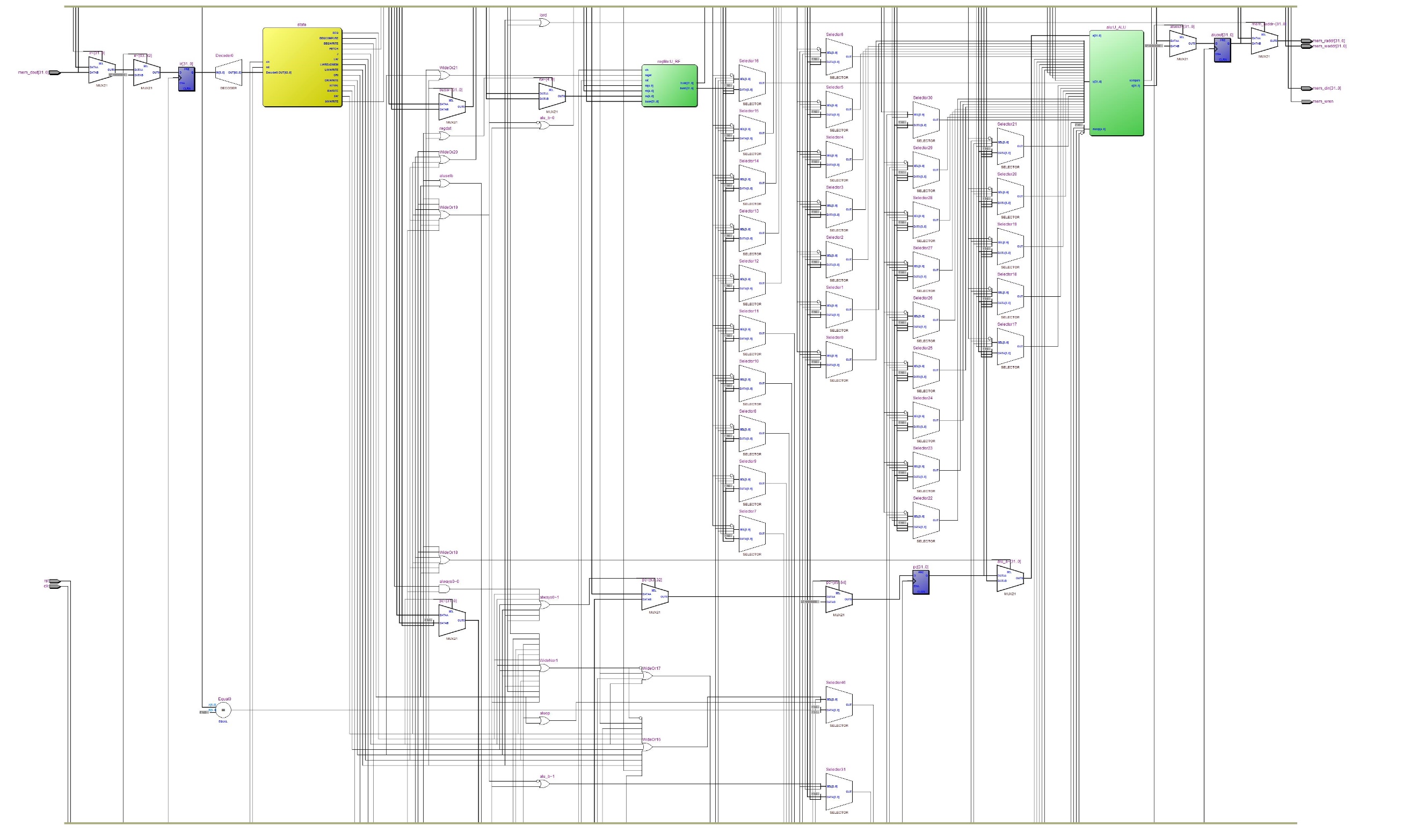


**实现结果**









**评分标准**

从设计思路、仿真结果、实现结果等方面进行综合评价，全部满分共计24分。

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 1、设计思路 | 10 | 8 | 6 | 4 | 0 |
| 查看设计文档思路是否清晰，描述是否完整 | 优秀，数据通路描述准确、控制通路表格正确 | 很好，文档较为清楚 | 及格，文档较完整 | 待改进，文档不清或错误较多 | 无文档 |
| 2、仿真结果 | 10 | 8 | 6 | 4 | 0 |
| 主要通过测试激励进行评估，可以用提交者的测试激励，也可以用自己的测试，验证功能是否正确。 | 优秀，7条指令100%验证通过（尽量用自己的测试程序，与提交的测试程序进行交叉验证） | 很好，1~2条错误 | 及格，3条指令错误 | 待改进，50%以上功能点错误 | 基本不对，编译不通过等 |
| 3、实现结果 | 10 | 8 | 6 | 4 | 0 |
| 是否有Quartus布线结果 | - | - | - | 有最高主频、面积占用率等信息 | 无 |