Reducing the Barrier to Post-Moore Era Hardware Innovation

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No Silver Bullet
Essence and Accidents of Software Engineering

– Fred Brooks, 1986

DARPA UPSIDE program (2012-2018)

Unconventional Processing of Signals for Intelligent Data Exploitation

Objective:

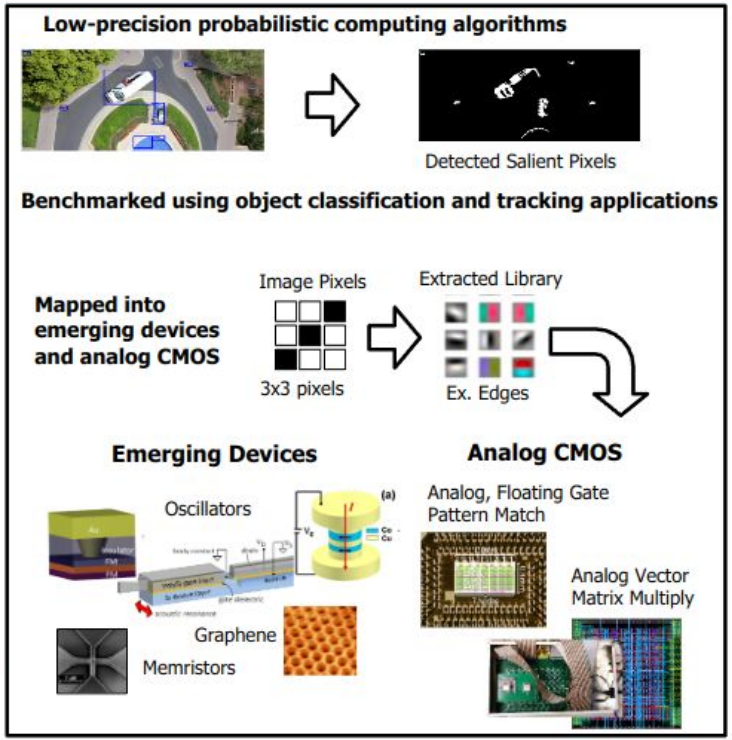
Exploit the physics of emerging devices, analog CMOS, and non-Boolean computational models to achieve new levels of performance and power for real-time sensor imaging systems.

Approach:

TA1: Image Application for Benchmarking: Recreate a traditional image processing pipeline (IPP) using UPSIDE Compute models showing no degradation in performance.

TA2: MS CMOS Demonstration: Mixed signal CMOS implementation of the computational model and system test bed showing **1x10^{5}x** combined speed-power improvement for analog CMOS.

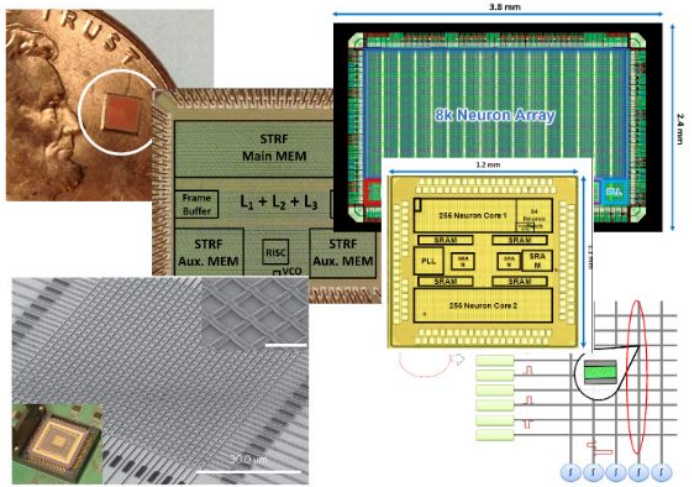
TA3: Emerging Device Implementation: Image processing demonstration combining next-generation devices with new computation model. **1x10^{7}x (projected)**



Goal: Demonstrate the capability and pathway toward embedded computing efficiency in ISR applications w/ >1,000x processing speed and >10,000x improvement in power consumption

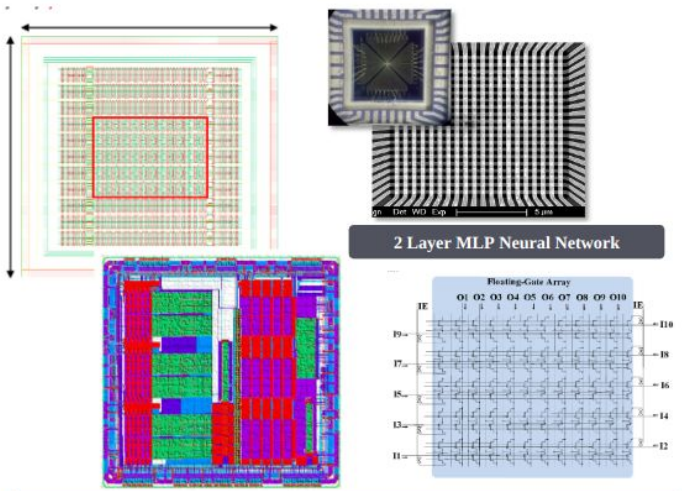
DARPA Selected UPSIDE results

University of Michigan



- Mixed signal processing (50TOPS/W)
- Sparse image reconstruction in memristors
- Numerous publications (Nature, …)

UCSB



- First memristor based multilayer perceptron
- Flash based 55nm analog computing (>10TOPS/W)
- Numerous publications (Nature, …)

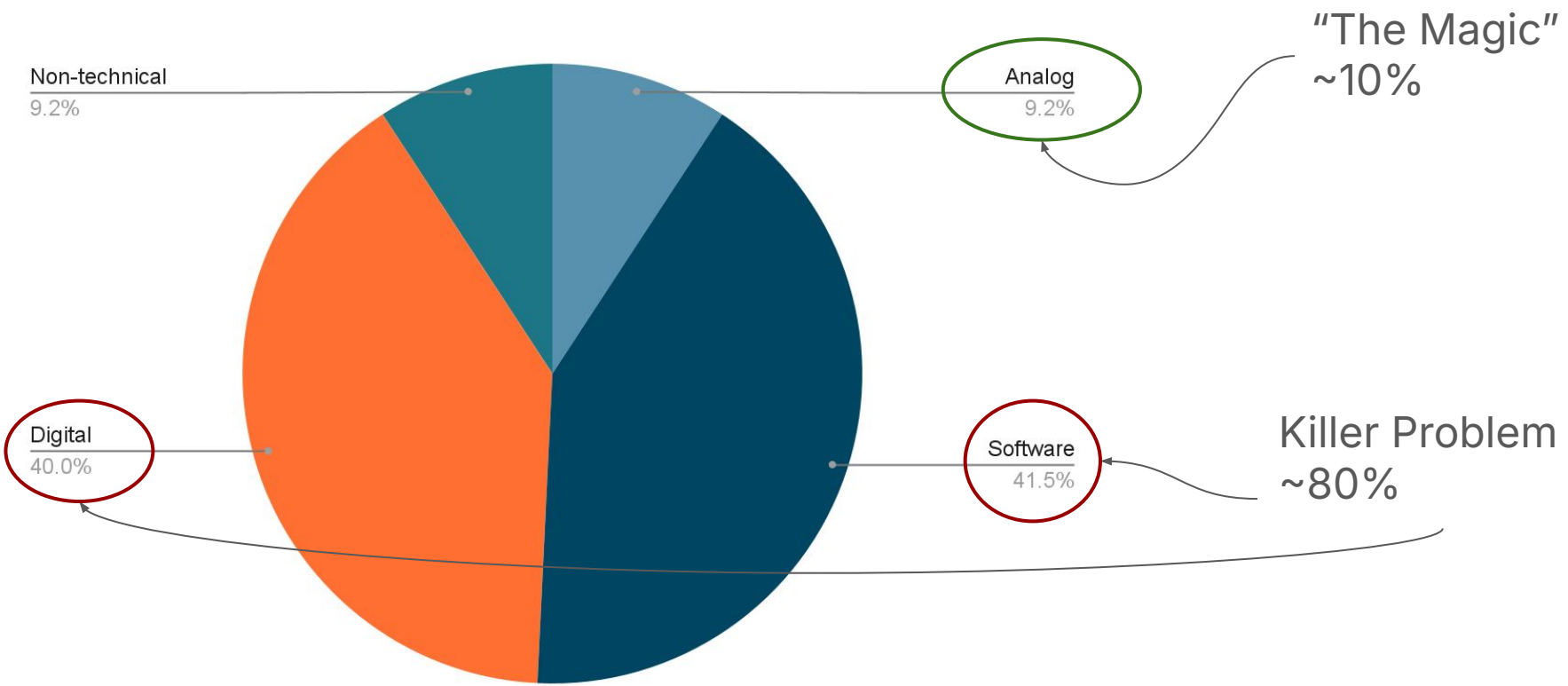
Conclusion:
Fantastic work
Analog>>Digital

But what about:
Applications?
Speed?
Integration?
Scaling?
Dynamic range?
Manufacturing?
Interfacing?
Amdahl?
Transition?
Portability?

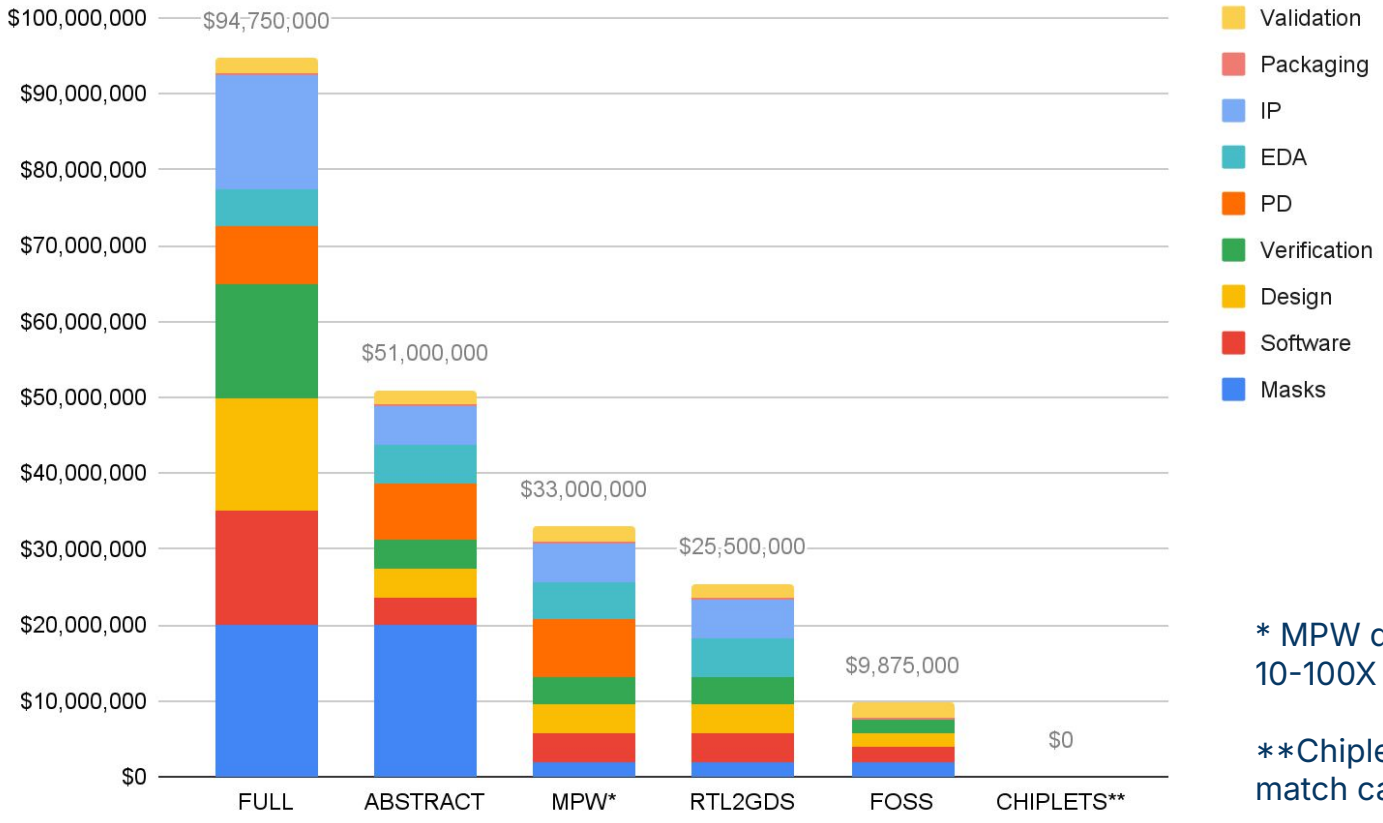
Really Important Unanswered Questions

- **All non digital technologies**:
  - Amdahl, SW, general performance, system, HVM?....
- **Quantum**: What is the application?
- **Biological**: What is the application?
- **Analog**: How will you interface with digital & scale?

Staff Count of a Failed Analog Computing Startup



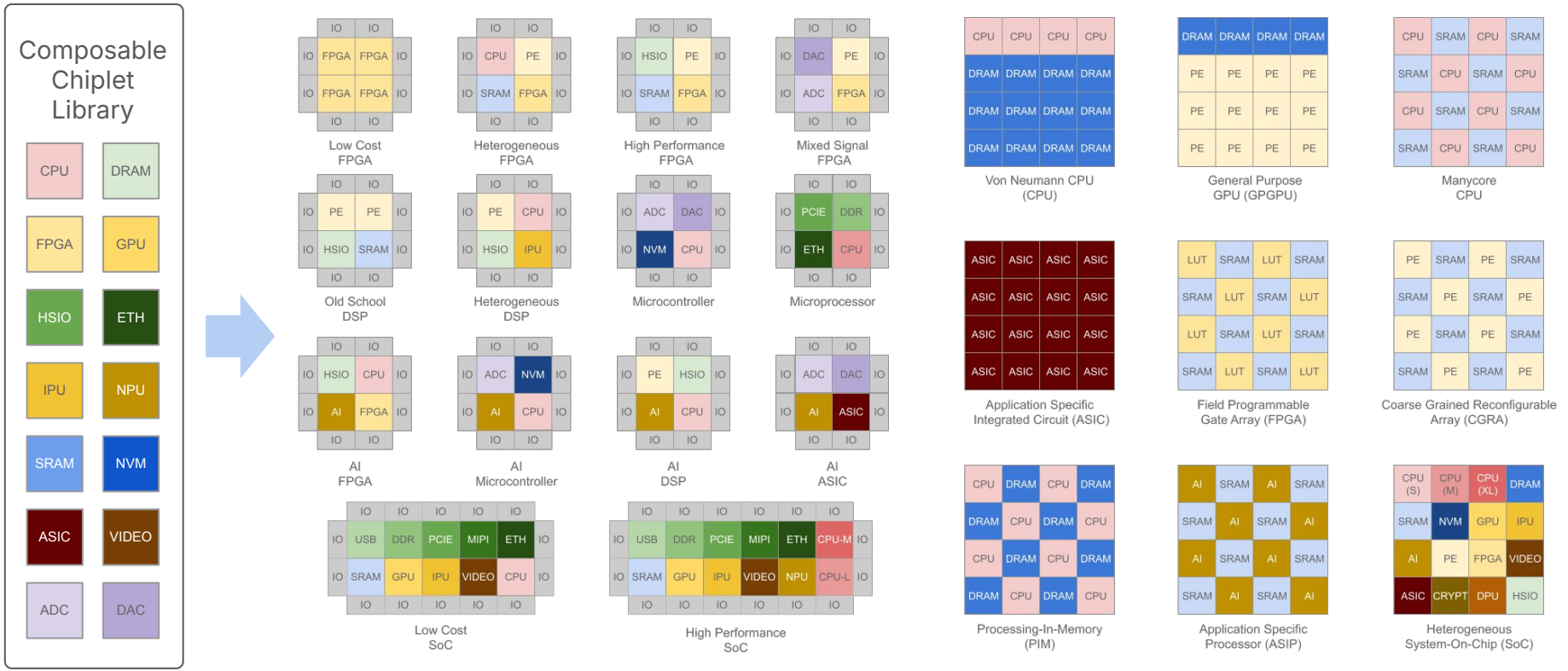
Chiplets: Best Path to Lowering the Barrier to Innovation



* MPW drives up unit cost by 10-100X

**Chiplets assume mix and match catalog

Chiplets: The New Amino Acids of Silicon Systems



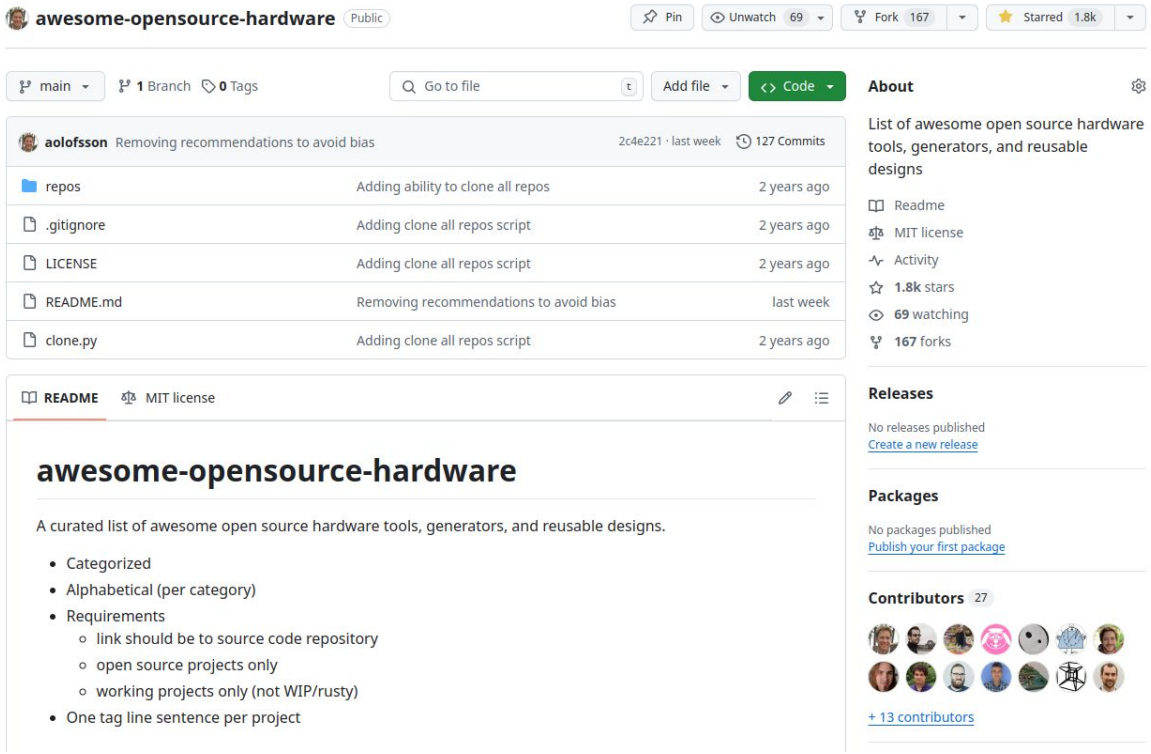
"Finite investment, infinite possibilities"

Missing Chiplet Technologies

- Full-stack chiplet standards
- Open market chiplets
- Automated chip layout compilers
- Cost effective chiplet emulation
- Self service emulation infrastructure
- Silicon interposer access
- Automated high mix package assembly

What I have been working on since 2017...

Hardware field is mostly failing at collaboration!



- **https://github.com/aolofsson/awesome-opensource-hardware**

- **450+** open source repos
- Amazing growth in 10 years
- Limited collaboration

Recommendation:

- Identify the gaps
- Fund the boring stuff
- Don’t rely on students for critical infrastructure.
- Enforce standards/discipline
- Learn from DoE HPC SW success?

Walking the walk…

- **Hardware Compiler:**

https://github.com/siliconcompiler/siliconcompiler

- **Target Agnostic Libraries:**

https://github.com/siliconcompiler/lambdalib

- **Virtual PDKs:**

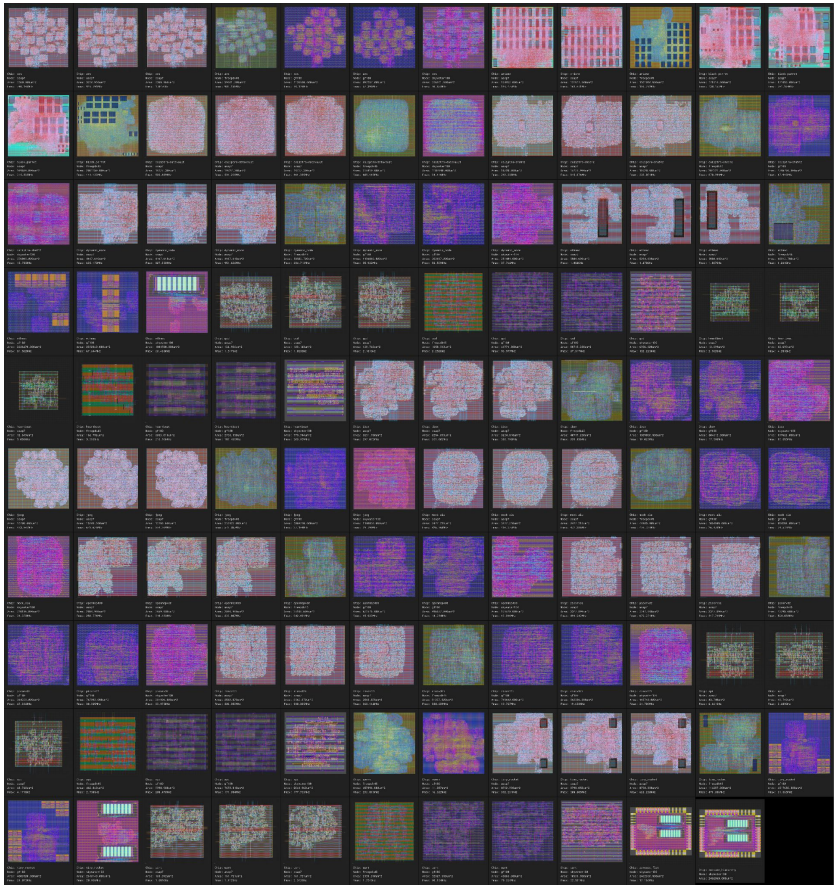
https://github.com/siliconcompiler/lambdapdk

- **Universal Memory Interface:**

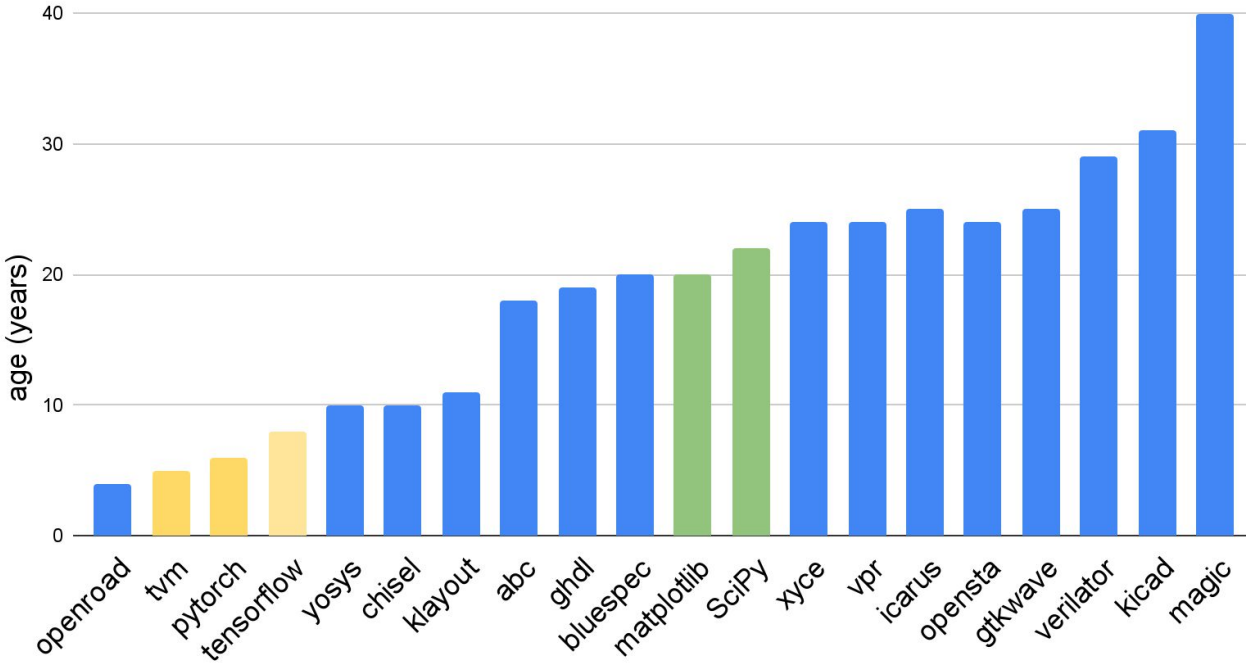
https://github.com/zeroasiccorp/umi

- **Digital Twin Distributed (Chiplet) Emulator:**

https://github.com/zeroasiccorp/switchboard



Infrastructure Must be Built to Last!



- Build to scale (LLVM inspired)
- Plan for 10 years
- Developer redundancy
- Ensure long term funding
- Make wise choices!
- Leverage others

List of “Boring” Unsolved Infrastructure Problems

- High quality open source digital **IP** (see DARPA POSH, 2017)
- Automated **RTL2GDS** flows (see DARPA IDEA, 2017)
- Common chiplet **standards** (see DARPA CHIPS, 2017)
- ML hardware **compilers** (see DARPA RTML, 2019)
- Common CMOS+X **test** vehicles (see NATCAST TVIP)
- **Packaging** infrastructure, non existent (see NAPMP)
- High quality open source **analog** IP, currently at zero (?)
- Open source analog circuit **data** sets for EDA/AI (?)
- Creating the RISC-V equiv for ..AI, analog, fpga,... (?)
- Proxy **PDKs** for analog and digital to get around NDA (?)
- Standard **packaging** MPW infrastructure (?)
- Standard free and fast **MPWs** (3 month turn, not 12)